INTEGRATED CIRCUITS, MONOLITHIC, CMOS AND HBT ON SiGe:C, 1.6 TO 12 GHz FREQUENCY SYNTHESIZER WITH INTEGRATED SIGMA DELTA MODULATOR FRACTIONAL-N PLL

BASED ON TYPE NOV1G14

ESCC Detail Specification No. 9202/085

Issue 1	July 2021

Document Custodian: European Space Agency – see https://escies.org

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DOCUMENTATION CHANGE NOTICE

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DCR No.	CHANGE DESCRIPTION

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1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 920208501R

- Detail Specification Reference: 9202085
- Component Type Variant Number: 01
- Total Dose Radiation Level Letter: R (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Finish	Weight max g	Total Dose Radiation Level Letter
01	NOV1G14	CQFN-32	14	0.2	R [100krad(Si)]

The terminal finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

The total dose radiation level letter shall be as defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
V_{DDA} Supply Voltage	V_{DDA}	0 to 3.5	V	Note 1
V_{DDB} Supply Voltage	V_{DDB}	0 to 5.4	V	Note 2
Input Voltage Range	V_{IN}	0 to V_{DDA}	V	Inputs: SPI_*, Reset_ext, Fine_in, Coarse_in
Device Power Dissipation (Continuous)	P_D	2.2	W	Maximum DC power
Reference Input Power (Continuous)	P_{REF}	+13	dBm	
External RF Input Power (Continuous)	P_{RF}	+13	dBm	
Operating Temperature Range	T_{op}	-55 to +125	°C	T_{case}, package backside; Note 3
Storage Temperature Range	T_{stg}	-65 to +150	°C	
Junction Temperature	T_j	+150	°C	
Thermal Resistance, Junction to Case	$R_{th(j-c)}$	15	°C/W	
Soldering Temperature	T_{sol}	+260	°C	Note 4

NOTES:

1. All voltages are with respect to GND. Device is functional for $3.1V \leq V_{DDA} \leq 3.5V$.
2. All voltages are with respect to GND. Device is functional for $4.8V \leq V_{DDB} \leq 5.4V$.
3. Device is functional at temperatures between T_{case} = -40°C(*) to +85°C.
   (*) Operation below room temperature (see Para. 2.3.1) requires an external 3.5V VCO voltage supply (connection of VCO_ldo and VCO_ldox via 24Ω to AMP_ldo is recommended; see Para. 1.9).
4. Duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same terminal shall not be re-soldered until 3 minutes have elapsed.

1.6 HANDLING PRECAUTIONS

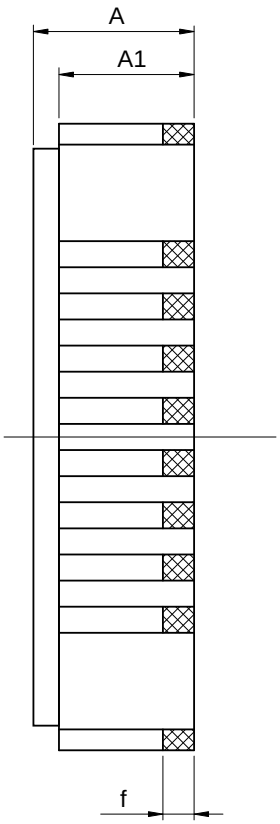
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 200 Volts.

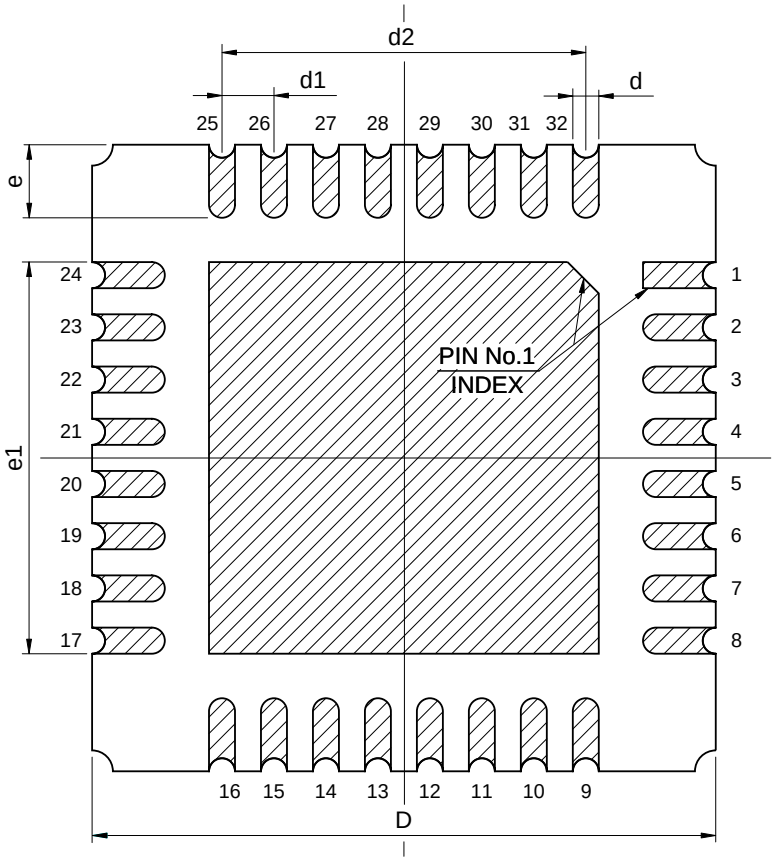
1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

Ceramic Quad Package (CQFN-32) – 32 Terminals

Side View



Backside View

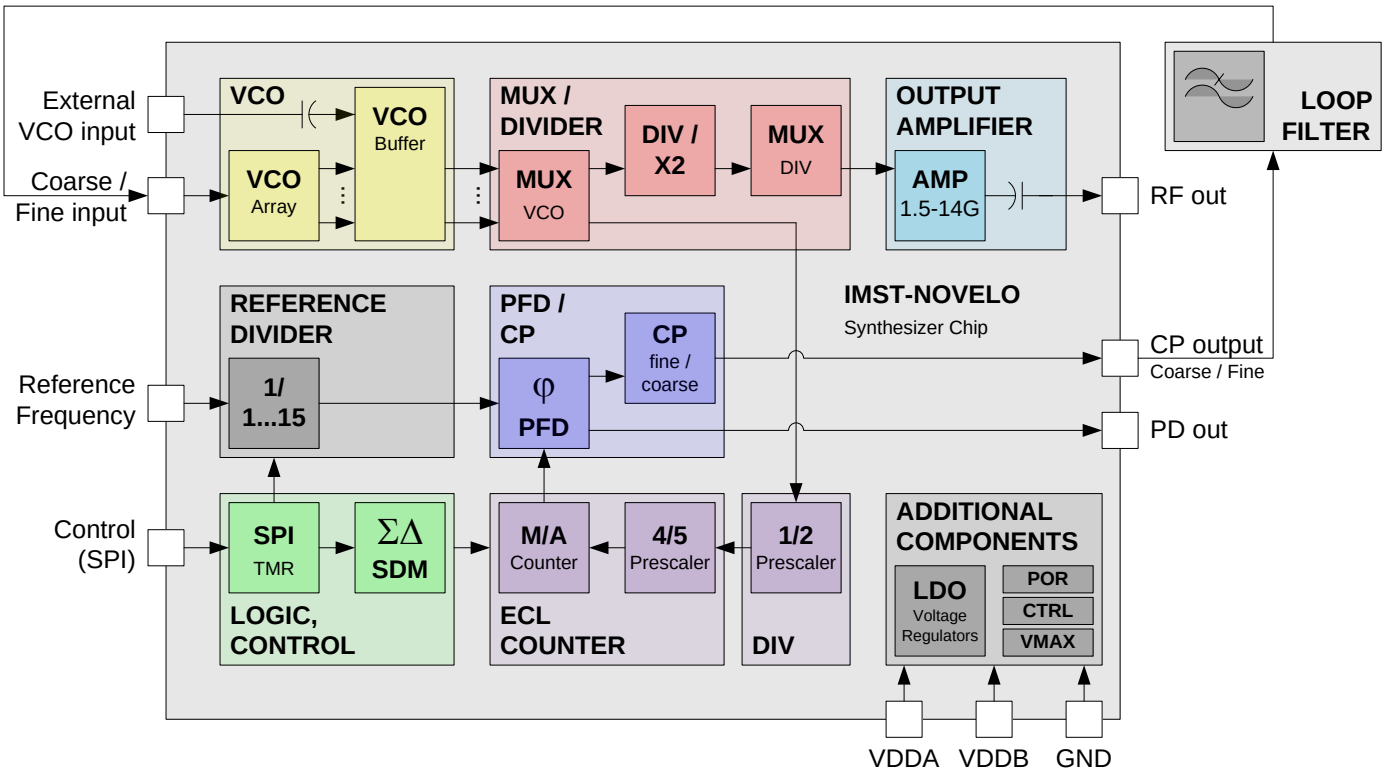


Symbols	Dimensions (mm)		Remarks
	Min	Max	
A	1.4	1.77	Overall thickness including soldered lid
A1	1.17	1.43	Package thickness without lid
D	5.85	6.2	Overall package width and length (Note 4)
d	0.25 TYPICAL		Terminal pad width (Note 2)
d1	0.50 BSC		Terminal pad spacing (Note 3)
d2	3.37	3.63	Overall terminal pad spacing (Notes 2, 4)
e	0.70 TYPICAL		Terminal pad length (Note 2)
e1	3.65	3.85	Exposed terminal pad width and length (Note 2)
f	0.30 TYPICAL		Side metallization (Note 2)

NOTES:

1. Terminal identification is specified by reference to the index corner mark on the bottom of the package and the Pin No. 1 index, as shown. Terminal numbers increase counter clockwise if viewed from top of the package.
2. Applies to all 32 terminals (8 per side).
3. 28 places.
4. The overall terminal pad spacing centrelines on each of the 4 sides shall be located within ±0.15mm of the applicable package centreline.

1.8 FUNCTIONAL DIAGRAM



1.9 PIN ASSIGNMENT AND DESCRIPTION

The table below describes each pin's assignment, type and standard, plus a brief description of its functionality.

Pin No.	Pin Name	Pin Type	Pin Standard (Note 1)	Description
1	PD_up	Output (CMOS)	ESD	Phase detection output UP. Turns from HIGH to LOW if reference frequency is ahead of feedback frequency. Maximum load 500Ω.
2	PD_down	Output (CMOS)	ESD	Phase detection output DOWN. Turns to LOW if feedback frequency is ahead of reference frequency. Maximum load = 500Ω.
3	CP_vcc	Input (Power)	VDD	External supply voltage (type V_{DDA}, I_{max} = 20mA). Note 2.
4	CP_ldo	Output (DC)	VDD	LDO voltage regulator output (+2.7V, generated on-chip). LDOA domain. Note 2.
5	REF_in	Input (CMOS)	RF	External reference clock frequency (100MHz nominal). The input is DC coupled, an external decoupling capacitor (1nF) is necessary.
6	SPI_clk	Input (CMOS)	ESD	Clock for Serial Peripheral Interface (SPI, readout frequency max = 4KHz, write frequency max = 1MHz).

Pin No.	Pin Name	Pin Type	Pin Standard (Note 1)	Description
7	SPI_data_in	Input (CMOS)	ESD	SPI data input.
8	SPI_data_out	Output (CMOS)	ESD	SPI data output (low current)
9	Reset_ext	Input (CMOS)	ESD	External reset (LOW active, HIGH at normal operation).
10	SPI_enable	Input (CMOS)	ESD	SPI enable (LOW active, HIGH at normal operation).
11	LockDetect_A (LockDetect_D)	Output (Output, CMOS)	ESD	Analog PFD lock detect output voltage (0 to 2.5V). (Alternative: Digital lock detect output; also provided via SPI)
12	CMOS_ldo	Output (DC)	VDD	LDO voltage regulator output (+2.5V, generated on-chip). LDOC domain. Note 2.
13	CMOS_vcc	Input (Power)	VDD	External supply voltage (type V_{DDA}, I_{max} = 30mA). Note 2.
14	CNTR_ldo	Output (DC)	VDD	LDO voltage regulator output (+2.7V, generated on-chip). LDOA domain. Note 2.
15	CNTR_vcc	Input (Power)	VDD	External supply voltage (type V_{DDA}, I_{max} = 170mA). Note 2.
16	DIV_vcc	Input (Power)	VDD	External supply voltage (type V_{DDA}, I_{max} = 20mA). Note 2.
17	DIV_ldo	Output (DC)	VDD	LDO voltage regulator output (+2.7V, generated on-chip). LDOA domain. Note 2.
18	VCOx_ldo	Output* (DC) * Input if required	VDD	LDO voltage regulator output for VCOs 1, 3, and 5; (+4.0V, generated on-chip*). Supply voltage for VCOx-LDO provided via AMP_vcc. *) Disabled output and external input of 3.5V is required if full temperature range usage is intended (connection via 24Ω to AMP_ldo recommended). LDOB domain. Note 2.
19	AMP_vcc	Input (Power)	VDD	External supply voltage (type V_{DDB}, I_{max} = 100mA). Note 2.
20	AMP_ldo	Output (DC)	VDD	LDO voltage regulator output (+4.0V, generated on-chip). Additional VCO voltage supply possible (3.5V, via 24Ω resistor, connected to VCO_ldo and VCOx_ldo). LDOB domain. Note 2.
21	RF_outN	Output	RF	Differential RF output (N), AC coupled to on-chip voltages, but 1KΩ to GND for ESD protection.

Pin No.	Pin Name	Pin Type	Pin Standard (Note 1)	Description
22	RF_outP	Output	RF	Differential RF output (P), AC coupled to on-chip voltages, but 1KΩ to GND for ESD protection. Single ended output possible, but termination of the unused port via 50Ω load required to avoid RF distribution inside the package.
23	BUF_ldo	Output (DC)	VDD	LDO voltage regulator output (+2.7V, generated on-chip). LDOA domain. Note 2.
24	BUF_vcc	Input (Power)	VDD	External supply voltage (type V_{DDA}, I_{max} = 30 mA). Note 2.
25	VCO_vcc	Input (Power)	VDD	External supply voltage (type V_{DDB}, I_{max} = 30 mA). Note 2.
26	VCO_extN	Input	RF	Differential external RF input (N), AC coupled to on-chip voltages, but 1KΩ to GND for ESD protection. Single ended input with limited functionality. Termination of the unused port with 50Ω recommended.
27	VCO_extP	Input	RF	Differential external RF input (P), AC coupled to on-chip voltages, but 1KΩ to GND for ESD protection. Single ended input with limited functionality. Termination of the unused port with 50Ω recommended.
28	VCO_ldo	Output* (DC) * Input if required	VDD	LDO voltage regulator output for VCOs 2, 4, 6, and 7; (+4.0V, generated on-chip*) *) Disabled output and external input of 3.5V is required if full temperature range usage is intended (connection via 24Ω to AMP_ldo recommended). LDOA domain. Note 2.
29	Fine_in	Input	ESD	Fine voltage control input for on-chip VCOs (0 to 2.7V). External connection to Fine_out via filter needed.
30	Coarse_in	Input	ESD	Coarse voltage control input for on-chip VCOs (0 to 2.7V). External connection to Fine_out via filter needed.
31	Fine_out	Output	ESD	Fine charge pump output current.
32	Coarse_out	Output	ESD	Coarse charge pump output current.
Exp. Pad	global_gnd	Ground	GND	Exposed ground (GND) pad for DC and RF; Provides good thermal contact for heat dissipation. Note 3

NOTES:

1. Where:
   - ESD = ESD protected pins
   - VDD = Supply related pins
   - RF = RF input/output pins
2. The following off-chip shunt capacitors are required to be used at all voltage supply and LDO ports: 100pF, as close as possible to the chip package; 100nF and 2.2µF.
3. Power Dissipation of the device is specified in Para. 1.5.

4. The following table below defines the pin groups applied during testing:

Pin Group No.	Type	Total No. of Pins	Pin Numbers
1	CMOS Input	4	6, 7, 9, 10 (SPI*, Reset_ext)
2	Reference Frequency Input	1	5 (REF_in)
3	RF Input	2	26, 27 (VCO_extN, VCO_extP)
4	High Current CMOS Output	2	1, 2 (PD_up, PD_down)
5	Low Current CMOS Output	1	8 (SPI_data_out)
6	RF Output	2	21, 22 (RF_outN, RF_outP)
7	DC Supply	7	3, 13, 15, 16, 19, 24, 25 (*vcc)
8	DC Regulated Output	8	4, 12, 14, 17, 18, 20, 23, 28 (*ldo)
9 (1)	Charge Pump Outputs	2	31, 32 (Coarse_out, Fine_out)
10 (1)	Charge Pump Inputs	2	29, 30 (Fine_in, Coarse_in)
11 (1)	Analog Lock Detect Output	1	11 (LockDetect*)
12 (1)	Ground	1	Exposed pad (global_gnd)

(1) Included for information only; these pin groups are not included in testing.

1.10 FUNCTIONAL DESCRIPTION

1.10.1 Overview

NOV1G14 is a full functional fractional-N synthesizer. The frequency generation is performed internally, by an array of voltage-controlled oscillators with 7 VCOs covering the frequency range between 6 and 12GHz. By means of RF dividers, the covered frequency range is extended down to 1.6GHz. With limited functionality, this frequency range can be extended to about 14GHz by using an internal times two frequency multiplier. Also, an external RF source can be used for frequency generation.

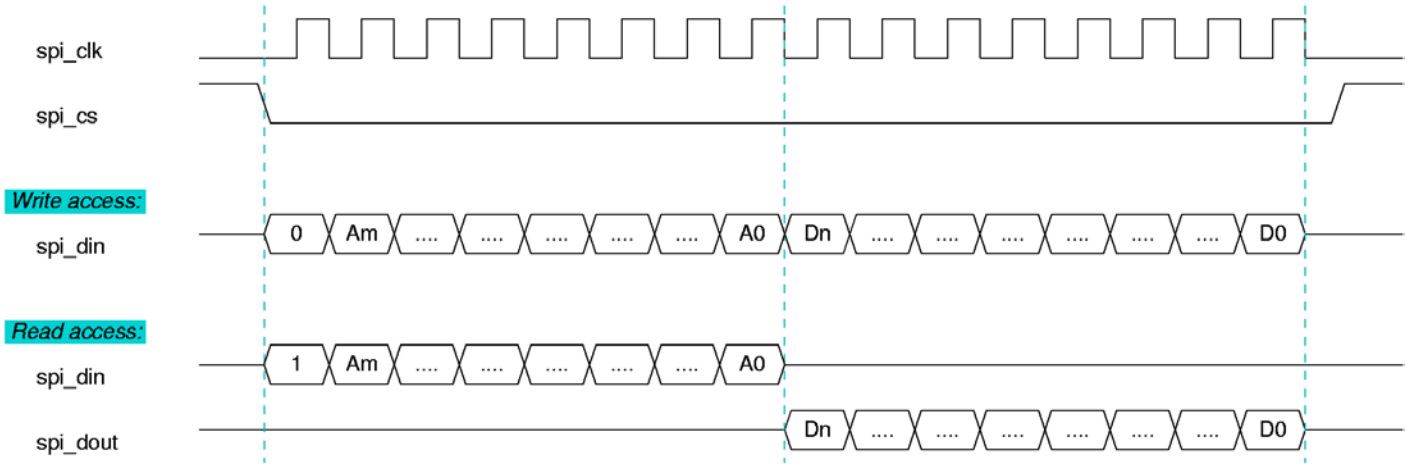
Via a multiplexer, either the buffered, direct VCO path or the divider/multiplier outputs are connected to the output amplifier. The feedback path with prescaler (divide-by-two circuit) and ECL based 4/5 dual modulus divider in combination with a master and assistant (M/A) counter is fed directly from the VCO multiplexer. The ECL-counter output is connected to a phase frequency detector (PFD), which generates voltage up- and down-pulses depending on the down-divided signal phase compared to the reference frequency phase. The following charge pump (CP) converts these pulses into up- and down-currents, charging external loop filter capacitances. The voltages across the capacitances regulate the VCO output frequency; the loop (PLL) is closed.

The synthesizer can be operated in two modes, integer and fractional. During integer mode, a fixed divider ratio is applied to the divider chain. This way, the output frequency can be adjusted to a multiple of divider ratio and reference frequency (e.g. 2 x 45 x 100MHz = 9GHz). To obtain frequencies smaller than the integer frequency steps, fractional mode is applied. In this case, via a programmable sigma delta modulator (SDM) based on CMOS logic, dynamic changes of the main divider factor N are performed (Gauss distribution). This results in a fractional main divider factor Q with the possibility to access frequencies down to 1 Hz step size at moderate spur and quantization noise levels.

1.10.2 Register Programming

In write mode (according to the figure below), the data sent over the SPI starts with a leading ‘0’, followed by the address of the desired control register with 7 bit length. The current status of the register can be read also, with a leading ‘1’ for read access. Each register has a width of two bytes, which leads to a total width of three bytes.

SERIAL INTERFACE TIMING CHART



REGISTER MAP

Control Registers (address range "0x00" to "0x09"; registers are read-write).

Address	Bit	Name	Function	Default
0x00 Divisor 0	15...0	divisor(35:20)	M/A-counter divisor bits 7...0, -1...-8 Integer divider values between 24 and 255 are possible (default is 45). Fractional digits are programmed via the 28 remaining bits of the three divisor registers. The M/A settings are calculated from the programmable integer divider value D with: D = 5A+4(M+1-A) and A ≤ M+1 A is calculated from the two LSB of D (max 3). For example, results the default divider setting with D = 45 in M = 10 and A = 1	0x2D00
0x01 Divisor 1	15...0	divisor(19:4)	Divisor bits -9...-24	0x0000
0x02 Divisor 2	15...12	divisor(3:0)	Divisor bits -25...-28	"0000"
	11...0	unused		

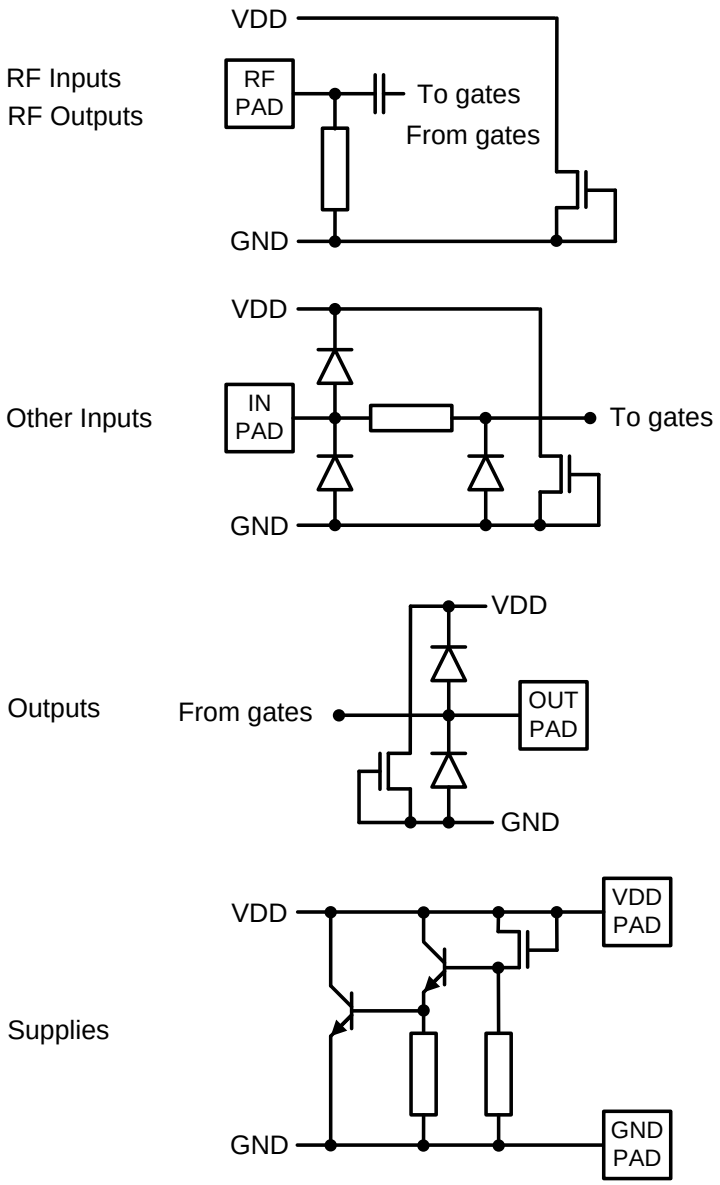
Address	Bit	Name	Function	Default
0x03 Config	15...8	unused		
	7	reset_sd	Low-active reset for Sigma Delta Modulator (SDM). ”0” integer mode, fixed divider ratio; ”1” fractional mode	"0"
	6...5	sd_mux	Number of SDM accumulator stages: ”00” 1 stage, ”01” 2 stages, ”10” 3 stages, ”11” 4 stages. Example: 3 stages lead to a max. divider ratio variation of 8 (23; from -3 to +4) around the integer part of the divisor	"00"
	4	ref_div_ bypass_en	Enable for reference clock bypass switch	"0"
	3...0	ref_div_ctrl	Divisor for reference clock divider (0…15). ”0” activates the divider bypass within the reference divider. ”1” divides by one.	"0000"
0x04 Preload	15...0	preload	Preloads first accumulator bits -1...-16	0x0000
0x05 CP	15...14	unused		
	13…12	cp_test	Test modus for charge pump currents. PFD switched to constant outputs. ”00” Test mode disabled ”01” UP current and PD_up active ”10” DOWN current and PD_down active ”11” UP and DOWN activated	"00"
	11	cp_fine_en	Enable for charge pump fine current	"1"
	10	cp_coarse_en	Enable for charge pump coarse current Coarse charge current is 500µA	"1"
	9...5	cp_fine	Charge pump fine current (Icpf) settings. Binary addition of 8mA (MSB), 4mA, 2mA, 1mA, 500μA (LSB)	"01000"
	4...0	unused		
0x06 Offset	15...10	unused		
	9...5	offset_fine	Fine offset current adjustment Iosf = n*Icpf/50; n 0…31	"00001"
	4...0	offset_coarse	Coarse offset current setting Iosc = n*100µA; n 0…31	"00001"
0x07 VCO	15...8	unused		
	7	ldo_vco_en	Enable for VCO LDO	"1"
	6...3	vco_band_ctrl	Band selection for internal VCO arrays. In the current configuration, 8 bands are used from "0000" (lowest) to "0111" (highest).	"0001"
	2...0	vco_ctrl	VCO control. "001" to "111" enables internal VCOs 1-7. "0" enables external VCO path	"110"

Address	Bit	Name	Function	Default
0x08 Enable	15…12	unused		
	11…9	div_path_en	Enable for 1 out of 7 divider paths or none "000". Selectable paths: "001" direct path, "010" divide by 2, "011" divide by 4 and "100" multiply by 2	"001"
	8	lock_detect_ dig_en	Enable for digital lock detect output	"0"
	7	lock_detect_ ana_en	Enable for analog lock detect buffer	"0"
	6	ldo_div_en	Enable for pre-divider and RF divider chain LDO	"1"
	5	ldo_buf_en	Enable for VCO output chain LDO	"1"
	4	ldo_amp_en	Enable for output power amplifier LDO	"1"
	3	pfd_vout_en	Enable for external PD up/down voltage output	"0"
	2	pfd_en	Enable for PFD	"1"
	1	div_fb_en	Enable for feedback clock pre-divider	"1"
	0	clk_fb_out_en	Enable for feedback clock test output (optional)	"0"
0x09 GPO	15...8	unused	General purpose outputs with default "1"	"1"
	7...3	unused	General purpose outputs with default "0"	"0"
	2	rf_mode	RF mode enable for output amplifier	"0"
	1	ecl_thres_ctrl	M-counter related threshold to define the feedback clock duty cycle (4 or 2 counter periods on 'HIGH'). "0" threshold 4 (min. div. ratio 32, consider SDM state). "1" enables T2 (needed for divider ratios below 32)	"0"
	0	ecl_ctrl_en	Enable for ECL counter	"0"

Status Registers (address range "0x40" to "0x41"; registers are read-only).

Address	Bit	Name	Function	Default
0x40 Status	15...9	Unused		
	8	lock_detect	PLL lock detect	"1"
	7...4	version	Version number (1)	"0001"
	3...0	subversion	Subversion number (5)	"0101"
0x41 GPI_reg	15...0	Unused	General-purpose inputs	

1.11 PROTECTION NETWORKS



2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests - Chart F3

(a) High Temperature Reverse Bias Burn-in and the subsequent Final Measurements for HTRB Burn-in shall be omitted.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

As a minimum the information to be marked on the component or the primary package shall be:

(a) The ESCC qualified components symbol (for ESCC qualified components only).
(b) The ESCC Component Number (see Para. 1.4.1).
(c) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{case} = +22 ±3°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
V_{DDA} Dynamic Supply Current	I_{DDA}	3005	Pin Group 7, Note 1 V_{DDA} = 3.5V, V_{DDB} = 5.4V, GND = 0V	-	300	mA
V_{DDB} Dynamic Supply Current	I_{DDB}	3005	Pin Group 7, Note 1 V_{DDA} = 3.5V, V_{DDB} = 5.4V, GND = 0V	-	200	mA
V_{DDA} Standby Supply Current	I_{DDAQ}	3005	Pin Group 7, Note 2 V_{DDA} = 3.5V, V_{DDB} = 5.4V, GND = 0V	-	50	mA
V_{DDB} Standby Supply Current	I_{DDBQ}	3005	Pin Group 7, Note 2 V_{DDA} = 3.5V, V_{DDB} = 5.4V, GND = 0V	-	10	mA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Functional Test, Typical Voltage (Relaxed Limits)	-	3014	V_{DDA} = 3.3V, Note 3 V_{DDB} = 5.1V, GND = 0V	Go / No-Go		-
Functional Test, Minimum Voltage (Specified Limits)	-	3014	V_{DDA} = 3.1V, Note 3 V_{DDB} = 4.8V, GND = 0V	Go / No-Go		-
Functional Test, Maximum Voltage (Specified Limits)	-	3014	V_{DDA} = 3.5V, Note 3 V_{DDB} = 5.4V, GND = 0V	Go / No-Go		-
LDO Minimum Voltage Test (LDOA Domain)	V_{LLDOAx}	-	Pin Group 8, Note 4, V_{DDA} = 3.1V, V_{DDB} = 4.8V, GND = 0V	2.6	2.8	V
LDO Maximum Voltage Test (LDOA Domain)	V_{HLDOAx}	-	Pin Group 8, Note 4, V_{DDA} = 3.5V, V_{DDB} = 5.4V, GND = 0V	2.6	2.8	V
LDO Minimum Voltage Test (LDOB Domain)	V_{LLDOBx}	-	Pin Group 8, Note 4, V_{DDA} = 3.1V, V_{DDB} = 4.8V, GND = 0V	3.9	4.1	V
LDO Maximum Voltage Test (LDOB Domain)	V_{HLDOBx}	-	Pin Group 8, Note 4, V_{DDA} = 3.5V, V_{DDB} = 5.4V, GND = 0V	3.9	4.1	V
LDO Minimum Voltage Test (LDOC Domain)	V_{LLDOCx}	-	Pin Group 8, Note 4, V_{DDA} = 3.1V, V_{DDB} = 4.8V, GND = 0V	2.4	2.6	V
LDO Maximum Voltage Test (LDOC Domain)	V_{HLDOCx}	-	Pin Group 8, Note 4, V_{DDA} = 3.5V, V_{DDB} = 5.4V, GND = 0V	2.4	2.6	V
CMOS Min. Input Voltage, Low Level (Min V_{DDA})	V_{ILSPI}	-	Pin Group 1, Note 5 V_{DDA} = 3.1 V, GND = 0V	2.5	-	V
CMOS Min. Input Voltage, High Level (Max V_{DDA})	V_{IHSPI}	-	Pin Group 1, Note 5 V_{DDA} = 3.5 V, GND = 0V	2.5	-	V
CMOS SPI Clock Maximum Input Frequency (SPI_clk)	f_{HSPIR}	-	Read	-	3	kHz
CMOS SPI Clock Maximum Input Frequency (SPI_clk)	f_{HSPIW}	-	Write	-	1	MHz
CMOS Output Voltage, High Level (High Current Buffer)	V_{OHPFD}	3006	Pin Group 4, Note 6	2.25	-	V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Analog Lock Detect Voltage	-	3014	Note 3	Go / No-Go		-
Reference Clock Input Sensitivity (Min. Power)	P_{LREF}	-	Pin Group 2, Note 7 f_{INREF} = 105MHz	-12	-	dBm
External RF Input Sensitivity (Min. Power)	P_{LEXTL}	-	Pin Group 3, Note 8 f_{EXT} = 6.0GHz	-	-15	dBm
External RF Input Sensitivity (Min. Power)	P_{LEXTN}	-	Pin Group 3, Note 8 f_{EXT} = 9.8GHz	-	-10	dBm
External RF Input Sensitivity (Min. Power)	P_{LEXTH}	-	Pin Group 3, Note 8 f_{EXT} = 12.0GHz	-	-5	dBm
External RF Input Frequency (Min. Frequency)	f_{LEXT}	-	Pin Group 3, Note 8 P_{EXT} = -15dBm	6.0	-	GHz
External RF Input Frequency (Max. Frequency)	f_{HEXT}	-	Pin Group 3, Note 8 P_{EXT} = -5dBm	-	12.0	GHz
RF Output (Min. Frequency)	f_{LOUT}	-	Pin Group 6, Note 9	1.6	-	GHz
RF Output (Max. Frequency)	f_{HOUT}	-	Pin Group 6, Note 9	-	12.0	GHz
RF Output (Min. Frequency Overlap)	f_{DOUT}	-	Pin Group 6, Note 9 f_{OUT} = 6.0 to 12.0GHz	8	-	MHz
RF Output (Min. Power)	P_{LOUT}	-	Pin Group 6, Note 9 f_{OUT} = 1.6 to 12.0GHz	-10	-	dBm
Phase Noise at 1kHz Offset	PN_{1K}	-	Pin Group 6, Note 10 f_{OUT} = 9.8GHz	-	-87	dBc/Hz
Phase Noise at 10kHz Offset	PN_{10K}	-	Pin Group 6, Note 10 f_{OUT} = 9.8GHz	-	-92	dBc/Hz
Phase Noise at 100kHz Offset	PN_{100K}	-	Pin Group 6, Note 10 f_{OUT} = 9.8GHz	-	-98	dBc/Hz
Phase Noise at 1MHz Offset	PN_{1M}	-	Pin Group 6, Note 10 f_{OUT} = 9.8GHz	-	-110	dBc/Hz
Phase Noise at 10MHz Offset	PN_{10M}	-	Pin Group 6, Note 10 f_{OUT} = 9.8GHz	-	-130	dBc/Hz

NOTES:

1. Dynamic current: For measurement of the dynamic current, supply voltages are set to maximum.
2. Standby current: During standby current test, on-chip LDOs and ECL are set to off-mode.
3. Functional test: During functional test, synthesizer is programmed in typical operation mode.
4. LDO voltage output test: Output voltage of each LDO is measured. The measurement accuracy shall be better than 50mV.

5. Input voltages: Maximum SPI input voltage according to applied V_{DDA} voltage. Tests of read/write at the given minimum SPI input voltage shall be performed at the given minimum frequencies. During this test, the complete pin group 1 is tested and the resulting voltage values shall be recorded.
6. PFD output voltages: Output voltage tested at maximum output load (500Ω). During measurements, output voltage shall be monitored and recorded.
7. REF measurements: Nominal reference frequency is 100MHz. During the reference frequency input test, the synthesizer is programmed at minimum power level and frequency above nominal.
8. External RF input: Measurement in differential mode. Monitoring of the divided frequency output signal.
9. RF measurements: Test on internal VCO array and the VCO sub-bands. Single ended measurement of output power and frequency for the main octave and the divided output signal at RF_{OUTN}. RF_{OUTP} terminated by 50Ω and connected to on-board power detect diode. Frequency overlap versus adjacent bands is determined by measuring the low and high corner of each VCO sub-band. Measurement accuracy shall be better than 100KHz and 1dB.
10. Phase Noise measurements: Phase Noise measurements shall be performed at 9.8GHz (single sideband), reference frequency input set to 100MHz and 13dBm, with individual charge pump settings.

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{case} = +85 (+0 -5)°C and T_{case} = -40 (+5 -0)°C.

The characteristics, test methods, conditions and limits shall be the same as specified in Para. 2.3.1, Room Temperature Electrical Measurements, except as follows:

Characteristics	Symbols	Test Conditions (Note 1)	Limits		Units
			Min	Max	
External RF Input Sensitivity (Min. Power)	P_{LEXTL}	As per Para. 2.3.1	-	-10	dBm
External RF Input Sensitivity (Min. Power)	P_{LEXTN}	As per Para. 2.3.1	-	0	dBm
External RF Input Sensitivity (Min. Power)	P_{LEXTH}	As per Para. 2.3.1	-	10	dBm
RF Output (Frequency Overlap f_{OUT} at Low Temperature)	f_{LTOUT}	Pin Group 6, As per Para. 2.3.1 f_{OUT} = 6.0 to 12.0GHz, T_{case} = -40°C Note 2	4	-	MHz
RF Output (Frequency Overlap f_{OUT} at High Temperature)	f_{HTOUT}	Pin Group 6, As per Para. 2.3.1 f_{OUT} = 6.0 to 12.0GHz, T_{case} = +85°C	4	-	MHz
RF Output (Frequency Overlap f_{OUT} Delta Temperature)	f_{DTOUT}	Pin Group 6, As per Para. 2.3.1 f_{OUT} = 6.0 to 12.0GHz, between T_{case} = -40 and +85°C, Notes 2, 3	4	-	MHz
RF Output (Min. Power f_{OUT})	P_{LTOUT}	Pin Group 6, As per Para. 2.3.1 f_{OUT} = 1.6 to 12.0GHz, T_{case} = +85°C, Note 4	-20	-	dBm

NOTES:

1. RF output frequency and phase noise measurements: Measurement procedure for temperature-based RF measurements will be identical to the measurements in Para. 2.3.1.
2. See Para. 1.5 Note 3.
3. Temperature range frequency overlap: Overlap calculation is based on frequency measurements at high and low temperature corners (T_{case} = -40 and +85°C). Worst case frequency overlap is calculated from measurement results of adjacent bands (maximum vs. minimum frequency) at opposite temperature corners.
4. RF power measurements: Worst case at maximum frequency in combination with high temperature.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the parameter drift value measurements shall be performed at T_{case} = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1 Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
V_{DDA} Dynamic Supply Current	I_{DDA}	±70	-	300	mA
V_{DDB} Dynamic Supply Current	I_{DDB}	±70	-	200	mA
LDO Minimum Voltage Test (LDOA Domain)	V_{LLDOAx}	±100	2600	2800	mV
LDO Maximum Voltage Test (LDOA Domain)	V_{HLDOAx}	±100	2600	2800	mV
LDO Minimum Voltage Test (LDOB Domain)	V_{LLDOBx}	±100	3900	4100	mV
LDO Maximum Voltage Test (LDOB Domain)	V_{HLDOBx}	±100	3900	4100	mV
LDO Minimum Voltage Test (LDOC Domain)	V_{LLDOCx}	±100	2400	2600	mV
LDO Maximum Voltage Test (LDOC Domain)	V_{HLDOCx}	±100	2400	2600	mV

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{case} = +22 ±3°C.

The characteristics, test methods, conditions and limits shall be the same as specified in Para. 2.3.1, Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{case}	+125 (+0 -5) (Note 1)	°C
V_{DDA} Supply Voltage	V_{DDA}	3.3 (±5%)	V
V_{DDB} Supply Voltage	V_{DDB}	5.1 (±5%)	V
Operating Conditions	-	See Note 2	-

NOTES:

1. T_{amb} shall be adjusted to achieve T_{case} = +125°C. Additional variation of T_{case} by ±2°C due to varying sockets, R_{th} and DUT power dissipation, is permitted.
2. During Power Burn-in using a suitable test set-up, the components shall be connected to the supply voltages, and programmed with a typical operation mode. The overall current consumption shall be traced. For verification of component functionality, monitoring of register settings and the equivalent DC voltage level of the RF output power (1.6GHz) shall be performed during testing, on all components.

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified in Para. 2.6 for Power Burn-in.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in Para. 1.4.2 or in the Purchase Order.

In unbiased condition (OFF), all component inputs related to the two supply voltage domains (V_{DDA}, V_{DDB}) will be short-circuited to ground (GND).

In biased condition (ON), using a suitable test set-up, the components shall be connected to the voltage supplies, and programmed with a typical operation mode. Functionality during the test shall be verified by monitoring the RF outputs of the components.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation testing the devices shall have successfully met Para. 2.3.1, Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at T_{case} = +22 ±3°C.

The characteristics, test methods, conditions and limits to be measured during and on completion of irradiation testing shall be the same as specified in Para. 2.3.1, Room Temperature Electrical Measurements.

APPENDIX A

AGREED DEVIATIONS FOR IMST GmbH (D)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 2.8.2 Electrical Measurements for Total Dose Radiation Testing	Electrical measurements during irradiation testing, at intermediate points and at the end of exposure, may be performed on selected characteristics. **Note**: On completion of irradiation testing, final electrical measurements as specified in Para. 2.3.1, Room Temperature Electrical Measurements shall be performed.