INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS DIGITAL, MEMORY, RADIATION HARDENED, FIELD PROGRAMMABLE GATE ARRAY, 3M GATES WITH 2856Mb OF INDEPENDENT RAM

BASED ON TYPE NX1H35AS

ESCC Detail Specification No. 9304/010

Issue 1	September 2022

Document Custodian: European Space Agency – see https://escies.org

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DCR No.	CHANGE DESCRIPTION

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1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component number shall be constituted as follows:

Example: 930401001A

- Detail Specification Reference: 9304010
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: A (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Lead/Terminal Material and Finish (Note 1)	Weight Max g	Total Dose Radiation Level Letter (Note 2)
01	NX1H35AS	CQFP-352	D2	28.6	A [300krad(Si)]
02	NX1H35AS	CLGA-625	D2	8.8	A [300krad(Si)]

NOTES:

1. The lead/terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.
2. The total dose radiation level letter shall be as defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage. Functional performance for extended periods at the maximum ratings may adversely affect device reliability.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltages	V_{DD} V_{CC}	-0.3 to 1.32 -0.3 to 3.6	V	Notes 1, 2
Input Voltage Range	V_{IN}	-0.5 to 3.6	V	Note 2
Output Voltage Range	V_{OUT}	-0.5 to 1.32	V	Note 2
Analog Core Supply Transient Voltage	V_{DD2V5A}	-0.3 to 2.75	V	
Device Power Dissipation	P_D	2.5	W	
Operating Temperature Range	T_{op}	-55 to +125	°C	At junction Note 3
Storage Temperature Range	T_{stg}	-65 to +150	°C	
Junction Temperature	T_j	+150	°C	
Thermal Resistance, Junction to Case Variant 01 Variant 02	$R_{th(j-c)}$	 2.8 2.55	°C/W	Over T_{op} Note 3
Soldering Temperature CQFP-352 case CLGA-625 case	T_{sol}	 +260 +235	°C	Note 4

NOTES:

1. V_{DD} is for core. V_{CC} is for I/O.
2. With reference to V_{SS} = 0V.
3. The maximum operating temperature at the junction, $T_{op(max)}$, shall be determined by thermal analysis of the programmed FPGA by the user, and shall not exceed the specified maximum rating.
4. Duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.

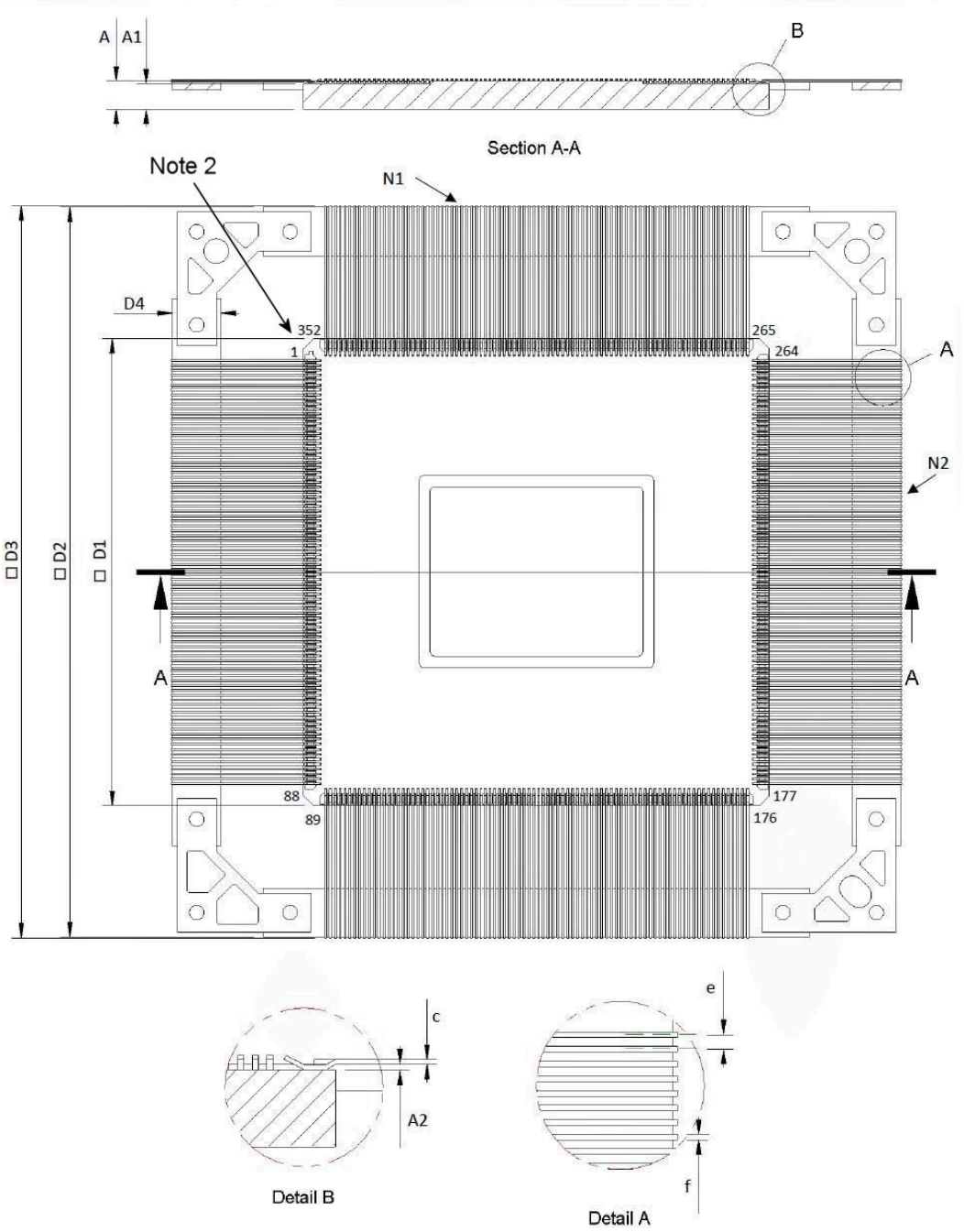
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800. All power, GND and signal terminals have a sensitivity range of 0 to ≤ 1000V except for Bank 1 I/O terminals, which have a sensitivity range of 0 to ≤ 750V.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.7.1 Ceramic Quad Flat Package (CQFP-352) - 352 Tied Leads



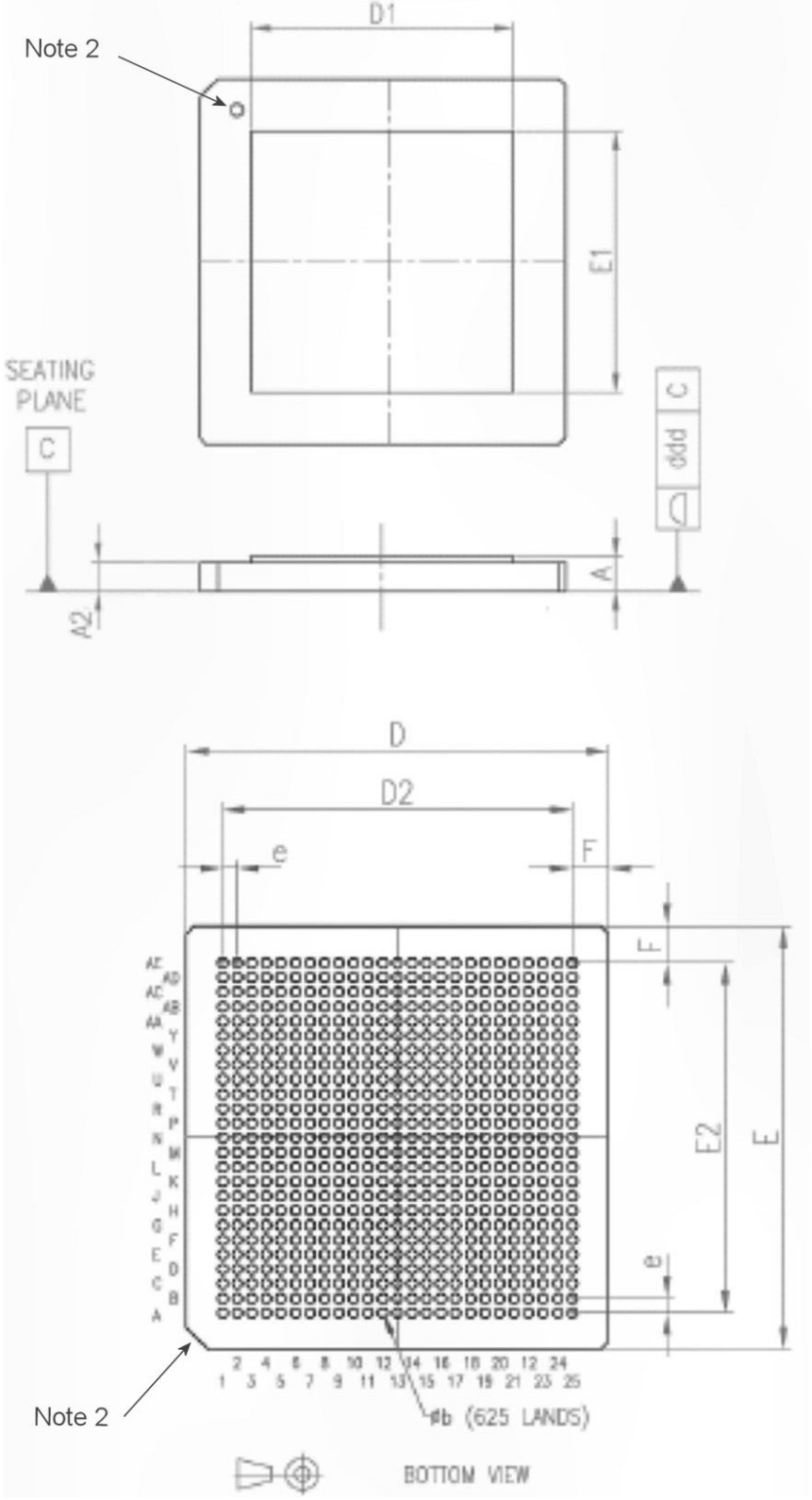
Symbols	Dimensions mm		Notes
	Min	Max	
A	2.52	3.51	
c	0.1	0.17	1
D1	47.67	48.33	
D2	74.62	75.38	

Symbols	Dimensions mm		Notes
	Min	Max	
D3	74.87	76.01	
D4	4.5	5.5	
e	0.5 BSC		
f			1
A1	0.17	0.24	
A2	2.37	2.87	1
N1	88 Leads		
N2	88 Leads		

NOTES:

1. Applies to all leads.
2. Terminal identification is specified by reference to the index corner as shown.

1.7.2 Ceramic Land Grid Array (CLGA-625) - 625 Lands

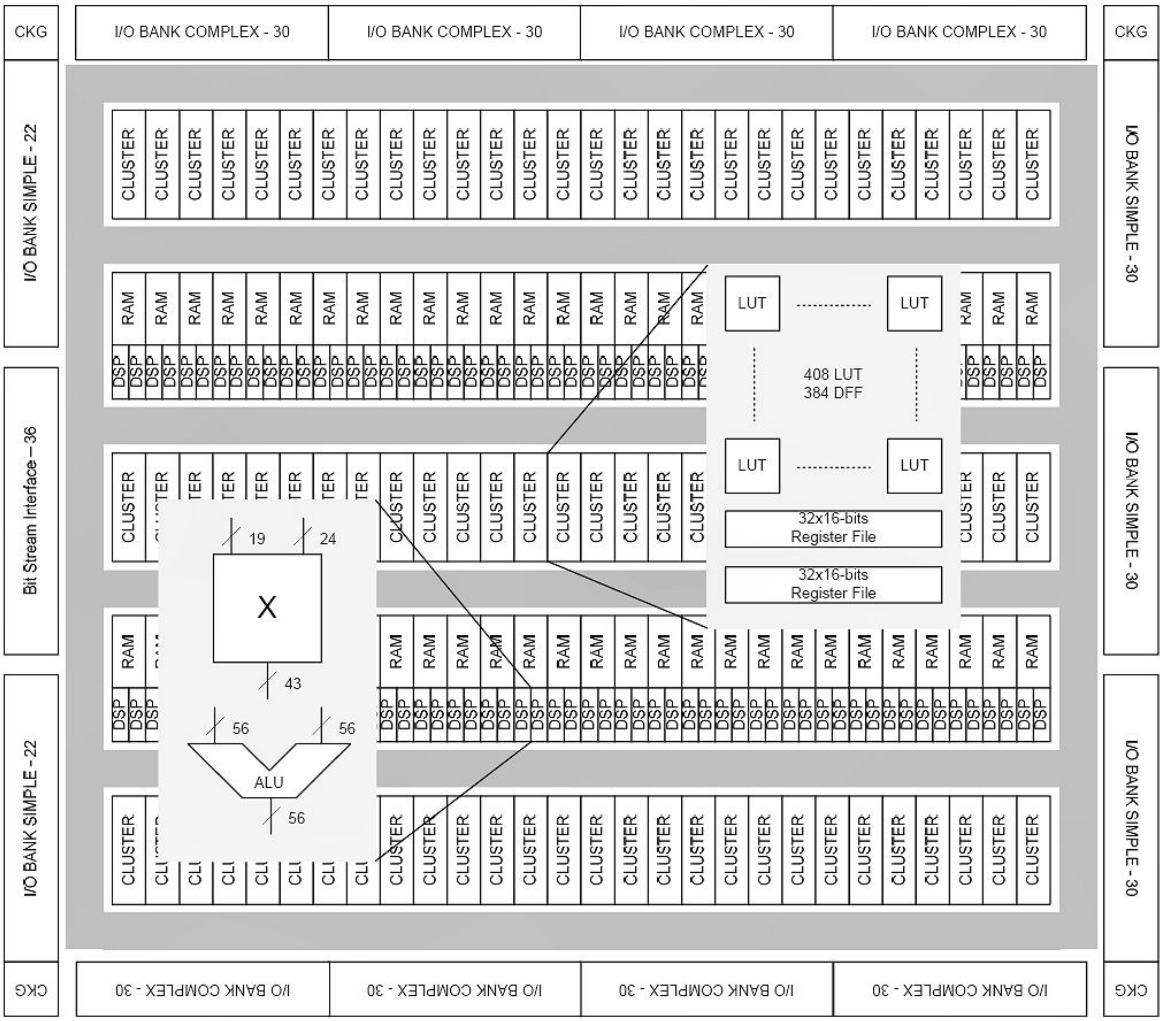


Symbols	Dimensions mm		Notes
	Min	Max	
A	3.29	4.02	
A2	3.06	3.74	
Øb	0.7	0.8	1
D / E	28.85	29.15	
D1	23.55	23.7	
E1	19.22	19.38	
D2 / E2	23.87	24.13	
e	0.87	1.13	
f	2.25	2.75	

NOTES:

1. Applies to all lands.
2. Terminal identification is specified by reference to the index corner as shown.

1.8 FUNCTIONAL DIAGRAM



NOTES:

1. Acronyms used are as follows:

   ALU = Arithmetic Logic Unit
   CKG = Clock Generator
   DFF = D-Type Flip Flop
   DSP = Digital Signal Processor
   LUT = Look Up Table

2. Variant 01 only has 192 of a total of 374 user-accessible I/Os from Simple Banks 0, 1, 6, 8 and Complex Banks 2, 5, 9, 12. See Para. 1.9.1.

3. Variant 02 has 374 user-accessible I/Os, i.e. all I/Os of Simple Banks 0, 1, 6, 7, 8 and all I/Os of Complex Banks 2, 3, 4, 5, 9, 10, 11, 12. See Para. 1.9.2.

1.9 PIN ASSIGNMENT

1.9.1 Pin Assignment for Variant 01 – CQFP-352 Case

Lead	Pin Name	Description
1	IO_B0D10N	Bank 0 (Simple) I/O
2	IO_B0D10P_CLK0	Bank 0 (Simple) I/O
3	VDDSENSE	VDDCORE Sense Return
4	GND	Bank 0 Internal GND Plane
5	VDDIO_0	Bank 0 I/O Supply
6	IO_B0D09N	Bank 0 (Simple) I/O
7	IO_B0D09P	Bank 0 (Simple) I/O
8	GNDCORE	Internal GND Plane
9	IO_B0D08N	Bank 0 (Simple) I/O
10	IO_B0D08P	Bank 0 (Simple) I/O
11	IO_B0D07N	Bank 0 (Simple) I/O
12	IO_B0D07P	Bank 0 (Simple) I/O
13	VDDIO_0	Bank 0 I/O Supply
14	IO_B0D06N	Bank 0 (Simple) I/O
15	IO_B0D06P	Bank 0 (Simple) I/O
16	IO_B0D05N	Bank 0 (Simple) I/O
17	IO_B0D05P	Bank 0 (Simple) I/O
18	VDD1V2	Internal VDD1V2 Plane
19	GND	Internal GND Plane
20	VDD2V5A	Internal VDD2V5A Ring
21	GND	Prog Bank Internal GND Plane
22	DOUT_P	Prog Bank Spacewire Configuration Output
23	DOUT_N	Prog Bank Spacewire Configuration Output
24	GND	Internal GND Plane
25	SOUT_P	Prog Bank Spacewire Configuration Output
26	SOUT_N	Prog Bank Spacewire Configuration Output
27	DIN_P	Prog Bank Spacewire Configuration Input
28	DIN_N	Prog Bank Spacewire Configuration Input
29	VDD1V2	Internal VDD1V2 Plane
30	SIN_P	Prog Bank Spacewire Configuration Input
31	SIN_N	Prog Bank Spacewire Configuration Input
32	VDDLVDS	Prog Bank 2.5V LVDS Supply (Spacewire)
33	RST_N	Prog Bank Hardware Reset Input
34	MODE0	Prog Bank Configuration Mode Input
35	MODE1	Prog Bank Configuration Mode Input
36	MODE2	Prog Bank Configuration Mode Input
37	GND	Internal GND Plane
38	MODE3	Prog Bank Configuration Mode Input
39	ERROR	Prog Bank Configuration Error Output
40	TCK	Prog Bank JTAG Clock Input
41	TRST	Prog Bank Active-low JTAG Reset Input
42	CLK	Prog Bank SlavePar Clock Input
43	TMS	Prog Bank JTAG TMS Input
44	TDI	Prog Bank JTAG TDI Input
45	TDO	Prog Bank JTAG TDO Output

Lead	Pin Name	Description
46	VDDIO_SERVICE	Prog Bank 3.3V Supply
47	GND	Internal GND Plane
48	READY	Prog Bank Configuration Ready Output
49	D0	Prog Bank SlavePar Data Bit 0
50	D1	Prog Bank SlavePar Data Bit 1
51	D2	Prog Bank SlavePar Data Bit 2
52	D3	Prog Bank SlavePar Data Bit 3
53	D4	Prog Bank SlavePar Data Bit 4
54	D5	Prog Bank SlavePar Data Bit 5
55	D6	Prog Bank SlavePar Data Bit 6
56	VDDIO_SERVICE	Prog Bank 3.3V Supply
57	GND	Internal GND Plane
58	D7	Prog Bank SlavePar Data Bit 7
59	D8	Prog Bank SlavePar Data Bit 8
60	D9	Prog Bank SlavePar Data Bit 9
61	D10	Prog Bank SlavePar Data Bit 10
62	D11	Prog Bank SlavePar Data Bit 11
63	D12	Prog Bank SlavePar Data Bit 12
64	D13	Prog Bank SlavePar Data Bit 13
65	D14	Prog Bank SlavePar Data Bit 14
66	GND	Internal GND Plane
67	D15	Prog Bank SlavePar Data Bit 15
68	CS_N	Prog Bank SlavePar Chip Select Input
69	WE_N	Prog Bank SlavePar Write Enable Input
70	DATA_OE	Prog Bank SlavePar Data Available Output
71	VDD2V5A	Internal VDD2V5A Ring
72	VDD1V2	Internal VDD1V2 Plane
73	GND	Internal GND Plane
74	VDDIO_1	Bank 1 I/O Supply
75	IO_B1D06N	Bank 1 (Simple) I/O
76	IO_B1D06P	Bank 1 (Simple) I/O
77	IO_B1D05N	Bank 1 (Simple) I/O
78	IO_B1D05P	Bank 1 (Simple) I/O
79	VDD1V2	Internal VDD1V2 Plane
80	IO_B1D04N	Bank 1 (Simple) I/O
81	IO_B1D04P	Bank 1 (Simple) I/O
82	IO_B1D03N	Bank 1 (Simple) I/O
83	IO_B1D03P	Bank 1 (Simple) I/O
84	GND	Internal GND Plane
85	VDDIO_1	Bank 1 I/O Supply
86	GND	Internal GND Plane
87	IO_B1D02N	Bank 1 (Simple) I/O
88	IO_B1D02P_CLK1	Bank 1 (Simple) I/O
89	IO_B1D01N	Bank 1 (Simple) I/O
90	IO_B1D01P_CLK0	Bank 1 (Simple) I/O
91	CG1_AGNDPLL	Clock Generator 1 PLL1 Analog GND
92	CG1_AVDDPLL	Clock Generator 1 PLL1 1.2V Analog Supply
93	GND	Internal GND Plane

Lead	Pin Name	Description
94	VDD1V2	Internal VDD1V2 Plane
95	IO_B2D15N_DQ_SWSI	Bank 2 (Complex) I/O
96	IO_B2D15P_DQ_SWSI	Bank 2 (Complex) I/O
97	IO_B2D14N_DQ_SWDI	Bank 2 (Complex) I/O
98	IO_B2D14P_DQ_SWDI	Bank 2 (Complex) I/O
99	GND	Internal GND Plane
100	VDDIO_2	Bank 2 I/O Supply
101	IO_B2D13N_DQS_SWSO	Bank 2 (Complex) I/O
102	IO_B2D13P_DQS_SWSO	Bank 2 (Complex) I/O
103	IO_B2D12N_DQ_SWDO	Bank 2 (Complex) I/O
104	IO_B2D12P_DQ_SWDO	Bank 2 (Complex) I/O
105	VTO_2	Bank 2 Termination Voltage
106	IO_B2D11N_DQ	Bank 2 (Complex) I/O
107	IO_B2D11P_DQ	Bank 2 (Complex) I/O
108	IO_B2D10N_DQ	Bank 2 (Complex) I/O
109	IO_B2D10P	Bank 2 (Complex) I/O
110	GND	Internal GND Plane
111	VDDIO_2	Bank 2 I/O Supply
112	IO_B2D09N	Bank 2 (Complex) I/O
113	IO_B2D09P_CLK1	Bank 2 (Complex) I/O
114	VDDS_2	Bank 2 Switch Supply
115	IO_B2D08N	Bank 2 (Complex) I/O
116	IO_B2D08P_CLK0	Bank 2 (Complex) I/O
117	IO_B2D07N	Bank 2 (Complex) I/O
118	IO_B2D07P	Bank 2 (Complex) I/O
119	GND	Internal GND Plane
120	VDDIO_2	Bank 2 I/O Supply
121	IO_B2D06N_CAL	Bank 2 (Complex) I/O
122	IO_B2D06P_DQ	Bank 2 (Complex) I/O
123	IO_B2D05N_DQ	Bank 2 (Complex) I/O
124	IO_B2D05P_DQ	Bank 2 (Complex) I/O
125	VTO_2	Bank 2 Termination Voltage
126	IO_B2D04N_DQ_SWSI	Bank 2 (Complex) I/O
127	IO_B2D04P_DQ_SWSI	Bank 2 (Complex) I/O
128	IO_B2D03N_DQS_SWDI	Bank 2 (Complex) I/O
129	IO_B2D03P_DQS_SWDI	Bank 2 (Complex) I/O
130	GND	Internal GND Plane
131	VDDIO_2	Bank 2 I/O Supply
132	IO_B2D02N_DQ_SWSO	Bank 2 (Complex) I/O
133	IO_B2D02P_DQ_SWSO	Bank 2 (Complex) I/O
134	IO_B2D01N_DQ_SWDO	Bank 2 (Complex) I/O
135	IO_B2D01P_DQ_SWDO	Bank 2 (Complex) I/O
136	VDD2V5A	Internal VDD2V5A Ring
137	GND	Internal GND Plane
138	VDD1V2	Internal VDD1V2 Plane
139	VDD2V5A	Internal VDD2V5A Ring
140	GND	Internal GND Plane
141	VDD1V2	Internal VDD1V2 Plane

Lead	Pin Name	Description
142	VDD2V5A	Internal VDD2V5A Ring
143	IO_B5D15N_DQ_SWSI	Bank 5 (Complex) I/O
144	IO_B5D15P_DQ_SWSI	Bank 5 (Complex) I/O
145	IO_B5D14N_DQ_SWDI	Bank 5 (Complex) I/O
146	IO_B5D14P_DQ_SWDI	Bank 5 (Complex) I/O
147	GND	Internal GND Plane
148	VDDIO_5	Bank 5 I/O Supply
149	IO_B5D13N_DQS_SWSO	Bank 5 (Complex) I/O
150	IO_B5D13P_DQS_SWSO	Bank 5 (Complex) I/O
151	IO_B5D12N_DQ_SWDO	Bank 5 (Complex) I/O
152	IO_B5D12P_DQ_SWDO	Bank 5 (Complex) I/O
153	VTO_5	Bank 5 Termination Voltage
154	IO_B5D11N_DQ	Bank 5 (Complex) I/O
155	IO_B5D11P_DQ	Bank 5 (Complex) I/O
156	IO_B5D10N_DQ	Bank 5 (Complex) I/O
157	IO_B5D10P	Bank 5 (Complex) I/O
158	GND	Internal GND Plane
159	VDDIO_5	Bank 5 I/O Supply
160	IO_B5D09N	Bank 5 (Complex) I/O
161	IO_B5D09P_CLK1	Bank 5 (Complex) I/O
162	VDDS_5	Bank 5 Switch Supply
163	IO_B5D08N	Bank 5 (Complex) I/O
164	IO_B5D08P_CLK0	Bank 5 (Complex) I/O
165	IO_B5D07N	Bank 5 (Complex) I/O
166	IO_B5D07P	Bank 5 (Complex) I/O
167	GND	Internal GND Plane
168	VDDIO_5	Bank 5 I/O Supply
169	IO_B5D06N_CAL	Bank 5 (Complex) I/O
170	IO_B5D06P_DQ	Bank 5 (Complex) I/O
171	IO_B5D05N_DQ	Bank 5 (Complex) I/O
172	IO_B5D05P_DQ	Bank 5 (Complex) I/O
173	VTO_5	Bank 5 Termination Voltage
174	IO_B5D04N_DQ_SWSI	Bank 5 (Complex) I/O
175	IO_B5D04P_DQ_SWSI	Bank 5 (Complex) I/O
176	IO_B5D03N_DQS_SWDI	Bank 5 (Complex) I/O
177	IO_B5D03P_DQS_SWDI	Bank 5 (Complex) I/O
178	GND	Internal GND Plane
179	VDDIO_5	Bank 5 I/O Supply
180	IO_B5D02N_DQ_SWSO	Bank 5 (Complex) I/O
181	IO_B5D02P_DQ_SWSO	Bank 5 (Complex) I/O
182	IO_B5D01N_DQ_SWDO	Bank 5 (Complex) I/O
183	IO_B5D01P_DQ_SWDO	Bank 5 (Complex) I/O
184	GND	Internal GND Plane
185	VDD1V2	Internal VDD1V2 Plane
186	CG2_AVDDPLL	Clock Generator 2 PLL2 1.2V Analog Supply
187	CG2_AGNDPLL	Clock Generator 2 PLL2 Analog GND
188	IO_B6D15N	Bank 6 (Simple) I/O
189	IO_B6D15P_CLK1	Bank 6 (Simple) I/O

Lead	Pin Name	Description
190	IO_B6D14N	Bank 6 (Simple) I/O
191	IO_B6D14P_CLK0	Bank 6 (Simple) I/O
192	IO_B6D13N	Bank 6 (Simple) I/O
193	IO_B6D13P	Bank 6 (Simple) I/O
194	VDD1V2	Internal VDD1V2 Plane
195	GND	Internal GND Plane
196	VDDIO_6	Bank 6 I/O Supply
197	IO_B6D12N	Bank 6 (Simple) I/O
198	IO_B6D12P	Bank 6 (Simple) I/O
199	IO_B6D11N	Bank 6 (Simple) I/O
200	IO_B6D11P	Bank 6 (Simple) I/O
201	GND	Internal GND Plane
202	IO_B6D10N	Bank 6 (Simple) I/O
203	IO_B6D10P	Bank 6 (Simple) I/O
204	IO_B6D09N	Bank 6 (Simple) I/O
205	IO_B6D09P	Bank 6 (Simple) I/O
206	GND	Internal GND Plane
207	VDDIO_6	Bank 6 I/O Supply
208	IO_B6D08N	Bank 6 (Simple) I/O
209	IO_B6D08P	Bank 6 (Simple) I/O
210	IO_B6D07N	Bank 6 (Simple) I/O
211	IO_B6D07P	Bank 6 (Simple) I/O
212	IO_B6D06N	Bank 6 (Simple) I/O
213	IO_B6D06P	Bank 6 (Simple) I/O
214	VDD1V2	Internal VDD1V2 Plane
215	IO_B6D05N	Bank 6 (Simple) I/O
216	IO_B6D05P	Bank 6 (Simple) I/O
217	GND	Internal GND Plane
218	VDD2V5A	Internal VDD2V5A Ring
219	VDD1V2	Internal VDD1V2 Plane
220	GND	Internal GND Plane
221	VDD2V5A	Internal VDD2V5A Ring
222	VDD1V2	Internal VDD1V2 Plane
223	IO_B8D12N	Bank 8 (Simple) I/O
224	IO_B8D12P	Bank 8 (Simple) I/O
225	IO_B8D11N	Bank 8 (Simple) I/O
226	IO_B8D11P	Bank 8 (Simple) I/O
227	GND	Internal GND Plane
228	IO_B8D10N	Bank 8 (Simple) I/O
229	IO_B8D10P	Bank 8 (Simple) I/O
230	IO_B8D09N	Bank 8 (Simple) I/O
231	IO_B8D09P	Bank 8 (Simple) I/O
232	GND	Internal GND Plane
233	VDDIO_8	Bank 8 I/O Supply
234	IO_B8D08N	Bank 8 (Simple) I/O
235	IO_B8D08P	Bank 8 (Simple) I/O
236	IO_B8D07N	Bank 8 (Simple) I/O
237	IO_B8D07P	Bank 8 (Simple) I/O

Lead	Pin Name	Description
238	IO_B8D06N	Bank 8 (Simple) I/O
239	IO_B8D06P	Bank 8 (Simple) I/O
240	VDD1V2	Internal VDD1V2 Plane
241	IO_B8D05N	Bank 8 (Simple) I/O
242	IO_B8D05P	Bank 8 (Simple) I/O
243	IO_B8D04N	Bank 8 (Simple) I/O
244	IO_B8D04P	Bank 8 (Simple) I/O
245	GND	Internal GND Plane
246	VDDIO_8	Bank 8 I/O Supply
247	GND	Internal GND Plane
248	IO_B8D03N	Bank 8 (Simple) I/O
249	IO_B8D03P	Bank 8 (Simple) I/O
250	IO_B8D02N	Bank 8 (Simple) I/O
251	IO_B8D02P_CLK1	Bank 8 (Simple) I/O
252	IO_B8D01N	Bank 8 (Simple) I/O
253	IO_B8D01P_CLK0	Bank 8 (Simple) I/O
254	CG3_AGNDPLL	Clock Generator 3 PLL3 Analog GND
255	CG3_AVDDPLL	Clock Generator 3 PLL3 1.2V Analog Supply
256	GND	Internal GND Plane
257	VDD1V2	Internal VDD1V2 Plane
258	IO_B9D15N_DQ_SWSI	Bank 9 (Complex) I/O
259	IO_B9D15P_DQ_SWSI	Bank 9 (Complex) I/O
260	IO_B9D14N_DQ_SWDI	Bank 9 (Complex) I/O
261	IO_B9D14P_DQ_SWDI	Bank 9 (Complex) I/O
262	GND	Internal GND Plane
263	VDDIO_9	Bank 9 I/O Supply
264	IO_B9D13N_DQS_SWSO	Bank 9 (Complex) I/O
265	IO_B9D13P_DQS_SWSO	Bank 9 (Complex) I/O
266	IO_B9D12N_DQ_SWDO	Bank 9 (Complex) I/O
267	IO_B9D12P_DQ_SWDO	Bank 9 (Complex) I/O
268	VTO_9	Bank 9 Termination Voltage
269	IO_B9D11N_DQ	Bank 9 (Complex) I/O
270	IO_B9D11P_DQ	Bank 9 (Complex) I/O
271	IO_B9D10N_DQ	Bank 9 (Complex) I/O
272	IO_B9D10P	Bank 9 (Complex) I/O
273	GND	Internal GND Plane
274	VDDIO_9	Bank 9 I/O Supply
275	IO_B9D09N	Bank 9 (Complex) I/O
276	IO_B9D09P_CLK1	Bank 9 (Complex) I/O
277	VDDS_9	Bank 9 Switch Supply
278	IO_B9D08N	Bank 9 (Complex) I/O
279	IO_B9D08P_CLK0	Bank 9 (Complex) I/O
280	IO_B9D07N	Bank 9 (Complex) I/O
281	IO_B9D07P	Bank 9 (Complex) I/O
282	GND	Bank 9 Internal GND Plane
283	VDDIO_9	Bank 9 I/O Supply
284	IO_B9D06N_CAL	Bank 9 (Complex) I/O
285	IO_B9D06P_DQ	Bank 9 (Complex) I/O

Lead	Pin Name	Description
286	IO_B9D05N_DQ	Bank 9 (Complex) I/O
287	IO_B9D05P_DQ	Bank 9 (Complex) I/O
288	VTO_9	Bank 9 Termination Voltage
289	IO_B9D04N_DQ_SWSI	Bank 9 (Complex) I/O
290	IO_B9D04P_DQ_SWSI	Bank 9 (Complex) I/O
291	IO_B9D03N_DQS_SWDI	Bank 9 (Complex) I/O
292	IO_B9D03P_DQS_SWDI	Bank 9 (Complex) I/O
293	GND	Internal GND Plane
294	VDDIO_9	Bank 9 I/O Supply
295	IO_B9D02N_DQ_SWSO	Bank 9 (Complex) I/O
296	IO_B9D02P_DQ_SWSO	Bank 9 (Complex) I/O
297	IO_B9D01N_DQ_SWDO	Bank 9 (Complex) I/O
298	IO_B9D01P_DQ_SWDO	Bank 9 (Complex) I/O
299	VDD2V5A	Internal VDD2V5A Ring
300	GND	Internal GND Plane
301	VDD1V2	Internal VDD1V2 Plane
302	VDD2V5A	Internal VDD2V5A Ring
303	GND	Internal GND Plane
304	VDD1V2	Internal VDD1V2 Plane
305	VDD2V5A	Internal VDD2V5A Ring
306	IO_B12D15N_DQ_SWSI	Bank 12 (Complex) I/O
307	IO_B12D15P_DQ_SWSI	Bank 12 (Complex) I/O
308	IO_B12D14N_DQ_SWDI	Bank 12 (Complex) I/O
309	IO_B12D14P_DQ_SWDI	Bank 12 (Complex) I/O
310	GND	Internal GND Plane
311	VDDIO_12	Bank 12 I/O Supply
312	IO_B12D13N_DQS_SWSO	Bank 12 (Complex) I/O
313	IO_B12D13P_DQS_SWSO	Bank 12 (Complex) I/O
314	IO_B12D12N_DQ_SWDO	Bank 12 (Complex) I/O
315	IO_B12D12P_DQ_SWDO	Bank 12 (Complex) I/O
316	VTO_12	Bank 12 Termination Voltage
317	IO_B12D11N_DQ	Bank 12 (Complex) I/O
318	IO_B12D11P_DQ	Bank 12 (Complex) I/O
319	IO_B12D10N_DQ	Bank 12 (Complex) I/O
320	IO_B12D10P	Bank 12 (Complex) I/O
321	GND	Internal GND Plane
322	VDDIO_12	Bank 12 I/O Supply
323	IO_B12D09N	Bank 12 (Complex) I/O
324	IO_B12D09P_CLK1	Bank 12 (Complex) I/O
325	VDDS_12	Bank 12 Switch Supply
326	IO_B12D08N	Bank 12 (Complex) I/O
327	IO_B12D08P_CLK0	Bank 12 (Complex) I/O
328	IO_B12D07N	Bank 12 (Complex) I/O
329	IO_B12D07P	Bank 12 (Complex) I/O
330	GND	Bank 12 Internal GND Plane
331	VDDIO_12	Bank 12 I/O Supply
332	IO_B12D06N_CAL	Bank 12 (Complex) I/O
333	IO_B12D06P_DQ	Bank 12 (Complex) I/O

Lead	Pin Name	Description
334	IO_B12D05N_DQ	Bank 12 (Complex) I/O
335	IO_B12D05P_DQ	Bank 12 (Complex) I/O
336	VTO_12	Bank 12 Termination Voltage
337	IO_B12D04N_DQ_SWSI	Bank 12 (Complex) I/O
338	IO_B12D04P_DQ_SWSI	Bank 12 (Complex) I/O
339	IO_B12D03N_DQS_SWDI	Bank 12 (Complex) I/O
340	IO_B12D03P_DQS_SWDI	Bank 12 (Complex) I/O
341	GND	Internal GND Plane
342	VDDIO_12	Bank 12 I/O Supply
343	IO_B12D02N_DQ_SWSO	Bank 12 (Complex) I/O
344	IO_B12D02P_DQ_SWSO	Bank 12 (Complex) I/O
345	IO_B12D01N_DQ_SWDO	Bank 12 (Complex) I/O
346	IO_B12D01P_DQ_SWDO	Bank 12 (Complex) I/O
347	GND	Internal GND Plane
348	VDD1V2	Internal VDD1V2 Plane
349	CG0_AVDDPLL	Clock Generator 0 PLL0 1.2V Analog Supply
350	CG0_AGNDPLL	Clock Generator 0 PLL0 Analog GND
351	IO_B0D11N	Bank 0 (Simple) I/O
352	IO_B0D11P_CLK1	Bank 0 (Simple) I/O

1.9.2 Pin Assignment for Variant 02 – CLGA-652 Case

Land	Pin Name	Description
A1	IO_B12D04P_DQ_SWSI	Bank 12 (Complex) I/O
A2	VDDIO_12	Bank 12 I/O Supply
A3	VDDS_12	Bank 12 Switch Supply
A4	IO_B12D08P_CLK0	Bank 12 (Complex) I/O
A5	VDDIO_12	Bank 12 I/O Supply
A6	VDD2V5A	Internal VDD2V5A Ring
A7	GND	Internal GND Plane
A8	IO_B11D05P_DQ	Bank 11 (Complex) I/O
A9	VDDIO_11	Bank 11 I/O Supply
A10	VDDS_11	Bank 11 Switch Supply
A11	IO_B11D09P	Bank 11 (Complex) I/O
A12	VTO_11	Bank 11 Termination Voltage
A13	VDD2V5A	Internal VDD2V5A Ring
A14	IO_B10D03P_DQS_SWDI	Bank 10 (Complex) I/O
A15	VDDIO_10	Bank 10 I/O Supply
A16	VDDS_10	Bank 10 Switch Supply
A17	IO_B10D12N_DQ_SWDO	Bank 10 (Complex) I/O
A18	IO_B10D12P_DQ_SWDO	Bank 10 (Complex) I/O
A19	GND	Internal GND Plane
A20	VDD2V5A	Internal VDD2V5A Ring
A21	VDDIO_9	Bank 9 I/O Supply
A22	IO_B9D06P_DQ	Bank 9 (Complex) I/O
A23	VDDS_9	Bank 9 Switch Supply
A24	VDDIO_9	Bank 9 I/O Supply
A25	IO_B9D12P_DQ_SWDO	Bank 9 (Complex) I/O
B1	IO_B12D04N_DQ_SWSI	Bank 12 (Complex) I/O
B2	VTO_12	Bank 12 Termination Voltage

Land	Pin Name	Description
B3	GND	Internal GND Plane
B4	IO_B12D08N	Bank 12 (Complex) I/O
B5	VTO_12	Bank 12 Termination Voltage
B6	GND	Internal GND Plane
B7	VDDIO_11	Bank 11 I/O Supply
B8	VTO_11	Bank 11 Termination Voltage
B9	IO_B11D05N_DQ	Bank 11 (Complex) I/O
B10	GND	Internal GND Plane
B11	IO_B11D09N	Bank 11 (Complex) I/O
B12	IO_B11D13P_DQS_SWSO	Bank 11 (Complex) I/O
B13	VDDIO_10	Bank 10 I/O Supply
B14	VTO_10	Bank 10 Termination Voltage
B15	IO_B10D03N_DQS_SWDI	Bank 10 (Complex) I/O
B16	GND	Internal GND Plane
B17	IO_B10D07P	Bank 10 (Complex) I/O
B18	VTO_10	Bank 10 Termination Voltage
B19	VDDIO_10	Bank 10 I/O Supply
B20	GND	Internal GND Plane
B21	VTO_9	Bank 9 Termination Voltage
B22	IO_B9D06N_CAL	Bank 9 (Complex) I/O
B23	GND	Internal GND Plane
B24	VTO_9	Bank 9 Termination Voltage
B25	IO_B9D12N_DQ_SWDO	Bank 9 (Complex) I/O
C1	VDDIO_12	Bank 12 I/O Supply
C2	IO_B12D05N_DQ	Bank 12 (Complex) I/O
C3	IO_B12D05P_DQ	Bank 12 (Complex) I/O
C4	IO_B12D07P	Bank 12 (Complex) I/O
C5	IO_B12D10P	Bank 12 (Complex) I/O
C6	IO_B12D12P_DQ_SWDO	Bank 12 (Complex) I/O
C7	IO_B12D12N_DQ_SWDO	Bank 12 (Complex) I/O
C8	IO_B11D03P_DQS_SWDI	Bank 11 (Complex) I/O
C9	IO_B11D06P_DQ	Bank 11 (Complex) I/O
C10	IO_B11D08N	Bank 11 (Complex) I/O
C11	IO_B11D08P	Bank 11 (Complex) I/O
C12	IO_B11D13N_DQS_SWSO	Bank 11 (Complex) I/O
C13	GND	Bank 11 Internal GND Plane
C14	GND	Internal GND Plane
C15	IO_B10D02P_DQ_SWSO	Bank 10 (Complex) I/O
C16	IO_B10D04P_DQ_SWSI	Bank 10 (Complex) I/O
C17	IO_B10D07N	Bank 10 (Complex) I/O
C18	IO_B10D13P_DQS_SWSO	Bank 10 (Complex) I/O
C19	IO_B9D01N_DQ_SWDO	Bank 9 (Complex) I/O
C20	IO_B9D01P_DQ_SWDO	Bank 9 (Complex) I/O
C21	IO_B9D07P	Bank 9 (Complex) I/O
C22	IO_B9D08P_CLK0	Bank 9 (Complex) I/O
C23	IO_B9D11N_DQ	Bank 9 (Complex) I/O
C24	IO_B9D11P_DQ	Bank 9 (Complex) I/O
C25	VDDIO_9	Bank 9 I/O Supply
D1	CG0_AVDDPLL	Clock Generator 0 PLL0 1.2V Analog Supply
D2	GND	Bank 12 Internal GND Plane
D3	IO_B12D03P_DQS_SWDI	Bank 12 (Complex) I/O
D4	IO_B12D06P_DQ	Bank 12 (Complex) I/O
D5	IO_B12D07N	Bank 12 (Complex) I/O

Land	Pin Name	Description
D6	IO_B12D10N_DQ	Bank 12 (Complex) I/O
D7	IO_B12D11P_DQ	Bank 12 (Complex) I/O
D8	IO_B11D03N_DQS_SWDI	Bank 11 (Complex) I/O
D9	IO_B11D06N_CAL	Bank 11 (Complex) I/O
D10	IO_B11D07P	Bank 11 (Complex) I/O
D11	IO_B11D10P	Bank 11 (Complex) I/O
D12	VDDIO_11	Bank 11 I/O Supply
D13	IO_B11D14P_DQ_SWDI	Bank 11 (Complex) I/O
D14	IO_B10D02N_DQ_SWSO	Bank 10 (Complex) I/O
D15	IO_B10D04N_DQ_SWSI	Bank 10 (Complex) I/O
D16	IO_B10D08N	Bank 10 (Complex) I/O
D17	IO_B10D08P	Bank 10 (Complex) I/O
D18	IO_B10D13N_DQS_SWSO	Bank 10 (Complex) I/O
D19	IO_B9D02P_DQ_SWSO	Bank 9 (Complex) I/O
D20	IO_B9D03P_DQS_SWDI	Bank 9 (Complex) I/O
D21	IO_B9D07N	Bank 9 (Complex) I/O
D22	IO_B9D08N	Bank 9 (Complex) I/O
D23	IO_B9D13P_DQS_SWSO	Bank 9 (Complex) I/O
D24	GND	Bank 9 Internal GND Plane
D25	CG3_AVDDPLL	Clock Generator 3 PLL3 1.2V Analog Supply
E1	CG0_AGNDPLL	Clock Generator 0 PLL0 Analog GND
E2	CG0_ASUBPLL	Clock Generator 0 PLL0 Substrate → AGND
E3	IO_B12D01P_DQ_SWDO	Bank 12 (Complex) I/O
E4	IO_B12D03N_DQS_SWDI	Bank 12 (Complex) I/O
E5	IO_B12D06N_CAL	Bank 12 (Complex) I/O
E6	IO_B12D09P_CLK1	Bank 12 (Complex) I/O
E7	IO_B12D11N_DQ	Bank 12 (Complex) I/O
E8	IO_B11D01P_DQ_SWDO	Bank 11 (Complex) I/O
E9	IO_B11D04P_DQ_SWSI	Bank 11 (Complex) I/O
E10	IO_B11D07N	Bank 11 (Complex) I/O
E11	IO_B11D10N_DQ	Bank 11 (Complex) I/O
E12	GND	Internal GND Plane
E13	IO_B11D14N_DQ_SWDI	Bank 11 (Complex) I/O
E14	IO_B10D01P_DQ_SWDO	Bank 10 (Complex) I/O
E15	IO_B10D05P_DQ	Bank 10 (Complex) I/O
E16	IO_B10D09P	Bank 10 (Complex) I/O
E17	IO_B10D14P_DQ_SWDI	Bank 10 (Complex) I/O
E18	IO_B9D02N_DQ_SWSO	Bank 9 (Complex) I/O
E19	IO_B9D03N_DQS_SWDI	Bank 9 (Complex) I/O
E20	IO_B9D04P_DQ_SWSI	Bank 9 (Complex) I/O
E21	IO_B9D09P_CLK1	Bank 9 (Complex) I/O
E22	IO_B9D13N_DQS_SWSO	Bank 9 (Complex) I/O
E23	IO_B9D15P_DQ_SWSI	Bank 9 (Complex) I/O
E24	CG3_ASUBPLL	Clock Generator 3 PLL3 Substrate → AGND
E25	CG3_AGNDPLL	Clock Generator 3 PLL3 Analog GND
F1	VDDIO_0	Bank 0 I/O Supply
F2	GND	Bank 0 Internal GND Plane
F3	IO_B0D08N	Bank 0 (Simple) I/O
F4	IO_B12D01N_DQ_SWDO	Bank 12 (Complex) I/O
F5	IO_B12D02P_DQ_SWSO	Bank 12 (Complex) I/O
F6	IO_B12D02N_DQ_SWSO	Bank 12 (Complex) I/O
F7	IO_B12D09N	Bank 12 (Complex) I/O
F8	IO_B12D15P_DQ_SWSI	Bank 12 (Complex) I/O

Land	Pin Name	Description
F9	IO_B11D01N_DQ_SWDO	Bank 11 (Complex) I/O
F10	IO_B11D04N_DQ_SWSI	Bank 11 (Complex) I/O
F11	IO_B11D11P_DQ	Bank 11 (Complex) I/O
F12	VDDIO_11	Bank 11 I/O Supply
F13	IO_B10D01N_DQ_SWDO	Bank 10 (Complex) I/O
F14	IO_B10D05N_DQ	Bank 10 (Complex) I/O
F15	IO_B10D09N	Bank 10 (Complex) I/O
F16	IO_B10D10P	Bank 10 (Complex) I/O
F17	IO_B10D14N_DQ_SWDI	Bank 10 (Complex) I/O
F18	GND	Internal GND Plane
F19	IO_B9D04N_DQ_SWSI	Bank 9 (Complex) I/O
F20	IO_B9D09N	Bank 9 (Complex) I/O
F21	IO_B9D14P_DQ_SWDI	Bank 9 (Complex) I/O
F22	IO_B9D15N_DQ_SWSI	Bank 9 (Complex) I/O
F23	IO_B8D01N	Bank 8 (Simple) I/O
F24	GND	Internal GND Plane
F25	VDDIO_8	Bank 8 I/O Supply
G1	IO_B0D05P	Bank 0 (Simple) I/O
G2	IO_B0D05N	Bank 0 (Simple) I/O
G3	IO_B0D08P	Bank 0 (Simple) I/O
G4	IO_B0D09P	Bank 0 (Simple) I/O
G5	IO_B0D09N	Bank 0 (Simple) I/O
G6	IO_B0D11P_CLK1	Bank 0 (Simple) I/O
G7	IO_B12D13P_DQS_SWSO	Bank 12 (Complex) I/O
G8	IO_B12D14P_DQ_SWDI	Bank 12 (Complex) I/O
G9	IO_B12D15N_DQ_SWSI	Bank 12 (Complex) I/O
G10	IO_B11D02P_DQ_SWSO	Bank 11 (Complex) I/O
G11	IO_B11D11N_DQ	Bank 11 (Complex) I/O
G12	IO_B11D15P_DQ_SWSI	Bank 11 (Complex) I/O
G13	GND	Internal GND Plane
G14	IO_B10D06P_DQ	Bank 10 (Complex) I/O
G15	IO_B10D10N_DQ	Bank 10 (Complex) I/O
G16	IO_B10D15P_DQ_SWSI	Bank 10 (Complex) I/O
G17	VDDIO_9	Bank 9 I/O Supply
G18	IO_B9D05P_DQ	Bank 9 (Complex) I/O
G19	IO_B9D10P	Bank 9 (Complex) I/O
G20	IO_B9D14N_DQ_SWDI	Bank 9 (Complex) I/O
G21	IO_B8D02N	Bank 8 (Simple) I/O
G22	IO_B8D02P_CLK1	Bank 8 (Simple) I/O
G23	IO_B8D01P_CLK0	Bank 8 (Simple) I/O
G24	IO_B8D03N	Bank 8 (Simple) I/O
G25	IO_B8D03P	Bank 8 (Simple) I/O
H1	IO_B0D01P	Bank 0 (Simple) I/O
H2	IO_B0D01N	Bank 0 (Simple) I/O
H3	IO_B0D06P	Bank 0 (Simple) I/O
H4	IO_B0D06N	Bank 0 (Simple) I/O
H5	IO_B0D07P	Bank 0 (Simple) I/O
H6	IO_B0D07N	Bank 0 (Simple) I/O
H7	IO_B0D11N	Bank 0 (Simple) I/O
H8	IO_B12D13N_DQS_SWSO	Bank 12 (Complex) I/O
H9	IO_B12D14N_DQ_SWDI	Bank 12 (Complex) I/O
H10	IO_B11D02N_DQ_SWSO	Bank 11 (Complex) I/O
H11	IO_B11D12P_DQ_SWDO	Bank 11 (Complex) I/O

Land	Pin Name	Description
H12	IO_B11D15N_DQ_SWSI	Bank 11 (Complex) I/O
H13	VDDIO_10	Bank 10 I/O Supply
H14	IO_B10D06N_CAL	Bank 10 (Complex) I/O
H15	IO_B10D11P_DQ	Bank 10 (Complex) I/O
H16	IO_B10D15N_DQ_SWSI	Bank 10 (Complex) I/O
H17	IO_B9D05N_DQ	Bank 9 (Complex) I/O
H18	IO_B9D10N_DQ	Bank 9 (Complex) I/O
H19	IO_B8D04N	Bank 8 (Simple) I/O
H20	IO_B8D04P	Bank 8 (Simple) I/O
H21	IO_B8D07N	Bank 8 (Simple) I/O
H22	IO_B8D07P	Bank 8 (Simple) I/O
H23	IO_B8D08N	Bank 8 (Simple) I/O
H24	IO_B8D08P	Bank 8 (Simple) I/O
H25	IO_B8D11N	Bank 8 (Simple) I/O
J1	VDDIO_0	Bank 0 I/O Supply
J2	GND	Internal GND Plane
J3	IO_B0D02P	Bank 0 (Simple) I/O
J4	IO_B0D02N	Bank 0 (Simple) I/O
J5	IO_B0D03P	Bank 0 (Simple) I/O
J6	IO_B0D03N	Bank 0 (Simple) I/O
J7	IO_B0D10P_CLK0	Bank 0 (Simple) I/O
J8	IO_B0D10N	Bank 0 (Simple) I/O
J9	VDDIO_12	Bank 12 I/O Supply
J10	GND	Internal GND Plane
J11	IO_B11D12N_DQ_SWDO	Bank 11 (Complex) I/O
J12	GND	Internal GND Plane
J13	VDD1V2	Internal VDD1V2 Plane
J14	GND	Internal GND Plane
J15	IO_B10D11N_DQ	Bank 10 (Complex) I/O
J16	IO_B8D05N	Bank 8 (Simple) I/O
J17	IO_B8D05P	Bank 8 (Simple) I/O
J18	IO_B8D06N	Bank 8 (Simple) I/O
J19	IO_B8D06P	Bank 8 (Simple) I/O
J20	IO_B8D09N	Bank 8 (Simple) I/O
J21	IO_B8D09P	Bank 8 (Simple) I/O
J22	IO_B8D10N	Bank 8 (Simple) I/O
J23	IO_B8D10P	Bank 8 (Simple) I/O
J24	IO_B8D11P	Bank 8 (Simple) I/O
J25	VDDIO_8	Bank 8 I/O Supply
K1	VDD2V5A	Internal VDD2V5A Ring
K2	GND	Prog Bank Internal GND Plane
K3	DOUT_N	Prog Bank Spacewire Configuration Output
K4	DOUT_P	Prog Bank Spacewire Configuration Output
K5	SOUT_N	Prog Bank Spacewire Configuration Output
K6	SOUT_P	Prog Bank Spacewire Configuration Output
K7	IO_B0D04P	Bank 0 (Simple) I/O
K8	IO_B0D04N	Bank 0 (Simple) I/O
K9	GND	Internal GND Plane
K10	VDD1V2	Internal VDD1V2 Plane
K11	GND	Internal GND Plane
K12	VDD1V2	Internal VDD1V2 Plane
K13	GND	Internal GND Plane
K14	VDD1V2	Internal VDD1V2 Plane

Land	Pin Name	Description
K15	GND	Internal GND Plane
K16	VDD1V2	Internal VDD1V2 Plane
K17	GND	Internal GND Plane
K18	VDDIO_8	Bank 8 I/O Supply
K19	IO_B8D14N	Bank 8 (Simple) I/O
K20	IO_B8D13N	Bank 8 (Simple) I/O
K21	IO_B8D13P	Bank 8 (Simple) I/O
K22	IO_B8D12N	Bank 8 (Simple) I/O
K23	IO_B8D12P	Bank 8 (Simple) I/O
K24	GND	Internal GND Plane
K25	VDD2V5A	Internal VDD2V5A Ring
L1	VDDLVDS	Prog Bank 2.5V LVDS Supply (Spacewire)
L2	DIN_N	Prog Bank Spacewire Configuration Input
L3	DIN_P	Prog Bank Spacewire Configuration Input
L4	SIN_N	Prog Bank Spacewire Configuration Input
L5	SIN_P	Prog Bank Spacewire Configuration Input
L6	RST_N	Prog Bank Hardware Reset Input
L7	MODE1	Prog Bank Configuration Mode Input
L8	MODE0	Prog Bank Configuration Mode Input
L9	VDDIO_0	Bank 0 I/O Supply
L10	GND	Internal GND Plane
L11	VDD1V2	Internal VDD1V2 Plane
L12	GND	Internal GND Plane
L13	VDD1V2	Internal VDD1V2 Plane
L14	GND	Internal GND Plane
L15	VDD1V2	Internal VDD1V2 Plane
L16	GND	Internal GND Plane
L17	IO_B8D15N	Bank 8 (Simple) I/O
L18	IO_B8D15P	Bank 8 (Simple) I/O
L19	IO_B8D14P	Bank 8 (Simple) I/O
L20	IO_B7D01N	Bank 7 (Simple) I/O
L21	IO_B7D01P	Bank 7 (Simple) I/O
L22	IO_B7D02N	Bank 7 (Simple) I/O
L23	IO_B7D02P	Bank 7 (Simple) I/O
L24	GND	Internal GND Plane
L25	VDDIO_7	Bank 7 I/O Supply
M1	TDI	Prog Bank JTAG TDI Input
M2	TMS	Prog Bank JTAG TMS Input
M3	CLK	Prog Bank SlavePar Clock Input
M4	TRST	Prog Bank Active-low JTAG Reset Input
M5	TCK	Prog Bank JTAG Clock Input
M6	GND	Internal GND Plane
M7	VDDIO_SERVICE	Prog Bank 3.3V Supply
M8	MODE2	Prog Bank Configuration Mode Input
M9	GND	Internal GND Plane
M10	VDD1V2	Internal VDD1V2 Plane
M11	GND	Internal GND Plane
M12	VDD1V2	Internal VDD1V2 Plane
M13	GND	Internal GND Plane
M14	VDD1V2	Internal VDD1V2 Plane
M15	GND	Internal GND Plane
M16	VDD1V2	Internal VDD1V2 Plane
M17	GND	Internal GND Plane

Land	Pin Name	Description
M18	IO_B7D06N	Bank 7 (Simple) I/O
M19	IO_B7D06P	Bank 7 (Simple) I/O
M20	IO_B7D05N	Bank 7 (Simple) I/O
M21	IO_B7D05P	Bank 7 (Simple) I/O
M22	IO_B7D04N	Bank 7 (Simple) I/O
M23	IO_B7D04P	Bank 7 (Simple) I/O
M24	IO_B7D03N	Bank 7 (Simple) I/O
M25	IO_B7D03P	Bank 7 (Simple) I/O
N1	VDDIO_SERVICE	Prog Bank 3.3V Supply
N2	GND	Internal GND Plane
N3	TDO	Prog Bank JTAG TDO Output
N4	GND	Internal GND Plane
N5	VDDIO_SERVICE	Prog Bank 3.3V Supply
N6	READY	Prog Bank Configuration Ready Output
N7	ERROR	Prog Bank Configuration Error Output
N8	MODE3	Prog Bank Configuration Mode Input
N9	VDDSENSE	VDDCORE Sense Return
N10	GND	Internal GND Plane
N11	VDD1V2	Internal VDD1V2 Plane
N12	GND	Internal GND Plane
N13	VDD1V2	Internal VDD1V2 Plane
N14	GND	Internal GND Plane
N15	VDD1V2	Internal VDD1V2 Plane
N16	GND	Internal GND Plane
N17	VDD1V2	Internal VDD1V2 Plane
N18	IO_B7D10N	Bank 7 (Simple) I/O
N19	IO_B7D10P	Bank 7 (Simple) I/O
N20	IO_B7D09N	Bank 7 (Simple) I/O
N21	IO_B7D09P	Bank 7 (Simple) I/O
N22	IO_B7D08N	Bank 7 (Simple) I/O
N23	IO_B7D08P	Bank 7 (Simple) I/O
N24	IO_B7D07N	Bank 7 (Simple) I/O
N25	IO_B7D07P	Bank 7 (Simple) I/O
P1	D4	Prog Bank SlavePar Data Bit 4
P2	D3	Prog Bank SlavePar Data Bit 3
P3	D2	Prog Bank SlavePar Data Bit 2
P4	D1	Prog Bank SlavePar Data Bit 1
P5	D0	Prog Bank SlavePar Data Bit 0
P6	D10	Prog Bank SlavePar Data Bit 10
P7	D9	Prog Bank SlavePar Data Bit 9
P8	D8	Prog Bank SlavePar Data Bit 8
P9	GND	Internal GND Plane
P10	VDD1V2	Internal VDD1V2 Plane
P11	GND	Internal GND Plane
P12	VDD1V2	Internal VDD1V2 Plane
P13	GND	Internal GND Plane
P14	VDD1V2	Internal VDD1V2 Plane
P15	GND	Internal GND Plane
P16	VDD1V2	Internal VDD1V2 Plane
P17	GND	Internal GND Plane
P18	IO_B7D14N	Bank 7 (Simple) I/O
P19	IO_B7D14P	Bank 7 (Simple) I/O
P20	IO_B7D13N	Bank 7 (Simple) I/O

Land	Pin Name	Description
P21	IO_B7D13P	Bank 7 (Simple) I/O
P22	IO_B7D12N	Bank 7 (Simple) I/O
P23	IO_B7D12P	Bank 7 (Simple) I/O
P24	IO_B7D11N	Bank 7 (Simple) I/O
P25	IO_B7D11P	Bank 7 (Simple) I/O
R1	VDDIO_SERVICE	Prog Bank 3.3V Supply
R2	CS_N	Prog Bank SlavePar Chip Select Input
R3	D7	Prog Bank SlavePar Data Bit 7
R4	D6	Prog Bank SlavePar Data Bit 6
R5	D5	Prog Bank SlavePar Data Bit 5
R6	D13	Prog Bank SlavePar Data Bit 13
R7	D12	Prog Bank SlavePar Data Bit 12
R8	D11	Prog Bank SlavePar Data Bit 11
R9	GND	Internal GND Plane
R10	GND	Internal GND Plane
R11	VDD1V2	Internal VDD1V2 Plane
R12	GND	Internal GND Plane
R13	VDD1V2	Internal VDD1V2 Plane
R14	GND	Internal GND Plane
R15	VDD1V2	Internal VDD1V2 Plane
R16	GND	Internal GND Plane
R17	IO_B6D06N	Bank 6 (Simple) I/O
R18	IO_B6D05N	Bank 6 (Simple) I/O
R19	IO_B6D05P	Bank 6 (Simple) I/O
R20	IO_B7D15N	Bank 7 (Simple) I/O
R21	IO_B7D15P	Bank 7 (Simple) I/O
R22	VDDIO_7	Bank 7 I/O Supply
R23	GND	Internal GND Plane
R24	GND	Internal GND Plane
R25	VDDIO_7	Bank 7 I/O Supply
T1	VDD2V5A	Internal VDD2V5A Ring
T2	GND	Internal GND Plane
T3	DATA_OE	Prog Bank SlavePar Data Available Output
T4	WE_N	Prog Bank SlavePar Write Enable Input
T5	D15	Prog Bank SlavePar Data Bit 15
T6	D14	Prog Bank SlavePar Data Bit 14
T7	IO_B1D11P	Bank 1 (Simple) I/O
T8	IO_B1D11N	Bank 1 (Simple) I/O
T9	VDDIO_1	Bank 1 I/O Supply
T10	VDD1V2	Internal VDD1V2 Plane
T11	GND	Internal GND Plane
T12	VDD1V2	Internal VDD1V2 Plane
T13	GND	Internal GND Plane
T14	VDD1V2	Internal VDD1V2 Plane
T15	GND	Internal GND Plane
T16	VDD1V2	Internal VDD1V2 Plane
T17	IO_B6D06P	Bank 6 (Simple) I/O
T18	IO_B6D07N	Bank 6 (Simple) I/O
T19	IO_B6D04N	Bank 6 (Simple) I/O
T20	VDDIO_6	Bank 6 I/O Supply
T21	GND	Internal GND Plane
T22	IO_B6D02N	Bank 6 (Simple) I/O
T23	GND	Internal GND Plane

Land	Pin Name	Description
T24	VDDIO_6	Bank 6 I/O Supply
T25	VDD2V5A	Internal VDD2V5A Ring
U1	VDDIO_1	Bank 1 I/O Supply
U2	GND	Internal GND Plane
U3	IO_B1D09P	Bank 1 (Simple) I/O
U4	IO_B1D09N	Bank 1 (Simple) I/O
U5	IO_B1D08N	Bank 1 (Simple) I/O
U6	IO_B1D10P	Bank 1 (Simple) I/O
U7	IO_B1D10N	Bank 1 (Simple) I/O
U8	IO_B1D05N	Bank 1 (Simple) I/O
U9	IO_B2D08N	Bank 2 (Complex) I/O
U10	IO_B2D08P_CLK0	Bank 2 (Complex) I/O
U11	IO_B3D08N	Bank 3 (Complex) I/O
U12	VDD1V2	Internal VDD1V2 Plane
U13	GND	Internal GND Plane
U14	VDD1V2	Internal VDD1V2 Plane
U15	IO_B4D08N	Bank 4 (Complex) I/O
U16	IO_B4D08P	Bank 4 (Complex) I/O
U17	GND	Internal GND Plane
U18	IO_B6D07P	Bank 6 (Simple) I/O
U19	IO_B6D08N	Bank 6 (Simple) I/O
U20	IO_B6D04P	Bank 6 (Simple) I/O
U21	IO_B6D03N	Bank 6 (Simple) I/O
U22	IO_B6D03P	Bank 6 (Simple) I/O
U23	IO_B6D02P	Bank 6 (Simple) I/O
U24	IO_B6D01N	Bank 6 (Simple) I/O
U25	IO_B6D01P	Bank 6 (Simple) I/O
V1	IO_B1D06P	Bank 1 (Simple) I/O
V2	IO_B1D06N	Bank 1 (Simple) I/O
V3	IO_B1D07P	Bank 1 (Simple) I/O
V4	IO_B1D07N	Bank 1 (Simple) I/O
V5	IO_B1D08P	Bank 1 (Simple) I/O
V6	IO_B1D04N	Bank 1 (Simple) I/O
V7	IO_B1D05P	Bank 1 (Simple) I/O
V8	IO_B2D09N	Bank 2 (Complex) I/O
V9	VDDIO_2	Bank 2 I/O Supply
V10	IO_B3D09N	Bank 3 (Complex) I/O
V11	IO_B3D08P	Bank 3 (Complex) I/O
V12	IO_B3D01N_DQ_SWDO	Bank 3 (Complex) I/O
V13	GND	Internal GND Plane
V14	IO_B4D09N	Bank 4 (Complex) I/O
V15	IO_B4D09P	Bank 4 (Complex) I/O
V16	IO_B4D07N	Bank 4 (Complex) I/O
V17	VDDIO_5	Bank 5 I/O Supply
V18	IO_B5D12N_DQ_SWDO	Bank 5 (Complex) I/O
V19	IO_B6D09N	Bank 6 (Simple) I/O
V20	IO_B6D08P	Bank 6 (Simple) I/O
V21	IO_B6D10N	Bank 6 (Simple) I/O
V22	IO_B6D10P	Bank 6 (Simple) I/O
V23	IO_B6D11N	Bank 6 (Simple) I/O
V24	IO_B6D11P	Bank 6 (Simple) I/O
V25	IO_B6D12N	Bank 6 (Simple) I/O
W1	IO_B1D02P_CLK1	Bank 1 (Simple) I/O

Land	Pin Name	Description
W2	IO_B1D02N	Bank 1 (Simple) I/O
W3	IO_B1D03P	Bank 1 (Simple) I/O
W4	IO_B1D03N	Bank 1 (Simple) I/O
W5	IO_B1D04P	Bank 1 (Simple) I/O
W6	IO_B2D11N_DQ	Bank 2 (Complex) I/O
W7	IO_B2D10N_DQ	Bank 2 (Complex) I/O
W8	IO_B2D09P_CLK1	Bank 2 (Complex) I/O
W9	GND	Internal GND Plane
W10	IO_B3D09P	Bank 3 (Complex) I/O
W11	IO_B3D07N	Bank 3 (Complex) I/O
W12	IO_B3D01P_DQ_SWDO	Bank 3 (Complex) I/O
W13	VDDIO_3	Bank 3 I/O Supply
W14	GND	Internal GND Plane
W15	IO_B4D10N_DQ	Bank 4 (Complex) I/O
W16	IO_B4D07P	Bank 4 (Complex) I/O
W17	IO_B5D14N_DQ_SWDI	Bank 5 (Complex) I/O
W18	IO_B5D12P_DQ_SWDO	Bank 5 (Complex) I/O
W19	IO_B5D11N_DQ	Bank 5 (Complex) I/O
W20	IO_B6D09P	Bank 6 (Simple) I/O
W21	IO_B6D14N	Bank 6 (Simple) I/O
W22	IO_B6D14P_CLK0	Bank 6 (Simple) I/O
W23	IO_B6D13N	Bank 6 (Simple) I/O
W24	IO_B6D13P	Bank 6 (Simple) I/O
W25	IO_B6D12P	Bank 6 (Simple) I/O
Y1	VDDIO_1	Bank 1 I/O Supply
Y2	GND	Internal GND Plane
Y3	IO_B1D01P_CLK0	Bank 1 (Simple) I/O
Y4	IO_B1D01N	Bank 1 (Simple) I/O
Y5	IO_B2D12P_DQ_SWDO	Bank 2 (Complex) I/O
Y6	IO_B2D11P_DQ	Bank 2 (Complex) I/O
Y7	IO_B2D10P	Bank 2 (Complex) I/O
Y8	IO_B2D07N	Bank 2 (Complex) I/O
Y9	IO_B3D11N_DQ	Bank 3 (Complex) I/O
Y10	IO_B3D10N_DQ	Bank 3 (Complex) I/O
Y11	IO_B3D07P	Bank 3 (Complex) I/O
Y12	IO_B3D02N_DQ_SWSO	Bank 3 (Complex) I/O
Y13	IO_B4D15N_DQ_SWSI	Bank 4 (Complex) I/O
Y14	VDDIO_4	Bank 4 I/O Supply
Y15	IO_B4D10P	Bank 4 (Complex) I/O
Y16	IO_B4D06N_CAL	Bank 4 (Complex) I/O
Y17	IO_B5D14P_DQ_SWDI	Bank 5 (Complex) I/O
Y18	IO_B5D13N_DQS_SWSO	Bank 5 (Complex) I/O
Y19	IO_B5D11P_DQ	Bank 5 (Complex) I/O
Y20	IO_B5D08N	Bank 5 (Complex) I/O
Y21	IO_B5D08P_CLK0	Bank 5 (Complex) I/O
Y22	IO_B6D15N	Bank 6 (Simple) I/O
Y23	IO_B6D15P_CLK1	Bank 6 (Simple) I/O
Y24	GND	Internal GND Plane
Y25	VDDIO_6	Bank 4 I/O Supply
AA1	CG1_AGNDPLL	Clock Generator 1 PLL1 Analog GND
AA2	CG1_ASUBPLL	Clock Generator 1 PLL1 Substrate → AGND
AA3	IO_B2D13N_DQS_SWSO	Bank 2 (Complex) I/O
AA4	IO_B2D12N_DQ_SWDO	Bank 2 (Complex) I/O

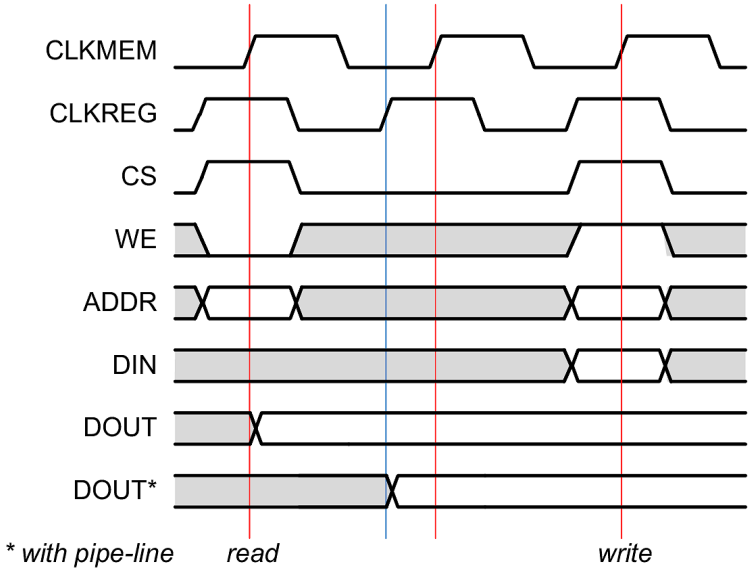
Land	Pin Name	Description
AA5	IO_B2D04N_DQ_SWSI	Bank 2 (Complex) I/O
AA6	IO_B2D02N_DQ_SWSO	Bank 2 (Complex) I/O
AA7	IO_B2D01N_DQ_SWDO	Bank 2 (Complex) I/O
AA8	IO_B2D07P	Bank 2 (Complex) I/O
AA9	IO_B3D11P_DQ	Bank 3 (Complex) I/O
AA10	IO_B3D10P	Bank 3 (Complex) I/O
AA11	IO_B3D03N_DQS_SWDI	Bank 3 (Complex) I/O
AA12	IO_B3D02P_DQ_SWSO	Bank 3 (Complex) I/O
AA13	IO_B4D15P_DQ_SWSI	Bank 3 (Complex) I/O
AA14	GND	Internal GND Plane
AA15	IO_B4D05N_DQ	Bank 4 (Complex) I/O
AA16	IO_B4D06P_DQ	Bank 4 (Complex) I/O
AA17	IO_B4D02N_DQ_SWSO	Bank 4 (Complex) I/O
AA18	IO_B5D13P_DQS_SWSO	Bank 5 (Complex) I/O
AA19	IO_B5D10N_DQ	Bank 5 (Complex) I/O
AA20	IO_B5D10P	Bank 5 (Complex) I/O
AA21	IO_B5D07N	Bank 5 (Complex) I/O
AA22	IO_B5D04N_DQ_SWSI	Bank 5 (Complex) I/O
AA23	IO_B5D03N_DQS_SWDI	Bank 5 (Complex) I/O
AA24	CG2_ASUBPLL	Clock Generator 2 PLL2 Substrate → AGND
AA25	CG2_AGNDPLL	Clock Generator 2 PLL2 Analog GND
AB1	CG1_AVDDPLL	Clock Generator 1 PLL1 1.2V Analog Supply
AB2	GND	Internal GND Plane
AB3	IO_B2D13P_DQS_SWSO	Bank 2 (Complex) I/O
AB4	IO_B2D06N_CAL	Bank 2 (Complex) I/O
AB5	IO_B2D04P_DQ_SWSI	Bank 2 (Complex) I/O
AB6	IO_B2D02P_DQ_SWSO	Bank 2 (Complex) I/O
AB7	IO_B2D01P_DQ_SWDO	Bank 2 (Complex) I/O
AB8	IO_B3D15N_DQ_SWSI	Bank 3 (Complex) I/O
AB9	IO_B3D14N_DQ_SWDI	Bank 3 (Complex) I/O
AB10	IO_B3D13N_DQS_SWSO	Bank 3 (Complex) I/O
AB11	IO_B3D06N_CAL	Bank 3 (Complex) I/O
AB12	IO_B3D03P_DQS_SWDI	Bank 3 (Complex) I/O
AB13	IO_B4D14N_DQ_SWDI	Bank 4 (Complex) I/O
AB14	VDDIO_4	Bank 4 I/O Supply
AB15	IO_B4D11N_DQ	Bank 4 (Complex) I/O
AB16	IO_B4D05P_DQ	Bank 4 (Complex) I/O
AB17	IO_B4D02P_DQ_SWSO	Bank 4 (Complex) I/O
AB18	IO_B4D01N_DQ_SWDO	Bank 4 (Complex) I/O
AB19	IO_B5D15N_DQ_SWSI	Bank 5 (Complex) I/O
AB20	IO_B5D09N	Bank 5 (Complex) I/O
AB21	IO_B5D07P	Bank 5 (Complex) I/O
AB22	IO_B5D04P_DQ_SWSI	Bank 5 (Complex) I/O
AB23	IO_B5D03P_DQS_SWDI	Bank 5 (Complex) I/O
AB24	GND	Internal GND Plane
AB25	CG2_AVDDPLL	Clock Generator 2 PLL2 1.2V Analog Supply
AC1	VDDIO_2	Bank 2 I/O Supply
AC2	IO_B2D14N_DQ_SWDI	Bank 2 (Complex) I/O
AC3	IO_B2D14P_DQ_SWDI	Bank 2 (Complex) I/O
AC4	IO_B2D06P_DQ	Bank 2 (Complex) I/O
AC5	IO_B2D03N_DQS_SWDI	Bank 2 (Complex) I/O
AC6	IO_B2D03P_DQS_SWDI	Bank 2 (Complex) I/O
AC7	IO_B3D15P_DQ_SWSI	Bank 3 (Complex) I/O

Land	Pin Name	Description
AC8	IO_B3D14P_DQ_SWDI	Bank 3 (Complex) I/O
AC9	IO_B3D13P_DQS_SWSO	Bank 3 (Complex) I/O
AC10	IO_B3D06P_DQ	Bank 3 (Complex) I/O
AC11	IO_B3D05N_DQ	Bank 3 (Complex) I/O
AC12	IO_B3D05P_DQ	Bank 3 (Complex) I/O
AC13	IO_B4D14P_DQ_SWDI	Bank 4 (Complex) I/O
AC14	IO_B4D13N_DQS_SWSO	Bank 4 (Complex) I/O
AC15	IO_B4D11P_DQ	Bank 4 (Complex) I/O
AC16	IO_B4D04N_DQ_SWSI	Bank 4 (Complex) I/O
AC17	IO_B4D04P_DQ_SWSI	Bank 4 (Complex) I/O
AC18	IO_B4D01P_DQ_SWDO	Bank 4 (Complex) I/O
AC19	IO_B5D15P_DQ_SWSI	Bank 5 (Complex) I/O
AC20	IO_B5D09P_CLK1	Bank 5 (Complex) I/O
AC21	IO_B5D06N_CAL	Bank 5 (Complex) I/O
AC22	IO_B5D06P_DQ	Bank 5 (Complex) I/O
AC23	IO_B5D02P_DQ_SWSO	Bank 5 (Complex) I/O
AC24	IO_B5D02N_DQ_SWSO	Bank 5 (Complex) I/O
AC25	VDDIO_5	Bank 5 I/O Supply
AD1	IO_B2D15N_DQ_SWSI	Bank 2 (Complex) I/O
AD2	VTO_2	Bank 2 Termination Voltage
AD3	GND	Internal GND Plane
AD4	IO_B2D05N_DQ	Bank 2 (Complex) I/O
AD5	VTO_2	Bank 2 Termination Voltage
AD6	GND	Internal GND Plane
AD7	VDDIO_3	Bank 3 I/O Supply
AD8	VTO_3	Bank 3 Termination Voltage
AD9	IO_B3D12N_DQ_SWDO	Bank 3 (Complex) I/O
AD10	GND	Internal GND Plane
AD11	IO_B3D04N_DQ_SWSI	Bank 3 (Complex) I/O
AD12	VTO_3	Bank 3 Termination Voltage
AD13	VDDIO_3	Bank 3 I/O Supply
AD14	IO_B4D13P_DQS_SWSO	Bank 4 (Complex) I/O
AD15	IO_B4D12N_DQ_SWDO	Bank 4 (Complex) I/O
AD16	GND	Internal GND Plane
AD17	IO_B4D03N_DQS_SWDI	Bank 4 (Complex) I/O
AD18	VTO_4	Bank 4 Termination Voltage
AD19	VDDIO_4	Bank 4 I/O Supply
AD20	GND	Internal GND Plane
AD21	VTO_5	Bank 5 Termination Voltage
AD22	IO_B5D05N_DQ	Bank 5 (Complex) I/O
AD23	GND	Internal GND Plane
AD24	VTO_5	Bank 5 Termination Voltage
AD25	IO_B5D01N_DQ_SWDO	Bank 5 (Complex) I/O
AE1	IO_B2D15P_DQ_SWSI	Bank 2 (Complex) I/O
AE2	VDDIO_2	Bank 2 I/O Supply
AE3	VDDS_2	Bank 2 Switch Supply
AE4	IO_B2D05P_DQ	Bank 2 (Complex) I/O
AE5	VDDIO_2	Bank 2 I/O Supply
AE6	VDD2V5A	Internal VDD2V5A Ring
AE7	GND	Internal GND Plane
AE8	IO_B3D12P_DQ_SWDO	Bank 3 (Complex) I/O
AE9	VDDIO_3	Bank 3 I/O Supply
AE10	VDDS_3	Bank 3 Switch Supply

Land	Pin Name	Description
AE11	IO_B3D04P_DQ_SWSI	Bank 3 (Complex) I/O
AE12	GND	Internal GND Plane
AE13	VDD2V5A	Internal VDD2V5A Ring
AE14	VTO_4	Bank 4 Termination Voltage
AE15	IO_B4D12P_DQ_SWDO	Bank 4 (Complex) I/O
AE16	VDDS_4	Bank 4 Switch Supply
AE17	VDDIO_4	Bank 4 I/O Supply
AE18	IO_B4D03P_DQS_SWDI	Bank 4 (Complex) I/O
AE19	GND	Internal GND Plane
AE20	VDD2V5A	Internal VDD2V5A Ring
AE21	VDDIO_5	Bank 5 I/O Supply
AE22	IO_B5D05P_DQ	Bank 5 (Complex) I/O
AE23	VDDS_5	Bank 5 Switch Supply
AE24	VDDIO_5	Bank 4 I/O Supply
AE25	IO_B5D01P_DQ_SWDO	Bank 5 (Complex) I/O

1.10 TIMING DIAGRAM

READ/WRITE TIMING

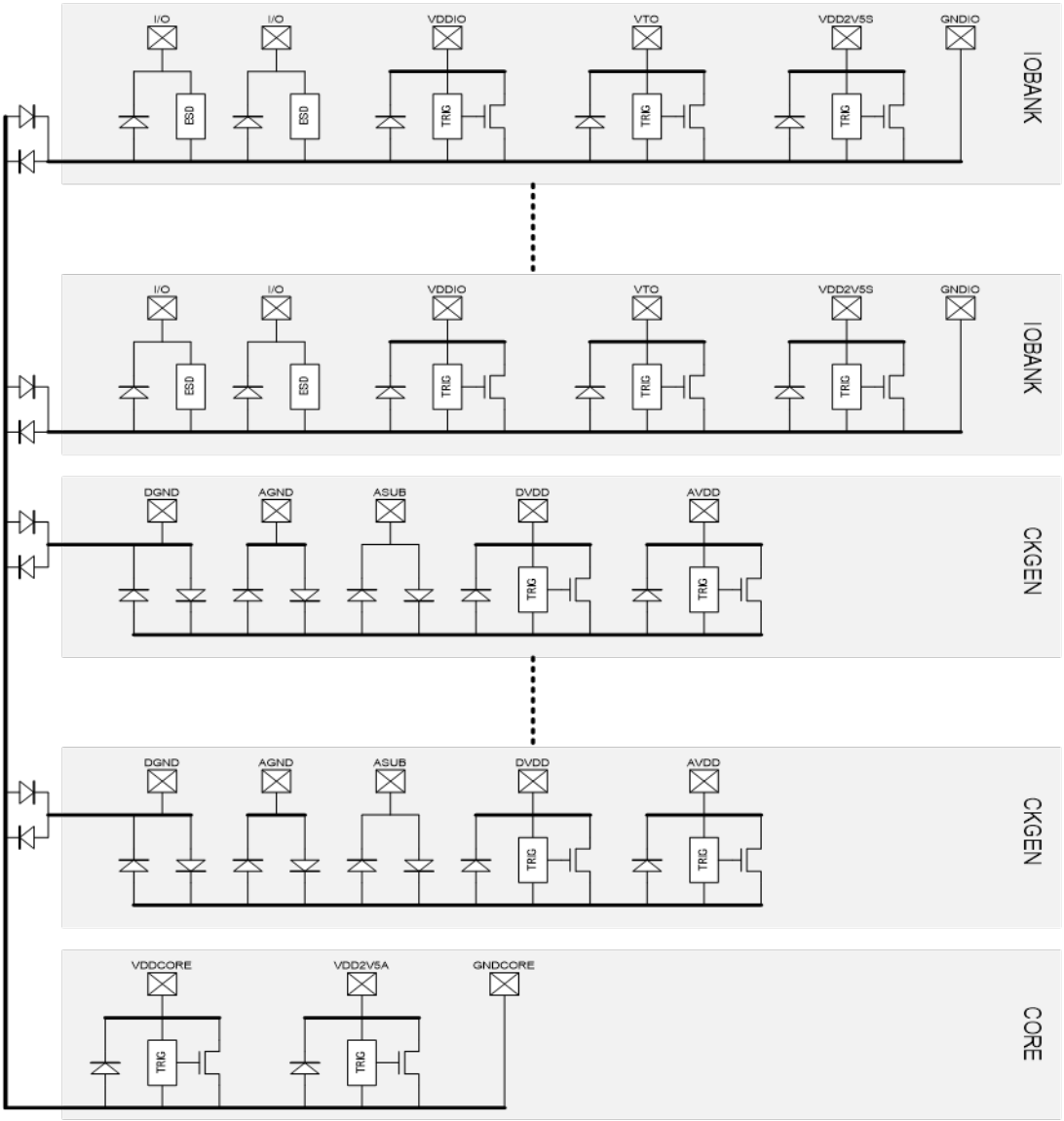


NOTES:

1. Memory Read Cycle: When the memory is enabled in a memory read cycle (CSx = 1 and WEx = 0), the address is stored on the rising memory clock (CLKMEMx) edge, and data appears at the output bus after the access time. The chronogram is shown on the Figure 6. The optional output pipeline registers are available in all memory configurations. These registers are clocked by CLKREGx signals, which may be different from the main memory clock signals CLKMEMx. The memory pipeline register may be forced to zero by asserting the synchronous RSTx signal. Both memory clocks and register clocks may have individually configured polarity. The presence of output pipeline registers is determined independently for each port.
2. Memory Write Cycle: When the memory is enabled in a memory write cycle (ENBx = 1 and WEx = 1), the address is stored and data is written to the memory on the rising edge of the memory clock (CLKMEMx). During a write access DOUT maintains the output previously generated by a read operation.

3. Simultaneous write by both ports of a same memory location or simultaneous read/write are not allowed.

1.11 I/O PROTECTION NETWORK



2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC

requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests – Chart F3

High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

As a minimum the information to be marked on the component shall be:

(a) The ESCC qualified components symbol (for ESCC qualified components only).
(b) The ESCC Component Number (see Para. 1.4.1).
(c) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated notes are given in Para. 2.3.3.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb} = +22 ±3 °C.

Characteristics	Symbols	Test Conditions (Note 1)	Limits		Units
			Min	Max	
Functional Test 1 (Structural Tests 1, 2, 3) (Note 2)	-		N/A		-
Total Supply Current in Reset Condition	I_{DD}		-	800	mA
Cold Sparing, Simple I/O Banks	I_{CSS}	V_{DD} = 0V	-	1	µA
Cold Sparing, Complex I/O Banks	I_{CSC}	V_{DD} = 0V	-	2	µA
Functional Test 2 (Structural Test 4) (Note 3)	-		N/A		-
LVDS Leakage Current, High Level	I_{OH_LVDS}	V_{DD}_LVDS = 0V	-	1	µA
LVDS Leakage Current, Low Level	I_{OL_LVDS}	V_{DD}_LVDS = 0V	-	1	µA
Functional Test 3 (Structural Test 5, "Scanshift")	-		N/A		-
Functional Test 4 (Structural Tests 6 and 7) (Note 4)	-		N/A		-
Functional Test 5 (Structural Tests 8 to 20) (Note 5)	-		N/A		-
Functional Test 6 (Functional Tests 21, 22 and 23) (Note 6)	-		N/A		-
LVDS Output Voltage, Low Level	V_{OL_LVDS}		-	700	mV

Characteristics	Symbols	Test Conditions (Note 1)	Limits		Units
			Min	Max	
LVDS Output Voltage, High Level	V_{OH_LVDS}		1.7	-	V
Functional Test 7 (Setup Test 1) (Note 7)	-		N/A		-
LVDS Output Differential Voltage	V_{OD_LVDS}	Pins DOUT_N, DOUT_P	360	782	mV
Functional Test 8 (Setup Test 2, all relays OFF_FT_1)	-		N/A		-
LVDS Common-Mode Differential Voltage Max	$V_{cm\_LVDSMax}$		-	1.7	V
LVDS Common-Mode Differential Voltage Min	$V_{cm\_LVDSMin}$		750	-	mV
LVDS Input Differential Voltage	V_{ID_LVDS}		100	-	mV
Functional Test 9 (Structural Test 24) (Note 8)	-		N/A		-
Functional Test 10 (Structural Tests 25 to 75) (Note 9)	-		N/A		-
Functional Test 11 (Structural Test 76, “I/Os BSCANOUT”, I/O Bank load: 2mA)	-		N/A		-
Output Voltage Low Level 1, I/O Banks	V_{OL1}	Load: 2mA	-	500	mV
Output Voltage High Level 1, I/O Banks	V_{OH1}	Load: 2mA	2	-	V
Functional Test 12 (Structural Test 77, “I/Os BSCANOUT”, I/O Bank load: 4mA)	-		N/A		-
Output Voltage Low Level 2, I/O Banks	V_{OL2}	Load: 4mA	-	500	mV
Output Voltage High Level 2, I/O Banks	V_{OH2}	Load: 4mA	2	-	V
Functional Test 13 (Structural Test 78, “I/Os BSCANOUT”, I/O Bank load: 8mA)	-		N/A		-
Output Voltage Low Level 3, I/O Banks	V_{OL3}	Load: 8mA	-	600	mV
Output Voltage High Level 3, I/O Banks	V_{OH3}	Load: 8mA	1.9	-	V
Functional Test 14 (Structural Test 79, “I/Os BSCANOUT”, I/O Bank load: 16mA)	-		N/A		-
Output Voltage Low Level 4, I/O Banks	V_{OL4}	Load: 16mA	-	800	mV
Output Voltage Low Level 4, I/O Banks (re-test)	V_{OL4_RETEST}	Load: 16mA	-	800	mV
Output Voltage High Level 4, I/O	V_{OH4}	Load: 16mA	1.7	-	V

Characteristics	Symbols	Test Conditions (Note 1)	Limits		Units
			Min	Max	
Banks					
Output Voltage High Level 4, I/O Banks (re-test)	V_{OH4_RETEST}	Load: 16mA	1.7	-	V
Functional Test 15 (Structural Test 80, “I/Os BSCANIN”, V_{IO}_BANK = 1.8V)	-		N/A		-
Low Input Voltage 1, I/O Banks	V_{IL1}	V_{IO}_BANK = 1.8V	-	630	mV
High Input Voltage 1, I/O Banks	V_{IH1}	V_{IO}_BANK = 1.8V	-	630	mV
Functional Test 16 (Structural Test 81, “I/Os BSCANIN”, V_{IO}_BANK = 2.5V)	-		N/A		-
Low Input Voltage 2, I/O Banks	V_{IL2}	V_{IO}_BANK = 2.5V	-	700	mV
High Input Voltage 2, I/O Banks	V_{IH2}	V_{IO}_BANK = 2.5V	-	700	mV
Functional Test 17 (Structural Test 82, “I/Os BSCANIN”, V_{IO}_BANK = 3.3V)	-		N/A		-
Low Input Voltage 3, I/O Banks	V_{IL3}	V_{IO}_BANK = 3.3V	-	800	mV
High Input Voltage 3, I/O Banks	V_{IH3}	V_{IO}_BANK = 3.3V	-	800	mV
High Input Current 1, Simple I/O Banks	I_{IH1}	V_{IO}_BANK = 1.8V	-5	10	µA
High Input Current 2, Complex I/O Banks	I_{IH2}	V_{IO}_BANK = 1.8V	-5	5	µA
High Input Current 3, Complex I/O Bank 2 with SPMU	I_{IH3}	V_{IO}_BANK = 1.8V	-5	5	µA
Low Input Current 1, I/O Banks	I_{IL1}	V_{IO}_BANK = 1.8V	-40	5	µA
High Input Current 4, Simple I/O Banks	I_{IH4}	V_{IO}_BANK = 2.5V	-5	20	µA
High Input Current 5, Complex I/O Banks	I_{IH5}	V_{IO}_BANK = 2.5V	-5	100	µA
High Input Current 6, Complex I/O Bank 2 with SPMU	I_{IH6}	V_{IO}_BANK = 2.5V	-5	100	µA
Low Input Current 2, I/O Banks	I_{IL2}	V_{IO}_BANK = 2.5V	-80	10	µA
High Input Current 7, Simple I/O Banks	I_{IH7}	V_{IO}_BANK = 3.3V	-5	25	µA
High Input Current 8, Complex I/O Banks	I_{IH8}	V_{IO}_BANK = 3.3V	-5	150	µA
High Input Current 9, Complex I/O Bank 2 with SPMU	I_{IH9}	V_{IO}_BANK = 3.3V	-5	180	µA
Low Input Current 3, I/O Banks	I_{IL3}	V_{IO}_BANK = 3.3V	-100	10	µA
Functional Test 18 (I/O Configuration Tests 1 to 3, I/Os Activity)	-		N/A		-
Functional Test 19	-		N/A		-

Characteristics	Symbols	Test Conditions (Note 1)	Limits		Units
			Min	Max	
(I/O Configuration Tests 4 to 10, Test of BSCAN with Specific Settings)					
Transition Time, High-to-Low 1	t_{phl1}	V_{IO}_BANK = 1.8V	0.4	3	ns
Transition Time, Low-to-High 1	t_{plh1}	V_{IO}_BANK = 1.8V	0.4	3	ns
Transition Time, High-to-Low 2	t_{phl2}	V_{IO}_BANK = 2.5V	0.4	3	ns
Transition Time, Low-to-High 2	t_{plh2}	V_{IO}_BANK = 2.5V	0.4	3	ns
Transition Time, High-to-Low 3	t_{phl3}	V_{IO}_BANK = 3.3V	0.4	3	ns
Transition Time, Low-to-High 3	t_{plh3}	V_{IO}_BANK = 3.3V	0.4	3	ns
Rise Times	$t_{r1.8}$	V_{IO}_BANK = 1.8V	20	100	ps
	$t_{r2.5}$	V_{IO}_BANK = 2.5V	20	100	ps
	$t_{r3.3}$	V_{IO}_BANK = 3.3V	20	100	ps
Fall Times	$t_{f1.8}$	V_{IO}_BANK = 1.8V	20	100	ps
	$t_{f2.5}$	V_{IO}_BANK = 2.5V	20	100	ps
	$t_{f3.3}$	V_{IO}_BANK = 3.3V	20	100	ps

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at $T_{op(max)}$ = +125 (+0 -5) °C and T_{amb} = -55 (+5 -0) °C.

The characteristics, test methods, conditions and limits shall be the same as specified in Para. 2.3.1, Room Temperature Electrical Measurements except where shown below.

Characteristics	Symbols	Test Conditions (Note 1)	Limits		Units
			Min	Max	
Low Input Current 1, I/O Banks	I_{IL1}	$T_{op(max)}$ = +125 (+0 -5) °C V_{IO}_BANK = 1.8V	-70	5	µA
High Input Current 5, Complex I/O Banks	I_{IH5}	$T_{op(max)}$ = +125 (+0 -5) °C V_{IO}_BANK = 2.5V	-5	150	µA
High Input Current 6, Complex I/O Bank 2 with SPMU	I_{IH6}	$T_{op(max)}$ = +125 (+0 -5) °C V_{IO}_BANK = 2.5V	-5	150	µA
Low Input Current 2, I/O Banks	I_{IL2}	$T_{op(max)}$ = +125 (+0 -5) °C V_{IO}_BANK = 2.5V	-110	10	µA
High Input Current 8, Complex I/O Banks	I_{IH8}	$T_{op(max)}$ = +125 (+0 -5) °C V_{IO}_BANK = 3.3V	-5	200	µA
High Input Current 9, Complex I/O Bank 2 with SPMU	I_{IH9}	$T_{op(max)}$ = +125 (+0 -5) °C V_{IO}_BANK = 3.3V	-5	250	µA
Low Input Current 3, I/O Banks	I_{IL3}	$T_{op(max)}$ = +125 (+0 -5) °C V_{IO}_BANK = 3.3V	-150	10	µA

2.3.3 Notes to Electrical Measurements at Room, High and Low Temperatures:

1. Unless otherwise specified: 1.08V < V_{DD} < 1.32V, 2.25V < V_{CC} < 2.75V.
2. Power-up sequence: Structural test 1 = check boot without POR, structural test 2 = check POR activation at V_{DDmax} only, structural test 3 = wait point for good temperature.

3. Structural Test 4 = thermal sensor scan preceded by: Thermal Sensors datalog (check all thermal sensors start) and JTAG ID readback.
4. Power-on sequence: Structural test 6 = check boot without POR, structural test 7 = check POR activation at V_{DD}max only.
5. Structural tests 8 through 15 = check driver lines, structural tests 16 through 20 = BSM scan-path.
6. Structural test 21 (Tx and Rx): V_{CM} = 1.25V / V_{INdiff} = 0.2V;
   Structural test 22 (Tx and Rx): V_{CM} = 0.8V / V_{INdiff} = 0.1V;
   Structural test 23 (Tx and Rx): V_{CM} = 1.3V / V_{INdiff} = 0.1V
7. Setup test 1 = all relays ON, 100Ω on LVDSout connected.
8. Structural test 24 (Tx): "BSM LVDS check INdiff".
9. Structural tests 25 to 75 include: Test of Mesh (tile); test of crossbar RI (tile); tests of system matrix; tests of global network; test of DSP; activity on I/Os; tests of PLL; test of I/O delay line; test of SPREG (in BSM); tests of DPREG (in tile); tests of DPRAM (in CGB).

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified the measurements shall be performed at T_{amb} = +22 ±3 °C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1, Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics (Note 1)	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Total Supply Current in Reset Condition	I_{DD}	±100mA	-	800	mA
LVDS Common-Mode Differential Voltage Max	$V_{cm\_LVDSMax}$	±100mV	-	1700	mV
LVDS Common-Mode Differential Voltage Min	$V_{cm\_LVDSMin}$	±100mV	750	-	mV
LVDS Output Differential Voltage	V_{OD_LVDS}	±50mV	360	782	mV
Output Voltage Low Level 1, I/O Banks	V_{OL1}	±150mV	-	500	mV
Output Voltage High Level 1, I/O Banks	V_{OH1}	±150mV	2000	-	mV

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified the measurements shall be performed at T_{amb} = +22 ±3 °C. Unless otherwise specified the characteristics, test methods, conditions and limits shall be the same as specified in Para. 2.3.1, Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Test Temperature	$T_{op(max)}$	+125 (+0 -5)	°C
Analog (VDDIO) Supply Voltage	V_{CC}	2.75 (+0, -0.05)	V
Digital (VDDCORE) Supply Voltage	V_{DD}	1.32 (+0 -0.05)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:
1. During Burn-in and Operating Life, the FPGA is configured and then stimuli are applied.
2. Test set-up shall be maintained within the Manufacturer's PID.

2.7 OPERATING LIFE CONDITIONS

Unless otherwise specified the conditions shall be as specified in Para. 2.6, Power Burn-in Conditions.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in Para. 1.4.2 or in the Purchase Order. The Radiation Dose Rate shall be within Window 2, i.e. 36 to 360 rad(Si)/hour.

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+20 ±2	°C
VDDSENSE Output pin	$V_{DDSENSE}$	1.2 (±10%)	V
All VDD2V5A pins	V_{DD2V5A}	2.5 (+0, -0.05)	V
Unused Inputs/Outputs/Supply Voltage pins	V_{IN} / V_{OUT} / V_{DD}	Not Connected	-
Analog (VDDIO) Supply Voltage	V_{CC}	3.3 (+0, -0.05)	V
Digital (VDDCORE) Supply Voltage	V_{DD}	1.2 (+0 -0.05)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:
1. Annealing shall be performed with the static bias conditions for a duration of 24 hours at the specified T_{amb} followed by 168 hours minimum at a temperature of +100 ±2 °C.
2. Test set-up shall be maintained within the Manufacturer's PID.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation testing the devices shall have successfully met Room Temperature Electrical Measurements specified in Para. 2.3.1.

Unless otherwise specified the measurements shall be performed at T_{amb} = +25 ±2 °C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1, Room Temperature Electrical Measurements.