INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS, LOW POWER, 8-BIT AVR® MICROCONTROLLER

BASED ON TYPE ATmegaS128

ESCC Detail Specification No. 9521/003

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION

TABLE OF CONTENTS

1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.

(b) MIL-STD-883, Test Method Standard for Microcircuits.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 952100301E

- Detail Specification Reference: 9521003
- Component Type Variant Number: 01
- Total Dose Radiation Level Letter: E (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter (Notes 2, 3)
01	ATmegaS128	CQFP-64	D2 (Note 1)	5	E [20krad(Si)]

NOTES:

1. The terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.
2. Total dose radiation level letters are defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.
3. The Total Dose Radiation Level Letter (E) is guaranteed for read-mode only, with no write operation in FLASH or EEPROM memory.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage. Functional performance for extended periods at the maximum ratings may adversely affect device reliability.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in the Test Methods and Procedures of the applicable ESCC generic specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{CC}	-0.5 to 4	V	Notes 1, 2
Input Voltage Range (except RST pin)	V_{IN}	-0.5 to V_{CC}+0.5	V	Note 2
Input Voltage Range (RST pin)	$V_{IN(reset)}$	-0.5 to 13	V	Note 2
Output Voltage Range (all Outputs)	V_{OUT}	-0.5 to V_{CC}+0.3	V	Note 2
DC Current per pin: I/Os V_{CC} V_{SS}	I_{DD}	 40 200 400	mA	
Operating Temperature Range	T_{op}	-55 to +125	°C	Note 1 T_{amb}
Storage Temperature Range	T_{stg}	-60 to +150	°C	
Junction Temperature	T_j	+175	°C	
Thermal Resistance, Junction-to-Case	$R_{th(j-c)}$	5	°C/W	
Soldering Temperature	T_{sol}	+345	°C	Note 3

NOTES:

1. The following operating conditions also apply. Device performance beyond these operating conditions is not guaranteed:

Characteristics	Symbols	Maximum Rated Operating Conditions	Units	Remarks
Supply Voltage	V_{CC}	3 to 3.6	V	Note 2
Analog Supply Voltage Range	AV_{CC}	V_{CC}-0.3 to V_{CC}+0.3	V	Note 2
Operating Temperature Range	T_{op}	As per Maximum Ratings table		T_{amb}

2. With reference to V_{SS} = 0V.
3. Duration 10 seconds maximum at a distance of not less than 1.6 mm from the device body and the same terminal shall not be re-soldered until 3 minutes have elapsed.

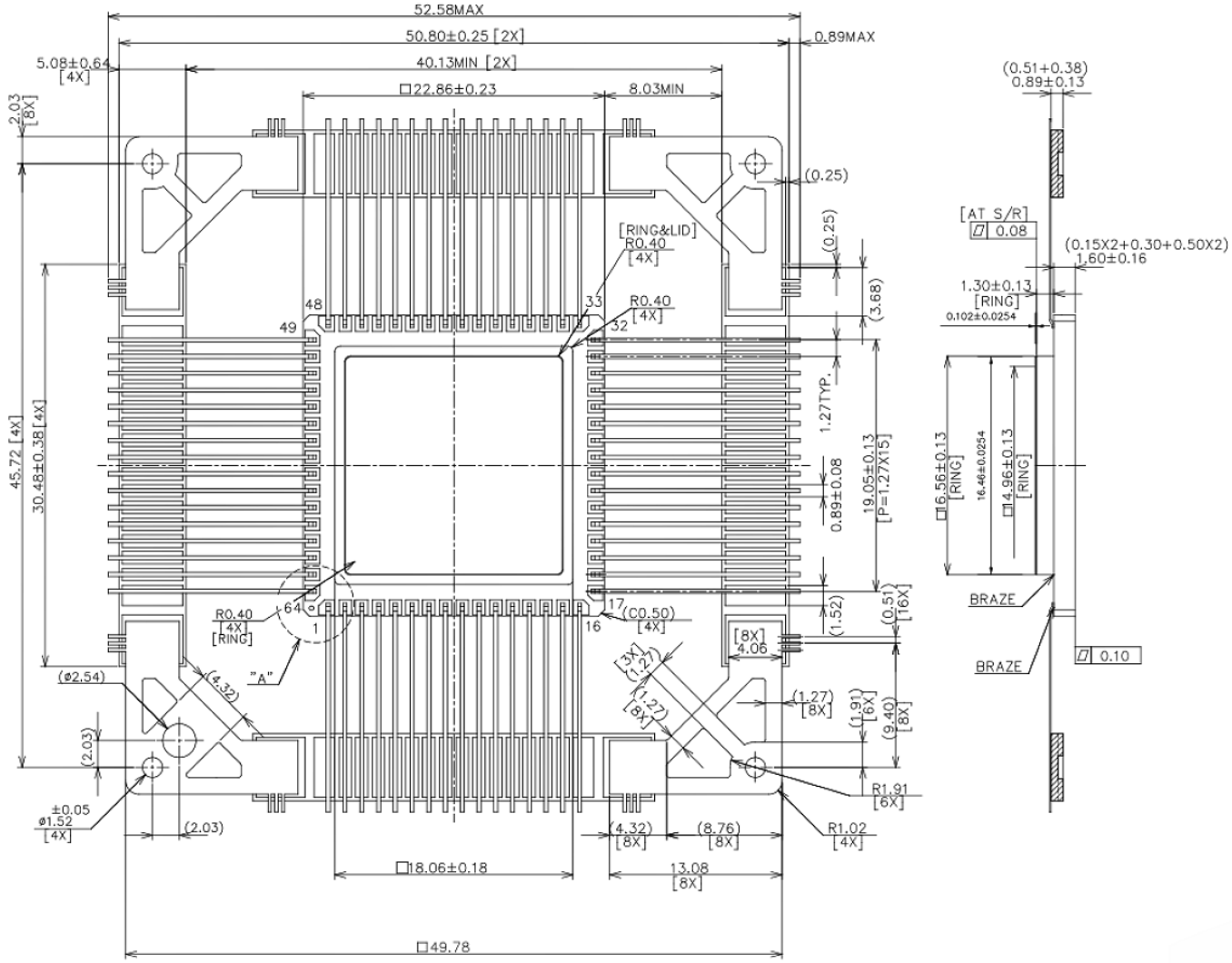
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 2000 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

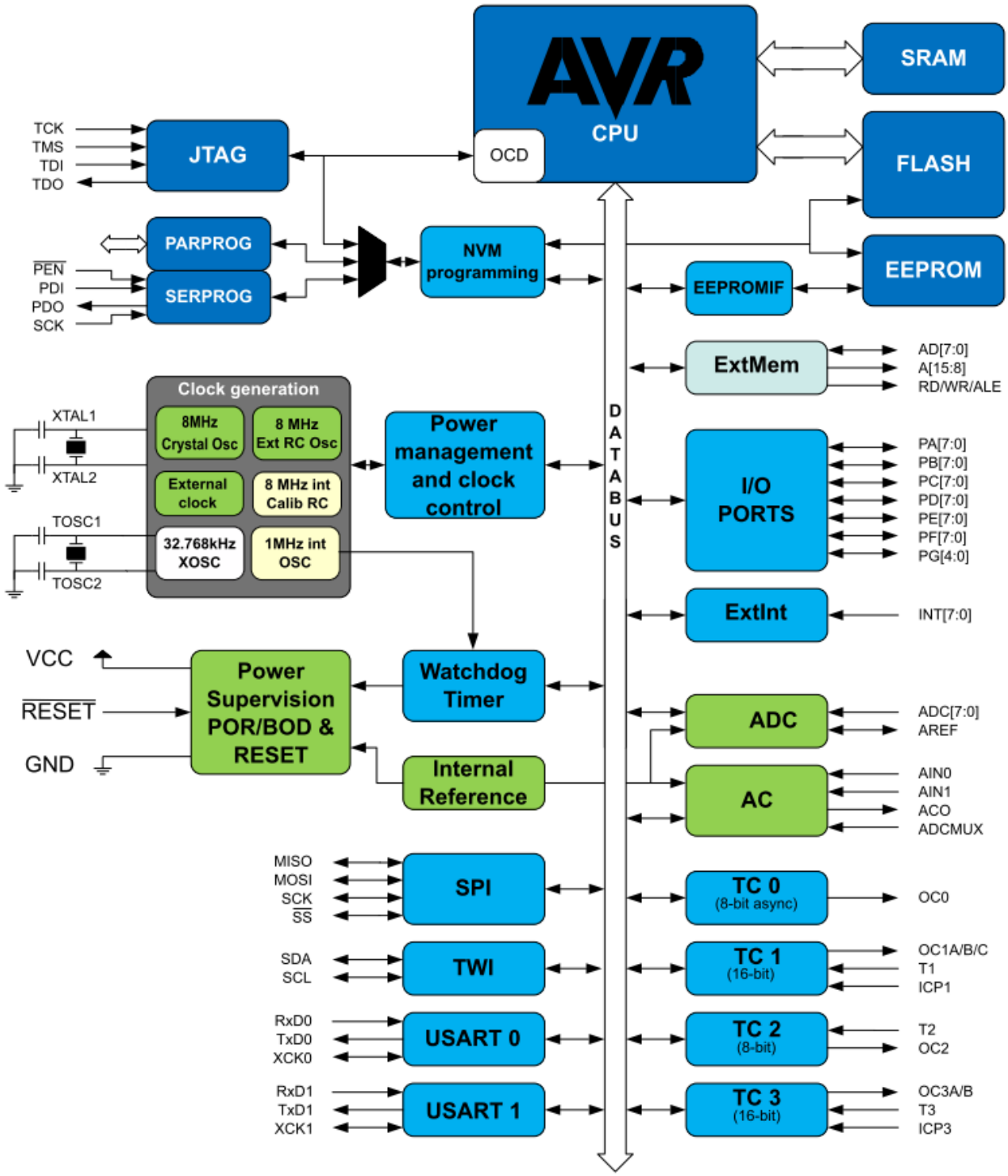
Ceramic Quad Flat Package (CQFP-64) – 64 Tied Leads
(all dimensions are in mm)



NOTES:

1. Terminal identification is specified by reference to the index mark, shown within “A”.
2. The lid is connected to ground.

1.8 FUNCTIONAL DIAGRAM



1.9 PIN ASSIGNMENT

Pin	Name	Type	Pin	Name	Type
1	PEN	I	33	PG0/WRN	I/O
2	PE0/RXD0/PDI	I/O	34	PG1/RDN	I/O
3	PE1/TXD0/PDO	I/O	35	PC0/A8	I/O
4	PE2/XCK0/AIN0	I/O	36	PC1/A9	I/O
5	PE3/OC3A/AIN1	I/O	37	PC2/A10	I/O
6	PE4/OC3B/INT4	I/O	38	PC3/A11	I/O
7	PE5/OC3C/INT5	I/O	39	PC4/A12	I/O
8	PE6/T3/INT6	I/O	40	PC5/A13	I/O
9	PE7/ICP3/INT7	I/O	41	PC6/A14	I/O
10	PB0/SS	I/O	42	PC7/A15	I/O
11	PB1/SCK	I/O	43	PG2/ALE	I/O
12	PB2/MOSI	I/O	44	PA7/AD7	I/O
13	PB3/MISO	I/O	45	PA6/AD6	I/O
14	PB4/OC0	I/O	46	PA5/AD5	I/O
15	PB5/OC1A	I/O	47	PA4/AD4	I/O
16	PB6/OC1B	I/O	48	PA3/AD3	I/O
17	PB7/OC2/OC1C	I/O	49	PA2/AD2	I/O
18	PG3/TOSC2	I/O	50	PA1/AD1	I/O
19	PG4/TOSC1	I/O	51	PA0/AD0	I/O
20	RST	I	52	VCC2	VCC
21	VCC1	VCC	53	GND2	Ground
22	GND1	Ground	54	PF7/ADC7/TDI	I/O
23	XTAL2	O	55	PF6/ADC6/TDO	I/O
24	XTAL1	I	56	PF5/ADC5/TMS	I/O
25	PD0/SCL/INT0	I/O	57	PF4/ADC4/TCK	I/O
26	PD1/SDA/INT1	I/O	58	PF3/ADC3	I/O
27	PD2/RXD/INT2	I/O	59	PF2/ADC2	I/O
28	PD3/TXD/INT3	I/O	60	PF1/ADC1	I/O
29	PD4/ICP1	I/O	61	PF0/ADC0	I/O
30	PD5/XCK1	I/O	62	AREF	I/O
31	PD6/T1	I/O	63	AGND	Ground
32	PD7/T2	I/O	64	AVCC	VCC

Pin Name	Function
Port A (PA7:PA0)	Port A is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running. Port A also serves the functions of various special features of the ATmegaS128 as listed in Alternate Functions of Port A.
Port B (PB7:PB0)	Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running. Port B also serves the functions of various special features of the ATmegaS128 as listed in Alternate Functions of Port B.
Port C (PC7:PC0)	Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running. Port C also serves the functions of special features of the ATmegaS128 as listed in Alternate Functions of Port C. In ATmega103 compatibility mode, Port C is output only, and the port C pins are not tri-stated when a reset condition becomes active. Note: The components are, by default, shipped in ATmega103 compatibility mode. Thus, if the parts are not programmed before they are put on the PCB, the Port C pins will be output during first power up, and until the ATmega103 compatibility mode is disabled.
Port D (PD7:PD0)	Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running. Port D also serves the functions of various special features of the ATmegaS128 as listed in Alternate Functions of Port D.
Port E (PE7:PE0)	Port E is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running. Port E also serves the functions of various special features of the ATmegaS128 as listed in Alternate Functions of Port E.
Port F (PF7:PF0)	Port F serves as the analog inputs to the A/D Converter. Port F also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port F output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port F pins that are externally pulled low will source current if the pull-up resistors are activated. The Port F pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PF7(TDI), PF5(TMS), and PF4(TCK) will be activated even if a Reset occurs. The TDO pin is tri-stated unless TAP states that shift out data are entered. Port F also serves the functions of the JTAG interface. In ATmega103 compatibility mode, Port F is an input Port only.

Pin Name	Function
Port G (PG4:PG0)	Port G is a 5-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port G output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port G pins that are externally pulled low will source current if the pull-up resistors are activated. The Port G pins are tri-stated when a reset condition becomes active, even if the clock is not running. Port G also serves the functions of various special features. The port G pins are tri-stated when a reset condition becomes active, even if the clock is not running. In ATmega103 compatibility mode, these pins only serve as strobe signals to the external memory as well as input to the 32kHz Oscillator, and the pins are initialized to PG0 = 1, PG1 = 1, and PG2 = 0 asynchronously when a reset condition becomes active, even if the clock is not running. PG3 and PG4 are oscillator pins.
RST	Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in System and Reset Characteristics. Shorter pulses are not guaranteed to generate a reset.
XTAL1	Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.
XTAL2	Output from the inverting Oscillator amplifier.
AVCC	AVCC is the supply voltage pin for Port F and the A/D Converter. It should be externally connected to VCC, even if the ADC is not used. If the ADC is used, it should be connected to VCC through a low-pass filter.
AREF	AREF is the analog reference pin for the A/D Converter.
PEN	PEN is a programming enable pin for the SPI Serial Programming mode, and is internally pulled high. By holding this pin low during a Power-on Reset, the device will enter the SPI Serial Programming mode. PEN has no function during normal operation.

1.10 PROTECTION NETWORK

Pads are protected with standard I/O protection, wafer manufacturer proprietary and confidential.

2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirements and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests for Packaged Components – Chart F3A

High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification (see Para. 1.7).
(b) The ESCC qualified components symbol (for ESCC qualified component only).
(c) The ESCC Component Number (see Para. 1.4.1).
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{case} = +25 (+3 -5)°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions 3V < V_{CC} < 3.6V (Notes 1, 2)	Limits		Units
				Min	Max	
Functional Tests	-	3014	Self-test, f = 8MHz	-	-	-
High Level Input Voltage	V_{IH}	-		2.2	V_{CC}+0.5	V
Low Level Input Voltage	V_{IL}	-		V_{SS}-500	800	mV
Low Level Output Voltage	V_{OL}	3007	V_{CC} = V_{CCmin} I_{OL} = 10mA All I/O Port pins, Output XTAL2	-	600	mV
High Level Output Voltage	V_{OH}	3006	V_{CC} = V_{CCmin} I_{OH} = -10mA All I/O Port pins, Output XTAL2	2.2	-	V
Low Level Input Current (Note 3)	I_{IL}	3009	V_{CC} = V_{CCmax} V_{IN} = V_{SS}	-1	1	µA
Low Level Input Current with Pull-up (Note 4)	I_{ILPU}	3009	V_{CC} = V_{CCmax} V_{IN} = V_{SS}	-180	-40	µA
High Level Input Current (Note 3)	I_{IH}	3010	V_{IN} = V_{CC} = V_{CCmax}	-1	1	µA
Dynamic Operating Current	I_{CCOP}	3005	V_{CC} = V_{CCmax}, f = 4MHz	-	5.5	mA
			V_{CC} = V_{CCmax}, f = 8MHz (Note 5)	-	19	
Idle Supply Current	I_{CCIDLE}	3005	V_{CC} = V_{CCmax}, f = 4MHz	-	2.5	mA
			V_{CC} = V_{CCmax}, f = 8MHz (Note 5)	-	11	
Power-down Supply Current	I_{CCPD}	3005	V_{CC} = V_{CCmax}, Watchdog Timer enabled	-	100	µA
			V_{CC} = V_{CCmax}, Watchdog Timer disabled	-	50	

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions $3V < V_{CC} < 3.6V$ (Notes 1, 2)	Limits		Units
				Min	Max	
1MHz Oscillator Frequency Accuracy after calibration	f_{ACC1}	-	V_{CC} = 3.3V	-3	3	%
2MHz Oscillator Frequency Accuracy after calibration	f_{ACC2}	-	V_{CC} = 3.3V	-3	3	%
4MHz Oscillator Frequency Accuracy after calibration	f_{ACC4}	-	V_{CC} = 3.3V	-3	3	%
8MHz Oscillator Frequency Accuracy after calibration	f_{ACC8}	-	V_{CC} = 3.3V	-3	3	%
Internal VREF	V_{REF}	-		2.3	2.7	V

NOTES:

1. Unless otherwise specified, all inputs and outputs shall be tested for each characteristic. Inputs not under test shall be V_{IN} = V_{SS} or V_{CC} and outputs not under test shall be open. V_{SS} = 0V.
2. Unless otherwise specified, output load = 70pF.
3. The following pins shall not be tested: RST, PEN, PA0 - PA7, PB0 - PB7, PC0 - PC7, PD0 - PD7, PE0 - PE7, PG0 - PG4.
4. Only pins RST, PEN, PA0 - PA7, PB0 - PB7, PC0 - PC7, PD0 - PD7, PE0 - PE7, PG0 - PG4 shall be tested.
5. I_{CCOP}, I_{CCIDLE} shall only be tested at f = 8MHz as part of specific characterisation testing (e.g., after a design or process change).

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{case} = +125 ±3°C and T_{case} = -55 ±3°C.

The characteristics, test methods, conditions and limits shall be as specified in Para. 2.3.1, Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{case} = +25 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1, Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Low Level Output Voltage	V_{OL}	±100	-	600	mV
High Level Output Voltage	V_{OH}	±0.1	2.2	-	V
Low Level Input Current	I_{IL}	±0.1	-1	1	µA
High Level Input Current	I_{IH}	±0.1	-1	1	µA
Idle Supply Current at 4MHz	I_{CCIDLE}	+0.25	-	2.5	mA

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{case} = +25 ±3°C.

The characteristics, test methods, conditions and limits shall be the same as specified in Para. 2.3.1, Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

Prior to submitting the parts to Burn-In or Operating Life, a specific application is loaded in the Flash memory. This application automatically starts after the RST pin is released. The correct behaviour of the device can be monitored with an on-board LED.

Characteristics (Note 1)	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125(+8 -0)	°C
Operating Frequency (Note 2)	f_{op}	8	MHz
Supply Voltage	V_{CC}	3.6	V

NOTES:

1. Pin connections shall be as follows, with NC = Not Connected:

Pin	Name	Serial R	Wired To	Pin	Name	Serial R	Wired To
1	PEN	10 kΩ	V_{CC}	33	PG0/WRN	-	NC
2	PE0/RXD0/PDI	-	NC	34	PG1/RDN	-	NC
3	PE1/TXD0/PDO	-	NC	35	PC0/A8	-	NC
4	PE2/XCK0/AIN0	-	NC	36	PC1/A9	-	NC
5	PE3/OC3A/AIN1	-	NC	37	PC2/A10	-	NC

Pin	Name	Serial R	Wired To	Pin	Name	Serial R	Wired To
6	PE4/OC3B/INT4	-	NC	38	PC3/A11	-	NC
7	PE5/OC3C/INT5	-	NC	39	PC4/A12	-	NC
8	PE6/T3/INT6	-	NC	40	PC5/A13	-	NC
9	PE7/ICP3/INT7	-	NC	41	PC6/A14	-	NC
10	PB0/SS	-	NC	42	PC7/A15	-	NC
11	PB1/SCK	-	NC	43	PG2/ALE	-	NC
12	PB2/MOSI	-	NC	44	PA7/AD7	-	NC
13	PB3/MISO	-	NC	45	PA6/AD6	-	NC
14	PB4/OC0	-	NC	46	PA5/AD5	-	NC
15	PB5/OC1A	-	NC	47	PA4/AD4	-	NC
16	PB6/OC1B	-	NC	48	PA3/AD3	-	NC
17	PB7/OC2/OC1C	-	NC	49	PA2/AD2	-	NC
18	PG3/TOSC2	-	NC	50	PA1/AD1	-	NC
19	PG4/TOSC1	1 kΩ	Ground	51	PA0/AD0	-	NC
20	RST	-	NC	52	VCC2	-	V_{CC}
21	VCC1	-	V_{CC}	53	GND2	-	Ground
22	GND1	-	Ground	54	PF7/ADC7/TDI	1 kΩ	Ground
23	XTAL2	-	NC	55	PF6/ADC6/TDO	1 kΩ	Ground
24	XTAL1	1 kΩ	1.65 MHz	56	PF5/ADC5/TMS	1 kΩ	Ground
25	PD0/SCL/INT0	-	NC	57	PF4/ADC4/TCK	1 kΩ	Ground
26	PD1/SDA/INT1	-	NC	58	PF3/ADC3	1 kΩ	Ground
27	PD2/RXD/INT2	-	NC	59	PF2/ADC2	1 kΩ	Ground
28	PD3/TXD/INT3		LED control	60	PF1/ADC1	1 kΩ	Ground
29	PD4/ICP1	-	NC	61	PF0/ADC0	1 kΩ	Ground
30	PD5/XCK1	-	NC	62	AREF	-	Ground
31	PD6/T1	-	NC	63	AGND	-	Ground
32	PD7/T2	-	NC	64	AVCC	-	V_{CC}

2. Running self-tests.

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified in Para. 2.6, Power Burn-in Conditions.

2.8 TOTAL DOSE IRRADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Irradiation testing shall be carried out in dose rate Window 2 ("Low Rate"): 36 to 360 rad(Si)/hour, as defined in ESCC Basic Specification No. 22900.

Continuous bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in Para. 1.4.2 or in the Purchase Order.

Characteristics (Note 1)	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+22±3	°C
Supply Voltage	V_{CC}	3.6	V

NOTES:

1. Pin connections shall be as follows, with NC = Not Connected:

Pin	Name	Serial R	Wired To	Pin	Name	Serial R	Wired To
1	PEN	-	NC	33	PG0/WRN	10 kΩ	Ground
2	PE0/RXD0/PDI	10 kΩ	Ground	34	PG1/RDN	10 kΩ	Ground
3	PE1/TXD0/PDO	10 kΩ	Ground	35	PC0/A8	10 kΩ	Ground
4	PE2/XCK0/AIN0	10 kΩ	Ground	36	PC1/A9	10 kΩ	Ground
5	PE3/OC3A/AIN1	10 kΩ	Ground	37	PC2/A10	10 kΩ	Ground
6	PE4/OC3B/INT4	10 kΩ	Ground	38	PC3/A11	10 kΩ	Ground
7	PE5/OC3C/INT5	10 kΩ	Ground	39	PC4/A12	10 kΩ	Ground
8	PE6/T3/INT6	10 kΩ	Ground	40	PC5/A13	10 kΩ	Ground
9	PE7/ICP3/INT7	10 kΩ	Ground	41	PC6/A14	10 kΩ	Ground
10	PB0/SS	10 kΩ	Ground	42	PC7/A15	10 kΩ	Ground
11	PB1/SCK	10 kΩ	Ground	43	PG2/ALE	10 kΩ	Ground
12	PB2/MOSI	10 kΩ	Ground	44	PA7/AD7	10 kΩ	Ground
13	PB3/MISO	10 kΩ	Ground	45	PA6/AD6	10 kΩ	Ground
14	PB4/OC0	10 kΩ	Ground	46	PA5/AD5	10 kΩ	Ground
15	PB5/OC1A	10 kΩ	Ground	47	PA4/AD4	10 kΩ	Ground
16	PB6/OC1B	10 kΩ	Ground	48	PA3/AD3	10 kΩ	Ground
17	PB7/OC2/OC1C	10 kΩ	Ground	49	PA2/AD2	10 kΩ	Ground
18	PG3/TOSC2	10 kΩ	Ground	50	PA1/AD1	10 kΩ	Ground
19	PG4/TOSC1	10 kΩ	Ground	51	PA0/AD0	10 kΩ	Ground
20	RST	10 kΩ	Ground	52	VCC2	-	V_{CC}
21	VCC1	-	V_{CC}	53	GND2	-	Ground
22	GND1	-	Ground	54	PF7/ADC7/TDI	10 kΩ	Ground
23	XTAL2	-	NC	55	PF6/ADC6/TDO	10 kΩ	Ground
24	XTAL1	10 kΩ	Ground	56	PF5/ADC5/TMS	10 kΩ	Ground
25	PD0/SCL/INT0	10 kΩ	NC	57	PF4/ADC4/TCK	10 kΩ	Ground

Pin	Name	Serial R	Wired To	Pin	Name	Serial R	Wired To
26	PD1/SDA/INT1	10 kΩ	Ground	58	PF3/ADC3	10 kΩ	Ground
27	PD2/RXD/INT2	10 kΩ	Ground	59	PF2/ADC2	10 kΩ	Ground
28	PD3/TXD/INT3	10 kΩ	Ground	60	PF1/ADC1	10 kΩ	Ground
29	PD4/ICP1	10 kΩ	Ground	61	PF0/ADC0	10 kΩ	Ground
30	PD5/XCK1	10 kΩ	Ground	62	AREF	10 kΩ	Ground
31	PD6/T1	10 kΩ	Ground	63	AGND	-	NC
32	PD7/T2	10 kΩ	Ground	64	AVCC	-	V_{CC}

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to, during and on completion of irradiation testing the devices shall have successfully met the Room Temperature Electrical Measurements specified in Para. 2.3.1.

Unless otherwise stated the measurements shall be performed at T_{case} = +25 ±3°C.

The characteristics, test methods, conditions and limits shall be as per the corresponding test defined in Para. 2.3.1, Room Temperature Electrical Measurements.

APPENDIX A

AGREED DEVIATIONS FOR MICROCHIP (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 2.8.1, Bias Conditions and Total Dose Level for Total Dose Radiation Testing	The maximum total dose radiation exposure level applicable to the total dose radiation test shall be 30krad(Si) or as stipulated in the Purchase Order. **NOTE:** The total dose radiation level letter (E) shall remain unchanged (see Para. 1.4.2) unless an alternative radiation test level has been stipulated in the Purchase Order.