INTEGRATED CIRCUITS:

MONOLITHIC MICROCIRCUITS, WIRE-BONDED, PLASTIC ENCAPSULATED AND FLIP-CHIP MONOLITHIC MICROCIRCUITS, WITH ORGANIC SUBSTRATE

ESCC Generic Specification No. 9030

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DCR No.	CHANGE DESCRIPTION

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1 INTRODUCTION

1.1 SCOPE

This specification defines the general requirements for the qualification, qualification maintenance, procurement, and delivery of the following Integrated Circuits for space applications:

- Monolithic Microcircuits, wire-bonded, plastic encapsulated (see Para. 3)
- Flip-Chip Monolithic Microcircuits, with organic substrate (see Para. 3)

This specification contains the appropriate inspection and test schedules and also specifies the data documentation requirements.

Copper wire bonding is not covered by this specification.

1.2 APPLICABILITY

This specification is primarily applicable to the granting of qualification approval to components qualified in accordance with one of the following ESCC methods:

(a) Qualification of Standard Components per this ESCC Generic Specification and ESCC Basic Specification No. 20100.

(b) Technology Flow Qualification per ESCC Basic Specification No. 25400.

It is also primarily applicable to the procurement of components so qualified.

This specification may also be applied to the procurement of unqualified components, recommendations for which are given in ESCC Basic Specification No. 23100.

2 APPLICABLE DOCUMENTS

The following documents form part of, and shall be read in conjunction with, this specification. The relevant issues shall be those in effect on the date of starting qualification or placing the Purchase Order.

2.1 ESCC SPECIFICATIONS

- No. 20100, Requirements for the Qualification of Standard Electronic Components for Space Application.
- No. 20600, Preservation, Packaging and Dispatch of ESCC Components.
- No. 21300, Terms, Definitions, Abbreviations, Symbols and Units.
- No. 21700, General Requirements for the Marking of ESCC Components.
- No. 22600, Requirements for the Evaluation of Standard Electronic Components for Space Application.
- No. 22800, ESCC Non-Conformance Control System.
- No. 22900, Total Dose Steady-State Irradiation Test Method.
- No. 23100, Recommendations on the use of the ESCC Specification System for the Evaluation and Procurement of Unqualified Components.
- No. 23500, Lead Materials and Finishes for Components for Space Application.
- No. 23800, Electrostatic Discharge Sensitivity Test Method.
- No. 24600, Minimum Quality System Requirements.
- No. 24800, Resistance to Solvents of Marking, Materials and Finishes.
- No. 25200, Application of Scanning Acoustic Microscopy to Plastic Encapsulated Devices

- No. 25300, Decapsulation of Plastic Encapsulated Semiconductor Devices
- No. 25400, Requirements for the Technology Flow Qualification of Electronic Components for Space Application.
- REP005, Qualified Parts List.
- REP006, Qualified Manufacturers List

For qualification and qualification maintenance or procurement of qualified components, with the exception of ESCC Basic Specifications Nos. 20100, 21700, 22800, 24600 and 25400, where Manufacturers' specifications are equivalent to, or more stringent than, the ESCC Basic Specifications listed above, they may be used in place of the latter, subject to the approval of the ESCC Executive. Such replacements shall be clearly identified in the applicable Process Identification Document (PID).

For procurement of unqualified components, where Manufacturers' specifications are equivalent to or more stringent than the ESCC Basic Specifications listed above, they may be used in place of the latter subject to the approval of the Orderer.

Such replacements may be listed in an appendix to the appropriate Detail Specification at the request of the Manufacturer or Orderer, subject to the approval of the ESCC Executive.

Unless otherwise stated herein, references within the text of this specification to "the Detail Specification" shall mean the relevant ESCC Detail Specification.

2.2 OTHER (REFERENCE) DOCUMENTS

- ECSS-Q-ST-60, Electrical, Electronic and Electromechanical (EEE) Components.
- J-STD-020, IPC/Jedec Standard for Moisture/Reflow Sensitivity Classification for Non-Hermetic Surface-Mount Devices.
- J-STD-033, IPC/Jedec Standard for Handling, Packing, Shipping and Use of Moisture, Reflow, and Process Sensitive Devices.
- JESD22-A101, EIA/Jedec Standard Test Method: Steady-State Temperature-Humidity Bias Life Test.
- JESD22-A102 EIA/Jedec Standard Test Method: Accelerated Moisture Resistance - Unbiased Autoclave.
- JESD22-A104, EIA/Jedec Standard Test Method: Temperature Cycling.
- JESD22-A108, EIA/Jedec Standard Test Method: Temperature, Bias, and Operating Life.
- JESD22-A110, EIA/Jedec Standard Test Method: Highly Accelerated Temperature and Humidity Stress Test (HAST).
- JESD22-A113, EIA/Jedec Standard Test Method: Preconditioning of Non-hermetic Surface Mount Devices prior to Reliability Testing.
- JESD22-A118, EIA/Jedec Standard Test Method: Accelerated Moisture Resistance - Unbiased Hast.
- JESD22-B101, EIA/Jedec Standard Test Method: External Visual.
- JESD22-B102, EIA/Jedec Standard Test Method: Solderability.
- JESD22-B116, EIA/Jedec Standard Test Method: Wire Bond Shear Test.
- JESD22-B117, EIA/Jedec Standard Test Method: Solder Ball Shear.
- MIL-STD-883, Test Methods and Procedures for Micro-electronics.

2.3 ORDER OF PRECEDENCE

For the purpose of interpretation and in case of conflict with regard to documentation, the following order of precedence shall apply:

(a) ESCC Detail Specification.
(b) ESCC Generic Specification.
(c) ESCC Basic Specification.
(d) Other documents, if referenced herein.

3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

The terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply. In addition, the following shall apply:

o Integrated Circuit (Microcircuit):	A small circuit having a high equivalent circuit element density, which is considered as a single part composed of interconnected elements on or within a single substrate to perform an electronic circuit function. Monolithic microcircuits are considered as Integrated Circuits.
o Monolithic Microcircuit:	A microcircuit consisting exclusively of elements formed in situ on or within a single semiconductor substrate with at least one of the elements formed within the substrate (with a single semiconductor die).
o Wire-Bonded Integrated Circuit:	A monolithic microcircuit with the die backside bonded to the package cavity or organic substrate, and wire-bonded to either a metal lead-frame or an organic substrate with solder balls or columns.
o Flip-Chip Integrated Circuit:	A monolithic microcircuit with bumps attached to the active side of the die, connected top side down to an organic substrate, with underfill, and solder balls or columns.
o Add-on Components:	Capacitors and/or resistors mounted in and electrically connected to a Flip-Chip Integrated Circuit assembly. Other component types are not permitted.
o Plastic Encapsulation	Encapsulation by means of being moulded within moulding compound.
o Cavity Packaged Component	A Flip-Chip Integrated Circuit that has some internal electrical connections not fully embedded in moulding compound.

4 REQUIREMENTS

4.1 GENERAL

Unless otherwise specified, the requirements for the qualification of a component shall be in accordance with ESCC Basic Specification No. 20100.

The requirements for Technology Flow Qualification and the listing of qualified component types shall be in accordance with ESCC Basic Specification No. 25400.

The test requirements for procurement of both qualified and unqualified components (see Chart F1) shall comprise:

- Wafer Lot Acceptance with, if stipulated in the Purchase Order, total dose radiation testing.
- Special In-Process Controls.
- Screening Tests.
- Periodic Testing (for qualified components only).
- Lot Validation Testing if stipulated in the Purchase Order.

4.1.1 Specifications

For qualification, qualification maintenance, procurement and delivery of components in conformity with this specification, the applicable specifications listed in Section 2 of this document shall apply in total unless otherwise specified herein or in the Detail Specification.

4.1.2 Conditions and Methods of Test

The conditions and methods of test shall be in accordance with this specification, the ESCC Basic Specifications referenced herein and the Detail Specification.

4.1.3 Manufacturer's Responsibility for Performance of Tests and Inspections

The Manufacturer shall be responsible for the performance of tests and inspections required by the applicable specifications. These tests and inspections shall be performed at the plant of the Manufacturer of the components unless it is agreed by the ESCC Executive (for qualification, qualification maintenance, or procurement of qualified components) or the Orderer (for procurement of unqualified components), to use an approved external facility.

4.1.4 Inspection Rights

The ESCC Executive (for qualification, qualification maintenance, or procurement of qualified components) or the Orderer (for procurement of unqualified components if stipulated in the Purchase Order) reserves the right to monitor any of the tests and inspections scheduled in the applicable specifications.

4.1.5 Customer Source Inspections

4.1.5.1 Pre-Encapsulation Customer Source Inspection

If stipulated in the Purchase Order, the Orderer may perform a source inspection at the Manufacturer's facility prior to Encapsulation / Moulding / Lid Attach / Heat-Spreader Placement (as applicable) (e.g. perform Internal Visual Inspection, witness of Die Shear Strength and Wire Bond Pull). Details of the inspections to be performed or witnessed and the required period of notification shall be as stipulated in the Purchase Order.

For Flip-Chip Integrated Circuit components, the inspection may be performed on piece parts prior to or after die to substrate attachment unless otherwise stated in the Detail Specification.

4.1.5.2 Final Customer Source Inspection

If stipulated in the Purchase Order, the Orderer may perform a source inspection at the Manufacturer's facility prior to delivery at an appropriate point during testing that has been agreed with the Manufacturer (e.g., witness of final Room Temperature Electrical Measurements; performance of External Visual Inspection and Dimension Check; review of the data documentation package). Details of the inspections to be performed or witnessed and the required period of notification shall be as stipulated in the Purchase Order.

4.2 QUALIFICATION AND QUALIFICATION MAINTENANCE REQUIREMENTS ON A MANUFACTURER

To obtain and maintain the qualification of a component, or family of components, a Manufacturer shall satisfy the requirements of ESCC Basic Specification No. 20100.

To obtain and maintain the qualification of a component produced using a qualified Technology Flow, a Manufacturer shall satisfy the requirements of ESCC Basic Specification No. 25400.

4.3 DELIVERABLE COMPONENTS

4.3.1 ESCC Qualified Components

Components delivered to this specification shall be processed and inspected in accordance with the relevant Process Identification Document (PID).

4.3.2 ESCC Components

Each component, irrespective of qualification status, identified with an ESCC component number and delivered to this specification shall:

- be traceable. Each component shall be traceable to its production lot.
- have satisfactorily completed all the tests required by the relevant issues of the applicable specifications.
- be produced from lots that are considered by the Manufacturer to be capable of passing all applicable tests, and sequences of tests, that are defined in Chart F4A or F4B, as applicable. The Manufacturer shall not knowingly supply components that cannot meet this requirement. In the event that, subsequent to delivery and prior to operational use, a component is found to be in a condition such that, demonstrably, it could not have passed these tests at the time of manufacture, this shall be grounds for rejection of the delivered lot.

4.3.3 Lot Failure

Lot failure may occur during Wafer Lot Acceptance (Chart F2), Special In-Process Controls (Chart F2), Screening Tests (Chart F3), or Qualification, Periodic Testing and Lot Validation Testing (Charts F4A and F4B).

Should such failure occur during qualification, qualification maintenance or procurement of qualified components the Manufacturer shall initiate the non-conformance procedure in accordance with ESCC Basic Specification No. 22800. The Manufacturer shall notify the Orderer and the ESCC Executive by any appropriate written means, within 5 working days, giving details of the number and mode of failure and the suspected cause. No further testing or analysis shall be performed on the failed components until so instructed by the ESCC Executive.

Should such failure occur during procurement of unqualified components the Manufacturer shall notify the Orderer by any appropriate written means within 5 working days, giving details of the number and mode of failure and the suspected cause. No further testing or analysis shall be performed on the failed components until so instructed by the Orderer. The Orderer shall inform the Manufacturer within 5 working days of receipt of notification what action shall be taken.

4.4 MARKING

All components procured and delivered to this specification shall be marked in accordance with ESCC Basic Specification No. 21700.

4.5 CONSTRUCTION, MATERIALS AND FINISHES

Specific requirements for materials and finishes are specified in the Detail Specification. Where a definite material or finish is not specified a material or finish shall be used so as to ensure that the component meets the performance requirements of this specification and the Detail Specification. Acceptance or approval of any constituent material or finish does not guarantee acceptance of the finished product.

All materials and finishes of the components specified in the Detail Specification shall comply with the restrictions on materials specified in ESCC Basic Specification No. 22600.

The glass transition temperature, T_g, shall be declared in the Detail Specification.

4.6 ADD-ON COMPONENTS REQUIREMENTS

Only applicable to Flip-Chip Integrated Circuit components.

The selection of add-on components shall be made in accordance with the requirements of ECSS-Q-ST-60.

All Add-on Components (i.e., capacitors and resistors only) incorporated into deliverable components shall be procured as traceable homogeneous lots.

For qualified Flip-Chip Integrated Circuit components, the PID shall include a list of Add-on Components which have been successfully tested according to the requirements of this specification and approved for their inclusion in the PID by the ESCC Executive.

For qualified Flip-Chip Integrated Circuit components, if available, Add-on Components shall be ESCC Qualified as evidenced by a listing in the current ESCC Qualified Parts List REP005 or ESCC Qualified Manufacturers List REP006. If the required component types are not available, ECSS-Q-ST-60 requirements for Class 1 components shall be applied.

Documentation requirements for Add-on Components shall be as specified in Para. 9.7.

4.7 RADIATION TESTING

For qualification or qualification maintenance total dose radiation testing shall be performed when specified in the Detail Specification to the specified total dose level.

For procurement, as stipulated in the Purchase Order, total dose radiation testing shall be performed to the total dose level specified in the Detail Specification or to an alternate level if so stipulated in the Purchase Order.

The qualification status of the procured components shall not be impacted by any change to the total dose level applied.

For procurement, any lot of components that fails the specified total dose radiation test level may be accepted to a lower level of radiation subject to satisfactory test results at the lower level. In this case the total dose radiation level letter for the lot shall be modified accordingly.

5 PRODUCTION CONTROL

5.1 GENERAL

Unless otherwise specified herein or in the Detail Specification, all lots of components used for qualification and qualification maintenance, Lot Validation Testing and for delivery shall be subject to tests and inspections in accordance with Chart F2 in the sequence shown.

Any components which do not meet these requirements shall be removed from the lot and at no future time be resubmitted to the requirements of this specification.

The applicable test requirements are detailed in the paragraphs referenced in Chart F2.

For qualified components, the full production control provisions are defined in the PID.

In the case of lot failure, the Manufacturer shall act in accordance with Para. 4.3.3.

5.1.1 Rework and Repair

Any rework or repair procedures shall be agreed with the ESCC Executive (for qualification, qualification maintenance, or procurement of qualified components) or the Orderer (for procurement of unqualified components).

For qualified components, all rework and repair processes shall have been fully specified, documented and qualified by the Manufacturer, and shall be listed in the PID.

Unless otherwise specified, the following specific rework and repair requirements shall apply:

(a) For Wire-Bonded Integrated Circuit components: The rebonding of wires during assembly is not permitted.

(b) For components with column grid array packages: The entire column may be replaced only once.

(c) For Flip-Chip Integrated Circuit components:

- Any polymer attached Add-on Component may be replaced twice at a given location.
- Any solder attached Add-on Component may be replaced once at a given location.
- The total number of replacements shall be limited to a maximum of 10% of the total number of Add-on Components.
- There shall be a maximum of 4 heating cycles for Add-on Component removal.
- It shall be demonstrated that the reliability of the remaining Add-on Components is not impacted.
- Neither rework nor repair of Flip-Chip attachment to the substrate (including underfill) is allowed.
- No thermal interface material rework is allowed after cure.
- For the purposes of rework or repair, no delidding is allowed where there is a physical link between die and lid (thermal interface material or other). If there is no physical link between die and lid, the components may be delidded and relidded provided that:
  - No more than one delid-relid cycle is performed.
  - Suitable screening tests shall be performed on the delidded-relidded components. These screening tests shall be defined at the stage when the delidding-relidding takes place and depend on the type of repair performed.

5.2 WAFER LOT ACCEPTANCE

5.2.1 Process Monitoring Review

Process monitoring review shall be done in compliance with the Manufacturer's SPC rules described in the PID (for qualification, qualification maintenance or procurement of qualified components).

A wafer shall be rejected if one or more process control data parameters exceed the allowed distribution as specified in the PID (for qualification, qualification maintenance or procurement of qualified components).

5.2.2 Wafer Lot Screening

Wafer Lot Screening shall consist of the following:

- 100% Die Visual Inspection in accordance with Para. 8.1(a), either as an on-wafer inspection or after dice separation.

NOTE: Wafer Lot Screening may be performed on a selected sublot basis. The selected sublot shall consist of a minimum of the components necessary for delivery, testing and allowable failures.

5.2.3 Scanning Electron Microscope (SEM) Inspection

Semiconductor dice incorporated into components supplied to this specification shall originate from a wafer lot that has been subjected to, and successfully met, the Scanning Electron Microscope Inspection requirements in accordance with Para. 8.2.

5.2.4 Total Dose Radiation Testing

For qualification or qualification maintenance:

- If specified in the Detail Specification, semiconductor dice incorporated into components shall originate from a wafer lot which has been subjected to and successfully completed Total Dose Radiation Testing in accordance with Para. 8.3 to the specified total dose level.

During procurement:

- If specified in the Detail Specification and stipulated in the Purchase Order, semiconductor dice incorporated into components shall originate from a wafer lot which has been subjected to and successfully completed Total Dose Radiation Testing in accordance with Para. 8.3 to the stipulated total dose level.

5.2.5 Documentation

Documentation of Wafer Lot Acceptance shall be in accordance with Para. 9.5.

5.3 SPECIAL IN-PROCESS CONTROLS

Review of Special In-Process Controls (Chart F2) shall be done in compliance with the Manufacturer's SPC rules described in the PID (for qualification, qualification maintenance or procurement of qualified components).

A wafer shall be rejected if one or more process control data parameters exceed the allowed distribution as specified in the PID (for qualification, qualification maintenance or procurement of qualified components).

Sampling for all Special In-Process Controls shall be agreed with the ESCC Executive (for qualification, qualification maintenance or procurement of qualified components) or the Orderer (for procurement of unqualified components). If sampling is specified for any test or inspection in Special In-Process Controls, it may be used by the Manufacturer as a guideline for the actual sampling to be applied.

5.3.1 Die Shear Strength or Substrate Attach Strength (for Wire-Bonded Integrated Circuits)

Either Die Shear Strength or Substrate Attach Strength, as applicable, shall be performed on a quantity of components as specified in the PID in accordance with Para. 8.4(a).

A single failure shall be cause for lot failure. These tests are considered as destructive and therefore components so tested shall not form part of the delivery lot.

NOTE:

Die Shear Strength or Substrate Attach Strength may be performed subsequent to encapsulation / moulding / lid attach / heat-spreader placement (as applicable) at the Manufacturer's discretion. In this case, a quantity of components as specified in the PID shall be de-encapsulated in accordance with ESCC Basic Specification No. 25300, or equivalent, to enable the test.

Any observed defect determined to have resulted from the de-encapsulation process may be ignored subject to the approval of the ESCC Executive.

5.3.2 Wire Bond Pull and Wire Bond Shear (for Wire-Bonded Integrated Circuits)

Both Wire Bond Pull and Wire Bond Shear shall be performed on a quantity of components as specified in the PID in accordance with Para. 8.5.

A single failure shall be cause for lot failure. These tests are considered as destructive and therefore components so tested shall not form part of the delivery lot.

NOTE:

Wire Bond Pull and Wire Bond Shear may be performed subsequent to encapsulation / moulding / lid attach / heat-spreader placement (as applicable) at the Manufacturer's discretion. In this case, a quantity of components as specified in the PID shall be de-encapsulated in accordance with ESCC Basic Specification No. 25300, or equivalent, to enable the tests.

Any observed defect determined to have resulted from the de-encapsulation process may be ignored subject to the approval of the ESCC Executive.

5.3.3 Internal Visual Inspection

(a) For Wire-Bonded and Flip-Chip Integrated Circuit components: Internal Visual Inspection in accordance with Para. 8.1(b) on a quantity of components as specified in the PID.

(b) For Flip-Chip Integrated Circuit components prior to die attach, as follows:

- A quantity of packages/substrates as specified in the PID shall be visually inspected to ensure the reliable soldering of bumps on lands.

(c) For Flip-Chip Integrated Circuit components, as follows:

- Visual inspection of Add-on Components, as applicable, in accordance with Para. 8.1(c) on a quantity of samples as specified in the PID

NOTE:

Internal Visual Inspection (see (a), (b), (c) above) may be performed subsequent to encapsulation / moulding / lid attach / heat-spreader placement (as applicable) at the Manufacturer's discretion. In this case, a quantity of components as specified in the PID shall be de-encapsulated in accordance with ESCC Basic Specification No. 25300, or equivalent, to enable the inspection. Components so tested shall not form part of the delivery lot.

Any observed defect determined to have resulted from the de-encapsulation process may be ignored subject to the approval of the ESCC Executive.

Where Internal Visual Inspection (see (a), (b), (c) above) has been performed on a 100% basis, any failures shall be removed from the lot. Where Internal Visual Inspection is performed on a sample basis, a single failure shall be cause for lot failure.

5.3.4 Scanning Acoustic Microscopy (SAM)

SAM shall be performed in accordance with Para. 8.6 on a quantity of components as specified in the PID.

A single failure shall be cause for lot failure unless a 100% inspection is subsequently performed.

5.3.5 Lid Attach Strength

Lid Pull or Lid Shear, as applicable and as specified in the Detail Specification, shall be performed in accordance with Para. 8.7 on a quantity of components as specified in the PID.

A single failure shall be cause for lot failure. This test is considered as destructive and therefore components so tested shall not form part of the delivery lot.

5.3.6 Ball or Column Terminal Strength

Ball or Column (as applicable) Terminal Strength shall be performed in accordance with Para. 8.8(b) or 8.8(c) on a quantity of components as specified in the PID.

A single failure shall be cause for lot failure. This test is considered as destructive and therefore components so tested shall not form part of the delivery lot.

5.3.7 Bond Shear (for Flip-Chip Integrated Circuits)

Bond Shear (Flip-Chip) shall be performed in accordance with Para. 8.4(b) on a quantity of components as specified in the PID.

A single failure shall be cause for lot failure. This test is considered as destructive and therefore components so tested shall not form part of the delivery lot.

5.3.8 Add-on Components Die Shear Strength or Substrate Attach Strength (for Flip-Chip Integrated Circuits)

Either Die Shear Strength or Substrate Attach Strength, as applicable, shall be performed on mounted Add-on Components in accordance with Para. 8.4(c) on a quantity of components as specified in the PID.

A single failure shall be cause for lot failure. This test is considered as destructive and therefore components so tested shall not form part of the delivery lot.

5.3.9 Dimension Check

Dimension Check shall be performed in accordance with Para. 8.8 on 3 samples only. In the event of any failure, a 100% Dimension Check shall be performed.

5.3.10 Weight

The maximum weight of the component specified in the Detail Specification shall be guaranteed but not tested.

5.3.11 Documentation

Documentation of Special In-Process Controls shall be in accordance with Para. 9.6.

6 SCREENING TESTS

6.1 GENERAL

Unless otherwise specified herein or in the Detail Specification, all lots of components used for qualification and qualification maintenance, Lot Validation Testing, and for delivery, shall be subjected to tests and inspections in accordance with Chart F3 in the sequence shown.

All components shall be serialised prior to the tests and inspections.

Any components which do not meet these requirements shall be removed from the lot and at no future time be resubmitted to the requirements of this specification.

The applicable test methods and conditions are specified in the paragraphs referenced in Chart F3.

6.2 FAILURE CRITERIA

6.2.1 Environmental and Mechanical Test Failure

The following shall be counted as component failures:

- Components which fail during tests for which the pass/fail criteria are inherent in the test method, i.e., Radiographic Inspection, SAM, External Visual Inspection and Solderability.

6.2.2 Parameter Drift Failure

The acceptable change limits are shown in Parameter Drift Values in the Detail Specification. A component shall be counted as a parameter drift failure if the changes during High Temperature Reverse Bias Burn-in or during Power Burn-in are larger than the drift values (Δ) specified.

6.2.3 Parameter Limit Failure

A component shall be counted as a limit failure if one or more parameters exceed the limits shown in Room Temperature Electrical Measurements or High and Low Temperatures Electrical Measurements in the Detail Specification.

Any component which exhibits a limit failure prior to the submission to HTRB Burn-in shall be rejected and not counted when determining lot rejection.

6.2.4 Other Failures

A component shall be counted as a failure in any of the following cases:

- Visual failure.
- Mechanical failure.
- Handling failure.
- Lost component.

6.3 FAILED COMPONENTS

A component shall be considered as a failed component if it exhibits one or more of the failure modes described in Para. 6.2.

6.4 LOT FAILURE

In the case of lot failure, the Manufacturer shall act in accordance with Para. 4.3.3.

6.4.1 Lot Failure during 100% Testing

If the number of components failed on the basis of the failure criteria specified in Paras. 6.2.2 and 6.2.3 exceeds 5% (rounded upwards to the nearest whole number) of the components submitted to High Temperature Reverse Bias Burn-in (or Power Burn-in if HTRB Burn-in is not being performed) of Chart F3, the lot shall be considered as failed.

If a lot is composed of groups of components of one family defined in one ESCC Detail Specification, but separately identifiable for any reason, then the lot failure criteria shall apply separately to each identifiable group.

6.4.2 Lot Failure during Sample Testing

A lot shall be considered as failed if the number of allowable failures during sample testing as specified herein or in the Detail Specification, is exceeded.

Unless otherwise specified, if a lot failure occurs, a 100% testing may be performed but the cumulative percent defective shall not exceed that specified in Para. 6.4.1.

No failures are allowed for the Solderability test.

6.5 DOCUMENTATION

Documentation of Screening Tests shall be in accordance with Para. 9.8.

7 QUALIFICATION, QUALIFICATION MAINTENANCE AND LOT VALIDATION TESTING

The requirements of this paragraph are applicable to the tests performed on components or test structures as part of qualification or qualification maintenance in accordance with either ESCC Basic Specification No. 20100 or 25400 as applicable. They are also applicable to Lot Validation Testing as part of the procurement of qualified or unqualified components.

7.1 QUALIFICATION TESTING

7.1.1 General

Qualification testing shall be in accordance with the requirements specified in Chart F4A or F4B as follows:

- Chart F4A: for Wire-Bonded Integrated Circuits
- Chart F4B: for Flip-Chip Integrated Circuits

The tests of Charts F4A and F4B shall be performed on the specified sample, chosen at random from the components which have successfully passed the tests in Chart F3.

This sample constitutes the Qualification Test Lot. The Qualification Test Lot is divided into subgroups of tests and, unless otherwise specified, all components assigned to a subgroup shall be subjected to all of the tests in that subgroup, in the sequence shown. The applicable test requirements are detailed in the paragraphs referenced in Charts F4A and F4B.

The conditions governing qualification testing are specified in ESCC Basic Specification No. 20100.

7.1.2 Distribution within the Qualification Test Lot

The Qualification Test Lot shall be comprised in accordance with the following provisions, depending on whether it is required to obtain qualification for a single component type or for a family of component types.

7.1.2.1 Single Component Type

When it is proposed to submit a single component type for qualification testing, the sample quantity shall be as specified in Chart F4A or F4B, Note 1. However, when such a single component type is to be qualified in more than one type of package, each package variation must be equally represented in the Environmental/Mechanical, Endurance and Assembly Capability Subgroups of Charts F4A and F4B. For this purpose, unless otherwise specified, the applicable sample distribution shall be the same as for the qualification of a family of component types as specified in Charts F4A and F4B, Note 2 or Note 3.

7.1.2.2 Family of Component Types

A family of component types is a series of components produced by the same manufacturing techniques, using the same types of machines and apparatus. Such components will be designed for the same supply, bias and signal voltages and for an input/output compatibility with each other under an established set of loading rules. They shall be produced using the same technology (e.g., the same diffusion schedules, method of metallisation, etc.) and identical design rules.

Qualification may be granted to a family of components subject to the successful outcome of the qualification testing of certain specified component types to represent the family.

Structurally similar components from such a family may be grouped together for the purpose of selecting samples for qualification testing. The component types selected must adequately represent all of the various mechanical, structural and electrical elements encountered within the family.

The component types chosen must be those that employ the extremes of design rules and tolerances and contain the maximum of internal sub-circuitry complexity, i.e., usually those that give the greatest risk of rejection.

When qualification is required for component types in more than one type of package, each package must be adequately represented in the Environmental/Mechanical, Endurance and Assembly Capability subgroups.

The component types may be specified by, but in any case, shall be agreed with the ESCC Executive prior to the commencement of qualification testing and the justification for the selection shall be declared in the qualification test report.

The number of component types selected as representative of the family will therefore determine the total number of components comprising the qualification test lot. Unless otherwise specified, depending on the number of types selected, the sample sizes shall be as specified in Charts F4A and F4B, Note 2 or Note 3.

In the case of four or more component types selected, different pass/fail criteria from those shown in Charts F4A and F4B may be applicable. When appropriate, these shall be agreed with the ESCC Executive prior to the commencement of qualification testing.

7.2 QUALIFICATION WITHIN A TECHNOLOGY FLOW

The qualification of a component produced using a qualified Technology Flow shall be in accordance with ESCC Basic Specification No. 25400.

7.3 QUALIFICATION MAINTENANCE (PERIODIC TESTING)

Qualification is maintained through periodic testing and the test requirements of Para. 7.1 shall apply. For each subgroup, the sample size, the test requirements and the period between successive subgroup testing shall be as specified in Charts F4A and F4B.

The conditions governing qualification maintenance are specified in ESCC Basic Specification No. 20100.

Qualification of a component, produced using a qualified Technology Flow, is maintained by the maintenance of the Technology Flow Qualification itself in accordance with ESCC Basic Specification No. 25400.

7.4 LOT VALIDATION TESTING

For procurement of qualified components, Lot Validation Testing is not required and shall only be performed if specifically stipulated in the Purchase Order.

For procurement of unqualified components, the need for Lot Validation Testing shall be determined by the Orderer (ref. ESCC Basic Specification No. 23100).

When Lot Validation Testing is required, it shall consist of the performance of one or more of the tests or subgroup test sequences of Chart F4A or F4B, as applicable. The testing to be performed and the sample size shall be as stipulated in the Purchase Order.

When procurement of more than one component type is involved from a family, range or series, the selection of representative samples shall also be stipulated in the Purchase Order.

7.5 FAILURE CRITERIA

The following criteria shall apply to qualification, qualification maintenance and Lot Validation Testing.

7.5.1 Environmental and Mechanical Test Failure

The following shall be counted as component failures:

- Components which fail during tests for which the pass/fail criteria are inherent in the test method, e.g., Solderability, Terminal Strength, etc.

7.5.2 Electrical Failure

The following shall be counted as component failures:

- Components which fail one or more of the applicable limits at each of the relevant data points specified for environmental, mechanical and endurance testing in Intermediate and End-Point Electrical Measurements in the Detail Specification.

7.5.3 Other Failures

A component shall be counted as a failure in any of the following cases:

- Visual failure
- Mechanical failure
- Handling failure
- Lost component

7.6 FAILED COMPONENTS

A component shall be considered as failed if it exhibits one or more of the failure modes detailed in Para. 7.5.

When requested by the ESCC Executive (for qualification, qualification maintenance or procurement of qualified components) or the Orderer (for procurement of qualified or unqualified components), failure analysis of failed components shall be performed under the responsibility of the Manufacturer and the results provided.

Failed components shall be retained at the Manufacturer's plant until the final disposition has been agreed and certified.

7.7 LOT FAILURE

For qualification and qualification maintenance, the lot shall be considered as failed if one component in any subgroup of Chart F4A or F4B, as applicable, is a failed component based on the criteria specified in Para. 7.5.

For procurement, the lot shall be considered as failed if one component in any test specified for Lot Validation Testing is a failed component based on the criteria specified in Para. 7.5.

In the case of lot failure, the Manufacturer shall act in accordance with Para. 4.3.3.

7.8 QUALIFICATION, PERIODIC TESTING AND LOT VALIDATION TESTING SAMPLES

All tests of Charts F4A and F4B are considered to be destructive and therefore components so tested shall not form part of the delivery lot.

7.9 DOCUMENTATION

Documentation of Qualification, Periodic Testing and Lot Validation Testing shall be in accordance with Para. 9.9.

8 TEST METHODS AND PROCEDURES

If a Manufacturer elects to eliminate or modify a test method or procedure, the Manufacturer is still responsible for delivering components that meet all of the performance, quality and reliability requirements defined in this specification and the Detail Specification.

For a qualified component, documentation supporting the change shall be approved by the ESCC Executive and retained by the Manufacturer. It shall be copied, when requested, to the ESCC Executive. The change shall be specified in an appendix to the Detail Specification and in the PID.

For an unqualified component, the change shall be approved by the Orderer. The change may be specified in an appendix to the Detail Specification at the request of the Manufacturer or Orderer, subject to the approval of the ESCC Executive.

8.1 INTERNAL VISUAL INSPECTION

(a) Die Visual Inspection:
MIL-STD-883, Test Method 2010 Condition A (Class level S).

(b) Internal Visual Inspection of Wired-bonded and Flip-Chip Integrated Circuits:
MIL-STD-883, Test Method 2010, Condition A (Class level S) (or MIL-STD-883, Test Method 2013 and 2014).

- Test Samples:
  - During Special In-Process Controls (Chart F2): See Para. 5.3.3(a).
  - During Qualification, Periodic Testing and Lot Validation Testing (Charts F4A and F4B): All components in each applicable subgroup.

(c) Visual Inspection of Add-on Components (Flip-Chip Integrated Circuits):
MIL-STD-883, Test Method 2032 Class H, and MIL-STD-883, Test Method 2017 Class H (or MIL-STD-883, Test Method 2013 and 2014) (see Para. 5.3.3).

- Test Samples:
  - During Special In-Process Controls (Chart F2): See Para. 5.3.3(c).
  - During Qualification, Periodic Testing and Lot Validation Testing (Charts F4A and F4B): All components in each applicable subgroup.

8.2 SCANNING ELECTRON MICROSCOPE INSPECTION

MIL-STD-883, Test Method 2018.

NOTE:

For components manufactured with semiconductor processes that defeat the objectives of the above specification, the deviations from the specified requirements shall be identified in the PID and the Detail Specification.

8.3 TOTAL DOSE RADIATION TESTING

ESCC Basic Specification No. 22900 to the total dose level specified in the Detail Specification or as stipulated in the Purchase Order.

8.4 DIE SHEAR STRENGTH, SUBSTRATE ATTACH STRENGTH OR BOND SHEAR

(a) For Wire-Bonded Integrated Circuit components:
Die Shear Strength, or Substrate Attach Strength (as applicable): MIL-STD-883, Test Method 2019 or 2027.

Individual separation forces and categories shall be recorded. A single failure shall be cause for lot failure.

- Test Samples:
  - During Special In-Process Controls (Chart F2): See Para. 5.3.1.
  - During Qualification, Periodic Testing and Lot Validation Testing (Chart F4A): All components in the applicable subgroup.

(b) For Flip-Chip Integrated Circuit components:
Bond Shear (Flip-Chip): MIL-STD-883, Test Method 2011 Test Condition F.

Individual separation forces and categories shall be recorded. A single failure shall be cause for lot failure.

(c) For Add-on Components mounted in Flip-Chip Integrated Circuit components:
Die Shear Strength or Substrate Attach Strength (as applicable): MIL-STD-883, Test Method 2019 or 2027.

- Test Samples:
  - During Special In-Process Controls (Chart F2): See Para. 5.3.8.
  - During Qualification, Periodic Testing and Lot Validation Testing (Chart F4B): All or 10, whichever is less, of the Add-on components in a single test sample selected from the components in the Assembly Capability Subgroup.

Individual separation forces and categories shall be recorded. A single failure shall be cause for lot failure.

8.5 WIRE BOND PULL AND WIRE BOND SHEAR

For Wire-Bonded Integrated Circuit components.

(a) Wire Bond Pull:
MIL-STD-883, Test Method 2011.
- Test Conditions: Test condition C or D.

(b) Wire Bond Shear:
JESD22-B116.

Test Samples:
- During Special In-Process Controls (Chart F2): See Para. 5.3.2.
- During Qualification, Periodic Testing and Lot Validation Testing (Chart F4A): The required test samples are specified in the Assembly Capability Subgroup:
  - Quantity of internal bond wires ≤ 24 bonds: test 50% Wire Bond Pull, 50% Wire Bond Shear.
  - Quantity of internal bond wires > 24 bonds: test 25% Wire Bond Pull, 25% Wire Bond Shear.

Individual separation forces and categories shall be recorded. A single failure shall be cause for lot failure.

8.6 SCANNING ACOUSTIC MICROSCOPY

ESCC Basic Specification No. 25200, plus additional SAM requirements as specified in the Detail Specification, including specific inspection requirements applicable to all thermal interface materials.

NOTE:
Components submitted to SAM shall be subjected to a final drying phase consisting of a minimum bake of duration 1 hour at T_{amb} = +125°C. J-STD-033 may be used as a guideline for the appropriate drying conditions.

- Test Samples:
  - During Special In-Process Controls (Chart F2): See Para. 5.3.4.
  - During Screening Tests (Chart F3): 22 components or 10% of the lot, whichever is greater. In the event of a failure, the lot shall be tested 100%.
  - During Qualification, Periodic Testing and Lot Validation Testing (Charts F4A and F4B): All components in each applicable subgroup.

The following additional reject criteria shall also apply:

(a) For Wire-Bonded Integrated Circuits with a metal lead-frame:
1. No delamination on the active side of the die
2. No delamination on any wire bonding surface including the down-bond area or the lead-frame of lead-on-chip (LOC) components.
3. No surface-breaking feature delaminated over its entire length. A surface-breaking feature includes lead fingers, tie bars, heat-spreader alignment features, heat slugs, etc..
4. No delamination/cracking > 50% of the die attach area:
   i. in components with exposed die pad used for thermal conductivity
   ii. for components that require electrical contact to the backside of the die
5. Delamination of more than half of the backside of the die paddle/plastic interface.
6. Any void in moulding compound crossing wire-bond.

(b) For Wire-Bonded Integrated Circuits with an organic substrate:
1. No delamination on the active side of the die
2. No delamination on any wire bonding surface including the down-bond area or the lead-frame of lead-on-chip (LOC) components.
3. No delamination on any electrical contact surface of the laminate.
4. No delamination within the substrate.
5. No delamination/cracking > 50% of the die attach area:
   i. in components with exposed die pad used for thermal conductivity
   ii. for components that require electrical contact to the backside of the die
6. No surface-breaking feature delaminated over its entire length. A surface-breaking feature includes lead fingers, tie bars, heat-spreader alignment features, heat slugs, etc..
7. Any void in moulding compound crossing wire-bond.

(c) For Flip-Chip Integrated Circuits:
1. No delamination on the active side of the die
2. No delamination on any electrical contact surface of the laminate.
3. No surface-breaking feature delaminated over its entire length. A surface-breaking feature includes lead fingers, laminate, laminate metallization, PTH, heat slugs, etc.
4. No delamination/cracking between underfill resin and chip, or underfill resin and substrate/solder mask.
5. No delamination within the substrate.

8.7 LID ATTACH STRENGTH

MIL-STD-883, Test Method 2027 (Pull test) or 2019 (Shear test). All test results shall be recorded

- Failure criteria: < 200% (2X) of the calculated minimum die attach strength.

8.8 TERMINAL STRENGTH

All test results shall be recorded.

(a) For chip carrier packages: MIL-STD-883, Test Method 2004, Test Condition D.

(b) For ball grid array packages: JESD22-B117; 45 balls from 2 devices minimum, unless otherwise specified (see Para. 5.3.6).

(c) For column grid array packages: MIL-STD-883, Test Method 2038; 45 columns from 2 devices minimum, unless otherwise specified (see Para. 5.3.6).

(d) For other packages: MIL-STD-883, Test Method 2004, Test Condition B2; 3 leads (excluding corner leads) or 10% of the leads (whichever is greater) randomly selected on each component.

8.9 DIMENSION CHECK

MIL-STD-883, Test Method 2016, and the Detail Specification. In the event of any failure a 100% Dimension Check shall be performed

8.10 RADIOGRAPHIC INSPECTION

MIL-STD-883, Test Method 2012.

8.11 CONSTANT ACCELERATION
Cavity Packaged Components only.

8.11.1 During Screening Tests (Chart F3)
Unless otherwise specified in the Detail Specification:

(a) For packages with total area ≤ 645mm^2: MIL-STD-883, Test Method 2001, Test Condition B.
(b) For packages with total area > 645mm^2 and ≤ 1290mm^2: MIL-STD-883, Test Method 2001, Test Condition A.
(c) For packages > 1290mm^2: Shall not be performed.

8.11.2 During Qualification, Periodic Testing and Lot Validation Testing (Chart F4B)
MIL-STD-883, Test Method 2001, Test Condition E (resultant centrifugal acceleration to be in the Y1 axis only). For components which have a package weight of 5 grammes or more, or whose inner seal or cavity perimeter is more than 5 cm, Condition D shall be used.

8.12 TEMPERATURE CYCLING

8.12.1 During Screening Tests (Chart F3)
MIL-STD-883, Test Method 1010. Test Condition B, 20 cycles.

8.12.2 During Qualification, Periodic Testing and Lot Validation Testing (Charts F4A and F4B)
MIL-STD-883, Test Method 1010, Test Condition B, 500 cycles.

8.13 BAKE
All components shall be subjected a Bake with the same conditions as used for the final drying phase after SAM; see Para. 8.6. Components that have already been subjected to drying after SAM, during Screening Tests (Chart F3), shall not be resubjected to Bake.

8.14 ELECTRICAL MEASUREMENTS

8.14.1 Parameter Drift Values
At each of the relevant data points during Screening Tests (Chart F3), Parameter Drift Values shall be measured as specified in the Detail Specification. All values obtained shall be recorded against serial numbers and the parameter drift calculated.

8.14.2 Room Temperature Electrical Measurements
Room Temperature Electrical Measurements shall be performed as specified in the Detail Specification. All values obtained shall be recorded against serial numbers.

8.14.3 High and Low Temperatures Electrical Measurements
High and Low Temperatures Electrical Measurements shall be performed as specified in the Detail Specification. All values obtained shall be recorded against serial numbers.

8.14.4 Intermediate and End-Point Electrical Measurements
At each of the relevant data points during Qualification, Periodic Testing and Lot Validation Testing (Charts F4A and F4B), Intermediate and End-Point Electrical Measurements shall be performed as specified in the Detail Specification. All values obtained shall be recorded against serial numbers and the parameter drift calculated, if specified.

8.15 HIGH TEMPERATURE REVERSE BIAS BURN-IN
MIL-STD-883, Test Method 1015, Test Condition A.

- Duration and Test Conditions: As specified, where applicable, in High Temperature Reverse Bias Burn-in in the Detail Specification.
- Data Points:
  As specified in the Parameter Drift Values in the Detail Specification at 0 hour (initial) and T (+24 -0) hours (where T is the specified duration). Drift shall be related to the initial measurement.

8.16 POWER BURN-IN
MIL-STD-883, Test Method 1015, Test Condition B, D or E.

- Duration: Unless otherwise specified in the Detail Specification, components shall be subjected to a total Power Burn-in period of 240 (+24 -0) hours.
- Test Conditions: As specified in Power Burn-in in the Detail Specification.

  The alternative temperature and time combinations per MIL-STD-883 Test Method 1015 are permissible provided that the maximum operating ratings for a component are not exceeded.
- Data Points:
  As specified in Parameter Drift Values in the Detail Specification at T (+24 -0) hours (where T is the specified duration).

  If High Temperature Reverse Bias Burn-in is not being performed, the 0 hour (initial) measurement is also required. Drift shall be related to the initial measurement for Power Burn-in.

8.17 EXTERNAL VISUAL INSPECTION
External Visual Inspection shall be performed in accordance with MIL-STD-883, Test Method 2009 and JESD22-B101.

8.18 SOLDERABILITY
For procurement lots: 3 samples. A single failure shall be cause for lot failure.

MIL-STD-883, Test Method 2003 or JESD22-B102, to be performed on all terminals.

Solderability testing may be performed on electrical rejects. The test samples used must be of the same package type and must have been manufactured using the same process, at the same time and have been subjected to the same screening as the packages of the delivery lot with which they are associated.

For components with gold plated lead finish, activated fluxes (RMA, RA and OA) may be used but shall be immediately cleaned off after dipping, using an acceptable solvent.

Solderability testing is classed as destructive and therefore components so tested shall not form part of the delivery lot.

8.19 PRECONDITIONING

JESD22-A113. The applicable moisture sensitivity level, MSL, (in accordance with J-STD-020) shall be as specified in Maximum Ratings in the Detail Specification.

- Data Points:
  As specified in Intermediate and End-Point Electrical Measurements in the Detail Specification prior to and on completion of testing. If drift values are specified, the drift shall always be related to the 0 hour measurement.

8.20 UNBIASED TEMPERATURE-HUMIDITY TEST

One of the following tests shall be performed:

(a) JESD22-A118 (accelerated moisture resistance - unbiased HAST) with Test Conditions:
- Duration: 96 hours
- Temperature: +130°C
- Relative humidity: 85%
- Pressure: 230kPa

or

- Duration: 264 hours
- Temperature: +110°C
- Relative humidity: 85%
- Pressure: 122kPa

(b) JESD22-A102 (accelerated moisture resistance – unbiased autoclave) with Test Conditions:
- Duration: 96 hours
- Temperature: +121°C
- Relative humidity: 100%

(c) JESD22-A101 (steady-state temperature-humidity life test but with no bias applied) with Test Conditions:
- Duration: 1000 hours
- Temperature: +85°C
- Relative humidity: 85%

8.21 BIASED TEMPERATURE-HUMIDITY TEST

One of the following tests shall be performed:

(a) JESD22-A101 (steady-state temperature-humidity bias life test) with Test Conditions:
- Duration: 1000 hours
- Temperature: +85°C
- Relative humidity: 85%

(b) JESD22-A110 (Highly Accelerated Temperature and Humidity Stress Test (HAST)) with Test Conditions:
- Duration: 96 hours
- Temperature: +130°C
- Relative humidity: 85%

or

- Duration: 264 hours
- Temperature: +110°C
- Relative humidity: 85%

8.22 OPERATING LIFE

MIL-STD-883, Test Method 1005 or JESD22-A108.

- Duration: 2000 hours, unless otherwise specified in the Detail specification.
- Conditions: As specified in Operating Life in the Detail Specification.
- Data Points:
  As specified in Intermediate and End-Point Electrical Measurements in the Detail Specification at 0 hour, 1000 ±48 hours and 2000 ±48 hours. If drift values are specified, the drift shall always be related to the 0 hour measurement.

8.23 PERMANENCE OF MARKING

ESCC Basic Specification No. 24800.

8.24 MECHANICAL SHOCK

Cavity Packaged Components only.

Unless otherwise specified in the Detail Specification:

(a) For packages ≤ 1290mm^2: MIL-STD-883, Test Method 2002, Test Condition B.

(b) For packages > 1290mm^2: MIL-STD-883, Test Method 2002, Test Condition B, except the peak level shall be 1000g.

8.25 VIBRATION

Cavity Packaged Components only.

MIL-STD-883, Test Method 2007, Test Condition A.

9 DATA DOCUMENTATION

9.1 GENERAL

For the qualification, qualification maintenance and procurement for each lot a data documentation package shall exist in a printed or electronic form.

This package shall be compiled from:

(a) Cover sheet (or sheets).
(b) List of equipment (testing and measuring).
(c) List of test references.
(d) Wafer Lot Acceptance data (Chart F2).
(e) Special In-Process Controls data (Chart F2).
(f) Add-on Components procurement data (when applicable).
(g) Screening Tests data (Chart F3).
(h) Qualification, Periodic Testing and Lot Validation Testing (when applicable) data (Charts F4A or F4B).
(i) Failed components list and failure analysis report (when applicable).
(j) Certificate of Conformity.

Items (a) to (j) inclusive shall be grouped, preferably as subpackages and, for identification purposes, each page shall include the following information:

- ESCC Component Number.
- Manufacturer's name.
- Lot identification.
- Date of establishment of the document.
- Page number.

Whenever possible, documentation should preferably be available in electronic format suitable for reading using a compatible PC. The format supplied shall be legible, durable and indexed. The preferred storage medium is CD-ROM and the preferred file format is PDF.

9.1.1 Qualification and Qualification Maintenance

In the case of qualification or qualification maintenance, the items listed in Para. 9.1(a) to (j) are required.

9.1.2 Component Procurement and Delivery

For all deliveries of components procured to this specification, the following documentation shall be supplied:

(a) Cover sheet (if all of the information is not included on the Certificate of Conformity).
(b) Certificate of Conformity (including range of delivered serial numbers).

9.1.3 Additional Documentation

The Manufacturer shall deliver additional documentation containing data and reports to the Orderer, if stipulated in the Purchase Order.

9.1.4 Data Retention/Data Access

If not delivered, all data shall be retained by the Manufacturer for a minimum of 5 years during which time it shall be available for review, if requested, by the Orderer or the ESCC Executive (for qualified components).

9.2 COVER SHEET(S)

The cover sheet(s) of the data documentation package shall include as a minimum:

(a) Reference to the Detail Specification, including issue and date.
(b) Reference to the applicable ESCC Generic Specification, including issue and date.
(c) ESCC Component Number and the Manufacturer's part type number.
(d) Lot identification.
(e) Range of delivered serial numbers.
(f) Number of the Purchase Order.
(g) Total dose radiation test level (if applicable).
(h) Information relative to any additions to this specification and/or the Detail Specification.
(i) Manufacturer's name and address.
(j) Location of the manufacturing plant (specify place of diffusion, assembly and test).
(k) Signature on behalf of Manufacturer.
(l) Total number of pages of the data package.

9.3 LIST OF EQUIPMENT USED

A list of equipment used for tests and measurements shall be prepared. Where applicable, this list shall contain inventory number, Manufacturer's type number, serial number, etc. This list shall indicate for which tests such equipment was used.

9.4 LIST OF TEST REFERENCES

This list shall include all Manufacturer's references or codes which are necessary to correlate the test data provided with the applicable tests specified in the tables of the Detail Specification.

9.5 WAFER LOT ACCEPTANCE DATA (CHART F2)

For Die Visual Inspection, a test result summary shall be compiled giving the total number of dice submitted and the total number of dice rejected.

Data of SEM Inspection shall be prepared in accordance with the requirements of MIL-STD-883, Test Method 2018.

A total dose radiation test report shall be prepared in accordance with the requirements of ESCC Basic Specification No. 22900 (if specified).

9.6 SPECIAL IN-PROCESS CONTROLS DATA (CHART F2)

A test result summary shall be compiled showing the total number of components submitted to, and the total number rejected after each of the tests. Sampling details shall be provided. For all Die Shear Strength and Substrate Attach Strength tests, plus Bond Shear (Flip-Chip), Wire Bond Pull, Wire Bond Shear, Lid Attach Strength, Ball and Column Terminal Strength tests, the test results shall be recorded.

9.7 ADD-ON COMPONENTS PROCUREMENT DATA (PARA. 4.6)

A summary of the procurement details applicable to all Add-on Components for Flip-Chip Integrated Circuit components shall be complied including:

- Procurement specification(s) number and quality level
- Manufacturer's name and location
- Lot identification
- Certificate of Conformity
- Traceability information against Flip-Chip Integrated Circuit component serial number

9.8 SCREENING TESTS DATA (CHART F3)

A test result summary shall be compiled showing the total number of components submitted to and the total number rejected after each of the tests. For each test requiring electrical measurements, the results shall be recorded against component serial number. Component drift calculations shall be recorded for each specified test against component serial number. For Radiographic Inspection and Scanning Acoustic Microscopy, photographic results shall be recorded against component serial number.

9.9 QUALIFICATION, PERIODIC TESTING AND LOT VALIDATION TESTING DATA (CHARTS F4A AND F4B)

9.9.1 Qualification Testing

A test result summary shall be compiled showing the components submitted to, and the number rejected after each test in each subgroup. Component serial numbers for each subgroup shall be identified. For each test requiring electrical measurements, the results shall be recorded against component serial number. Where a drift value is specified during a test the drift calculation shall be recorded against component serial number.

9.9.2 Periodic Testing for Qualification Maintenance

A test result summary shall be compiled showing the components submitted to and the number rejected after each test in each subgroup. Component serial numbers for each subgroup shall be identified. For each test requiring electrical measurements, the results shall be recorded against component serial number. Where a drift value is specified during a test the drift calculation shall be recorded against component serial number.

In addition to the full test data, a report shall be compiled for each subgroup of Chart F4A or F4B, as applicable, to act as the most recent Periodic Testing summary. These reports shall include a list of all tests performed in each subgroup, the ESCC Component Numbers and quantities of components tested, a statement confirming all the results were satisfactory, the date the tests were performed and a reference to the full test data.

9.9.3 Lot Validation Testing

A test result summary shall be compiled showing the components submitted to and the number rejected after each test in each subgroup (as applicable). Component serial numbers for each subgroup shall be identified. For each test requiring electrical measurements, the results shall be recorded against component serial number. Where a drift value is specified during a test the drift calculation shall be recorded against component serial number.

9.10 FAILED COMPONENTS LIST AND FAILURE ANALYSIS REPORT

The failed components list and failure analysis report shall provide full details of:

(a) The reference and description of the test or measurement performed as defined in this specification and/or the Detail Specification during Wafer Lot Acceptance, Special In-Process Controls, Screening Tests, and Qualification, Periodic Testing and Lot Validation Testing.

(b) Traceability information including wafer lot and serial number (if applicable) of the failed component.

(c) The failed parameter and the failure mode of the component.

(d) Detailed failure analysis (if requested by the ESCC Executive or Orderer).

9.11 CERTIFICATE OF CONFORMITY

A Certificate of Conformity shall be established in accordance with the requirements of ESCC Basic Specification Nos. 20100 or 25400.

10 DELIVERY

For procurement, for each order, the items forming the delivery are:

(a) The delivery lot.

(b) The components used for Lot Validation Testing (as applicable), but not forming part of the delivery lot, if stipulated in the Purchase Order.

(c) The relevant documentation in accordance with the requirements of Paras. 9.1.2 and 9.1.3.

In the case of a component for which a valid qualification is in force, all data of all components submitted to Lot Validation Testing shall also be copied, when requested, to the ESCC Executive.

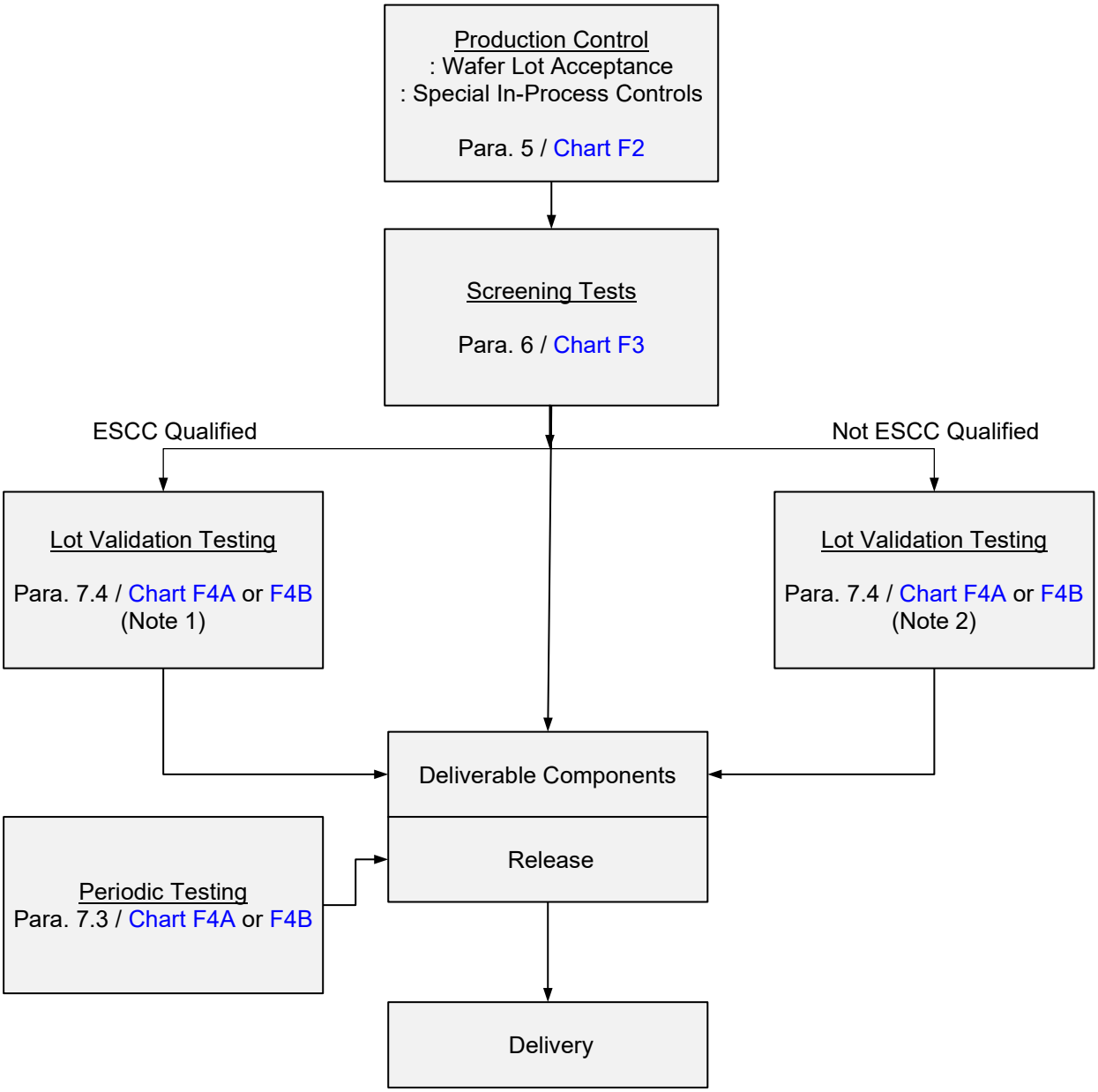
For qualification or qualification maintenance, the disposition of the Qualification Test Lot and its related documentation shall be as specified in ESCC Basic Specification Nos. 20100 or 25400 and the relevant paragraphs of Section 9 of this specification.

11 PACKAGING AND DISPATCH

The packaging and dispatch of components to this specification shall be in accordance with the requirements of ESCC Basic Specification No. 20600.

12 CHARTS

12.1 CHART F1 - GENERAL FLOW FOR PROCUREMENT



NOTES:

1. Lot Validation Testing is not required for qualified components unless specifically stipulated in the Purchase Order.
2. For unqualified components, the need for Lot Validation Testing shall be determined by the Orderer and the required testing shall be as stipulated in the Purchase Order (ref. ESCC Basic Specification No. 23100).

12.2 CHART F2 - PRODUCTION CONTROL

COMPONENT LOT MANUFACTURING

WAFER LOT ACCEPTANCE	
Para. 5.2.1	Process Monitoring Review
Para. 5.2.2	Die Visual Inspection (Wafer Lot Screening) (1)
-	Wafer Dicing
Para. 5.2.3	SEM Inspection (2)
Para. 5.2.4	Total Dose Radiation Testing (2) (3)

SPECIAL IN-PROCESS CONTROLS (4) (5)			
WIRE-BONDED INTEGRATED CIRCUIT COMPONENTS		FLIP-CHIP INTEGRATED CIRCUIT COMPONENTS	
-	Die Attach	Para. 5.3.3(b)	Package/Substrate Visual Inspection (6)
Para. 5.3.1	Die Shear Strength or Substrate Attach Strength (6)	-	Die Attach
-	Wire Bonding	Para. 5.3.7	Bond Shear (Flip-Chip) (8)
Para. 5.3.2	Wire Bond Pull and Wire Bond Shear (6)	-	Underfill
Para. 5.3.3(a)	Internal Visual Inspection (6)	Para. 5.3.4	SAM
-	Encapsulation / Moulding / Lid Attach / Heat-Spreader Placement (7)	Para. 5.3.3(a)	Internal Visual Inspection (6)
Para. 5.3.4	SAM	-	Add-on Components Attach (7)
Para. 5.3.5	Lid Attach Strength (7)	Para. 5.3.8	Add-on Components Die Shear Strength or Substrate Attach Strength (7)
-	Ball or Column Attach (7)	Para. 5.3.3(c)	Visual Inspection of Add-on Components (6) (7)
Para. 5.3.6	Ball or Column Terminal Strength (7)	-	Encapsulation / Moulding / Lid Attach / Heat-Spreader Placement (7)
		Para. 5.3.4	SAM
		Para. 5.3.5	Lid Attach Strength (7)
		-	Ball or Column Attach (7)
		Para. 5.3.6	Ball or Column Terminal Strength (7)

Para. 5.3.9	Dimension Check (2)
Para. 5.3.10	Weight (9)

TO CHART F3 – SCREENING TESTS

NOTES:

1. May be performed either on-wafer or after dice separation.
2. Performed on a sample basis.
3. Only required if specified in the Detail Specification and stipulated in the Purchase Order.
4. Special In-Process Controls shall be performed on a sample basis which shall be agreed with the ESCC Executive.
5. Unless otherwise specified, the sequence of Special In-Process Controls is at the discretion of the Manufacturer subject to the approval of the ESCC Executive.

6. This test/inspection may be performed subsequent to encapsulation / moulding / lid attach / heat-spreader placement.
7. As applicable (see the Detail Specification for details).
8. Bond Shear (Flip-Chip) shall be performed prior to Underfill.
9. Guaranteed but not tested.

12.3 CHART F3 - SCREENING TESTS

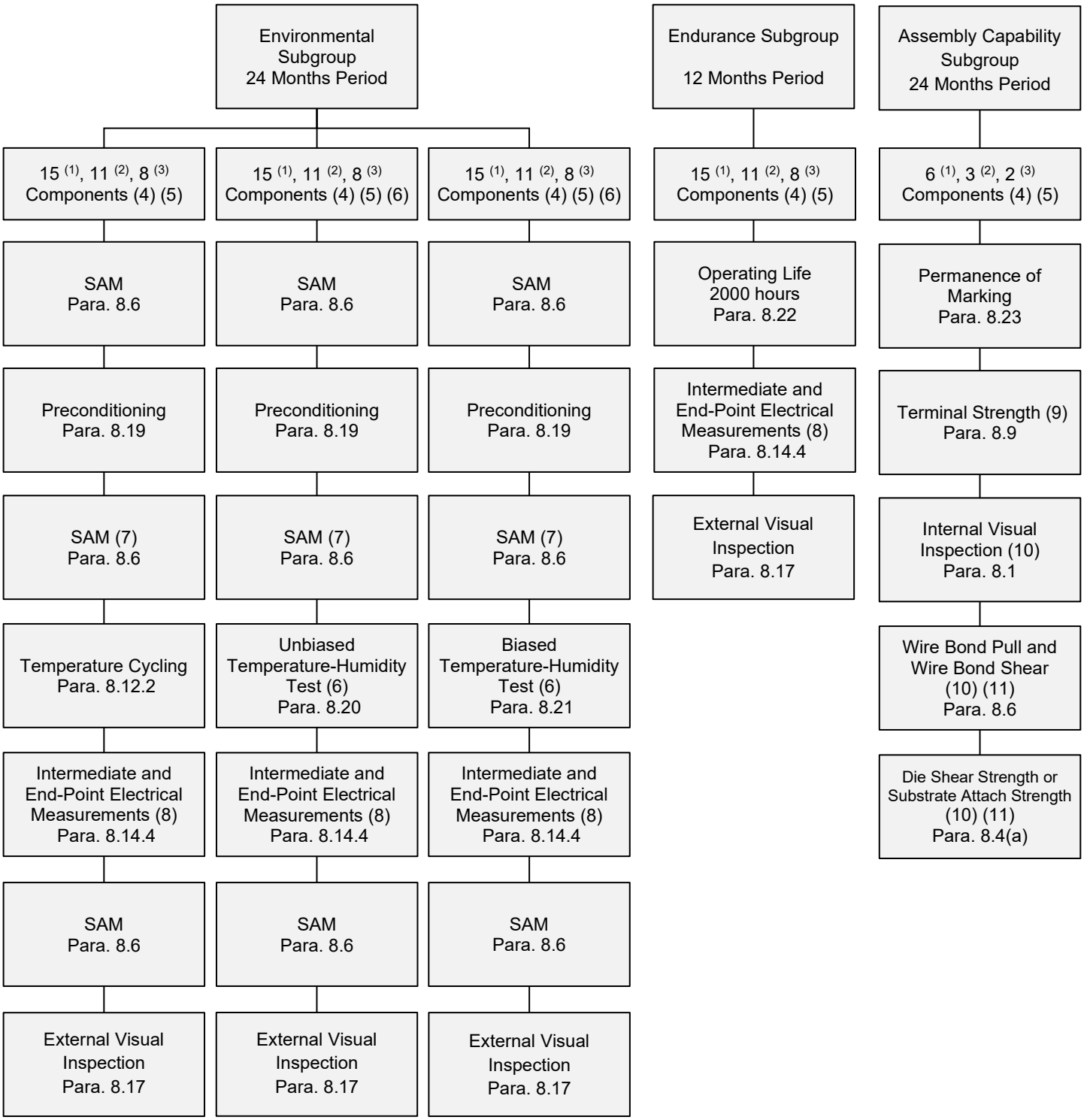
COMPONENTS FROM PRODUCTION CONTROL	
Para. 6.1	Serialisation
Para. 8.10	Radiographic Inspection
Para. 8.11.1	Constant Acceleration (1)
Para. 8.12.1	Temperature Cycling
Para. 8.6	SAM (2)
Para. 8.13	Bake
Para. 8.14.1	Parameter Drift Values (Initial Measurements)
Para. 8.15	High Temperature Reverse Bias Burn-in
Para. 8.14.1	Parameter Drift Values (Final Measurements for HTRB Burn-in; Initial Measurements for Power Burn-in) (3)
Para. 8.16	Power Burn-in
Para. 8.14.1	Parameter Drift Values (Final Measurements) (3)
Para. 8.14.2	Room Temperature Electrical Measurements (3) (4)
Para. 8.14.3	High and Low Temperatures Electrical Measurements (3)
Para. 6.4	Check for Lot Failure (5)
Para. 8.17	External Visual Inspection
Para. 8.18	Solderability (2) (3)
TO CHART F4A OR F4B WHEN/AS APPLICABLE	

NOTES:

1. Only applicable to Cavity Packaged Components (see the Detail Specification for details).
2. Performed on a sample basis.
3. The lot failure criteria of Para. 6.4 apply to this test.
4. Measurements of Parameter Drift Values need not be repeated in Room Temperature Electrical Measurements.
5. Check for Lot Failure shall take into account all electrical parameter failures that may occur during Screening Tests in accordance with Paras. 8.14.1, 8.14.2, 8.14.3 subsequent to HTRB Burn-in.

12.4 CHART F4 - QUALIFICATION, PERIODIC TESTING AND LOT VALIDATION TESTING

12.4.1 Chart F4A – Qualification, Periodic Testing and Lot Validation Testing for Wire-Bonded Integrated Circuit Components

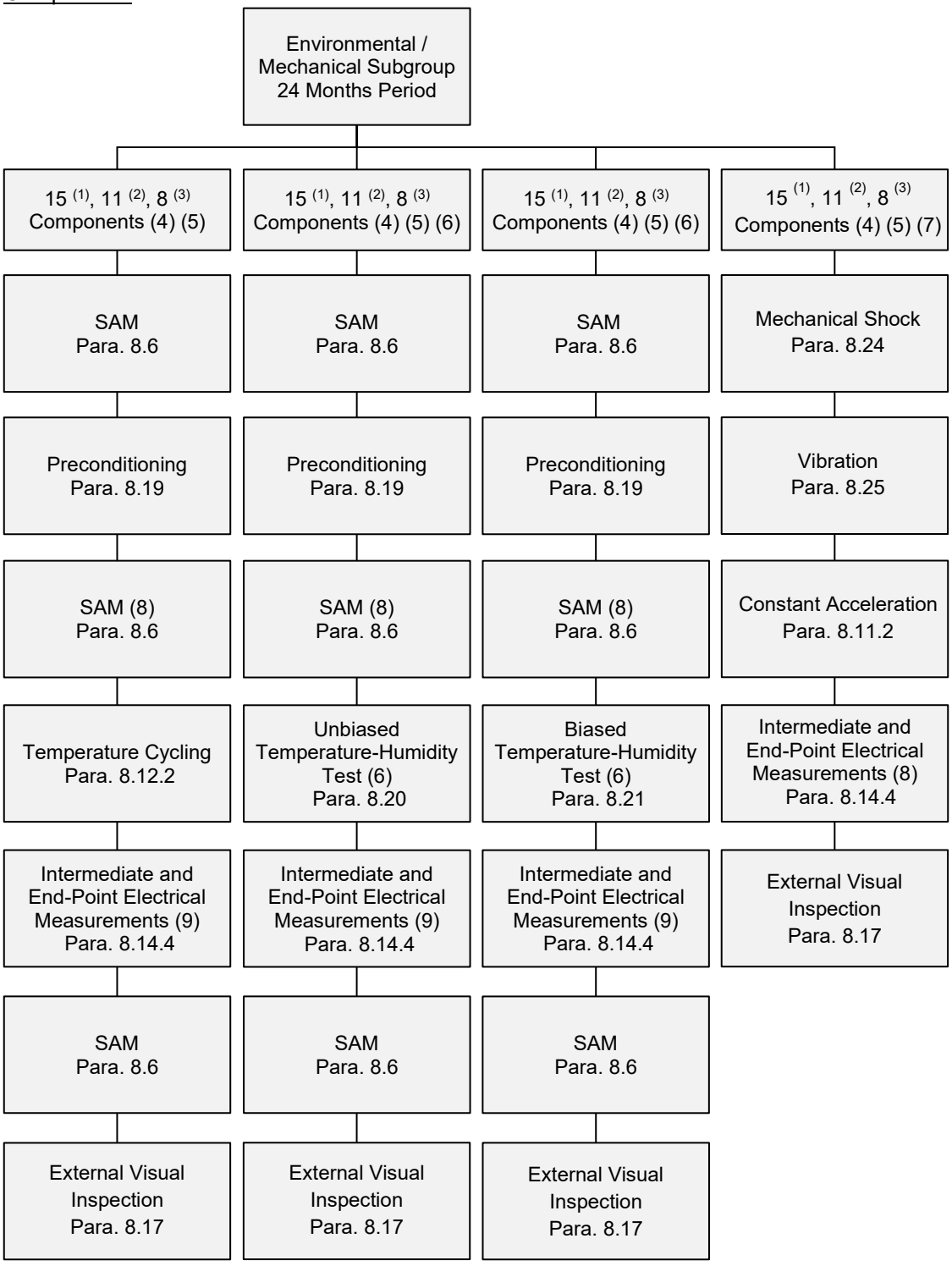


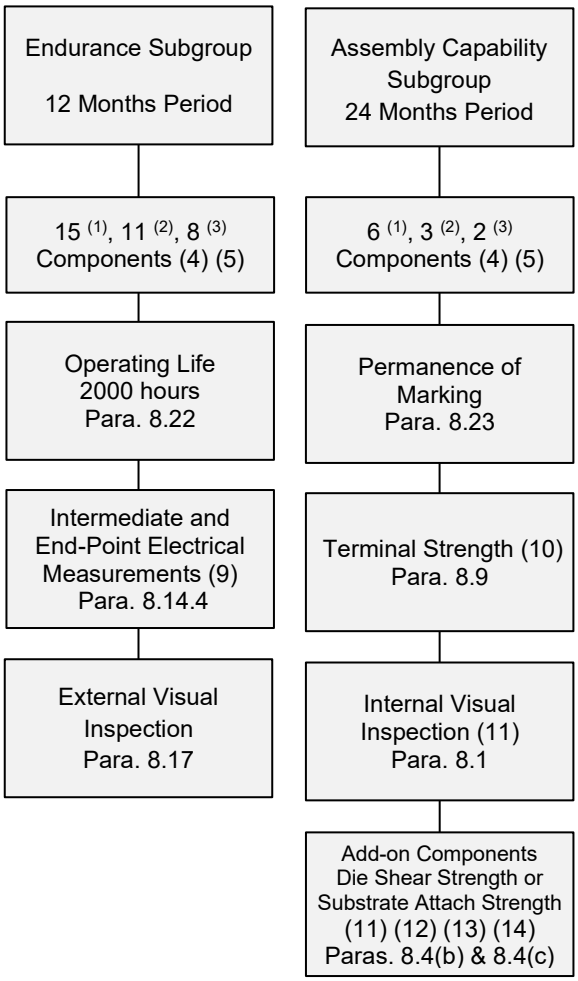
NOTES:

1. The quantity for qualification and qualification maintenance of a single type (see Para. 7.1.2.1).
2. The quantity per type for qualification and qualification maintenance of two types selected (see Para. 7.1.2.2).

3. The quantity per type for qualification and qualification maintenance of three or more types selected (see Para. 7.1.2.2).
4. For distribution within the subgroups, see Para. 7.1.2 for qualification and qualification maintenance, and Para. 7.4 for Lot Validation Testing.
5. No failures are permitted.
6. The Manufacturer shall perform either one or both test sequence(s) containing the Unbiased Temperature-Humidity Test and the Biased Temperature-Humidity Test, depending on their relevance to the component(s) under test (see the Detail Specification for details).
7. Test is optional at the Manufacturer's discretion.
8. Unless otherwise specified in the Detail Specification, electrical measurements shall be performed at room, high and low temperatures.
9. May be performed at any point during the subgroup, depending on package configuration.
10. The components shall be de-encapsulated in accordance with ESCC Basic Specification No. 25300, or equivalent, to facilitate Internal Visual Inspection, Wire Bond Pull and Wire Bond Shear, and either Die Shear Strength or Substrate Attach Strength. Any observed defect determined to have resulted from the de-encapsulation process may be ignored subject to the approval of the ESCC Executive.
11. Wire Bond Pull and Wire Bond Shear, and Die Shear Strength or Substrate Attach Strength may be replaced by a technical justification supported by Special In-Process Controls data or other verification processes which demonstrate the requirements, subject to the approval of the ESCC Executive.

12.4.2 Chart F4B – Qualification, Periodic Testing and Lot Validation Testing for Flip-Chip Integrated Circuit Components





NOTES:

1. The quantity for qualification and qualification maintenance of a single type (see Para. 7.1.2.1).
2. The quantity per type for qualification and qualification maintenance of two types selected (see Para. 7.1.2.2).
3. The quantity per type for qualification and qualification maintenance of three or more types selected (see Para. 7.1.2.2).
4. For distribution within the subgroups, see Para. 7.1.2 for qualification and qualification maintenance, and Para. 7.4 for Lot Validation Testing.
5. No failures are permitted.
6. The Manufacturer shall perform either one or both test sequence(s) containing the Unbiased Temperature-Humidity Test and the Biased Temperature-Humidity Test, depending on their relevance to the component(s) under test (see the Detail Specification for details).
7. Mechanical Subgroup tests shall only be performed for Cavity Packaged Components (see the Detail Specification for details).
8. Test is optional at the Manufacturer's discretion.
9. Unless otherwise specified in the Detail Specification, electrical measurements shall be performed at room, high and low temperatures.
10. May be performed at any point during the subgroup, depending on package configuration.
11. The components shall be de-encapsulated in accordance with ESCC Basic Specification No. 25300, or equivalent, to facilitate Internal Visual Inspection, and Add-on Components Die Shear Strength or Substrate Attach Strength. Any observed defect determined to have resulted from the de-encapsulation process may be ignored subject to the approval of the ESCC Executive.

12. Only 1 sample shall be tested.
13. Add-on Components Die Shear Strength or Substrate Attach Strength may be replaced by a technical justification supported by Special In-Process Controls data or other verification processes which demonstrate the requirements, subject to the approval of the ESCC Executive.
14. As applicable (see the Detail Specification for details).