EVALUATION TEST PROGRAMME FOR INTEGRATED CIRCUITS:

MONOLITHIC MICROCIRCUITS, WIRE-BONDED, PLASTIC ENCAPSULATED AND FLIP-CHIP MONOLITHIC MICROCIRCUITS, WITH ORGANIC SUBSTRATE

ESCC Basic Specification No. 2269030

Issue 1	March 2023

Document Custodian: European Space Agency – see https://escies.org

LEGAL DISCLAIMER AND COPYRIGHT

DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION

TABLE OF CONTENTS

1 PURPOSE

The purpose of this specification is to establish the procedure to be followed in the evaluation of component capabilities as required for space applications and thereby to anticipate, as far as possible, component behaviour during qualification testing. Therefore, the aim of such testing shall be to overstress specific characteristics of the component concerned with a view to the detection of possible failure modes. Additionally, a detailed destructive physical analysis shall be performed to detect any design and construction defects which may affect the reliability of the component and to facilitate failure analysis activities. The evaluation shall also include a check of the susceptibility of the component to ESD damage.

2 APPLICABLE DOCUMENTS

The following documents form part of, and shall be read in conjunction with, this specification. The relevant issues shall be those in effect at the date of commencement of the evaluation.

2.1 ESCC SPECIFICATIONS

- No. 9030, Integrated Circuits: Monolithic Microcircuits, Wire-Bonded, Plastic Encapsulated and Flip-Chip Monolithic Microcircuits, with Organic Substrate.
- No. 20100, Requirements for the Qualification of Standard Electronic Components for Space Application.
- No. 21001, Destructive Physical Analysis of EEE Components
- No. 21300, Terms, Definitions, Abbreviations, Symbols and Units.
- No. 22500, Guidelines for Displacement Damage Irradiation Testing.
- No. 22600, Requirements for the Evaluation of Standard Electronic Components for Space Application.
- No. 22900, Total Dose Steady-State Irradiation Test Method.
- No. 23800, Electrostatic Discharge Sensitivity Test Method.
- No. 24800, Resistance to Solvents of Marking, Materials and Finishes.
- No. 25100, Single Event Effects Test Method and Guidelines
- No. 25200, Application of Scanning Acoustic Microscopy to Plastic Encapsulated Devices.
- No. 25300, Decapsulation of Plastic Encapsulated Semiconductor Devices.

NOTE:
Unless otherwise stated herein, reference within the text of this specification to "the Detail Specification" shall mean the relevant ESCC Detail Specification.

2.2 OTHER (REFERENCE) DOCUMENTS

- ECSS-Q-ST-60, Electrical, Electronic and Electromechanical (EEE) Components.
- ECSS-Q-ST-70-02, Thermal Vacuum Test for the Screening of Space Materials.
- MIL-STD-883, Test Methods and Procedures for Microelectronics.
- ASTM E595-15, Standard Test Method for Total Mass Loss and Collected Volatile Condensable Materials from Outgassing in a Vacuum Environment.
- J-STD-020, IPC/JEDEC Standard for Moisture/Reflow Sensitivity Classification for Non-Hermetic Surface-Mount Devices.
- J-STD-033, IPC/JEDEC Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.

- JESD22-A101, EIA/JEDEC Standard Test Method: Steady-State Temperature-Humidity Bias Life Test.
- JESD22-A102, EIA/JEDEC Standard Test Method: Accelerated Moisture Resistance - Unbiased Autoclave.
- JESD22-A103, EIA/JEDEC Standard Test Method: High Temperature Storage Life.
- JESD22-A108, EIA/JEDEC Standard Test Method: Temperature, Bias, And Operating Life.
- JESD22-A110, EIA/JEDEC Standard Test Method: Highly Accelerated Temperature and Humidity Stress Test (HAST).
- JESD22-A113, EIA/JEDEC Standard Test Method: Preconditioning of Non-Hermetic Surface Mount Devices Prior to Reliability Testing.
- JESD22-A118, EIA/JEDEC Standard Test Method: Accelerated Moisture Resistance - Unbiased Hast.
- JESD22-B102, EIA/JEDEC Standard Test Method: Solderability.
- JESD22-B116, EIA/JEDEC Standard Test Method: Wire Bond Shear Test.
- JESD22-B117, EIA/JEDEC Standard Test Method: Solder Ball Shear.

3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

The terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply. In addition, the following shall apply:

Integrated Circuit (Microcircuit):	A small circuit having a high equivalent circuit element density, which is considered as a single part composed of interconnected elements on or within a single substrate to perform an electronic circuit function. Monolithic microcircuits are considered as Integrated Circuits.
Monolithic Microcircuit:	A microcircuit consisting exclusively of elements formed in situ on or within a single semiconductor substrate with at least one of the elements formed within the substrate (with a single semiconductor die).
Wire-Bonded Integrated Circuit:	A monolithic microcircuit with the die backside bonded to the package cavity or organic substrate, and wire-bonded to either a metal lead-frame or an organic substrate with solder balls or columns.
Flip-Chip Integrated Circuit:	A monolithic microcircuit with bumps attached to the active side of the die, connected top side down to an organic substrate, with underfill, and solder balls or columns.
Add-on Components:	Capacitors and/or resistors mounted in and electrically connected to a Flip-Chip Integrated Circuit assembly. Other component types are not permitted.
Plastic Encapsulation	Encapsulation by means of being moulded within moulding compound.
Cavity Packaged Component	A Flip-Chip Integrated Circuit that has some internal electrical connections not fully embedded in moulding compound.

4 PROCEDURE

Standard components shall be selected from a homogeneous lot at the Manufacturer to be evaluated. These components shall not have been submitted to any screening or burn-in, but must have been manufactured in conformity with high reliability practice and an established Process Identification Document (PID) or an identifiable process which shall form the basis for the PID.

The tests specified in the programme shall be performed in the sequence shown in Chart I. All results shall be recorded and failed components submitted to a failure analysis. Probable failure modes and mechanisms shall be determined.

The evaluation test programme shall be performed, under the supervision of the ESCC Executive, by the Manufacturer or at a test laboratory approved by the ESCC Executive.

4.1 AGREED DEVIATIONS TO CHART I TEST REQUIREMENTS

Deviations to the test requirements of Chart I may be approved subject to full justification being provided by the Manufacturer to the ESCC Executive. Approved deviations shall be fully documented and all details shall be included in the Evaluation Test Programme.

4.2 MANDATORY PREREQUISITES FOR FLIP-CHIP INTEGRATED CIRCUIT COMPONENTS

Prior to the start of an evaluation implementing the requirements of this evaluation test programme, and in order to adequately comply with the requirements of ESCC Basic Specification Nos. 20100 and 22600, the Manufacturer shall have completed a development and process qualification plan specifically including assessments of, and creating specifications for, the following:

- Solder bump dimension and co-planarity.
- Electromigration at solder bump level.
- Alloy composition in compliance with ECSS-Q-ST-60.
- Ionic contamination resulting from the use of flux, and within the underfill.
- Electrical characterisation over the temperature range pre- and post- ball/column attachment.
- Level 2 interconnect (e.g., balls, columns) attachment to package, representative of manufacturing and screening effects.
- Organic substrate reliability evaluation
- Underfill and thermal interface material evaluation
- Adequacy of substrate finishing
- Package mounting on PCB.

Such assessments may be performed on representative test structures but, in any case, shall be fully documented and must be repeated in the event of material, process and supply chain changes.

The Manufacturer shall have systematic control over all materials used in the construction of the Flip-Chip Integrated Circuit components, particularly for underfill and thermal interface material. This shall be documented in the PID.

5 TEST PROGRAMME SEQUENCE AND SAMPLE DISTRIBUTION

5.1 SELECTION OF COMPONENTS FOR EVALUATION TESTING

The number of components to be selected for evaluation testing shall depend on whether a single component type or a family of parts is evaluated and the number of component types chosen to represent the family.

Up to 148 samples plus additional components/structures/materials, as/if required, (see Chart I) shall be used for each test programme.

The component types chosen to represent a family shall cover the range of components to be evaluated and be representative of the different package and pin configurations under consideration. They shall also be the most suitable for highlighting those characteristics and parameters that are pertinent to an investigation into failure modes and weaknesses.

The samples shall be as specified by, or as agreed with, the ESCC Executive.

The above-mentioned quantity shall be submitted to the full evaluation procedure whenever a new technology has been applied to the components concerned, where there is insufficient experience in their production.

5.2 DETAIL SPECIFICATIONS

Should a Detail Specification for the component(s) to be evaluated not exist, the Manufacturer shall prepare such a document(s) in accordance with the established ESCC format and submit it to the ESCC Executive for provisional approval. This shall then serve as a basis for the ordering and testing of the relevant components.

5.3 INSPECTION RIGHTS

The ESCC Executive reserves the right to inspect at any time the components processed for evaluation purposes. The Manufacturer shall notify the ESCC Executive at least three working days in advance of the date of internal visual inspection (but see Para. 5.4).

5.4 CONTROL DURING FABRICATION

The components shall be produced as defined in Para. 4 of this specification. Internal visual inspections shall be performed on the lot to be tested to the extent that this forms part of the Manufacturer's standard procedures. Progress of the components shall be observed closely and recorded together with an analysis of any reject. A chart showing the numbers in/out and failure cause for each fabrication stage shall be submitted to the ESCC Executive.

6 INSPECTION

6.1 GENERAL

The components shall be checked to verify their suitability for the Evaluation Test Programme. Defects or deviations from the established ESCC requirements may invalidate the evaluation. For each measurement or inspection performed, the results shall be summarised in terms of quantity tested, quantity passed and quantity rejected. If components are rejected, the reason shall be clearly identified.

6.2 DIMENSIONS (100%)

All components shall be inspected (go-no-go) in accordance with Physical Dimensions and Terminal Identification in the Detail Specification. Where gauges exist for performance of measurements, these may be used. For packages with a high pin count, the measurements may be performed using a sampling scheme which shall be approved by the ESCC Executive. Rejected components shall be replaced.

6.3 WEIGHT (100%)

All components shall be weighed (go-no-go). Any components that exceed the weight defined in the Detail Specification shall be rejected and replaced.

6.4 ELECTRICAL MEASUREMENTS (100%)

These measurements shall be performed (go-no-go) in accordance with Room Temperature Electrical Measurements in the Detail Specification at an ambient temperature of +22 ±3°C. Rejected components shall be replaced.

6.5 EXTERNAL VISUAL INSPECTION (100%)

All components shall be inspected in accordance with MIL-STD-883, Test Method 2009 and JESD22-B101. Rejected components shall be replaced.

6.6 SCANNING ACOUSTIC MICROSCOPY (SAM) (100%)

All components shall be tested in accordance with ESCC Basic Specification No. 25200, plus additional SAM requirements as specified in the Detail Specification, including specific inspection requirements applicable to all thermal interface materials. Rejected components shall be replaced.

NOTE:

Components submitted to SAM shall be subjected to a final drying phase consisting of a minimum bake of duration 1 hour at T_{amb} = +125°C. J-STD-033 may be used as a guideline for the appropriate drying conditions.

The following additional reject criteria shall also apply:

(a) For Wire-Bonded Integrated Circuits with a metal lead-frame:

1. No delamination on the active side of the die
2. No delamination on any wire bonding surface including the down-bond area or the lead-frame of lead-on-chip (LOC) components.
3. No surface-breaking feature delaminated over its entire length. A surface-breaking feature includes lead fingers, tie bars, heat-spreader alignment features, heat slugs, etc..
4. No delamination/cracking > 50% of the die attach area:
   i. in components with exposed die pad used for thermal conductivity
   ii. for components that require electrical contact to the backside of the die
5. Delamination of more than half of the backside of the die paddle/plastic interface.
6. Any void in moulding compound crossing wire-bond.

(b) For Wire-Bonded Integrated Circuits with an organic substrate:

1. No delamination on the active side of the die
2. No delamination on any wire bonding surface including the down-bond area or the lead-frame of lead-on-chip (LOC) components.
3. No delamination on any electrical contact surface of the laminate.
4. No delamination within the substrate.
5. No delamination/cracking > 50% of the die attach area:
   i. in components with exposed die pad used for thermal conductivity
   ii. for components that require electrical contact to the backside of the die
6. No surface-breaking feature delaminated over its entire length. A surface-breaking feature includes lead fingers, tie bars, heat-spreader alignment features, heat slugs, etc..
7. Any void in moulding compound crossing wire-bond.

(c) For Flip-Chip Integrated Circuits:

1. No delamination on the active side of the die
2. No delamination on any electrical contact surface of the laminate.
3. No surface-breaking feature delaminated over its entire length. A surface-breaking feature includes lead fingers, laminate, laminate metallization, PTH, heat slugs, etc.
4. No delamination/cracking between underfill resin and chip, or underfill resin and substrate/solder mask.
5. No delamination within the substrate.

6.7 RADIOGRAPHIC INSPECTION (100%)

All components shall be inspected in accordance with MIL-STD-883, Test Method 2012. Additional axes may be radiographed if, by so doing, it is possible to observe any faults. Rejected components shall be replaced.

6.8 MARKING AND SERIALISATION (100%)

All components shall be marked and serialised in accordance with the standard procedures of the Manufacturer concerned.

6.9 MATERIALS AND FINISHES

All non-metallic materials and finishes of the components specified herein shall be tested in accordance with ECSS-Q-ST-70-02 or ASTM E595-15 to verify their outgassing requirements, unless relevant data is available. See also Para. 8.3.4.1 herein.

6.10 COMPLETION OF INSPECTION

The completion of inspection shall result in a batch of components that have been verified as to their suitability for the Evaluation Test Programme, i.e., each component has satisfied the requirements of Paras. 6.2 to 6.9 inclusive.

7 INITIAL ELECTRICAL MEASUREMENTS (100% READ AND RECORD)

These measurements shall be performed in accordance with Room, High and Low Temperatures Electrical Measurements in the Detail Specification. All characteristics shall be recorded against serial numbers. Rejected components shall be replaced.

8 EVALUATION TEST PROGRAMME

8.1 GENERAL

The evaluation tests shall be performed as specified in Chart I. The components shall be randomly divided into groups and their associated subgroups in the quantities indicated in Chart I. When a family of components is under investigation, the variations within that family must be represented in each group/subgroup which might require samples in addition to the quantities specified in Chart I (see Para. 5.1).

The Subgroup 2A tests shall be completed and the results analysed before the Subgroup 3B tests are commenced.

All failed components shall be analysed. The depth of analysis shall depend upon the circumstances in which failure occurred and upon whether useful information may be gained. As a minimum, the failure mode shall be determined in each case. Components not failing catastrophically, i.e., those displaying out-of-tolerance electrical parameters, shall not be removed from the test sequence but monitored to observe degradation trends.

8.2 GROUP 1 - CONTROL GROUP

This group shall be retained for comparison purposes. Whenever electrical measurements are made on any components under test, these components shall also be measured.

8.3 GROUP 2 - DESTRUCTIVE TESTS

8.3.1 General

This group shall be randomly divided into subgroups in the quantities indicated in Chart I.

Testing of Integrated Circuit components with ball or column terminals (i.e., CGA or BGA) may be performed on parts without balls/columns unless otherwise specified.

The use of representative test structures (including empty packages) is subject to approval by the ESCC Executive and to be specified in advance in the applicable test plan.

8.3.1.1 Preconditioning / SAM

Components to be subjected to Subgroups 2A, 2C and 2D tests only shall first be subjected to the following:

(a) Preconditioning:
All components shall be subjected to preconditioning in accordance with JESD22-A113.
Prior to performing preconditioning, the moisture sensitivity level (MSL) of each component type being evaluated shall have been determined in accordance with J-STD-020 and approved by the ESCC Executive.

(b) Scanning Acoustic Microscopy (SAM): per Para. 6.6.

8.3.2 Subgroup 2A - Step-Stress Tests

8.3.2.1 General

This subgroup shall be randomly divided into further subgroups in the quantities indicated in Chart I.

For both the Temperature and Power Step-Stress Tests, the step-stress sequence shall be terminated when 50% (rounded up) of the specimens have been destroyed, unless practical reasons prevent this.

8.3.2.2 Subgroup 2A(i) - Determination of Thermal Resistance/Conductivity
MIL-STD-883, Method 1012.

8.3.2.3 Parameters to be measured during Step-Stress Tests
During step-stress tests, electrical measurements shall be made in accordance with Parameter Drift Values in the Detail Specification. If parameter drift values are not specified in the Detail Specification, then the parameters to be measured shall be selected from Room Temperature Electrical Measurements in the Detail Specification. In the case of doubt as to the applicability of any given parameter, the parameter shall be measured. Quiescent current (if applicable) shall be measured in all cases. At the termination of the step-stress sequences, any surviving components shall have their thermal resistance/conductivity measured as specified in Para. 8.3.2.2.

8.3.2.4 Subgroup 2A(ii) - Temperature Step-Stress Test
The tests in this subgroup shall be performed as specified in Chart II. Electrical measurements shall be made as defined in Para. 8.3.2.3 above. The starting temperature (which will be no higher than the maximum operating temperature as defined in the Detail Specification) and the temperature steps (with a maximum step of 25°C) to be employed will be decided by the ESCC Executive.

8.3.2.5 Subgroup 2A(iii) - Power Step-Stress Test
(a) Applicability
This test is only applicable to components where operation in circuits requiring transfer and dissipation of significant and/or varying levels of power is an intended feature of their design. The ESCC Executive shall review the component type and technology to determine the applicability of the test.

(b) Procedure
The tests in this subgroup shall be performed as specified in Chart III. Electrical measurements shall be made as defined in Para. 8.3.2.3 above. The starting power (which will be no higher than the maximum input power as defined in the Detail Specification) and the power steps (with a maximum step of 20%) to be employed will be decided by the ESCC Executive.

On completion of testing, Scanning Acoustic Microscopy (SAM) in accordance with Para. 6.6 shall be performed

8.3.2.6 Subgroup 2A(iv) – Intermittent Operating Life Test
(a) Applicability
This test is only applicable to components where operation in circuits requiring transfer and dissipation of significant and/or varying levels of power is an intended feature of their design. The ESCC Executive shall review the component type and technology to determine the applicability of the test.

(b) Procedure
The Components shall be subject to an Intermittent Operating Life test until failure or up to 6000 on/off cycles, whichever occurs first, at T_{amb} = +125°C per MIL-STD-883, Test Method 1006. The frequency and duration of the on and off cycles shall be as agreed with the ESCC Executive. The applied operating conditions during the on cycles shall use the maximum specified power and shall be subject to approval by the ESCC Executive.

Electrical measurements shall be performed in accordance with Para. 8.3.2.3 above before and after the test.

8.3.2.7 Analysis of Subgroups 2A(ii) and 2(iii)
The analysis of Subgroups 2A(ii) and 2A(iii) shall be presented to the ESCC Executive in a graphical form, supported by the actual results, as follows:

- The number of functional failures shall be plotted against each temperature or power level (as/if applicable) applied. The cumulative failure rate shall also be plotted.
- The parameters (as defined in Para. 8.3.2.3 above) shall be monitored, recorded and plotted against time for each temperature or power level (as/if applicable) as appropriate.
- The average drift of the parameters at each temperature or power level applied shall be plotted against temperature or power (as/if applicable) as appropriate.

The analysis of the results of Subgroup 2A(ii) and 2A(iii) (as/if applicable)) shall be used to determine the most effective temperatures and power (as/if applicable) for the accelerated electrical endurance test (Subgroup 3B).

8.3.3 Subgroup 2B - Radiation Test

8.3.3.1 Total Dose Steady-State Radiation Test (on 10 samples)
In accordance with ESCC Basic Specification No. 22900.

8.3.3.2 Single Event Effects Test (SEE) (on 2 samples minimum)
In accordance with ESCC Basic Specification No. 25100, if applicable.

8.3.3.3 Displacement Damage (on 6 samples minimum)
In accordance with ESCC Basic Specification No. 22500, if applicable.

8.3.4 Subgroup 2C - Construction Analysis
PRECAUTIONS: If it is known, or believed, that beryllium oxide or other toxic substances are used in the construction of the component, precautionary measures shall be employed.

8.3.4.1 Outgassing
ECSS-Q-ST-70-02 or ASTM E595-15 (performed on suitable raw material samples of all those used in the component).

8.3.4.2 De-encapsulation
The components shall be de-encapsulated to expose the internal structure of the component using a technique which does not impair the ability to observe defects. ESCC Basic Specification No. 25300 may be used as a guideline.

8.3.4.3 Internal Visual Inspection
Each component shall be visually inspected in accordance with MIL-STD-883, Test Method 2010 Condition A (Class level S), MIL-STD-883, Test Method 2013 and 2014, MIL-STD-883, Test Method 2032 Class H, and MIL-STD-883, Test Method 2017 Class H (as applicable). Photographs shall be taken as follows:

(a) An overall photograph of the opened component.
(b) An overall photograph of the die plus any Add-on Components.
(c) Photographs of any anomalies found.

8.3.4.4 Scanning Electron Microscope (SEM) Inspection

SEM shall be performed in accordance with MIL-STD-883, Method 2018

This inspection shall include, but shall not necessarily be limited to, examination of the following:

(a) Detailed examination of any anomalies identified by the internal visual inspection (as defined in Para. 8.3.4.3 above).

Photographs shall be taken of the above.

(b) Low magnification (up to 500x) shall be used to assess:
(i) Clearance of bond wires at the die edge (as applicable).
(ii) Quality of bonding at the die.
(iii) Quality of bonding at the post (as applicable).

Photographs shall be taken of the above.

(c) High magnification (1000x or greater) shall be used to assess:
(i) Metallisation coverage and consistency at steps.
(ii) Metallisation coverage at contact windows, bonding pads, etc.

Photographs shall be taken of the above.

In the case of components with a glassivated surface, this examination shall first be attempted through the glassivation.

If the resolution is inadequate, the glassivation shall be removed. This step must be postponed until the bond strength (Para. 8.3.4.5) test has been performed.

For components with multi-level metallisation, the upper layer(s) shall be removed to permit assessment of the above-mentioned features. This step shall also be postponed until the Wire Bond Pull and Wire Bond Shear tests (as defined in Para. 8.3.4.5) have been performed.

For deep sub-micron components, SEM inspection of the die may be impracticable; in which case the Manufacturer shall fully justify any deviations in accordance with Para. 4.1.

8.3.4.5 Wire Bond Pull and Wire Bond Shear

Not applicable to Flip-Chip Integrated Circuit components.

Both Wire Bond Pull and Wire Bond Shear shall be performed as follows:

(a) Wire Bond Pull: MIL-STD-883, Test Method 2011, Test Conditions: Test condition C or D.
(b) Wire Bond Shear: JESD22-B116.

8.3.4.6 Die Shear Strength, Substrate Attach Strength, or Bond Shear (Flip-chip)

(a) For Wire-Bonded Integrated Circuit components:
Either Die Shear Strength or Substrate Attach Strength, as applicable, shall be performed as follows:
- MIL-STD-883, Test Method 2019 or 2027.

Individual separation forces and categories shall be recorded.

(b) For Flip-Chip Integrated Circuit components:
Bond Shear (Flip-Chip) shall be performed as follows:
- MIL-STD-883, Test Method 2011 Test Condition F.

Individual separation forces and categories shall be recorded.

(c) For Add-on Components mounted in Flip-Chip Integrated Circuit components:
Either Die Shear Strength or Substrate Attach Strength, as applicable, shall be performed on mounted Add-on Components (as applicable) as follows:
- MIL-STD-883, Test Method 2019 or 2027.

Individual separation forces and categories shall be recorded.

8.3.4.7 Microsectioning

(a) Glassivation Layer Integrity (if applicable): MIL-STD-883, Method 2021.

(b) Mounting
The component(s) shall be mounted on a carrier or in a transparent thermosetting resin. This shall have a curing temperature below the maximum storage temperature of the component(s). The resin shall be evacuated after mixing and after the component has been mounted in the uncured resin.

(c) Microsectioning
The component(s) shall be ground and polished to achieve a surface finish of at least 0.1 micron. To improve definition and detail, chemical etches shall be used to highlight junction definition, metallographic features, etc. The following, not exhaustive, features shall be assessed:

(i) Diffusion and oxide characteristics.

(ii) Metal/semiconductor interfaces.

(iii) Metal/metal interfaces.

(iv) Thickness and consistency of layers; particularly insulating layers in components with multiple layer metallisation.

(v) Plating thickness and consistency on posts and pins.

(vi) Solder bumps/balls/columns shall be included.

(vii) Under bump metallization interface

(viii) Substrate vias

(ix) Substrate dielectric cracks or resin voids

Photographs shall be taken of the above.

8.3.4.8 Lid Attach Strength

Lid Pull or Lid Shear, as applicable, shall be performed in accordance with MIL-STD-883, Test Method 2027 (Pull test) or 2019 (Shear test).

8.3.4.9 Terminal Strength

(a) For chip carrier packages: MIL-STD-883, Test Method 2004, Test Condition D.

(b) For ball grid array packages: JESD22-B117.

(c) For column grid array packages: MIL-STD-883, Test Method 2038.

(d) For other packages: MIL-STD-883, Test Method 2004, Test Condition B2.

8.3.5 Subgroup 2D - Package Tests

8.3.5.1 General

The samples in this group shall be randomly divided between subgroups 2D(i) to 2D(iv) in the quantities indicated in Chart I.

8.3.5.2 Subgroup 2D(i) - Thermal Test

This test must be performed on electrically good components.

Components shall be subjected to the following tests sequence:

(a) Temperature Cycling: in accordance with MIL-STD-883, Test Method 1010, Test Condition B, 1500 cycles. Intermediate measurements may be performed at the discretion of the Manufacturer.

(b) Electrical measurements shall be performed in accordance with Room, High and Low Temperatures Electrical Measurements in the Detail Specification.

(c) Scanning Acoustic Microscopy (SAM), final inspection: per Para. 6.6.

(d) Destructive Physical Analysis (DPA): performed on 2 components selected at random from the test samples.

NOTE: The DPA content shall be proposed by the Manufacturer and subsequently agreed with the ESCC Executive. ESCC Basic Specification No. 21001 may be used as a guideline. DPA shall be performed by a laboratory mutually approved by the Manufacturer and by the ESCC Executive.

8.3.5.3 Subgroup 2D(ii) - Mechanical Tests

These tests shall only be performed for Cavity Packaged (Flip-Chip Integrated Circuit) Components.
These tests must be performed on electrically good components.

8.3.5.3.1 Subgroup 2D(ii-a)

Components shall be subjected to the following tests sequence:

(a) Mechanical Shock: as follows:
- For packages ≤ 1290mm^2: MIL-STD-883, Test Method 2002, Test Condition B, 50 shock pulses.
- For packages > 1290mm^2: MIL-STD-883, Test Method 2002, Test Condition B, except the peak level shall be 1000g, 50 shock pulses.

(b) Electrical measurements shall be performed in accordance with Room Temperature Electrical Measurements in the Detail Specification.

(c) Vibration: MIL-STD-883, Test Method 2007, Test Condition A. 40 cycles in each of the orientations X, Y, and Z (total of 120 times).

(d) Electrical measurements shall be performed in accordance with Room Temperature Electrical Measurements in the Detail Specification.

(e) Constant Acceleration: MIL-STD-883, Test Method 2001, Test Condition E (resultant centrifugal acceleration to be in the Y1 axis only). For components which have a package weight of 5 grammes or more, or whose inner seal or cavity perimeter is more than 5 cm, Condition D shall be used.

(f) Electrical measurements shall be performed in accordance with Room Temperature Electrical Measurements in the Detail Specification.

8.3.5.3.2 Subgroup 2D(ii-b):

All components subjected to Subgroup 2D(ii-a) tests, including any failures, shall be subjected to the following test sequence:

(a) Solderability: MIL-STD-883, Test Method 2003 or JESD22-B102, to be performed on all terminals.

(b) Permanence of Marking: ESCC Basic Specification No. 24800.

(c) Lid Attach Strength: per Para. 8.3.4.8.

(d) Terminal Strength: per Para. 8.3.4.9.

8.3.5.4 Subgroup 2D(iii) – Temperature-Humidity Tests

These tests must be performed on electrically good components.

Components shall be divided equally between the following 2 tests:

1. Unbiased Temperature-Humidity Test; see (a) below.
2. Biased Temperature-Humidity Test; see (b) below.

(a) Unbiased Temperature-Humidity Test

One of the following tests shall be performed subject to approval by the ESCC Executive:

i. JESD22-A118 (accelerated moisture resistance - unbiased HAST) with Test Conditions:

- Duration: 96 hours
- Temperature: +130°C
- Relative humidity: 85%
- Pressure: 230kPa

or

- Duration: 264 hours
- Temperature: +110°C
- Relative humidity: 85%
- Pressure: 122kPa

ii. JESD22-A102 (accelerated moisture resistance – unbiased autoclave) with Test Conditions:

- Duration: 96 hours
- Temperature: +121°C
- Relative humidity: 100%

iii. JESD22-A101 (steady-state temperature-humidity life test but with no bias applied) with Test Conditions:

- Duration: 1000 hours
- Temperature: +85°C
- Relative humidity: 85%

On completion of testing, Scanning Acoustic Microscopy (SAM) in accordance with Para. 6.6 shall be performed followed by electrical measurements in accordance with Room, High and Low Temperatures Electrical Measurements in the Detail Specification.

(b) Biased Temperature-Humidity Test

One of the following tests shall be performed subject to approval by the ESCC Executive:

i. JESD22-A101 (steady-state temperature-humidity bias life test) with Test Conditions:

- Duration: 1000 hours
- Temperature: +85°C
- Relative humidity: 85%

ii. JESD22-A110 (Highly Accelerated Temperature and Humidity Stress Test (HAST)) with Test Conditions:

- Duration: 96 hours
- Temperature: +130°C
- Relative humidity: 85%

or

- Duration: 264 hours
- Temperature: +110°C
- Relative humidity: 85%

On completion of testing, Scanning Acoustic Microscopy (SAM) in accordance with Para. 6.6 shall be performed followed by electrical measurements in accordance with Room, High and Low Temperatures Electrical Measurements in the Detail Specification.

8.3.5.5 Subgroup 2D(iv) – High Temperature Storage

This test must be performed on electrically good components.

Components shall be subjected to the following test:

(a) High Temperature Storage: JESD22-A103 applies, 2000 hours and 150°C

On completion of testing, electrical measurements shall be performed in accordance with Room, High and Low Temperatures Electrical Measurements in the Detail Specification

8.3.6 Subgroup 2E - Electrical Tests

The components in this subgroup shall be randomly divided between those tests that are performed.

8.3.6.1 Electrostatic Discharge Sensitivity (ESDS) Test

ESD testing shall be performed in accordance with ESCC Basic Specification No. 23800. If the component under examination is not categorised into one of the 3 classes listed, then the component shall be termed "unclassified".

When the evaluation covers a family or series of components, the types selected for this test shall be representative of all protection circuits within this family or series.

8.3.6.2 Characterisation

(a) Safe Operating Area

(i) Applicability

This test is only applicable to components where operation in circuits requiring transfer and dissipation of significant and/or varying levels of power is an intended feature of their design.

Additionally, it shall only be applied to integrated circuit components that do not have internal output protection circuitry. The ESCC Executive shall review the component type and technology to determine the applicability of the test.

(ii) Procedure

ESCC Executive shall review the component type and technology to determine the test conditions.

(b) Current Limits

The design of each component under investigation shall be examined to ensure that no part of the component carries more than the maximum current defined by the technology or process design rules.

(c) Breakdown Voltage, Input or Output

(i) Applicability

Applicable to digital components only.

(ii) Procedure

MIL-STD-883, Method 3008 shall be applied to find the limiting value.

(d) Input Interaction

(i) Applicability

Applicable to digital components only.

(ii) Digital Components Procedure

The truth table shall be applied at the maximum operating frequency under the conditions specified in the truth table.

(e) Verification of Functionality
The functionality of the component shall be explored over varying temperature ranges, levels of supply voltage, etc. The ESCC Executive shall review the component type and technology to determine the exact procedure to be adopted. Data shall be presented, preferably, in a graphical form: Schmoo plots for example.

8.4 GROUP 3 - ENDURANCE TESTS

8.4.1 General

This group shall be randomly divided into subgroups in the quantities indicated in Chart I (as applicable).

8.4.2 Subgroup 3A - High Temperature Reverse Bias (HTRB) Test

Unless otherwise specified in the Detail Specification, all components shall be subjected to the following test:

(a) High Temperature Reverse Bias Burn-In: duration and test conditions as specified, where applicable, in the Detail Specification.

On completion of testing, electrical measurements shall be performed in accordance with Room, High and Low Temperatures Electrical Measurements in the Detail Specification

8.4.3 Subgroup 3B - Accelerated Electrical Endurance Test

This group shall be randomly divided into 3 subgroups in the quantities indicated in Chart I. The applicable tests shall not be performed until the subgroup 2A tests have been completed and analysed, and 3 test conditions selected. The tests in this group shall be performed as specified in Chart IV.

The temperatures T_1, T_2 and T_3 shall be chosen such that within approximately 1000, 500 and 168 hours, the parameter(s) defined in Para. 8.3.2.3 above can be expected to have drifted to an extreme of the permitted range. A common applied power (if applicable) also determined from the Subgroup 2A tests, shall be used. If the power step-stress test (as defined in Para. 8.3.2.5) was not performed, the components shall be operated at their maximum rated dissipation.

Electrical measurements shall be performed in accordance with Para. 8.3.2.3 above at the following times:

T_1 (1000 hrs)	T_2 (500 hrs)	T_3 (168 hrs)
168 (+24 -0) hrs	168 (+24 -0) hrs	168 (+24 -0) hrs
500 (+24 -0) hrs	500 (+24 -0) hrs	-
1000 (+24 -0) hrs	-	-

Failed components shall be removed for analysis as specified in Para. 8.1.

8.4.4 Subgroup 3C - Extended Burn-in Test

The components shall be tested for 1000 hours in accordance with MIL-STD-883, Test Method 1015, Test Condition B, D or E, at the conditions defined in the Detail Specification for Power Burn-in.

Electrical measurements shall be performed in accordance with Para. 8.3.2.3 above at the following times: 168 (+24 -0) hrs, 500 (+24 -0) hrs and 1000 (+24 -0) hrs.

If the conditions determined for the Subgroup 3B T_1 1000 hour Accelerated Electrical Endurance Test in Para. 8.4.3 above are identical to those defined for Power Burn-in, this test shall not be performed.

If the conditions defined for the Subgroup 3D Extended Life Test in Para. 8.4.5 are identical to those defined for Power Burn-in, this test shall not be performed.

8.4.5 Subgroup 3D - Extended Life Test

The Components shall be subject to a Life test for 4000 hours at T_{amb} = +125°C per MIL-STD-883, Test Method 1005 or JESD22-A108. The applied operating conditions shall be based on the conditions defined in the Detail Specification for Operating Life and shall be subject to approval by the ESCC Executive.

Time temperature regression per MIL-STD-883 Method 1005 Class S may be applied.

Electrical measurements shall be performed in accordance with Para. 8.3.2.3 above at the following times: 168 (+24 -0) hrs, 500 (+24 -0) hrs, 1000 (+24 -0) hrs, 2000 (+24 -0) and 4000 (+24 -0) hrs.

8.5 GROUP 4 - RESERVE

Should any additional tests be considered necessary, the components in this subgroup shall be used.

9 DATA DOCUMENTATION

9.1 GENERAL REQUIREMENTS

An evaluation test report shall be established. This shall comprise the following:

(a) Cover sheet (or sheets).
(b) List of equipment (testing and measuring).
(c) List of test references.
(d) Sample identification.
(e) Production data.
(f) Inspection data.
(g) Initial electrical measurements.
(h) Group 1 - Control Group data.
(i) Group 2 – Preconditioning/SAM data.
(j) Subgroup 2A(i) - Thermal Resistance/Conductivity data.
(k) Subgroup 2A(ii) - Temperature Step-Stress test data.
(l) Subgroup 2A(iii) - Power Step-Stress test data (if applicable).
(m) Subgroup 2B - Radiation test data.
(n) Subgroup 2C - Construction Analysis data.
(o) Subgroup 2D - Package tests data including Subgroups 2D(i), 2D(ii-a), 2D(ii-b), 2D(iii), 2D(iv).
(p) Subgroup 2E - Electrical tests data.
(q) Subgroup 3A - HTRB test data (if applicable).
(r) Subgroup 3B - Accelerated Electrical Endurance test data.
(s) Subgroup 3C - Extended Burn-in test data.
(t) Subgroup 3D - Extended Life Test data.
(u) Group 4 - Reserve data (if applicable).
(v) Summary of results and conclusions.

Items (a) to (v) inclusive shall be grouped, preferably as subpackages, and for identification purposes, each page shall include the following information:

- Manufacturer's/test house's name.
- Lot identification.
- Date of establishment of the document.
- Page number.

9.2 COVER SHEET(S)

The cover sheet (or sheets) of the evaluation test report shall include as a minimum:

(a) Reference to this document, including issue and date.
(b) Component type(s) and number(s).
(c) Lot(s) identification.
(d) Manufacturer's/test house's name and address.
(e) Location of the manufacturing plant/test house.
(f) Signature on behalf of the Manufacturer/test house.
(g) Total number of pages of the evaluation test report.

9.3 LIST OF EQUIPMENT USED

A list of equipment used for tests and measurements shall be included in the evaluation test report. Where applicable, this list shall contain the inventory number, Manufacturer type number, serial number, calibration status data, etc. This list shall indicate for which tests such equipment was used.

9.4 LIST OF TEST REFERENCES

This list shall include all references or codes which are necessary to correlate the test data provided with the applicable tests.

9.5 SAMPLE IDENTIFICATION (PARA. 5.1)

This shall identify the criteria used for the selection of the particular components used for the tests when evaluating a range of components by means of representative samples.

9.6 PRODUCTION DATA (PARA. 5.4)

The progress of the components through the normal manufacturing processes shall be documented. The components failing a particular process shall be detailed, together with the reason for their removal.

9.7 INSPECTION DATA (PARA. 6)

The number of components subjected to each test shall be identified together with the number and reason for any rejects. SAM images and radiographs of any failed components shall be presented.

9.8 INITIAL ELECTRICAL MEASUREMENTS (PARA. 7)

All data shall be recorded against serial numbers. A histogram of component parameters shall be produced.

9.9 GROUP 1 - CONTROL GROUP DATA (PARA. 8.2)

All data shall be recorded against serial numbers.

9.10 GROUP 2 – PRECONDITIONING / SAM DATA (PARA. 8.3.1.1)

All data shall be recorded against serial numbers. Moisture sensitivity level (MSL) shall be recorded. SAM images of any failed components shall be presented.

9.11 SUBGROUP 2A - STEP-STRESS TESTS DATA (PARA. 8.3.2)

9.11.1 Subgroup 2A(i) - Thermal Resistance/Conductivity Data (Para. 8.3.2.2)

All data shall be recorded against serial numbers.

9.11.2 Subgroup 2A(ii) - Temperature Step-Stress Test Data (Para. 8.3.2.4)

All data shall be recorded against serial numbers. This shall include:

(a) Starting temperature.
(b) Temperature steps.
(c) Electrical measurements tabulated for each step.
(d) Graphical output as defined in Para. 8.3.2.7.
(e) Analysis of any failed components as defined in Para. 8.1.
(f) Thermal resistance/conductivity measurements from surviving components as defined in Para. 8.3.2.2.

9.11.3 Subgroup 2A(iii) - Power Step-Stress Test Data (Para. 8.3.2.5) (if applicable)
All data shall be recorded against serial numbers. This shall include:

(a) Starting power.
(b) Power steps.
(c) Electrical measurements tabulated for each step.
(d) Graphical output as defined in Para. 8.3.2.7.
(e) Analysis of any failed components as defined in Para. 8.1.
(f) Thermal resistance/conductivity measurements from surviving components as defined in Para. 8.3.2.2.
(g) SAM images of any failed components shall be presented.

9.11.4 Subgroup 2A(iv) – Intermittent Operating Life Test Data (Para. 8.3.2.6 (if applicable)
All data shall be recorded against serial numbers. This shall include:

(a) Frequency and duration of the on/off cycles.
(b) Quantity of on/off cycles for each component.
(c) Applied operating conditions.
(d) Electrical measurements.
(e) Analysis of any failed components as defined in Para. 8.1.

9.12 SUBGROUP 2B - RADIATION TESTS DATA (PARA. 8.3.3)
All data shall be recorded against serial numbers. This shall include, as applicable:

(a) Total dose steady-state radiation test data
(b) Single Event Effects test data.
(c) Displacement Damage test data.

9.13 SUBGROUP 2C - CONSTRUCTION ANALYSIS DATA (PARA. 8.3.4)
All data shall be recorded against serial numbers. This shall include:

(a) Outgassing data (if applicable).
(b) External visual Photographs.
(c) SEM photographs.
(d) Results of Wire Bond Pull and Wire Bond Shear test (if applicable).
(e) Results of Die Shear Strength, Substrate Attach Strength or Bond Shear (Flip-chip) test (as applicable).
(f) Glassivation layer integrity test data (if applicable).
(g) Microsectioning photographs.
(h) Lid Attach Strength results.
(i) Terminal Strength test results.

9.14 SUBGROUP 2D - PACKAGE TESTS DATA (PARA. 8.3.5)
All data shall be recorded against serial numbers. This shall include:

(a) Subgroup 2D(i) - Thermal tests data. SAM images of any failed components shall be presented.
(b) Subgroup 2D(ii-a) and 2D(ii-b) (if applicable) - Mechanical tests data.
(c) Subgroup 2D(iii) – Temperature-Humidity test data. SAM images of any failed components shall be presented.
(d) Subgroup 2D(iv) – High Temperature Storage test data.

9.15 SUBGROUP 2E - ELECTRICAL TESTS DATA (PARA. 8.3.6)
All data shall be recorded against serial numbers. This shall include:

(a) ESDS test data.
(b) Characterisation data.

9.16 GROUP 3 - ENDURANCE TESTS DATA (PARA. 8.4)

9.16.1 Subgroup 3A - High Temperature Reverse Bias (HTRB) Test Data (Para. 8.4.2)
All data shall be recorded against serial numbers.

9.16.2 Subgroup 3B - Accelerated Electrical Endurance Test Data (Para. 8.4.3)
All data shall be recorded against serial numbers. This shall include:

(a) Temperatures T_1, T_2 and T_3 chosen.
(b) Power chosen.
(c) Electrical measurements tabulated and plotted for each time as defined in Para. 8.4.3.
(d) Drift values referred to the initial electrical measurements (Para. 7).
(e) Analysis of any failed components as defined in Para. 8.1.

9.16.3 Subgroup 3C - Extended Burn-in Test Data (Para. 8.4.4)
All data shall be recorded against serial numbers.

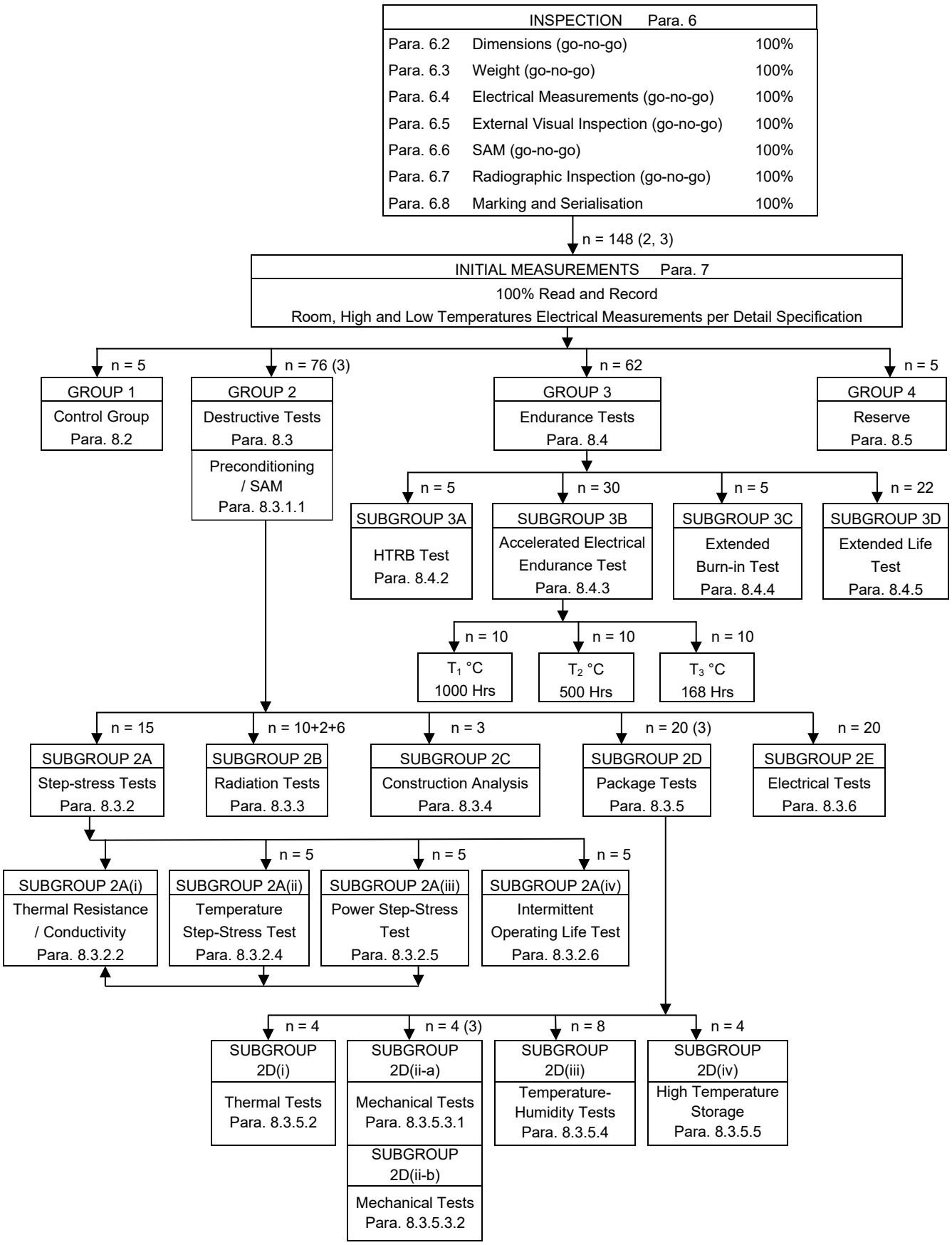
9.16.4 Subgroup 3D - Extended Life Test Data (Para. 8.4.5)
All data shall be recorded against serial numbers.

9.17 GROUP 4 - RESERVE DATA (PARA. 8.5) (IF APPLICABLE)
All data shall be recorded against serial numbers.

9.18 SUMMARY OF RESULTS AND CONCLUSIONS
The above shall be briefly reviewed, indicating the success or otherwise of the evaluation test programme.

Any production screens that need to be introduced into the PID shall be outlined.

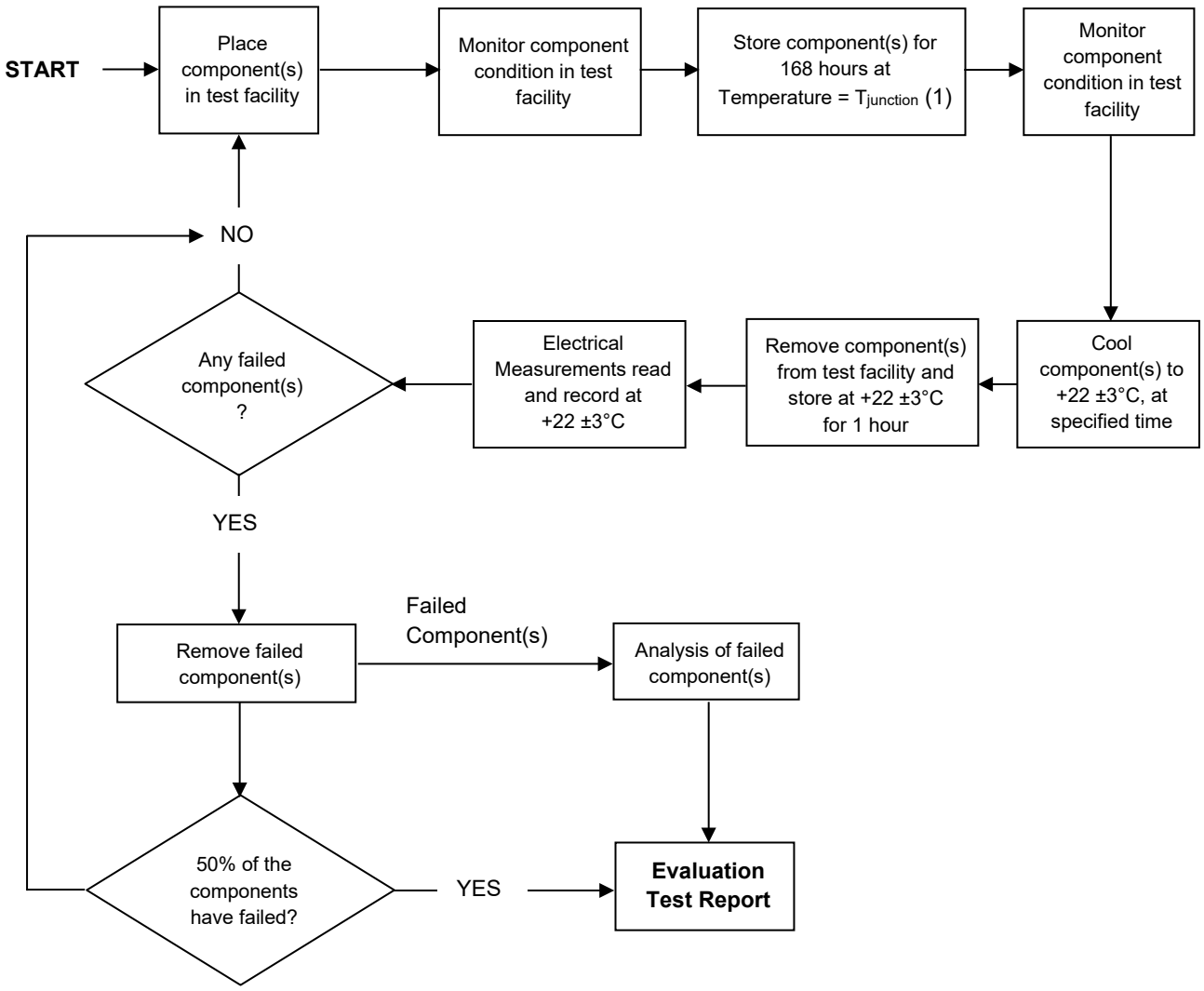
CHART I – EVALUATION TEST PROGRAMME (1)



NOTES:

1. Unless otherwise specified, the quantity of components required for testing in each Group/Subgroup is indicated by the letter n.
2. Additional test components/structures/materials may also be required (see Para. 5.1)
3. Subgroups 2D(ii-a) and 2D(ii-b) tests shall only be performed for Cavity Packaged (Flip-Chip Integrated Circuit) Components.

CHART II – TEMPERATURE STEP-STRESS SEQUENCE (SEE PARA. 8.3.2.4)



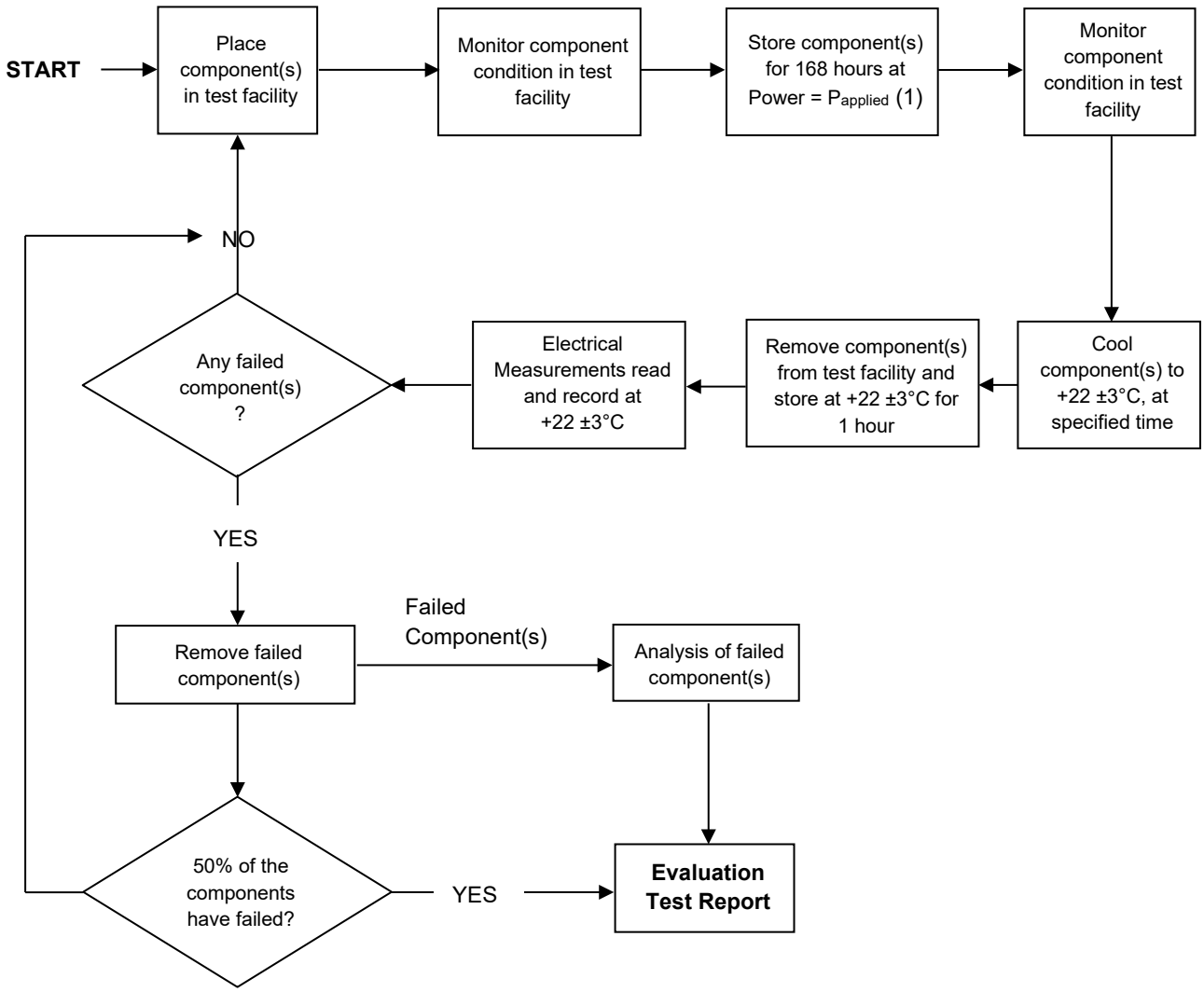
NOTES

1. Temperature steps with $T_{junction}$:

   First step: T_0 (°C)
   T_1 (°C)
   T_2 (°C)
   Last step: T_n (°C)

   with (T_n > … T_2 > T_1 > T_0)

CHART III - POWER STEP-STRESS SEQUENCE (SEE PARA. 8.3.2.5)



NOTES

1. Power steps with $P_{applied}$:
   First step: P_0 (W)
   P_1 (W)
   P_2 (W)
   Last step: P_n (W)

   with ($P_n > \ldots P_2 > P_1 > P_0$)

CHART IV – ACCELERATED ELECTRICAL ENDURANCE TEST (SEE PARA. 8.4.3)