INTEGRATED CIRCUITS, SILICON MONOLITHIC, RADIATION-HARDENED 32-BIT CORTEX®-M7 MICROCONTROLLER, 300MHz, AFE-DAC

BASED ON TYPE SAMV71RT

ESCC Detail Specification No. 9512/007

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DOCUMENTATION CHANGE NOTICE

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DCR No.	CHANGE DESCRIPTION

TABLE OF CONTENTS

1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.

(b) MIL-STD-883, Test Method Standard for Microcircuits.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 951200701R

- Detail Specification Reference: 9512007
- Component Type Variant Number: 01
- Total Dose Radiation Level Letter: E (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter (Note 2)
01	SAMV71RT	CQFP-144	D2 (Note 1)	7	E [20krad(Si)]

NOTES:

1. The terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.
2. Total dose radiation level letters are defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage. Functional performance for extended periods at the maximum ratings may adversely affect device reliability.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in the Test Methods and Procedures of the applicable ESCC generic specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD} V_{CC}	-0.3 to 1.4 -0.3 to 4	V	Notes 1, 2, 3
DC Output Current	I_{OUT}	150	mA	All I/Os
Operating Temperature Range	T_{op}	-55 to +125	°C	Note 1 T_{amb}
Storage Temperature Range	T_{stg}	-60 to +150	°C	
Junction Temperature	T_j	+175	°C	
Thermal Resistance, Junction-to-Case	$R_{th(j-c)}$	5	°C/W	
Soldering Temperature	T_{sol}	+345	°C	Note 4

NOTES:

1. The following operating conditions also apply. Device performance beyond these operating conditions is not guaranteed:

Characteristics	Symbols	Maximum Rated Operating Conditions	Units	Remarks
Supply Voltage	V_{DD} V_{CC}	1.2 to 1.32 3 to 3.6	V	Notes 2, 3
Operating Temperature Range	T_{op}	As per Maximum Ratings table		T_{amb}

2. V_{DD} is for Core and V_{CC} is for I/O.
3. With reference to V_{SS} = 0V.
4. Duration 10 seconds maximum at a distance of not less than 1.6 mm from the device body and the same terminal shall not be re-soldered until 3 minutes have elapsed.

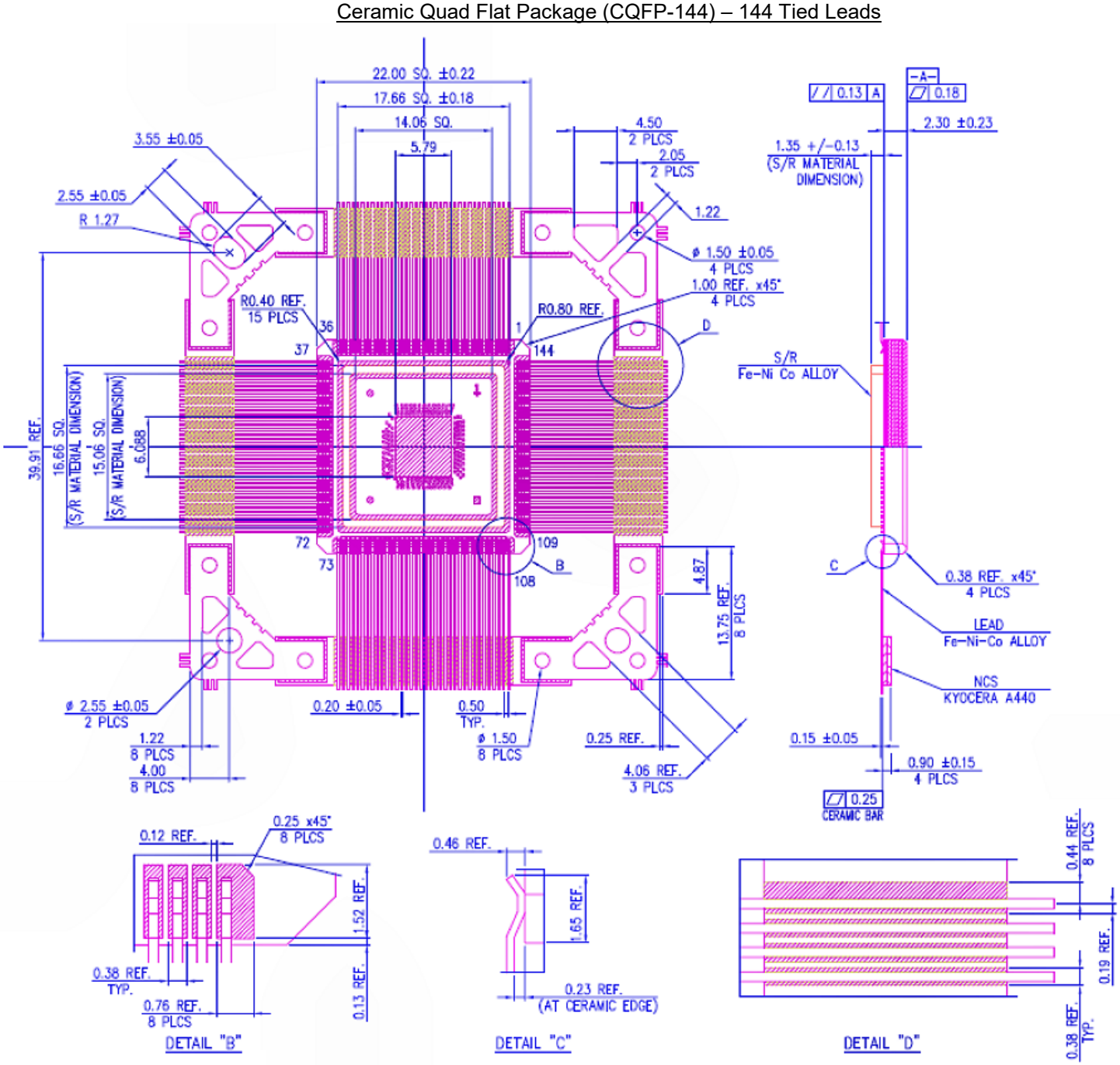
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

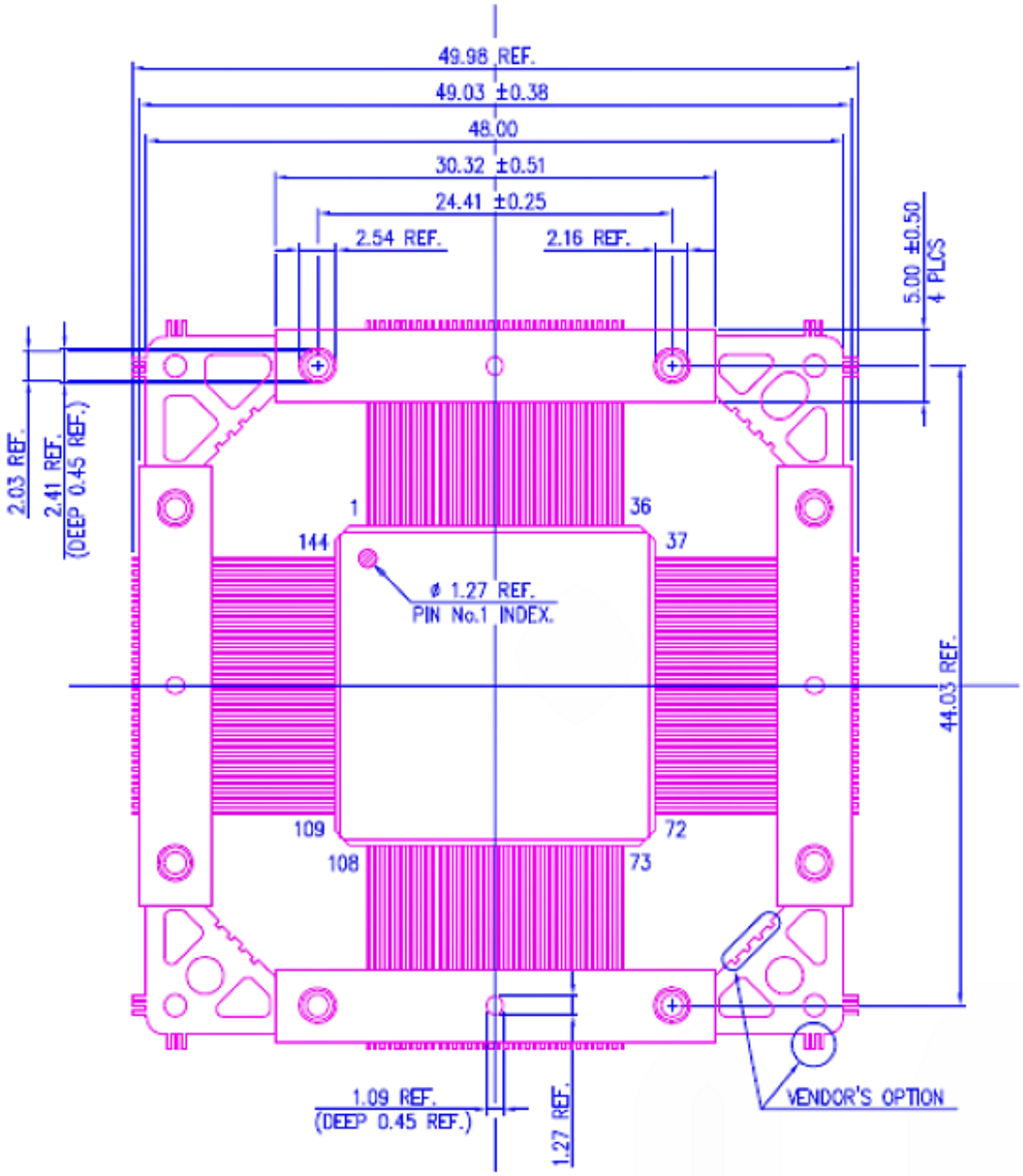
These components are categorised as Class 2 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 3000 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

Ceramic Quad Flat Package (CQFP-144) – 144 Tied Leads



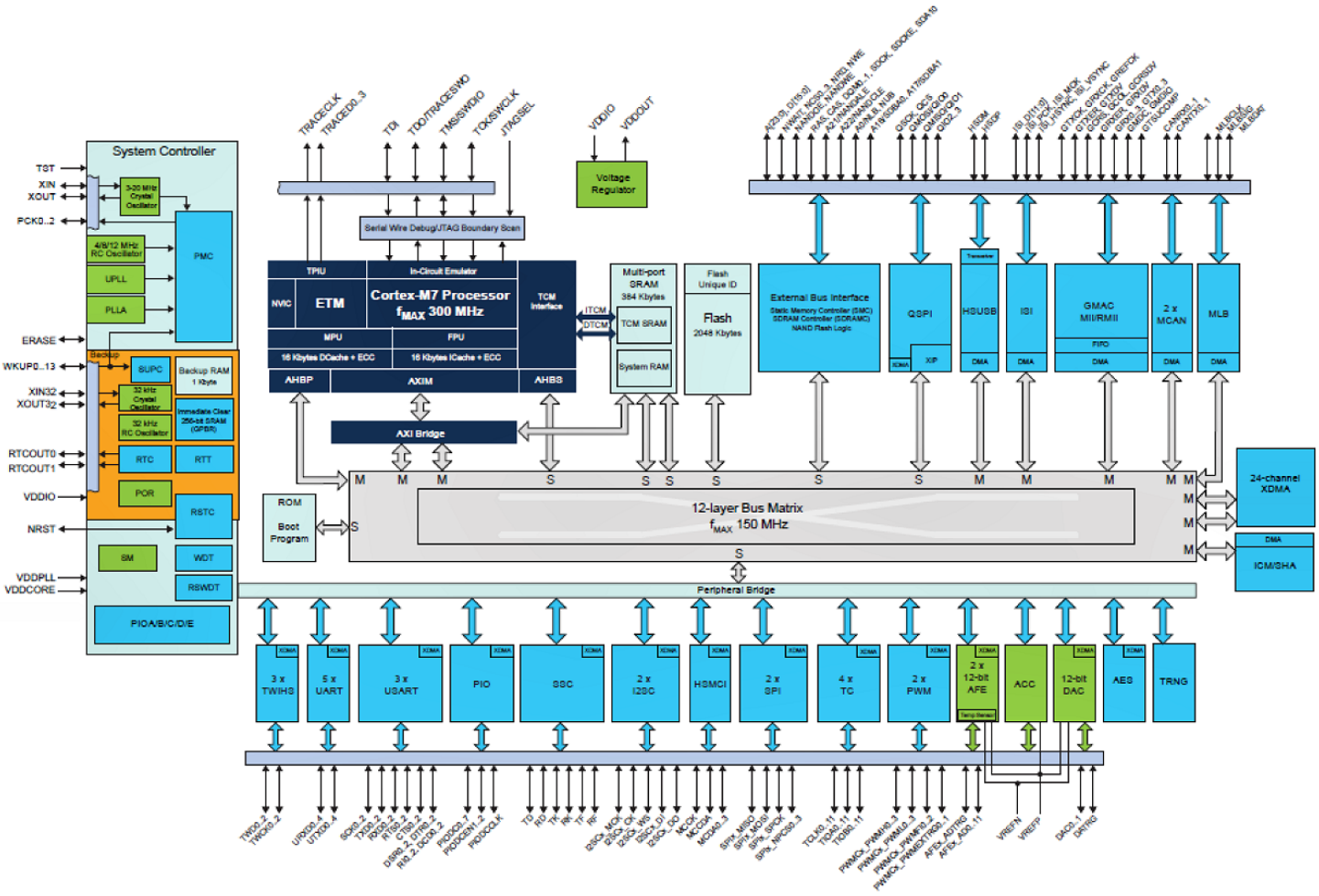
Ceramic Quad Flat Package (CQFP-144) – 144 Tied Leads (Cont.)



NOTES:

1. Terminal identification is specified by reference to the index mark.

1.8 FUNCTIONAL DIAGRAM



1.9 PIN ASSIGNMENT

Pin Number	Pin Name	Description
1	PD0	I/O Controller Pin
2	PD31	I/O Controller Pin
3	VDDOUT	Output Supply Voltage
4	PE0	I/O Controller Pin
5	VDDIN	Input Supply Voltage
6	PE1	I/O Controller Pin
7	PE2	I/O Controller Pin
8	ADVREFN	ADC, DAC and Analog Comparator Negative Reference
9	ADVREFP	ADC, DAC and Analog Comparator Positive Reference
10	PE3	I/O Controller Pin
11	PC0	I/O Controller Pin
12	PC27	I/O Controller Pin
13	PC26	I/O Controller Pin

Pin Number	Pin Name	Description
14	PC31	I/O Controller Pin
15	PC30	I/O Controller Pin
16	PC29	I/O Controller Pin
17	PC12	I/O Controller Pin
18	PC15	I/O Controller Pin
19	PC13	I/O Controller Pin
20	PB1	I/O Controller Pin
21	PB0	I/O Controller Pin
22	PA20	I/O Controller Pin
23	PA19	I/O Controller Pin
24	PA18	I/O Controller Pin
25	PA17	I/O Controller Pin
26	PB2	I/O Controller Pin
27	PE4	I/O Controller Pin
28	PE5	I/O Controller Pin
29	VDDCORE	Supply voltage for Core, embedded memories and peripherals
30	VDDIO	Supply voltage for Peripheral I/O lines (Input/Output Buffers), backup part, 1kbytes of backup SRAM, 32kHz crystal oscillator, oscillator pads
31	PB3	I/O Controller Pin
32	PA21	I/O Controller Pin
33	VDDCORE	Supply voltage for Core, embedded memories and peripherals
34	PD30	I/O Controller Pin
35	PA7/XIN	I/O Controller Pin / Main Oscillator Input
36	PA8/XOUT	I/O Controller Pin / Main Oscillator Output
37	PA22	I/O Controller Pin
38	PC1	I/O Controller Pin
39	PC2	I/O Controller Pin
40	PC3	I/O Controller Pin
41	PC4	I/O Controller Pin
42	PA13	I/O Controller Pin
43	VDDIO	Supply voltage for Peripheral I/O lines (Input/Output Buffers), backup part, 1kbytes of backup SRAM, 32kHz crystal oscillator, oscillator pads.
44	GND	Ground Pin
45	PA16	I/O Controller Pin
46	PA23	I/O Controller Pin
47	PD27	I/O Controller Pin
48	PC7	I/O Controller Pin
49	PA15	I/O Controller Pin

Pin Number	Pin Name	Description
50	VDDCORE	Supply voltage for Core, embedded memories and peripherals
51	PA14	I/O Controller Pin
52	PD25	I/O Controller Pin
53	PD26	I/O Controller Pin
54	PC6	I/O Controller Pin
55	PD24	I/O Controller Pin
56	PA24	I/O Controller Pin
57	PD23	I/O Controller Pin
58	PC5	I/O Controller Pin
59	PA25	I/O Controller Pin
60	PD22	I/O Controller Pin
61	GND	Ground Pin
62	PA26	I/O Controller Pin
63	PD21	I/O Controller Pin
64	PA11	I/O Controller Pin
65	PD20	I/O Controller Pin
66	PA10	I/O Controller Pin
67	PD19	I/O Controller Pin
68	PA12	I/O Controller Pin
69	PD18	I/O Controller Pin
70	PA27	I/O Controller Pin
71	PD28	I/O Controller Pin
72	VDDIO	Supply voltage for Peripheral I/O lines (Input/Output Buffers), backup part, 1kbytes of backup SRAM, 32kHz crystal oscillator, oscillator pads.
73	PA5	I/O Controller Pin
74	PD17	I/O Controller Pin
75	PA9	I/O Controller Pin
76	PC28	I/O Controller Pin
77	PA4	I/O Controller Pin
78	PD16	I/O Controller Pin
79	PB6/TMS	I/O Controller Pin / Test Mode Select
80	VDDIO	Supply voltage for Peripheral I/O lines (Input/Output Buffers), backup part, 1kbytes of backup SRAM, 32kHz crystal oscillator, oscillator pads.
81	VDDCORE	Supply voltage for Core, embedded memories and peripherals
82	PC8	I/O Controller Pin
83	NRST	Synchronous Microcontroller Reset
84	PD14	I/O Controller Pin
85	TST	Test Select

Pin Number	Pin Name	Description
86	PC9	I/O Controller Pin
87	PB12/ERASE	I/O Controller Pin / Flash and NVM Configuration Bits Erase
88	PD13	I/O Controller Pin
89	PB7/TCK	I/O Controller Pin / Test Clock
90	PC10	I/O Controller Pin
91	PA3	I/O Controller Pin
92	PD12	I/O Controller Pin
93	PA2	I/O Controller Pin
94	PC11	I/O Controller Pin
95	GND	Ground Pin
96	VDDIO	Supply voltage for Peripheral I/O lines (Input/Output Buffers), backup part, 1kbytes of backup SRAM, 32kHz crystal oscillator, oscillator pads.
97	PC14	I/O Controller Pin
98	PD11	I/O Controller Pin
99	PA1	I/O Controller Pin
100	PC16	I/O Controller Pin
101	PD10	I/O Controller Pin
102	PA0	I/O Controller Pin
103	PC17	I/O Controller Pin
104	JTAGSEL	JTAG Selection
105	PB4/TDI	I/O Controller Pin / Test Data In
106	PD15	I/O Controller Pin
107	VDDCORE	Supply voltage for Core, embedded memories and peripherals
108	PD29	I/O Controller Pin
109	PB5/TDO	I/O Controller Pin / Test Data Out
110	PD9	I/O Controller Pin
111	PC18	I/O Controller Pin
112	PA28	I/O Controller Pin
113	PD8	I/O Controller Pin
114	PA6	I/O Controller Pin
115	GND	Ground Pin
116	PA30	I/O Controller Pin
117	PC19	I/O Controller Pin
118	PA31	I/O Controller Pin
119	PD7	I/O Controller Pin
120	PC20	I/O Controller Pin
121	PD6	I/O Controller Pin

Pin Number	Pin Name	Description
122	PC21	I/O Controller Pin
123	VDDPLL	Dedicated Supply Voltage for PLL and the fast RC oscillator
124	PC22	I/O Controller Pin
125	PD5	I/O Controller Pin
126	PD4	I/O Controller Pin
127	PC23	I/O Controller Pin
128	PD3	I/O Controller Pin
129	PA29	I/O Controller Pin
130	PC24	I/O Controller Pin
131	PD2	I/O Controller Pin
132	PD1	I/O Controller Pin
133	PC25	I/O Controller Pin
134	VDDUTMII	Dedicated Supply Voltage for USB transceiver interface (not used, see Note 1)
135	GND	Ground Pin
136	HSDM	HS/FS Differential Data Line -
137	HSDP	HS/FS Differential Data Line +
138	GND	Ground Pin
139	VDDUTMIC	Dedicated Supply Voltage for USB transceiver (not used, see Note 1)
140	VBG	Bias Voltage Reference for USB
141	PB8/XOUT	I/O Controller Pin / Main Oscillator Output
142	PB9/XIN	I/O Controller Pin / Main Oscillator Input
143	VDDPLLUSB	Dedicated Supply Voltage for PLL USB UTMI PLL and the 3 to 21 MHz oscillator, (not used, see Note 1)
144	PB13	I/O Controller Pin

NOTES

1. The USB interface is not supported, therefore Pin Name and Description are for information only.

2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirements and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests for Packaged Components – Chart F3A
High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING
The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification (see Para. 1.7).
(b) The ESCC qualified components symbol (for ESCC qualified component only).
(c) The ESCC Component Number (see Para. 1.4.1).
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES
Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements
The measurements shall be performed at T_{case} = +25(+3 -5)°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions 1.2V < V_{DD} < 1.32V 3V < V_{CC} < 3.6V (Note 1)	Limits		Units
				Min	Max	
Functional Tests	-	3014	Self-tests	-	-	-
Low Level Output Voltage	V_{OL1}	3007	Pins GPIO_AD, GPIO, CLOCK I_{OL} = -2mA	-	400	mV
	V_{OL2}	3007	Pins GPIO_AD, GPIO, CLOCK I_{OL} = -5mA	-	400	mV
	V_{OL3}	3007	Pin GPIO_CLK I_{OL} = -3mA	-	400	mV
	V_{OL4}	3007	Pin GPIO_CLK, GPIO_MLB I_{OL} = -6mA	-	400	mV
High Level Output Voltage	V_{OH1}	3006	Pins GPIO_AD, GPIO, CLOCK I_{OH} = 2mA	V_{CC}-0.4	-	V
	V_{OH2}	3006	Pins GPIO_AD, GPIO, CLOCK I_{OH} = 5mA	V_{CC}-0.4	-	V
	V_{OH3}	3006	Pin GPIO_CLK I_{OH} = 3mA	V_{CC}-0.4	-	V
	V_{OH4}	3006	Pin GPIO_CLK, GPIO_MLB I_{OH} = 6mA	V_{CC}-0.4	-	V
Low Level Input Current	I_{IL}	3009	V_{IN} = V_{SS}	-1	1	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions $1.2V < V_{DD} < 1.32V$ $3V < V_{CC} < 3.6V$ (Note 1)	Limits		Units
				Min	Max	
Low Level Input Current with Pull-up	I_{ILPU}	3009	$V_{IN} = V_{SS}$	-60	-10	µA
High Level Input Current	I_{IH}	3010	$V_{IN} = V_{CC}$ max	-1	1	µA
High Level Input Current with Pull-down	I_{IHPD}	3010	$V_{IN} = V_{CC}$ max	-10	60	µA
Supply Current, Backup Mode	$I_{DDBackup1}$	3005	SRAM on V_{CC} = 3.6V	-	8.4	µA
	$I_{DDBackup2}$	3005	SRAM off V_{CC} = 3.6V	-	5.1	µA
Operating Period RC 32kHz	t_{OSC32k}	3003	f_{op}: 20kHz - 44kHz	22	50	µs
Operating Period RC 8MHz	t_{OSC8M}	3003	f_{op}: 7.94MHz - 8.06MHz	124	126	ns
Operating Period RC 12MHz	t_{OSC12M}	3003	f_{op}: 11.9MHz - 12.2MHz	82	84	ns
AFE Gain Error at 3.3V (Note 3)	GE_{AFE}	-	-	-0.3 (-12)	2.5 (+100)	% (LSB)
DAC Gain Error at 3.3V (Note 3)	GE_{DAC}	-	-	-1 (-40)	1 (+40)	%.FSR (LSB)
AFE Offset Error at 3.3V (Note 3)	OE_{AFE}	-	-	-20	+20	LSB
DAC Offset Error at 3.3V (Note 3)	OE_{DAC}	-	-	-8	8	mV

NOTES:

1. Unless otherwise specified, all inputs and outputs shall be tested for each characteristic. Inputs not under test shall be $V_{IN} = V_{SS}$ or V_{CC} and outputs not under test shall be open. V_{SS} = 0V.
2. I/O families:

   CLOCK = PA[7], PA[8], PB[8], PB[9]

   GPIO = PA[2], PA[4], PA[26], PA[28:30], PB[6], PB[7], PB[12], PD[1:3], PD[20], PD[26], PB[0:2]

   GPIO_AD = PA[0:1], PA[3], PA[5:6], PA[9], PA[10:13], PA[15:25], PA[27], PA[31], PB[3], PB[13], PC[0:31], PD[0], PD[11:19], PD[21:22], PD[24:25], PD[27:31], PE[0:5]

   GPIO_CLK= PA[14], PD[44:9], PD[23]

   GPIO_MLB= PB[4:5], PD[10]
3. This characteristic applies over a V_{REFP} range of 5% - 95%.

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{case} = +125 ±3°C and T_{case} = -55 ±3°C.

The characteristics, test methods, conditions and limits shall be the same as specified in Para. 2.3.1, Room Temperature Electrical Measurements, except for the parameters shown in the table below, at T_{case} = +125 ±3°C and except parameters t_{OSC32k} t_{OSC8M} t_{OSC12M} which are not tested:

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions 1.2V < V_{DD} < 1.32V 3V < V_{CC} < 3.6V (Note 1)	Limits		Units
				Min	Max	
High Level Input Current	I_{IH}	3010	V_{IN} = V_{CC} max	-2	2	µA
Supply Current, Backup Mode	$I_{DDBackup1}$	3005	SRAM on V_{CC} = 3.6V	-	80	µA
	$I_{DDBackup2}$	3005	SRAM off V_{CC} = 3.6V	-	38	µA

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{case} = +25(+3 -5)°C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1, Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Low Level Output Voltage	V_{OL1}	±100	-	400	mV
	V_{OL2}	±100	-	400	mV
	V_{OL3}	±100	-	400	mV
	V_{OL4}	±100	-	400	mV
High Level Output Voltage	V_{OH1}	±0.1	V_{CC}-0.4	-	V
	V_{OH2}	±0.1	V_{CC}-0.4	-	V
	V_{OH3}	±0.1	V_{CC}-0.4	-	V
	V_{OH4}	±0.1	V_{CC}-0.4	-	V
Low Level Input Current	I_{IL}	±50	-1000	1000	nA
High Level Input Current	I_{IH}	±50	-1000	1000	nA
Supply Current, Backup Mode	$I_{DDBackup1}$	±1	-	8.4	µA
	$I_{DDBackup2}$	±1	-	5.1	µA

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{case} = +25(+3 -5)°C.

The characteristics, test methods, conditions and limits shall be the same as specified in Para. 2.3.1, Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

Prior to submitting the parts to Burn-In or Operating Life, a specific application is loaded in the Flash memory. This application automatically starts after the RESET is released. The correct behaviour of the device can be monitored with an on-board LED.

The specific application will run with internal PLL @75MHz and will exercise the following function blocks:

1. HTOL_FLEXCOM_SPI
   FLEXCOM1 as master and FLEXCOM2 as slave / Hardware loop
2. HTOL_FLEXCOM_TWI
   FLEXCOM3 as master and FLEXCOM4 as slave / Hardware loop
3. HTOL_SPW
   Internal loopback
4. HTOL_CAN
   Internal loopback
5. HTOL_PIO
   Toggle of IOs
6. HTOL_TC
   Start TC0 to TC11, stop in interrupt handler
7. HTOL_FLEXCOMS
   USART mode on FLEXCOM0, 5, 6, 7, 8, 9
   Putchar and Getchar
8. HTOL_HEMC
   Enable ECC, write and read in external memory (not present)
9. HTOL_TRNG
   Run TRNG and read random value
10. HTOL_ICM
    Check integrity of regions
11. HTOL_XDMAC_PWM
    Load PWM duty cycle with DMA
12. HTOL_MEMORY
    Code in Flash memory with exec in Flexram.
    Read SRAM (768k-16k)
    Read Flash (128k)

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125(+8 -0)	°C
Core Supply Voltage	V_{DD}	1.32	V
I/O Supply Voltage	V_{CC}	3.6	V

NOTES:

1. Pin connections shall be as follows, where NC = not connected:

Pin	Pin Name	Serial Resistance	Wired To	Pin	Pin Name	Serial Resistance	Wired To
1	PD0	-	NC	73	PA5	-	NC
2	PD31	1kΩ+led	3.6V	74	PD17	-	NC
3	VDDOUT	-	(**)	75	PA9	-	NC
4	PE0	-	NC	76	PC28	-	NC
5	VDDIN	-	3.6V	77	PA4	-	NC
6	PE1	-	NC	78	PD16	-	NC
7	PE2	-	NC	79	PB6/TMS	-	NC
8	ADVREFN	-	Ground	80	VDDIO	-	3.6V
9	ADVREFP	-	3.6V	81	VDDCORE	-	“VDDOUT” Pin
10	PE3	-	NC	82	PC8	-	NC
11	PC0	-	NC	83	NRST	4.7kΩ	3.6V
12	PC27	-	NC	84	PD14	-	NC
13	PC26	-	NC	85	TST	-	NC
14	PC31	-	NC	86	PC9	-	NC
15	PC30	-	NC	87	PB12/ERASE	-	NC
16	PC29	-	NC	88	PD13	-	NC
17	PC12	-	NC	89	PB7/TCK	-	NC
18	PC15	-	NC	90	PC10	-	NC
19	PC13	-	NC	91	PA3	-	NC
20	PB1	-	NC	92	PD12	-	NC
21	PB0	-	NC	93	PA2	100kΩ	3.6V
22	PA20	-	NC	94	PC11	-	NC
23	PA19	-	NC	95	GND	-	NC
24	PA18	-	NC	96	VDDIO	-	3.6V
25	PA17	-	NC	97	PC14	-	NC
26	PB2	-	NC	98	PD11	-	NC
27	PE4	-	NC	99	PA1	-	NC
28	PE5	-	NC	100	PC16	-	NC
29	VDDCORE	-	“VDDOUT” Pin	101	PD10	-	NC
30	VDDIO	-	3.6V	102	PA0	-	NC
31	PB3	-	NC	103	PC17	-	NC
32	PA21	-	NC	104	JTAGSEL	-	NC
33	VDDCORE	-	“VDDOUT” Pin	105	PB4/TDI	-	NC
34	PD30	-	NC	106	PD15	-	NC
35	PA7/XIN	-	NC	107	VDDCORE	-	“VDDOUT” Pin
36	PA8/XOUT	-	NC	108	PD29	-	NC
37	PA22	-	NC	109	PB5/TDO	-	NC

Pin	Pin Name	Serial Resistance	Wired To	Pin	Pin Name	Serial Resistance	Wired To
38	PC1	-	NC	110	PD9	-	NC
39	PC2	-	NC	111	PC18	-	NC
40	PC3	-	NC	112	PA28	-	NC
41	PC4	-	NC	113	PD8	-	NC
42	PA13	-	NC	114	PA6	-	NC
43	VDDIO	-	3.6V	115	GND	-	Ground
44	GND	-	Ground	116	PA30	-	NC
45	PA16	100kΩ	3.6V	117	PC19	-	NC
46	PA23	-	NC	118	PA31	-	NC
47	PD27	-	NC	119	PD7	-	NC
48	PC7	-	NC	120	PC20	-	NC
49	PA15	-	NC	121	PD6	-	NC
50	VDDCORE	-	“VDDOUT” Pin	122	PC21	-	NC
51	PA14	-	NC	123	VDDPLL	10µH + 2.2Ω	“VDDOUT” Pin
52	PD25	-	NC	124	PC22	-	NC
53	PD26	-	NC	125	PD5	-	NC
54	PC6	-	NC	126	PD4	-	NC
55	PD24	-	NC	127	PC23	-	NC
56	PA24	-	NC	128	PD3	-	NC
57	PD23	-	NC	129	PA29	-	NC
58	PC5	-	NC	130	PC24	-	NC
59	PA25	-	NC	131	PD2	-	NC
60	PD22	-	NC	132	PD1	-	NC
61	GND	-	Ground	133	PC25	-	NC
62	PA26	-	NC	134	VDDUTMII	-	3.6V
63	PD21	-	NC	135	GND	-	Ground
64	PA11	-	NC	136	HSDM	-	NC
65	PD20	-	NC	137	HSDP	-	NC
66	PA10	-	NC	138	GND	-	GND
67	PD19	-	NC	139	VDDUTMIC	10µH + 2.2Ω	“VDDOUT” Pin
68	PA12	-	NC	140	VBG	5.62kΩ	GND
69	PD18	-	NC	141	PB8/XOUT	-	NC
70	PA27	-	NC	142	PB9/XIN	-	NC
71	PD28	-	NC	143	VDDPLLUSB	-	3.6V
72	VDDIO	-	3.6V	144	PB13	-	NC

(**) Pin 3 is connected to Pins 29, 33, 50, 81, 107, 123 and 139.

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified in Para. 2.6, Power Burn-in Conditions.

2.8 TOTAL DOSE IRRADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in Para. 1.4.2 or in the Purchase Order.

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+25(+3 -5)	°C
Core Supply Voltage	V_{DD}	1.32	V
I/O Supply Voltage	V_{CC}	3.6	V

NOTES:

1. Pin connections shall be as follows:

Pin	Pin Name	Serial Resistance	Wired To	Pin	Pin Name	Serial Resistance	Wired To
1	PD0	100kΩ	3.6V	73	PA5	100kΩ	3.6V
2	PD31	100kΩ	3.6V	74	PD17	100kΩ	3.6V
3	VDDOUT	-	(**)	75	PA9	100kΩ	3.6V
4	PE0	100kΩ	3.6V	76	PC28	100kΩ	3.6V
5	VDDIN	-	3.6V	77	PA4	100kΩ	3.6V
6	PE1	100kΩ	3.6V	78	PD16	100kΩ	3.6V
7	PE2	100kΩ	3.6V	79	PB6/TMS	100kΩ	3.6V
8	ADVREFN	-	Ground	80	VDDIO	-	3.6V
9	ADVREFP	-	3.6V	81	VDDCORE	-	“VDDOUT” Pin
10	PE3	100kΩ	3.6V	82	PC8	100kΩ	3.6V
11	PC0	100kΩ	3.6V	83	NRST	-	Ground
12	PC27	100kΩ	3.6V	84	PD14	100kΩ	3.6V
13	PC26	100kΩ	3.6V	85	TST	-	Ground
14	PC31	100kΩ	3.6V	86	PC9	100kΩ	3.6V
15	PC30	100kΩ	3.6V	87	PB12/ERASE	100kΩ	Ground
16	PC29	100kΩ	3.6V	88	PD13	100kΩ	3.6V
17	PC12	100kΩ	3.6V	89	PB7/TCK	100kΩ	3.6V
18	PC15	100kΩ	3.6V	90	PC10	100kΩ	3.6V
19	PC13	100kΩ	3.6V	91	PA3	100kΩ	3.6V
20	PB1	100kΩ	3.6V	92	PD12	100kΩ	3.6V
21	PB0	100kΩ	3.6V	93	PA2	100kΩ	3.6V
22	PA20	100kΩ	3.6V	94	PC11	100kΩ	3.6V
23	PA19	100kΩ	3.6V	95	GND	-	Ground

Pin	Pin Name	Serial Resistance	Wired To	Pin	Pin Name	Serial Resistance	Wired To
24	PA18	100kΩ	3.6V	96	VDDIO	-	3.6V
25	PA17	100kΩ	3.6V	97	PC14	100kΩ	3.6V
26	PB2	100kΩ	3.6V	98	PD11	100kΩ	3.6V
27	PE4	100kΩ	3.6V	99	PA1	100kΩ	3.6V
28	PE5	100kΩ	3.6V	100	PC16	100kΩ	3.6V
29	VDDCORE	-	“VDDOUT” Pin	101	PD10	100kΩ	Ground
30	VDDIO	-	3.6V	102	PA0	100kΩ	3.6V
31	PB3	100kΩ	3.6V	103	PC17	100kΩ	3.6V
32	PA21	100kΩ	3.6V	104	JTAGSEL	-	Ground
33	VDDCORE	-	“VDDOUT” Pin	105	PB4/TDI	100kΩ	Ground
34	PD30	100kΩ	3.6V	106	PD15	100kΩ	3.6V
35	PA7/XIN	100kΩ	3.6V	107	VDDCORE	-	“VDDOUT” Pin
36	PA8/XOUT	100kΩ	3.6V	108	PD29	100kΩ	3.6V
37	PA22	100kΩ	3.6V	109	PB5/TDO	100kΩ	Ground
38	PC1	100kΩ	3.6V	110	PD9	100kΩ	3.6V
39	PC2	100kΩ	3.6V	111	PC18	100kΩ	3.6V
40	PC3	100kΩ	3.6V	112	PA28	100kΩ	3.6V
41	PC4	100kΩ	3.6V	113	PD8	100kΩ	3.6V
42	PA13	100kΩ	3.6V	114	PA6	100kΩ	3.6V
43	VDDIO	-	3.6V	115	GND	-	Ground
44	GND	-	Ground	116	PA30	100kΩ	3.6V
45	PA16	100kΩ	3.6V	117	PC19	100kΩ	3.6V
46	PA23	100kΩ	3.6V	118	PA31	100kΩ	3.6V
47	PD27	100kΩ	3.6V	119	PD7	100kΩ	3.6V
48	PC7	100kΩ	3.6V	120	PC20	100kΩ	3.6V
49	PA15	100kΩ	3.6V	121	PD6	100kΩ	3.6V
50	VDDCORE	-	“VDDOUT” Pin	122	PC21	100kΩ	3.6V
51	PA14	100kΩ	3.6V	123	VDDPLL	-	“VDDOUT” Pin
52	PD25	100kΩ	3.6V	124	PC22	100kΩ	3.6V
53	PD26	100kΩ	3.6V	125	PD5	100kΩ	3.6V
54	PC6	100kΩ	3.6V	126	PD4	100kΩ	3.6V
55	PD24	100kΩ	3.6V	127	PC23	100kΩ	3.6V
56	PA24	100kΩ	3.6V	128	PD3	100kΩ	3.6V
57	PD23	100kΩ	3.6V	129	PA29	100kΩ	3.6V
58	PC5	100kΩ	3.6V	130	PC24	100kΩ	3.6V
59	PA25	100kΩ	3.6V	131	PD2	100kΩ	3.6V
60	PD22	100kΩ	3.6V	132	PD1	100kΩ	3.6V

Pin	Pin Name	Serial Resistance	Wired To	Pin	Pin Name	Serial Resistance	Wired To
61	GND	-	Ground	133	PC25	100kΩ	3.6V
62	PA26	100kΩ	3.6V	134	VDDUTMII	-	3.6V
63	PD21	100kΩ	3.6V	135	GND	-	Ground
64	PA11	100kΩ	3.6V	136	HSDM	-	Ground
65	PD20	100kΩ	3.6V	137	HSDP	-	Ground
66	PA10	100kΩ	3.6V	138	GND	-	Ground
67	PD19	100kΩ	3.6V	139	VDDUTMIC	-	“VDDOUT” Pin
68	PA12	100kΩ	3.6V	140	VBG	100kΩ	Ground
69	PD18	100kΩ	3.6V	141	PB8/XOUT	100kΩ	3.6V
70	PA27	100kΩ	3.6V	142	PB9/XIN	100kΩ	3.6V
71	PD28	100kΩ	3.6V	143	VDDPLLUSB	-	3.6V
72	VDDIO	-	3.6V	144	PB13	100kΩ	3.6V

(**) Pin 3 is connected to Pins 29, 33, 50, 81, 107, 123 and 139.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to, during and on completion of irradiation testing the devices shall have successfully met the Room Temperature Electrical Measurements specified in Para. 2.3.1.

Unless otherwise stated the measurements shall be performed at T_{case} = +25(+3 -5)°C.

The characteristics, test methods, conditions and limits shall be as per the corresponding test defined in Para. 2.3.1, Room Temperature Electrical Measurements.