INTEGRATED CIRCUITS,

2 CHANNEL HIGH SPEED DRIVER

WITH SPST JFET SWITCHES

BASED ON TYPE DG181

ESCC Detail Specification No. 9408/001

ISSUE 1

October 2002

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Pages 1 to 26

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space components
coordination group

Issue/Rev.	Date	Approved by	
		SCCG Chairman	ESA Director General or his Deputy
Issue 2	February 1999		

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE Reference	Item	Approved DCR No.
		This Issue supersedes Issue 1 and incorporates all modifications defined in Revision 'A' to Issue 1 and the changes agreed in the following DCRs:-		
		Cover page		None
		DCN		None
		Para. 4.1	: Second paragraph added	21019
		Para. 4.2.2	: Deviation deleted and "None" substituted	21048
		Para. 4.2.4	: "None" deleted and Deviation (a) added	22919
		Para. 4.2.5	: "None" deleted and Deviation (a) added	22919
		Para. 4.3.3	: Deleted in toto	22921

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TABLES

FIGURES

APPENDICES (Applicable to specific Manufacturers only)
None.

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a 2 Channel High Speed Driver with SPST JFET switches based on Type DG181. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

Derate 6.0mW/°C at +75°C or above. See Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the integrated circuits specified herein are shown in Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 CIRCUIT SCHEMATIC

As per Figure 3(b).

1.8 FUNCTIONAL DIAGRAM

As per Figure 3(c).

1.9 HANDLING PRECAUTIONS

These devices are susceptible to damage by Electrostatic Discharge. Therefore suitable precautions shall be employed for protection during all phases of manufacture, test, packaging, shipping and any handling.

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
01	TO100	2(a)	D3 or D4
02	TO100	2(a)	D2
03	D.I.L.	2(b)	D3 or D4
04	D.I.L.	2(b)	D2

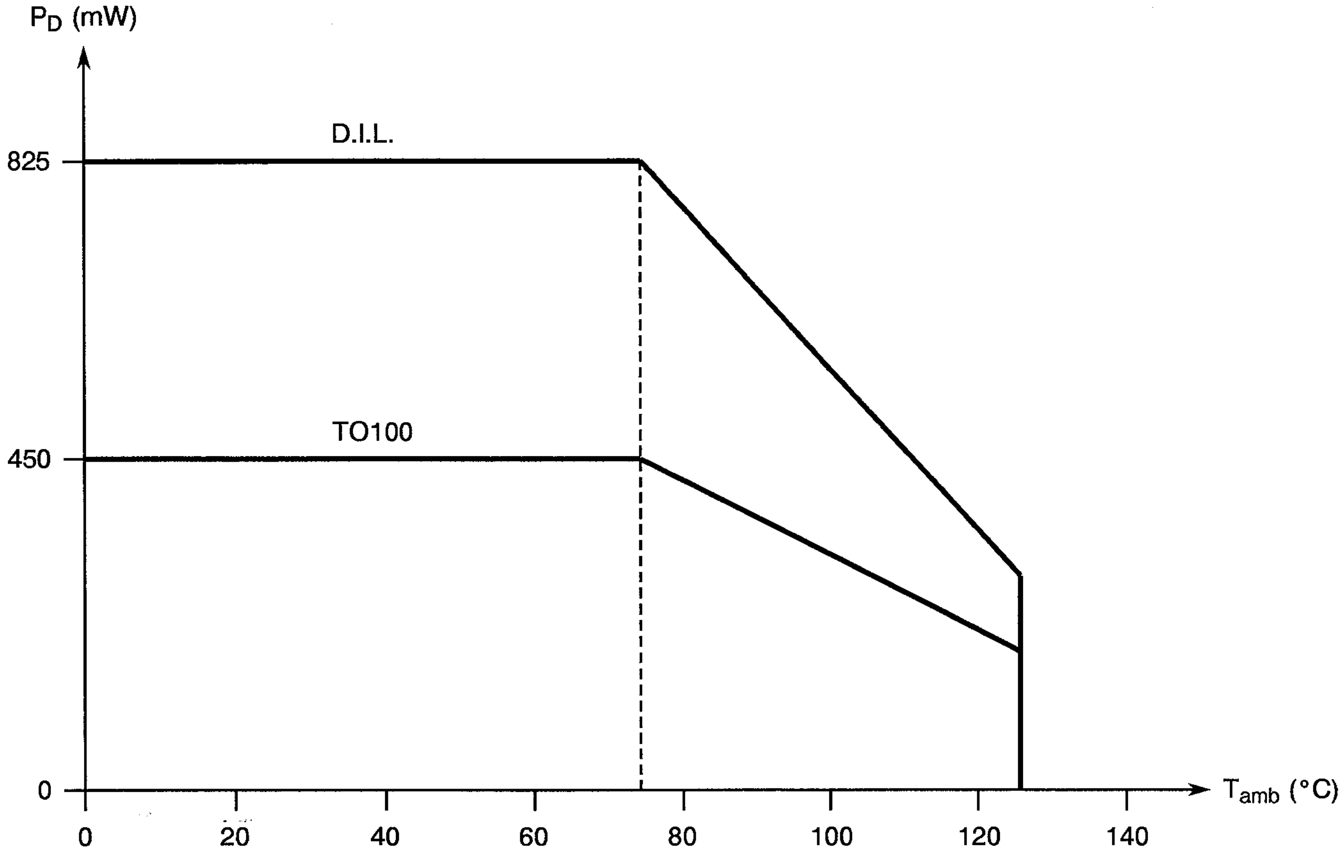
TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNITS	REMARKS
1	Total Supply Voltage	$V_{DD} - V_{SS}$	36	V	
2	Positive Supply to Drain	$V_{DD} - V_D$	33	V	
3	Drain to Negative Supply	$V_D - V_{SS}$	33	V	
4	Drain to Source Voltage	V_{DS}	±22	V	
5	Logic to Negative Supply	$V_L - V_{SS}$	36	V	
6	Logic to Input	$V_L - V_{IN}$	8.0	V	
7	Logic to Reference	$V_L - V_{REF}$	8.0	V	
8	Input to Reference	$V_{IN} - V_{REF}$	8.0	V	
9	Reference to Negative Supply	$V_R - V_{SS}$	27	V	
10	Current (any Terminal)	I	30	mA	
11	Storage Temperature	T_{stg}	−65 to +150	°C	
12	Operating Temperature	T_{op}	−55 to +125	°C	
13	Power Dissipation	P_D	450 825	mW	Notes 1 and 3 Notes 1 and 4
14	Soldering Temperature	T_{sol}	+260	°C	Note 2

NOTES

1. Device mounted with all leads welded or soldered to printed circuit board.
2. Duration 10 seconds maximum at a distance of not less than 1.5mm from the can and the same lead shall not be resoldered until 3 minutes have elapsed.
3. TO100 package.
4. D.I.L. package.

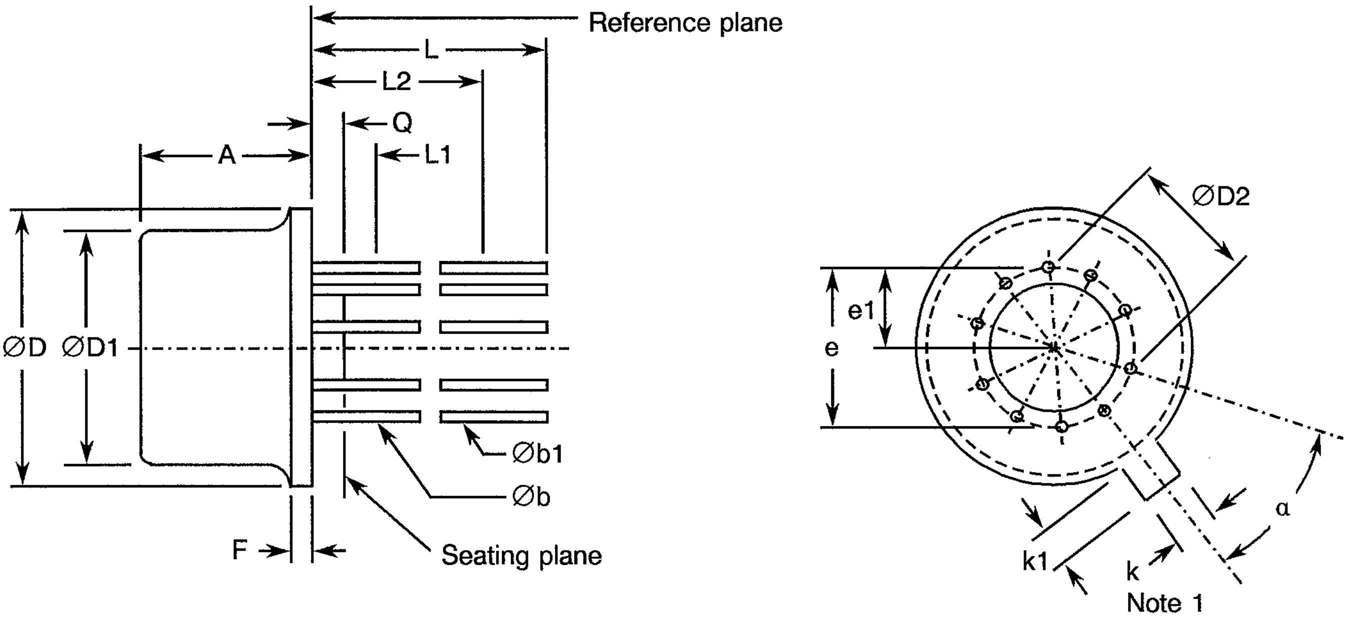
FIGURE 1 - PARAMETER DERATING INFORMATION



Device Dissipation versus Temperature

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - TO100 PACKAGE



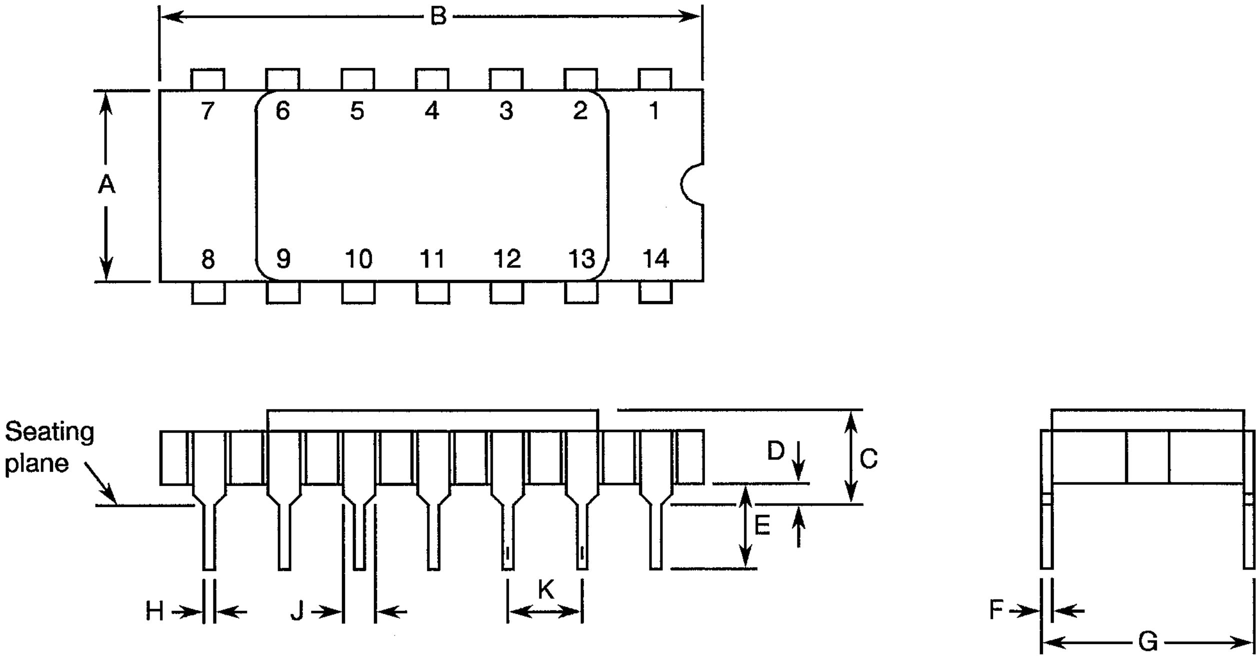
SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	4.19	4.70	
Øb	0.41	0.48	2
Øb1	0.41	0.53	2
ØD	8.51	9.40	
ØD1	7.75	8.51	
ØD2	3.56	4.06	
e	5.84 T.P.		4
e1	2.92 T.P.		4
F	-	1.02	
k	0.71	0.86	
k1	0.74	1.14	3
L	12.70	-	2
L1	-	1.27	2
L2	6.35	-	2
Q	0.25	1.02	
α	36° T.P.		4

NOTES

1. Index point shall be identified by a tab which shall correspond to Pin 10.
2. (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 12.70mm from the reference plane. Diameter is uncontrolled in L1 and beyond 12.70mm from the reference plane.
3. Measured from the maximum diameter of the product.
4. Leads having a maximum diameter 0.48mm measured 1.27mm + 0.03mm − 0.00mm below the seating plane of the product shall be within 0.18mm of their true position relative to a maximum width tab.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

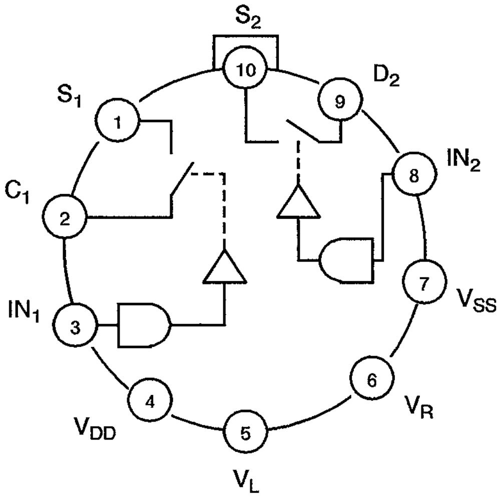
FIGURE 2(b) - D.I.L. PACKAGE



SYMBOL	MILLIMETRES	
	MIN.	MAX.
A	6.99	7.87
B	16.26	19.96
C	2.54	5.08
D	0.51	1.27
E	3.18	4.06
F	0.20	0.31
G	7.37	8.13
H	0.38	0.58
J	1.02	1.78
K	2.29	2.79

FIGURE 3(a) - PIN ASSIGNMENT

TO100 PACKAGE



D.I.L. PACKAGE

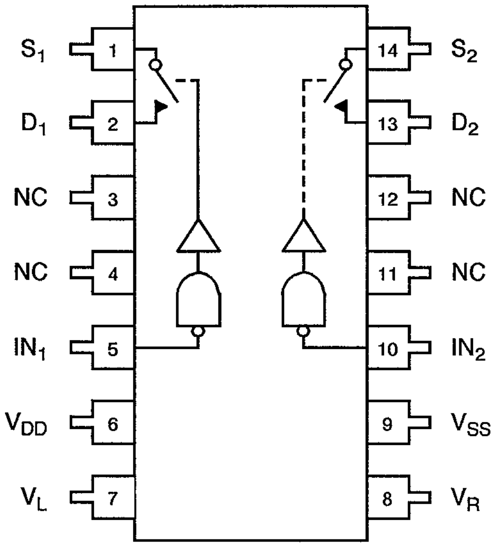


FIGURE 3(b) - CIRCUIT SCHEMATIC

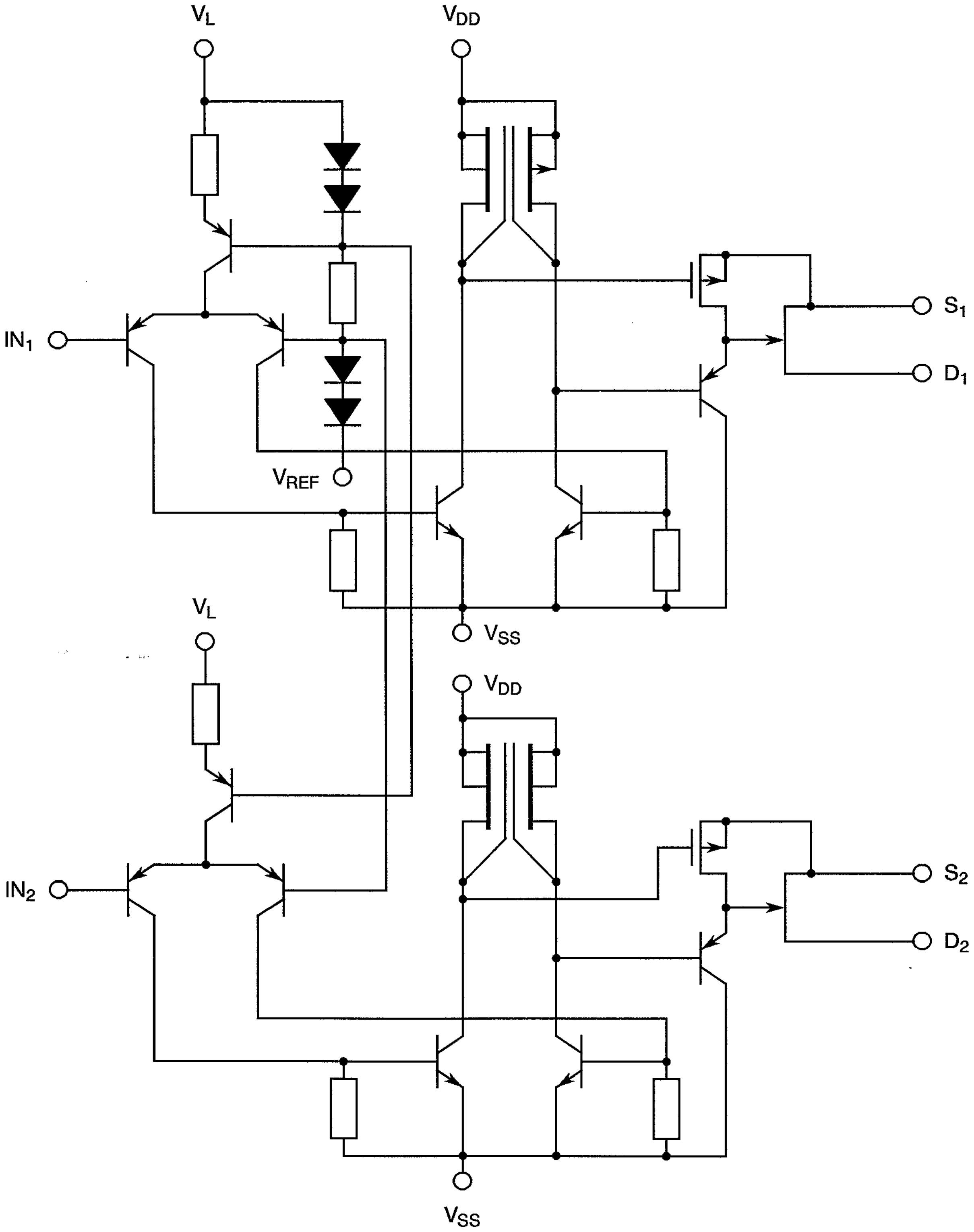
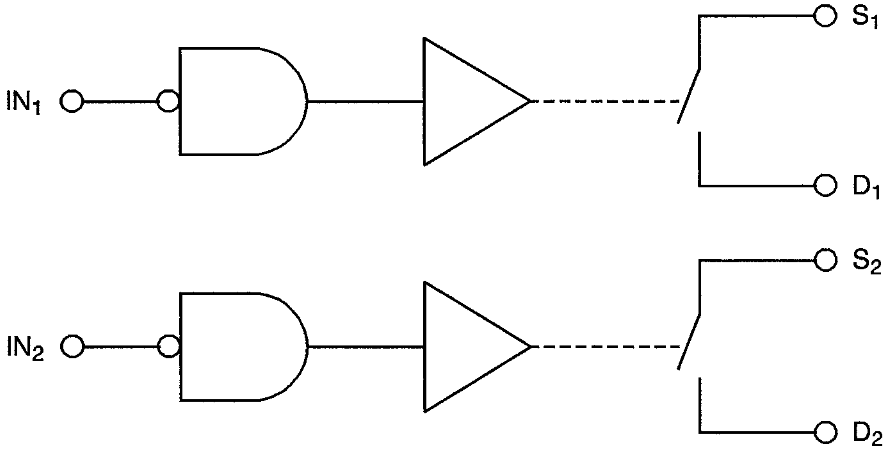


FIGURE 3(c) - FUNCTIONAL DIAGRAM



3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

V_L = Logic Voltage.
V_{DS} = Drain to Source Voltage.
V_{REF} = Reference Voltage.
$C_{D(OFF)}$ = Drain Off State Capacitance.
$C_{S(ON)}$ = Source On State Capacitance.
$r_{DS(ON)}$ = Drain Source on State Resistance.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

(a) Para. 7.7.1(a), High Temperature Reverse Bias Burn-in: Not applicable.

4.2.4 Deviations from Qualification Tests (Chart IV)

(a) The electrical measurements specified at the end of Subgroup I and II tests shall be carried out as stated in Table 2 of this specification.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

(a) The electrical measurements referenced 9.9.4 shall be performed as stated in Table 2 of this specification.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 0.15 grammes.

4.4 MATERIALS AND FINISHES

The materials shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals and the lids shall be welded, brazed or preform-soldered.

4.4.2 Lead Material and Finish

The material shall be Type 'D' with either Type '2' or Type '3 or 4' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of components delivered to this specification shall be in accordance with ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

4.5.2 Lead Identification

A tab shall be used to identify Pin 10.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:

9408001 02 B

Detail Specification Number —— 9408001

Type Variant (see Table 1(a)) —— 02

Testing Level (B or C, as applicable) —— B

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125$°C and -55°C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits and functional test sequence for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4. The circuits are considered to be for reference only.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +25 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for power burn-in shall be as specified in Table 5 of this specification.

4.7.3 Electrical Circuits for Power Burn-in

Circuits for use in performing the power burn-in tests are shown in Figure 5 of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	Characteristics	Symbol	Test Method MIL-STD		Test Fig.	Test Conditions (Note 1) (Pins Under Test)	Limits		Unit
			750	883			Min	Max	
1 to 2	Drain Source On Resistance	$r_{DS(ON)}$	3421	-	4(a)	$V_D = -7.5$, $I_S = 10mA$ $V_I = 0.8V$ (Pins 1-2, 9-10)	-	30	Ω
3 to 4	Source Off Leakage Current	$I_{S(OFF)}$	3413	-	4(b)	$V_D = -10V$, $V_S = 10V$ $V_{DD} = 10V$, $V_{SS} = -20V$ $V_I = 2.0V$ (Pins 1, 10)	-	1.0	nA
5 to 6	Source Off Leakage Current	$I_{S(OFF)}$	3413	-	4(b)	$V_D = -7.5V$, $V_S = 7.5V$ $V_I = 2.0V$ (Pins 1, 10)	-	1.0	nA
7 to 8	Drain Off Leakage Current	$I_{D(OFF)}$	3413	-	4(c)	$V_D = 10V$, $V_S = -10V$ $V_{DD} = 10V$, $V_{SS} = -20V$ $V_I = 2.0V$ (Pins 2, 9)	-	1.0	nA
9 to 10	Drain Off Leakage Current	$I_{D(OFF)}$	3413	-	4(c)	$V_D = 7.5V$, $V_S = -7.5V$ $V_I = 2.0V$ (Pins 2, 9)	-	1.0	nA
11 to 12	Channel On Leakage Current	$I_{D(ON)}$ $I_{S(ON)}$	3403	-	4(d)	$V_D = V_S = 7.5V$ $V_I = 0.8V$ (Pins 1, 10)	-	−2.0	nA
13 to 14	Input Current, Input Voltage Low	I_{IL}	-	3009	4(e)	$V_I = 0$ (Pins 3, 8)	-	−250	µA
15 to 16	Input Current, Input Voltage High	I_{IH}	-	3010	4(e)	$V_I = 5.0V$ (Pins 3, 8)	-	10	µA
17	Positive Supply Current	I_{DD}	-	3005	4(f)	Both $V_I = 0$ All channels on (Pin 4)	-	1.5	mA
18	Positive Supply Current	I_{DD}	-	3005	4(f)	Both $V_I = 5.0V$ All channels off (Pin 4)	-	1.5	mA
19	Negative Supply Current	I_{SS}	-	3005	4(g)	Both $V_I = 0$ All channels on (Pin 7)	-	−5.0	mA
20	Negative Supply Current	I_{SS}	-	3005	4(g)	Both $V_I = 5.0V$ All channels off (Pin 7)	-	−5.0	mA
21	Logic Supply Current	I_L	-	-	4(h)	Both $V_I = 0$ All channels on (Pin 5)	-	4.5	mA
22	Logic Supply Current	I_L	-	-	4(h)	Both $V_I = 5.0V$ All channels off (Pin 5)	-	4.5	mA

NOTES: See Page 17.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	Characteristics	Symbol	Test Method MIL-STD		Test Fig.	Test Conditions (Note 1) (Pins Under Test)	Limits		Unit
			750	883			Min	Max	
23	Reference Supply Current	I_R	-	-	4(i)	Both $V_I = 0$ All channels on (Pin 6)	-	-2.0	mA
24	Reference Supply Current	I_R	-	-	4(i)	Both $V_I = 5.0V$ All channels off (Pin 6)	-	-2.0	mA

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	Characteristics	Symbol	Test Method MIL-STD		Test Fig.	Test Conditions (Note 1) (Pins Under Test)	Limits		Unit
			750	883			Min	Max	
25	Turn On Time	t_{on}	-	3004	4(j)	-	-	150	ns
26	Turn Off Time	t_{off}	-	3004	4(j)	-	-	150	ns

NOTES

1. Unless otherwise noted: $V_{DD} = 15V$: $V_{SS} = -15V$
   $V_L = 5.0V$: $V_{REF} = 0$.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0−5) °C

No.	Characteristics	Symbol	Test Method MIL-STD		Test Fig.	Test Conditions (Note 1) (Pins Under Test)	Limits		Unit
			750	883			Min	Max	
1 to 2	Drain Source On Resistance	$r_{DS(ON)}$	3421	-	4(a)	$V_D = -7.5$, $I_S = 10mA$ $V_I = 0.8V$ (Pins 1-2, 9-10)	-	60	Ω
3 to 4	Source Off Leakage Current	$I_{S(OFF)}$	3413	-	4(b)	$V_D = -10V$, $V_S = 10V$ $V_{DD} = -10V$, $V_{SS} = 20V$ $V_I = 2.0V$ (Pins 1, 10)	-	100	nA
5 to 6	Source Off Leakage Current	$I_{S(OFF)}$	3413	-	4(b)	$V_D = -7.5V$, $V_S = 7.5V$ $V_I = 2.0V$ (Pins 1, 10)	-	100	nA
7 to 8	Drain Off Leakage Current	$I_{D(OFF)}$	3413	-	4(c)	$V_D = 10V$, $V_S = -10V$ $V_{DD} = 10V$, $V_{SS} = -20V$ $I_N = 2.0V$ (Pins 2, 9)	-	100	nA
9 to 10	Drain Off Leakage Current	$I_{D(OFF)}$	3413	-	4(c)	$V_D = 7.5V$, $V_S = -7.5V$ $V_I = 2.0V$ (Pins 2, 9)	-	100	nA
11 to 12	Channel On Leakage Current	$I_{D(ON)}$ $I_{S(ON)}$	3403	-	4(d)	$V_D = V_S = -7.5V$ $V_I = 0.8V$ (Pins 1, 10)	-	−200	nA
13 to 14	Input Current, Input Voltage Low	I_{IL}	-	3009	4(e)	$V_I = 0$ (Pins 3, 8)	-	−250	µA
15 to 16	Input Current, Input Voltage High	I_{IH}	-	3010	4(e)	$V_I = 5.0V$ (Pins 3, 8)	-	20	µA

NOTES: See Page 17.

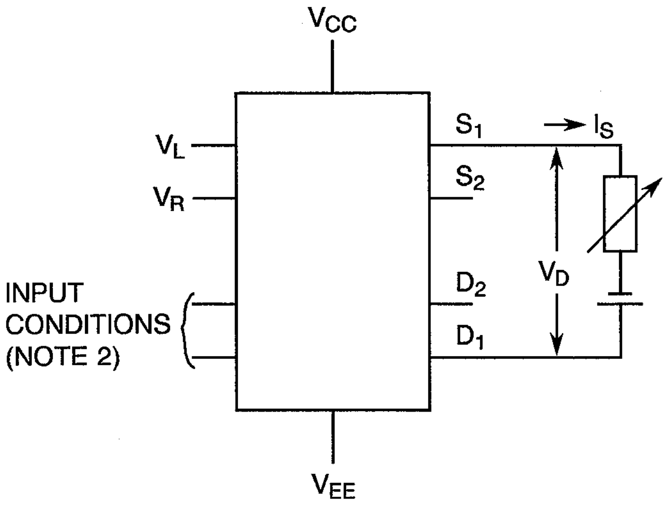
TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, −55(+5−0) °C

No.	Characteristics	Symbol	Test Method MIL-STD		Test Fig.	Test Conditions (Note 1) (Pins Under Test)	Limits		Unit
			750	883			Min	Max	
1 to 2	Drain Source On Resistance	$r_{DS(ON)}$	3421	-	4(a)	$V_D = -7.5$, $I_S = 10mA$ $V_I = 0.8V$ (Pins 1-2, 9-10)	-	30	Ω
13 to 14	Input Current, Input Voltage Low	I_{IL}	-	3009	4(e)	$V_I = 0$	-	−250	µA

NOTES: See Page 17.

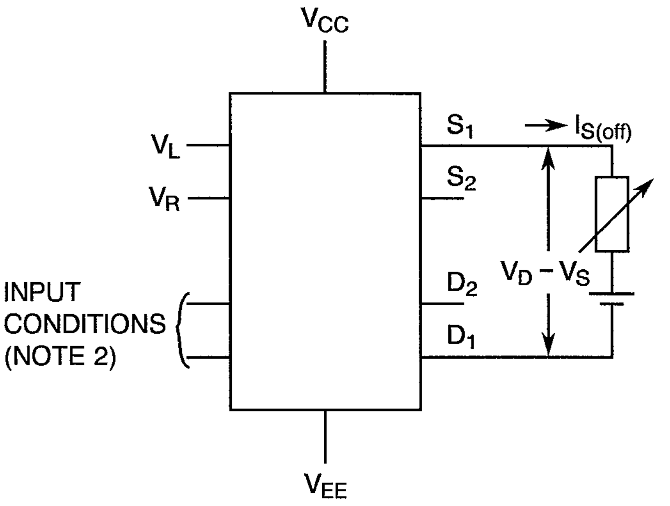
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - DRAIN SOURCE ON RESISTANCE



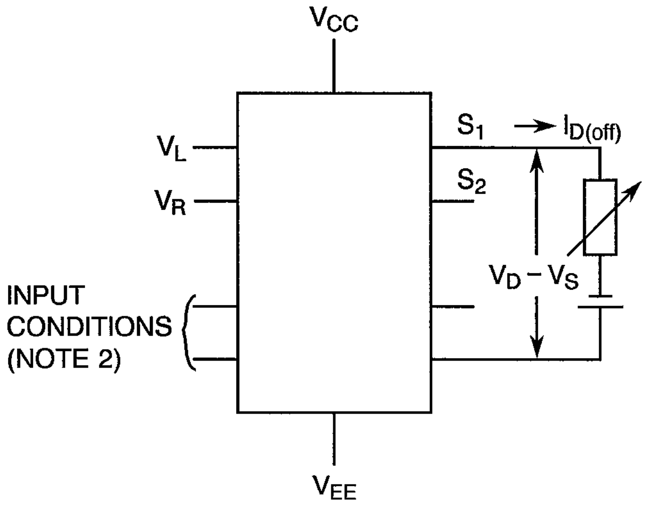
NOTES
1. Each input to be tested separately.
2. Both inputs low.

FIGURE 4(b) - SOURCE OFF LEAKAGE CURRENT



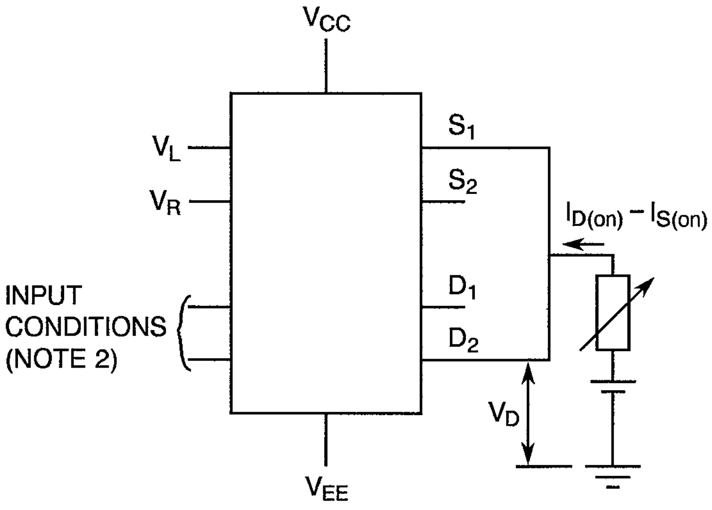
NOTES
1. Each channel to be tested separately.
2. Both inputs high.

FIGURE 4(c) - DRAIN OFF LEAKAGE CURRENT



NOTES
1. Each channel to be tested separately.
2. Both inputs high.

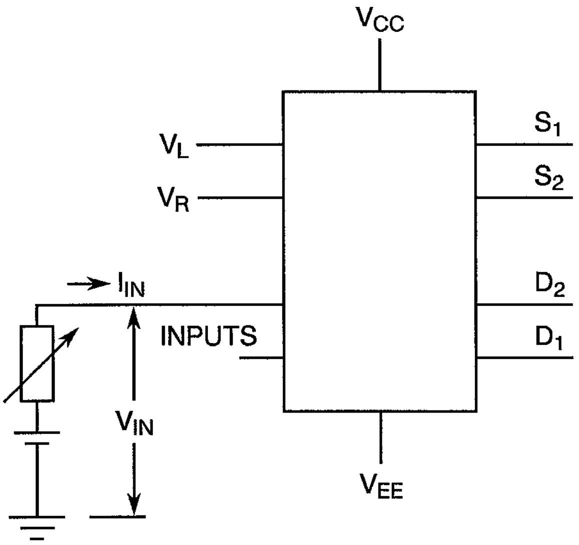
FIGURE 4(d) - CHANNEL ON LEAKAGE CURRENT



NOTES
1. Each channel to be tested separately.
2. Both inputs low.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

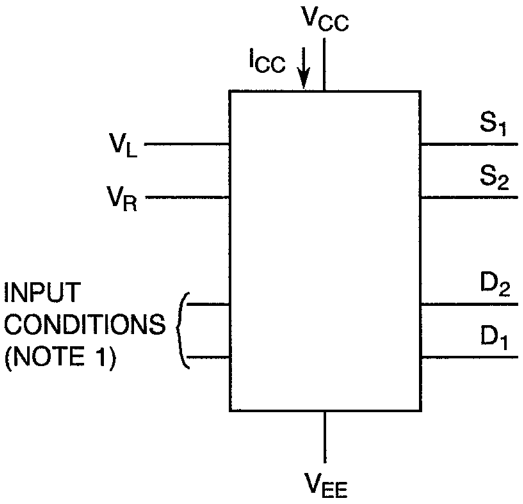
FIGURE 4(e) - INPUT CURRENT, INPUT VOLTAGE LOW AND INPUT CURRENT, INPUT VOLTAGE HIGH



NOTES

1. Each channel to be tested separately.

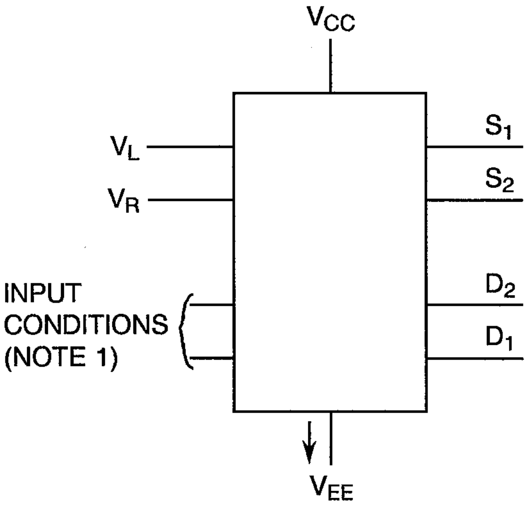
FIGURE 4(f) - COLLECTOR SUPPLY CURRENT



NOTES

1. Both inputs low.

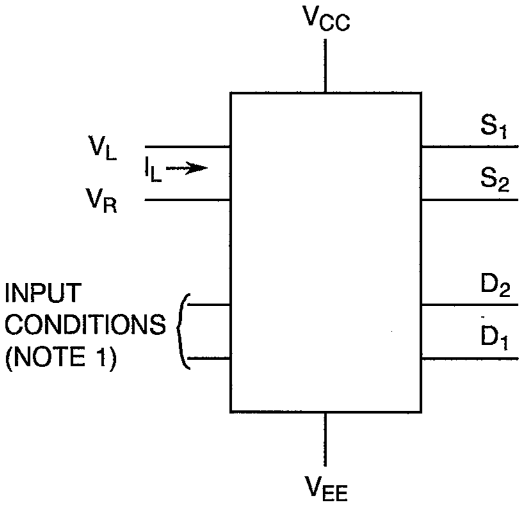
FIGURE 4(g) - EMITTER SUPPLY CURRENT



NOTES

1. Both inputs low.

FIGURE 4(h) - LOGIC SUPPLY

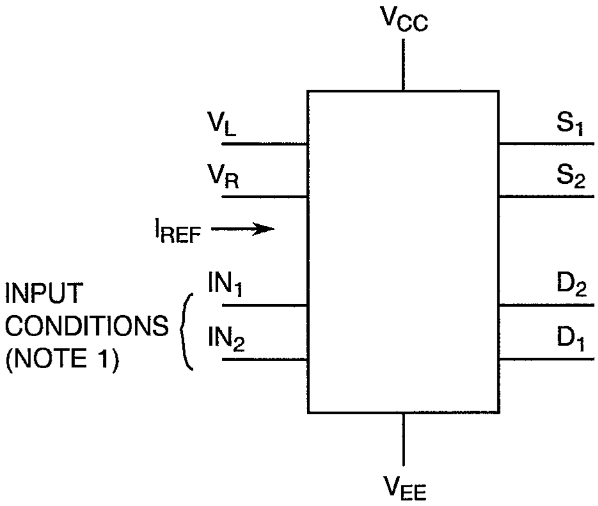


NOTES

1. Both inputs low.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - REFERENCE SUPPLY CURRENT

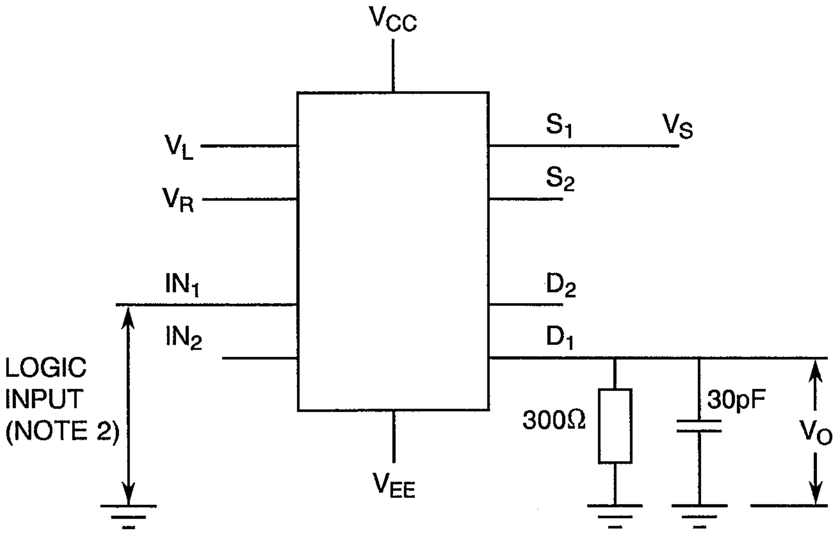


NOTES

1. Both inputs low.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(j) - DYNAMIC TEST AND SWITCHING WAVEFORMS



NOTES

1. Each switch to be tested separately.

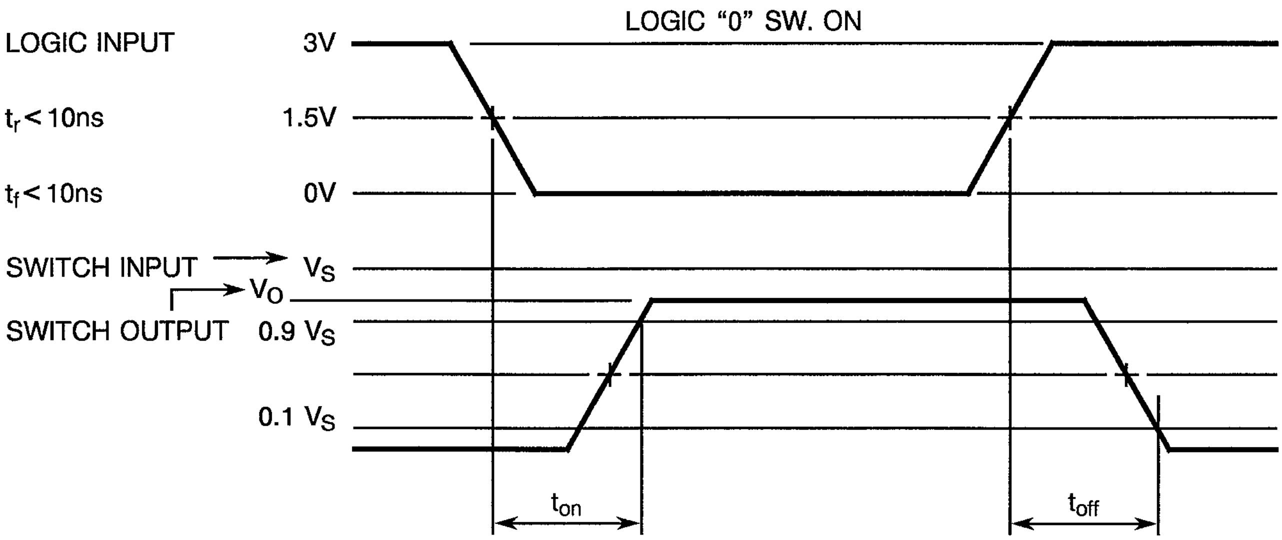


TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
1 to 2	Drain Source On Resistance	$r_{DS(on)}$	As per Table 2	As per Table 2	±3.0	Ω
3 to 4	Source Off Leakage Current	$I_{S(off)}$	As per Table 2	As per Table 2	±0.5	nA
7 to 8	Drain Off Leakage Current	$I_{D(off)}$	As per Table 2	As per Table 2	±0.5	nA

TABLE 5 - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0−5)	°C
2	Power Supply Voltage	V_{DD} V_{SS}	+15 −15	V
3	Logic Voltage	V_L	5.0	V

FIGURE 5 - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS - TO100 CASE

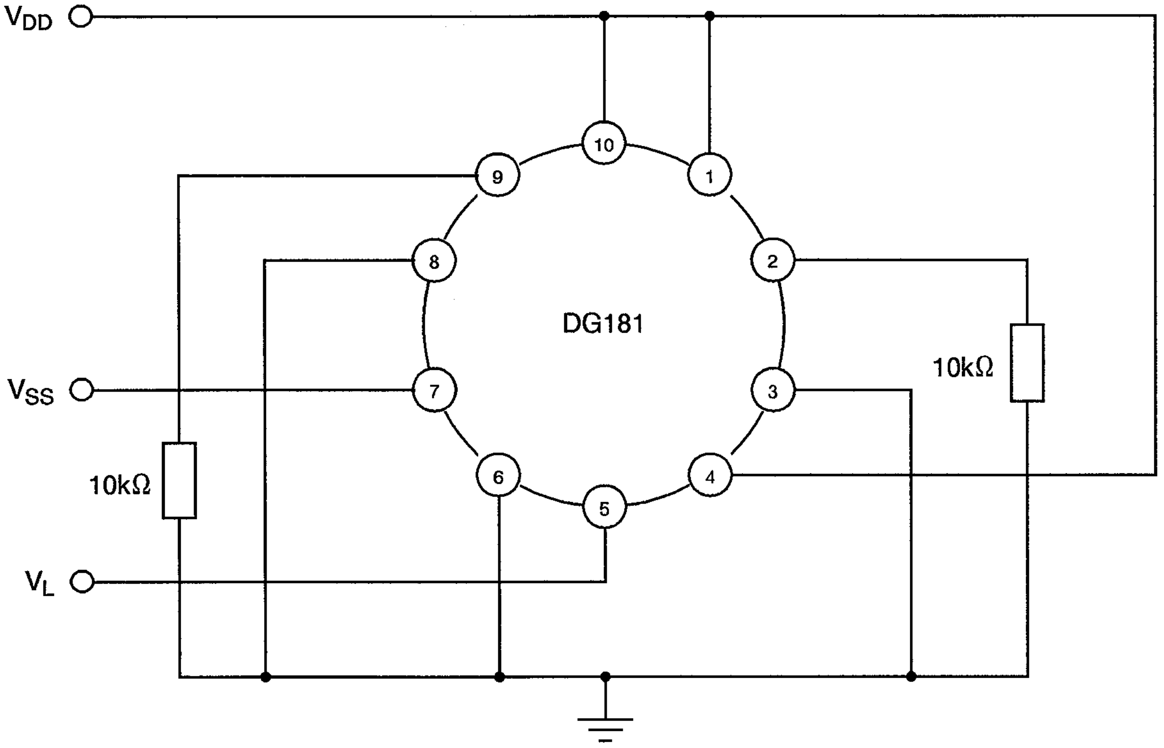
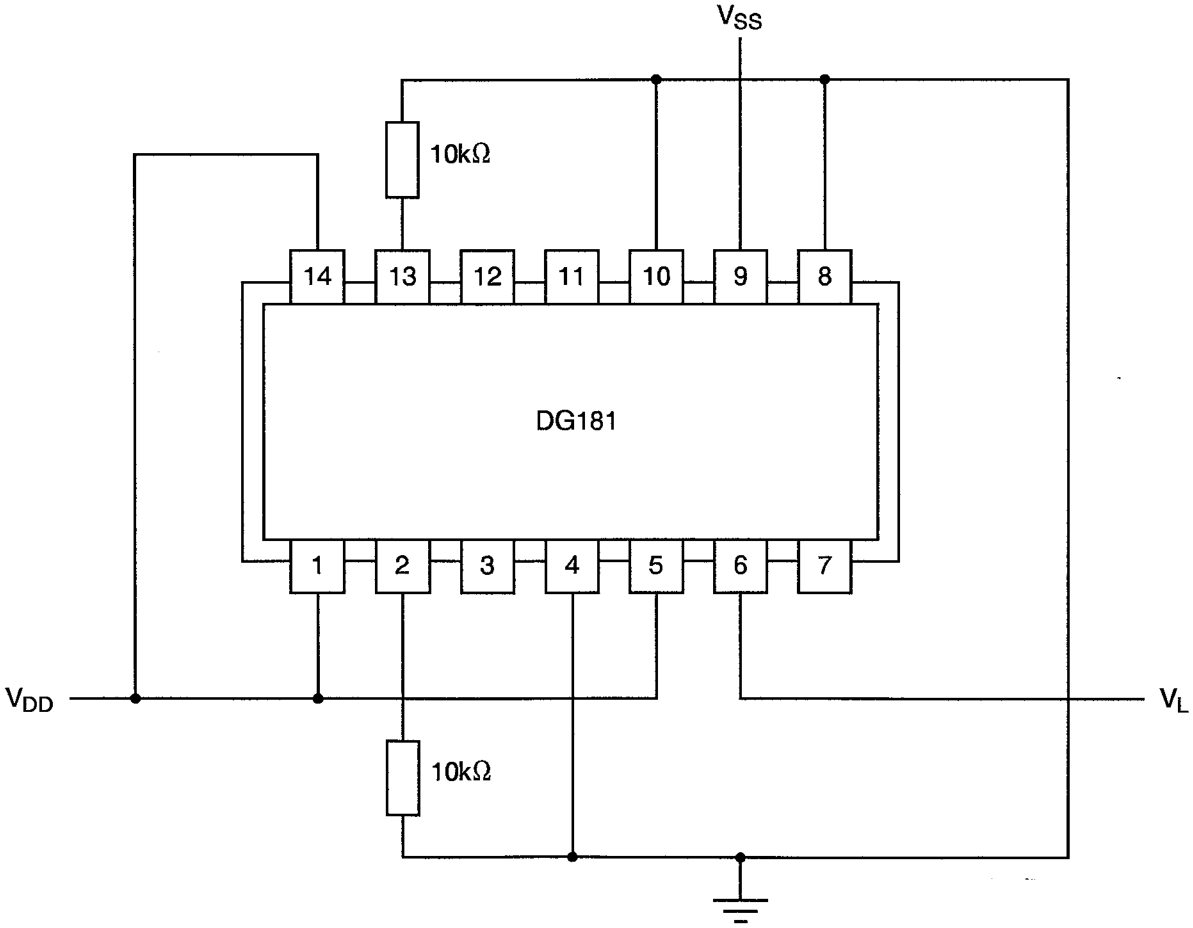


FIGURE 5 - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS - D.I.L. CASE



4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 2. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests (Part of Endurance Testing)

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5 of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5.

4.8.6 Conditions for High Temperature Storage Test (Part of Endurance Testing)

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The conditions for high temperature storage shall be $T_{amb} = +150(+0-5)$ °C.

TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
1 to 2	Drain Source On Resistance	$r_{DS(on)}$	As per Table 2	As per Table 2	-	30	Ω
3 to 4	Source Off Leakage Current	$I_{S(off)}$	As per Table 2	As per Table 2	-	1.0	nA
7 to 8	Drain Off Leakage Current	$I_{D(off)}$	As per Table 2	As per Table 2	-	1.0	nA