INTEGRATED CIRCUITS, DUAL 8-CHANNEL CMOS

ANALOGUE MULTIPLEXER,

BASED ON TYPE HI-507A

ESCC Detail Specification No. 9408/003

ISSUE 1

October 2002

Document Custodian: European Space Agency - see https://escies.org

european space agency
agence spatiale européenne

Pages 1 to 42

INTEGRATED CIRCUITS, DUAL 8-CHANNEL CMOS

ANALOGUE MULTIPLEXER,

BASED ON TYPE HI-507A

ESA/SCC Detail Specification No. 9408/003

space components
coordination group

Issue/Rev.	Date	Approved by	
		SCCG Chairman	ESA Director General or his Deputy
Issue 2	February 1999		

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE Reference	CHANGE Item	Approved DCR No.
		This Issue supersedes Issue 1 and incorporates all changes agreed in the following DCRs:-		
		Cover page		None
		DCN		None
		Table 1(a)	: Lead Finish column heading and entries amended	21025
		Para. 2	: Item "(c)" deleted and all subsequent items renumbered	21025
		Para. 4.2.2	: Deviation "(b)" deleted	21048
		Para. 4.2.3	: Deviation deleted and "None" added	23496
		Para. 4.2.4	: "None" deleted and Deviation "(a)" added	22919
		Para. 4.2.5	: "None" deleted and Deviation "(a)" added	22919
		Para. 4.4.2	: Existing text deleted and new text added	21025
		Para. 4.5.3	: Type Variant entry amended	21025
		Para. 4.7.1	: Second alinea added	23496
		Table 5(a)	: "N-Channels" added to Title	23496
			: Duration added to Table	23496
		Table 5(b)	: "P-Channels" added to Title	23496
			: Duration added to Table	23496
		Figure 5(a)	: "N-Channels" added to Title	23496
		Figure 5(b)	: "P-Channels" added to Title	23496

TABLE OF CONTENTS

		Page
1.	**GENERAL**	**5**
1.1	Scope	5
1.2	Component Type Variants	5
1.3	Maximum Ratings	5
1.4	Parameter Derating Information	5
1.5	Physical Dimensions	5
1.6	Pin Assignment	5
1.7	Truth Table	5
1.8	Circuit Schematic	5
1.9	Functional Diagram	5
1.10	Handling Precautions	5
2.	**APPLICABLE DOCUMENTS**	**5**
3.	**TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS**	**14**
4.	**REQUIREMENTS**	**14**
4.1	General	14
4.2	Deviations from Generic Specification	14
4.2.1	Deviations from Special In-Process Controls	14
4.2.2	Deviations from Final Production Tests	14
4.2.3	Deviations from Burn-in and Electrical Measurements	14
4.2.4	Deviations from Qualification Tests	14
4.2.5	Deviations from Lot Acceptance Tests	14
4.3	Mechanical Requirements	15
4.3.1	Dimension Check	15
4.3.2	Weight	15
4.4	Materials and Finishes	15
4.4.1	Case	15
4.4.2	Lead Material and Finish	15
4.5	Marking	15
4.5.1	General	15
4.5.2	Lead Identification	15
4.5.3	The SCC Component Number	15
4.5.4	Traceability Information	16
4.6	Electrical Measurements	16
4.6.1	Electrical Measurements at Room Temperature	16
4.6.2	Electrical Measurements at High and Low Temperatures	16
4.6.3	Circuits for Electrical Measurements	16
4.7	Burn-in Tests	16
4.7.1	Parameter Drift Values	16
4.7.2	Conditions for High Temperature Reverse Bias and Dynamic Burn-in	16
4.7.3	Electrical Circuits for High Temperature Reverse Bias and Dynamic Burn-in	16
4.8	Environmental and Endurance Tests	40
4.8.1	Electrical Measurements on Completion of Environmental Tests	40
4.8.2	Electrical Measurements at Intermediate Points during Endurance Tests	40
4.8.3	Electrical Measurements on Completion of Endurance Tests	40
4.8.4	Conditions for Operating Life Tests	40
4.8.5	Electrical Circuits for Operating Life Tests	40
4.8.6	Conditions for High Temperature Storage Test	40

Page

TABLES

1(a)	Type Variants	6
1(b)	Maximum Ratings	6
2	Electrical Measurements at Room Temperature - d.c. Parameters	17
	Electrical Measurements at Room Temperature - a.c. Parameters	21
3	Electrical Measurements at High and Low Temperatures	23
4	Parameter Drift Values	35
5(a)	Conditions for Burn-in High Temperature Reverse Bias, N-Channels	36
5(b)	Conditions for Burn-in High Temperature Reverse Bias, P-Channels	36
5(c)	Conditions for Burn-in, Dynamic and Operating Life Tests	37
6	Electrical Measurements at Intermediate Points and on Completion of Endurance Testing	41

FIGURES

1	Parameter Derating Information	7
2	Physical Dimensions	8
3(a)	Pin Assignment	9
3(b)	Decode Truth Table	9
3(c)	Circuit Schematic - Address Decoder	10
3(d)	Circuit Schematic - Address Input Buffer and Level Shifter	11
3(e)	Circuit Schematic - Multiplex Switch	12
3(f)	Functional Diagram	13
4	Circuits for Electrical Measurements	27
5(a)	Electrical Circuit for High Temperature Reverse Bias, N-Channels	38
5(b)	Electrical Circuit for High Temperature Reverse Bias, P-Channels	38
5(c)	Electrical Circuit for Burn-in, Dynamic and Operating Life Tests	39

APPENDICES (Applicable to specific Manufacturers only)

'A'	Agreed Deviations for Harris (US)	42

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a dual 8-channel, CMOS Analogue Multiplexer, based on Type HI-507A. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

As per Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the integrated circuits specified herein are shown in Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

As per Figure 3(b).

1.8 CIRCUIT SCHEMATIC

As per Figures 3(c), 3(d) and 3(e).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(f).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be taken for protection during all phases of manufacture, testing, packaging, shipment and any handling.

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

(c) MIL-STD-750, Test Methods for Semiconductor Devices.

(d) MIL-M-38510, Microcircuits, General Specification for.

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND FINISH
01	D.I.L	2	D2
02	D.I.L	2	D3 or D4

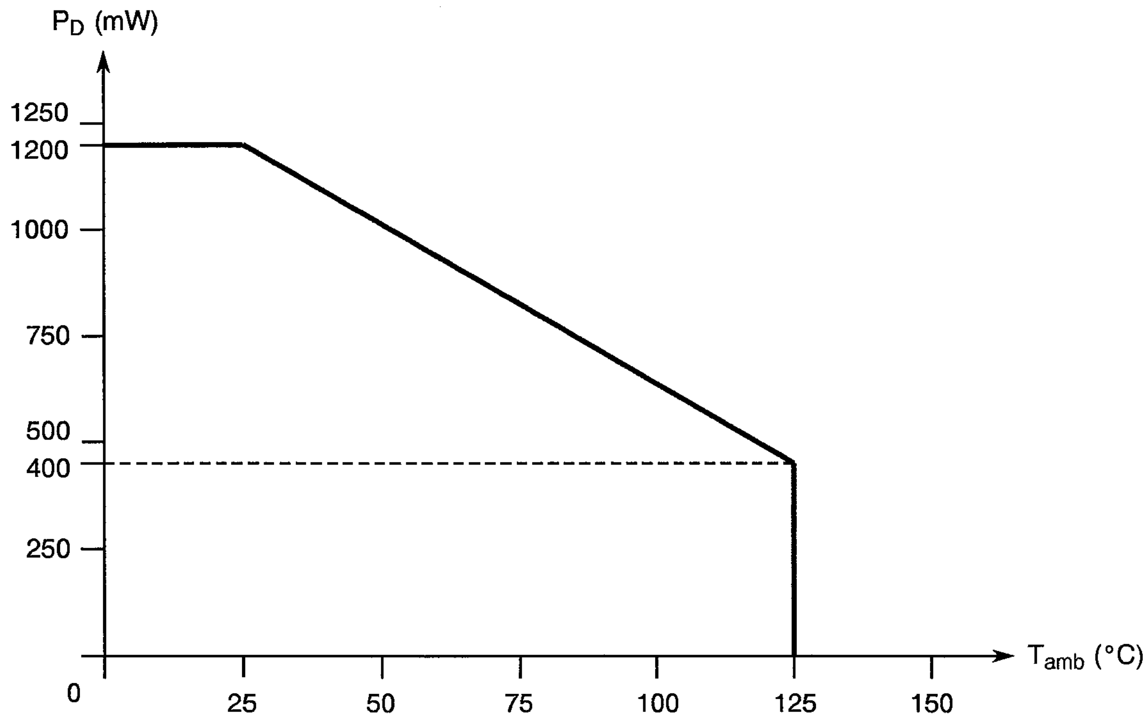
TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNITS	REMARKS
1	Supply Voltage	V_{DD} V_{SS}	+20 -20	V	
2	Power Dissipation	P_D	1200	mW	Note 1
3	Digital Input Overvoltage	V_{IN}	V_{DD} +4.0 V_{SS} -4.0	V	
4	Channel Input Overvoltage	V_{IN}	V_{DD} +20 V_{SS} -20	V	
5	Operating Temperature Range	T_{op}	-55 to +125	°C	
6	Storage Temperature Range	T_{stg}	-65 to +150	°C	
7	Reference Voltage to Ground	V_{REF}	20	V	
8	Soldering Temperature	T_{sol}	265	°C	Note 2

NOTES

1. At +25°C. For "derating with temperature", see Figure 1.
2. Duration 10 seconds maximum at a distance of not less than 1.5mm from the can and the same lead shall not be resoldered until 3 minutes have elapsed.

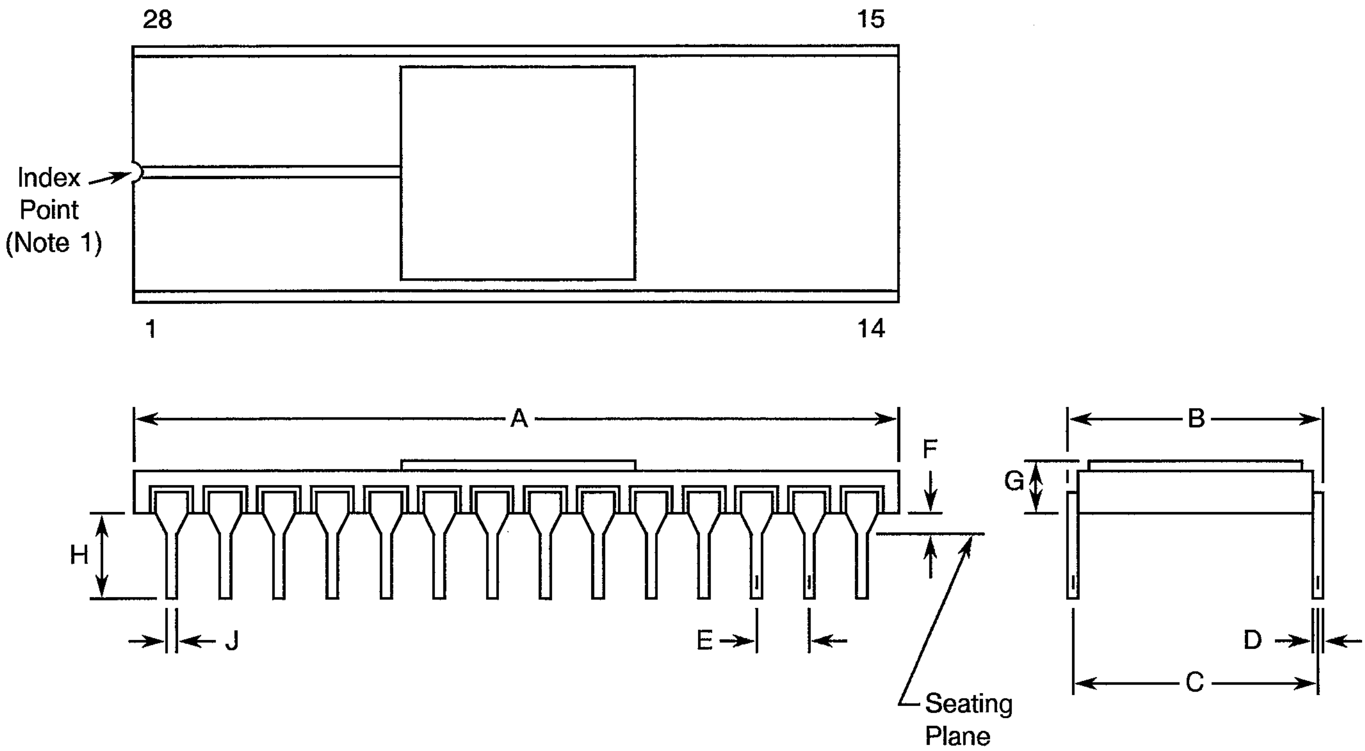
FIGURE 1 - PARAMETER DERATING INFORMATION



Device Dissipation versus Temperature

FIGURE 2 - PHYSICAL DIMENSIONS

DUAL-IN-LINE PACKAGE



SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	32.05	36.07	
B	-	15.49	
C	15.11	15.37	
D	0.20	0.30	
E	2.41	2.67	2
F	0.38	1.14	
G	1.91	2.67	
H	3.94	4.70	
J	0.41	0.51	

NOTES
1. A notch, as shown, shall be used for pin identification.
2. Non-accumulating

FIGURE 3(a) - PIN ASSIGNMENT

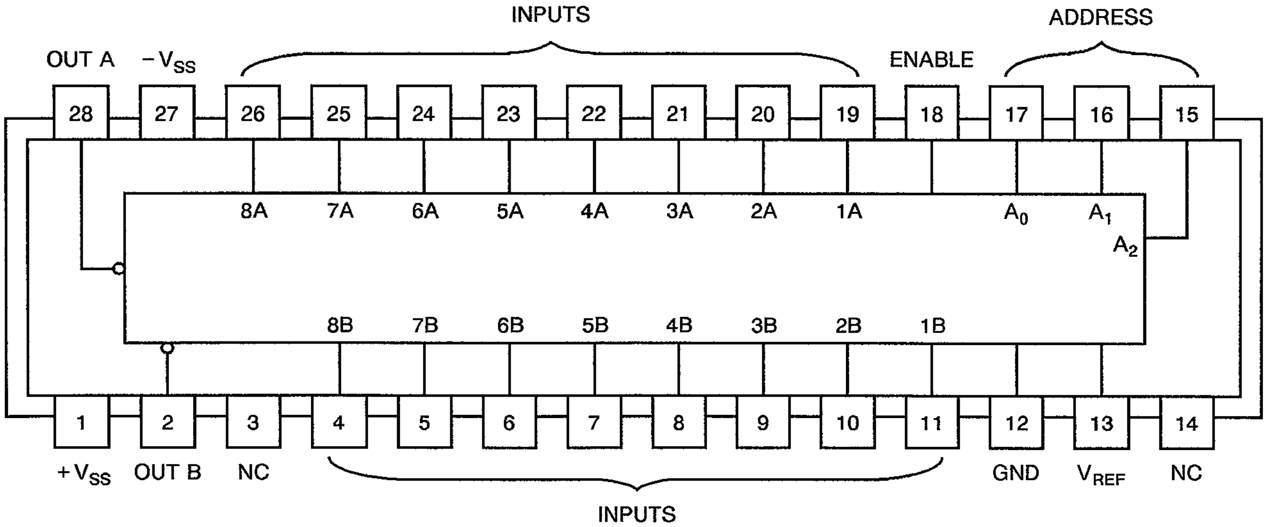


FIGURE 3(b) - TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

FIGURE 3(c) - CIRCUIT SCHEMATIC - ADDRESS DECODER

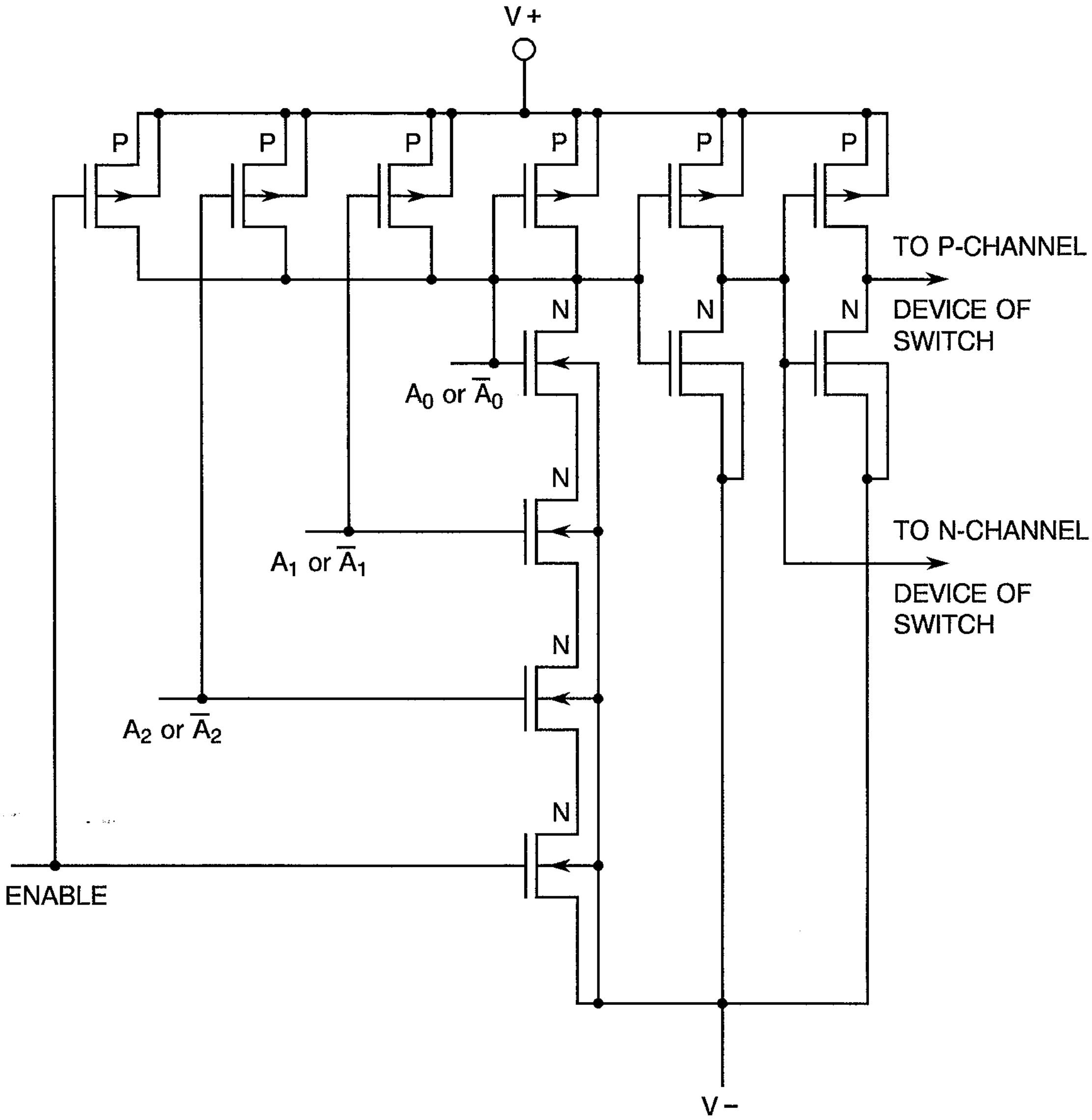


FIGURE 3(d) - CIRCUIT SCHEMATIC - ADDRESS INPUT BUFFER AND LEVEL SHIFTER

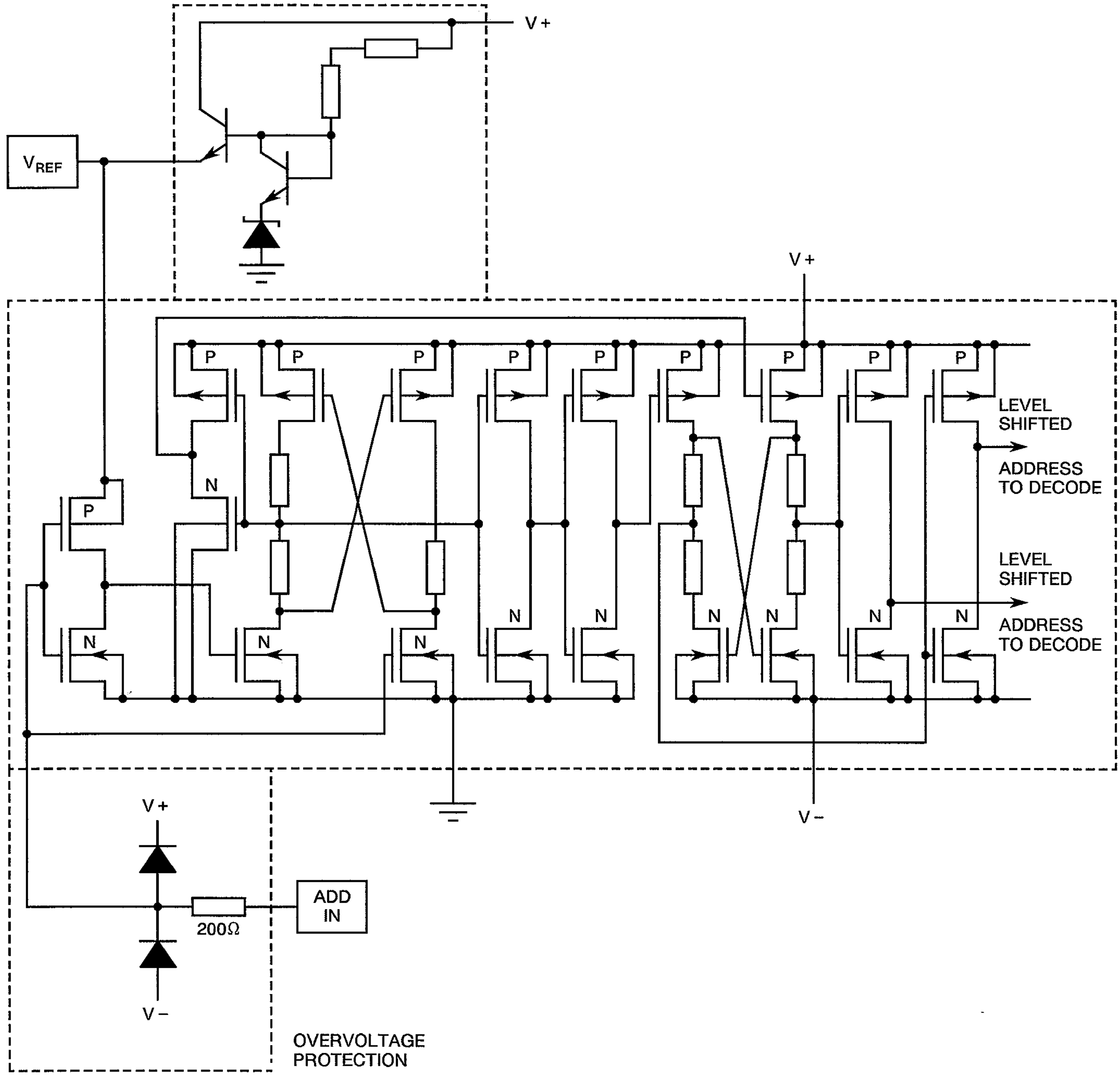


FIGURE 3(e) - CIRCUIT SCHEMATIC - MULTIPLEX SWITCH

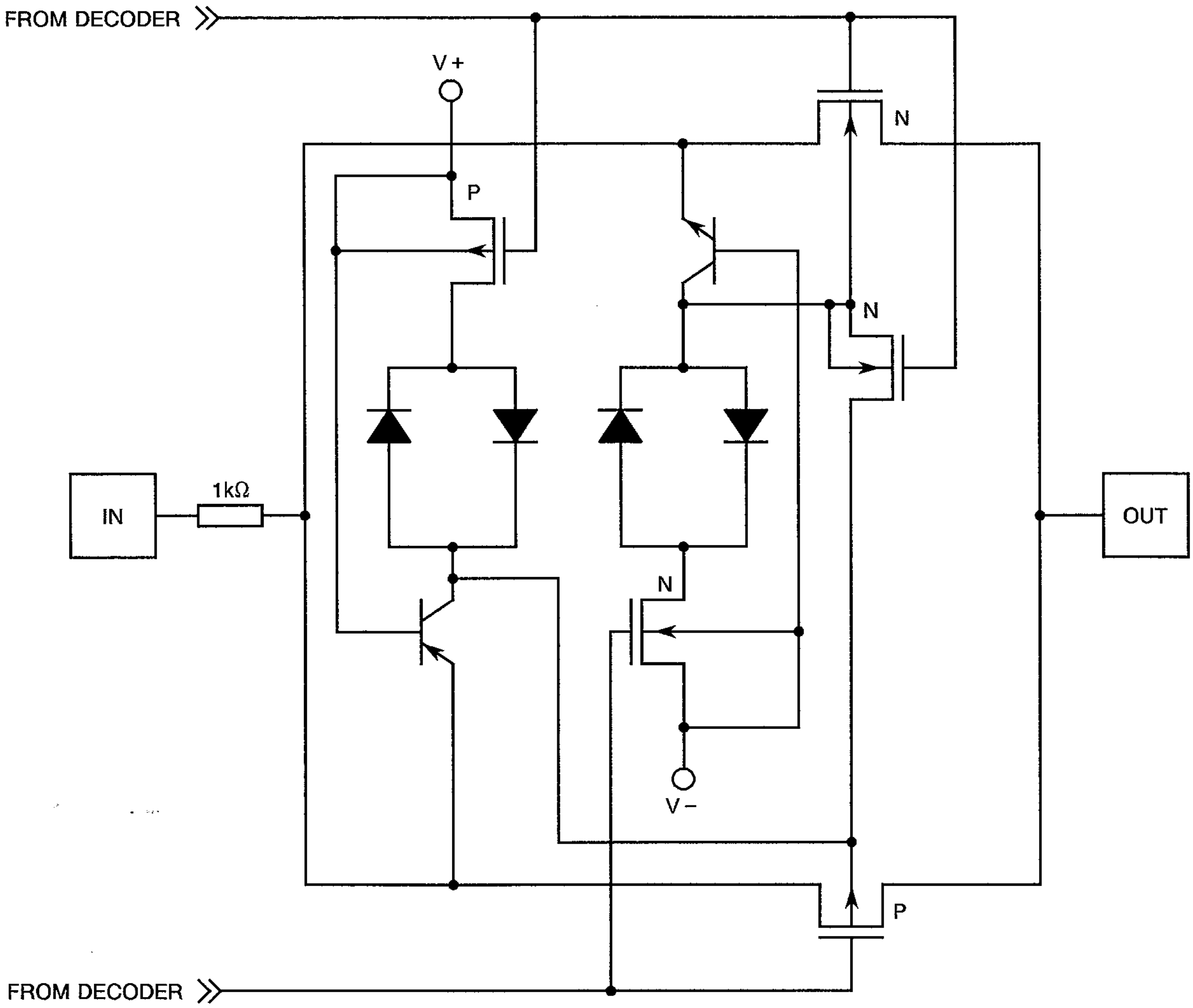
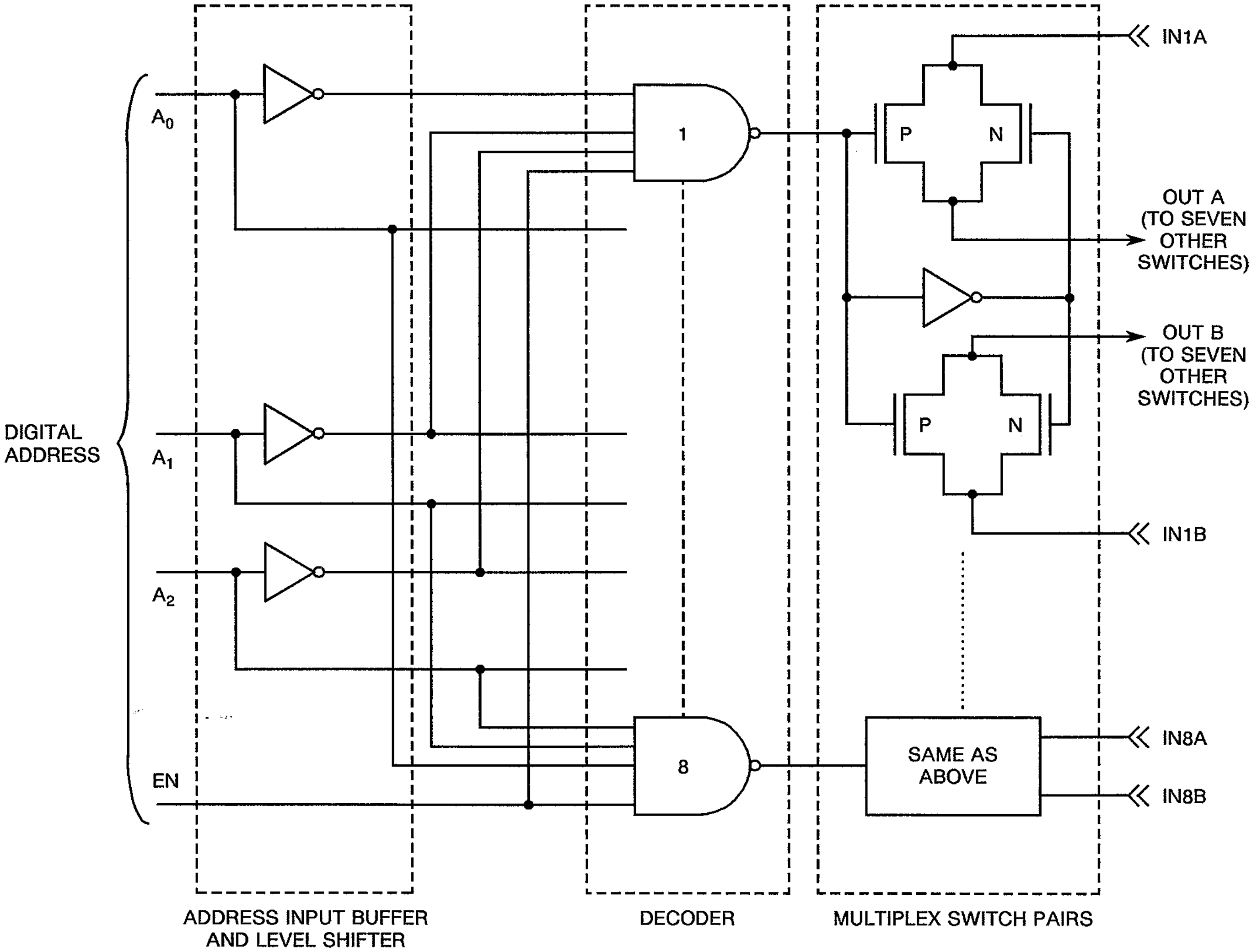


FIGURE 3(f) - FUNCTIONAL DIAGRAM



REPEATED TWICE

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

I_{OFF} = Channel "Off" Leakage Current.
I_{ON} = Channel "On" Leakage Current.
R_{ON} = Channel "On" Resistance.
t_{open} = Break-before-make Delay.
C_{INC} = Channel "Off" Input Capacitance.
C_{OC} = Channel "Off" Output Capacitance.
C_{IN} = Input Capacitance Address or Enable.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

(a) The following test shall be added to the chart after "Bond Strength Test" (Para. 9.2.1):-
"Die-shear Test: In accordance with Method 2019 of MIL-STD-883. The sample size shall be 3 devices with no failures permitted."

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

None.

4.2.4 Deviations from Qualification Tests (Chart IV)

(a) The electrical measurements specified at the end of Subgroup I and II tests shall be carried out as stated in Table 2 of this specification.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

(a) The electrical measurements referenced 9.9.4 shall be performed as stated in Table 2 of this specification.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 3.0 grammes.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body with side-brazed leads and a gold-plated lid.

4.4.2 Lead Material and Finish

The material shall be Type 'D' with either Type '2' or Type '3 or 4' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of components delivered to this specification shall be in accordance with ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

4.5.2 Lead Identification

An index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering shall be read with the index or tab on the left-hand side.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:

9408003 02 B

Detail Specification Number — 9408003

Type Variant (see Table 1(a)) — 02

Testing Level (B or C, as applicable) — B

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Tables 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ °C and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits and functional test sequence for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

For high temperature reverse bias burn-in, the parameter drift values (Δ) shall be applied before the N-Channel (0 hours) and after the P-Channel (144 hours) burn-in.

4.7.2 Conditions for High Temperature Reverse Bias and Dynamic Burn-in

The requirements for H.T.R.B. and dynamic burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for H.T.R.B. and dynamic burn-in shall be as specified in Tables 5(a), 5(b) and 5(c).

4.7.3 Electrical Circuits for High Temperature Reverse Bias and Dynamic Burn-in

Circuits for use in performing the H.T.R.B. and dynamic burn-in tests are shown in Figures 5(a), 5(b) and 5(c).

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	Characteristics	Symbol	MIL-STD-883 Test Method	Test Fig.	Test Conditions (Pins Under Test)	Limits Min	Limits Max	Unit
1	Functional Test	-	3005	3(b)	Verify Truth Table. $V_{DD} = 15V$, $V_{SS} = -15V$ V_{REF} = Open Note 1	-	-	mA
2	Quiescent Current (Positive)	I_{DD1}	3005	4(a)	V_{IN} (enable) = 4.0V V_{IN} (address) = 0.8V V_{IN} (all channels) = 0V $V_{DD} = 15V$, $V_{SS} = -15V$ V_{REF} = Open (Pin 1)	-	2.0	mA
3	Quiescent Current (Negative)	I_{SS1}	3005	4(a)	V_{IN} (enable) = 4.0V V_{IN} (address) = 0.8V V_{IN} (all channels) = 0V $V_{DD} = 15V$, $V_{SS} = -15V$ V_{REF} = Open (Pin 27)	−1.0	-	mA
4	Quiescent Standby Current (Positive)	I_{DD2}	3005	4(a)	V_{IN} (enable) = 0.8V V_{IN} (address) = 0.8V V_{IN} (all channels) = 0V $V_{DD} = 15V$, $V_{SS} = -15V$ V_{REF} = Open (Pin 1)	-	2.0	mA
5	Quiescent Standby Current (Negative)	I_{SS2}	3005	4(a)	V_{IN} (enable) = 0.8V V_{IN} (address) = 0.8V V_{IN} (all channels) = 0V $V_{DD} = 15V$, $V_{SS} = -15V$ V_{REF} = Open (Pin 27)	−1.0	-	mA
6 to 9	Input Current, Low Level Address or Enable	I_{IL}	3009	4(b)	V_{IN} (under test) = 0.8V V_{IN} (other inputs) = 15V $V_{DD} = 15V$, $V_{SS} = -15V$ V_{REF} = Open (Pins 15-16-17-18)	-	500	nA
10 to 13	Input Current, High Level Address or Enable	I_{IH}	3010	4(c)	V_{IN} (under test) = 4.0V V_{IN} (other inputs) = 0V $V_{DD} = 15V$, $V_{SS} = -15V$ V_{REF} = Open (Pins 15-16-17-18)	-	500	nA

NOTES: See Page 22.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	Characteristics	Symbol	MIL-STD-883 Test Method	Test Fig.	Test Conditions (Pins Under Test)	Limits Min	Limits Max	Unit
14 to 29	Channel "Off" Input Leakage Current (any Channel)	I_{OFF1}	-	4(d)	V_{IN} (enable) = 0.8V Address Inputs: V_{IL} = 0.8V, V_{IH} = 4.0V Channel Input Conditions: V_{IN} (under test) = 10V V_{IN} (other inputs) = − 10V V_{DD} = 15V, V_{SS} = − 15V V_{REF} = Open (Pins 4-2, 5-2, 6-2, 7-2, 8-2, 9-2, 10-2, 11-2, 19-28, 20-28, 21-28, 22-28, 23-28, 24-28, 25-28, 26-28)	-	10	nA
30 to 45	Channel "Off" Input Leakage Current (any Channel)	I_{OFF2}	-	4(d)	V_{IN} (enable) = 0.8V Address Inputs: V_{IL} = 0.8V, V_{IH} = 4.0V Channel Input Conditions: V_{IN} (under test) = − 10V V_{IN} (other inputs) = 10V V_{DD} = 15V, V_{SS} = − 15V V_{REF} = Open (Pins 4-2, 5-2, 6-2, 7-2, 8-2, 9-2, 10-2, 11-2, 19-28, 20-28, 21-28, 22-28, 23-28, 24-28, 25-28, 26-28)	-	10	nA
46 to 47	Channel "Off" Output Leakage Current (all Channels)	I_{OFF3}	-	4(e)	V_{IN} (address and enable) = 0.8V Channel Input Conditions: V_{IN} (under test) = − 10V V_{IN} (all inputs) = 10V V_{DD} = 15V, V_{SS} = − 15V V_{REF} = Open (Pins 2 to 4 thru 11, 28 to 19 thru 26)	-	10	nA
48 to 49	Channel "Off" Output Leakage Current (all Channels)	I_{OFF4}	-	4(e)	V_{IN} (address and enable) = 0.8V Channel Input Conditions: V_{IN} (under test) = 10V V_{IN} (all inputs) = − 10V V_{DD} = 15V, V_{SS} = − 15V V_{REF} = Open (Pins 2 to 4 thru 11, 28 to 19 thru 26)	-	10	nA

NOTES: See Page 22.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	Characteristics	Symbol	MIL-STD-883 Test Method	Test Fig.	Test Conditions (Pins Under Test)	Limits		Unit
						Min	Max	
50 to 65	Channel "Off" Output Leakage Current (Overvoltage Applied) (any Channel)	I_{OFF5}	-	4(f)	V_{IN} (enable) = 0.8V Address Inputs: V_{IL} = 0.8V, V_{IH} = 4.0V Channel Input Conditions: V_{IN} (under test) = 33V V_{OUT} (A or B) = 0V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open (Pins 4-2, 5-2, 6-2, 7-2, 8-2, 9-2, 10-2, 11-2, 19-28, 20-28, 21-28, 22-28, 23-28, 24-28, 25-28, 26-28)	-	2.0	A
66 to 81	Channel "Off" Output Leakage Current (Overvoltage Applied) (any Channel)	I_{OFF6}	-	4(f)	V_{IN} (enable) = 0.8V Address Inputs: V_{IL} = 0.8V, V_{IH} = 4.0V Channel Input Conditions: V_{IN} (under test) = −33V V_{OUT} (A or B) = 0V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open (Pins 4-2, 5-2, 6-2, 7-2, 8-2, 9-2, 10-2, 11-2, 19-28, 20-28, 21-28, 22-28, 23-28, 24-28, 25-28, 26-28)	-	2.0	A
82 to 97	Channel "On" Leakage Current	I_{ON1}	-	4(g)	V_{IN} (enable) = 4.0V Address Inputs: V_{IL} = 0.8V, V_{IH} = 4.0V Channel Input Conditions: V_{IN} (input/output under test) = 10V V_{IN} (other inputs) = −10V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open (Pins 4 & 2, 5 & 2, 6 & 2, 7 & 2, 8 & 2, 9 & 2, 10 & 2, 11 & 2, 19 & 28, 20 & 28, 21 & 28, 22 & 28, 23 & 28, 24 & 28, 25 & 28, 26 & 28)	-	10	nA

NOTES: See Page 22.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	Characteristics	Symbol	MIL-STD-883 Test Method	Test Fig.	Test Conditions (Pins Under Test)	Limits Min	Limits Max	Unit
98 to 113	Channel "On" Leakage Current	I_{ON2}	-	4(g)	V_{IN} (enable) = 4.0V Address Inputs: V_{IL} = 0.8V, V_{IH} = 4.0V Channel Input Conditions: V_{IN} (input/output under test) = −10V V_{IN} (other inputs) = 10V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open (Pins 4 & 2, 5 & 2, 6 & 2, 7 & 2, 8 & 2, 9 & 2, 10 & 2, 11 & 2, 19 & 28, 20 & 28, 21 & 28, 22 & 28, 23 & 28, 24 & 28, 25 & 28, 26 & 28)	-	10	nA
114 to 145	Channel "On" Resistance	R_{ON1}	-	4(h)	V_{IN} (enable) = 4.0V Address Inputs: V_{IL} = 0.8V, V_{IH} = 4.0V Channel Input Conditions: V_{IN} (under test) = 10V I_{IN} = 100µA V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open (Pins 2 to 4-5-6-7-8-9-10-11; 28 to 19-20-21-22-23-24-25-26; 4-5-6-7-8-9-10-11 to 2; 19-20-21-22-23-24-25-26 to 28)	-	1.5	kΩ

NOTES: See Page 22.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	Characteristics	Symbol	MIL-STD-883 Test Method	Test Fig.	Test Conditions (Pins Under Test)	Limits		Unit
						Min	Max	
146 to 149	Propagation Delay Address to Signal Out (Channel Turning On)	t_{PHL}	3003	4(i)	V_{IN} (enable) = 4.0V V_{IN} (address inputs) = Pulse Generator V_{IN} (A1 and B1) = 10V V_{IN} (A8 and B8) = − 10V V_{IN} (all other inputs) = 0V V_{DD} = 15V, V_{SS} = − 15V V_{REF} = Open (Pins 2-28)	-	1.0	µs
150 to 151	Propagation Delay Enable to Signal Out (Channel Turning On)	t_{PLH}	3003	4(j)	V_{IN} (enable) = Pulse Generator V_{IN} (address inputs) = 0.8V V_{IN} (A1 and B1) = 10V V_{DD} = 15V, V_{SS} = − 15V V_{REF} = Open (Pins 2-28)	-	1.0	µs
152 to 153	Propagation Delay Enable to Signal Out (Channel Turning Off)	t_{PHL}	3003	4(j)	V_{IN} (enable) = Pulse Generator V_{IN} (address inputs) = 4.0V V_{IN} (A8 and B8) = 10V V_{DD} = 15V, V_{SS} = − 15V V_{REF} = Open (Pins 2-28)	-	1.0	µs
154 to 157	Break-before-make Delay	t_{open}	3003	4(k)	V_{IN} (enable) = 4.0V V_{IN} (address inputs) = Pulse Generator V_{IN} (A1 and B1) = 5.0V V_{IN} (A8 and B8) = 5.0V V_{DD} = 15V, V_{SS} = − 15V V_{REF} = Open Note 2 (Pins 2-28)	50	-	ns
158 to 173	Channel "Off" Input Capacitance	C_{INC}	-	4(l)	V_{IN} (address and enable) = 0V f = 1.0MHz V_{DD} = V_{SS} = 0V V_{REF} = Open Note 2 (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	-	10	pF

NOTES: See Page 22.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	Characteristics	Symbol	MIL-STD-883 Test Method	Test Fig.	Test Conditions (Pins Under Test)	Limits		Unit
						Min	Max	
174 to 175	Channel "Off" Output Capacitance	C_{OC}	-	4(l)	V_{IN} (address and enable) = 0V $V_{DD} = V_{SS} = 0V$ V_{REF} = Open Note 2 (Pins 2-28)	-	100	pF
176 to 179	Input Capacitance Address or Enable	C_{IN}	-	4(m)	V_{IN} (not under test) = 0V $V_{DD} = V_{SS} = 0V$ V_{REF} = Open Note 2 (Pins 15-16-17-18)	-	10	pF

NOTES

1. Go-no-go test with $V_{IL} = 0.8V$, $V_{IH} = 4.0V$.
2. Guaranteed but not measured.
3. Guaranteed but not measured at $-55°C$.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, +125(+0−5) AND −55(+5−0) °C

No.	Characteristics	Symbol	MIL-STD-883 Test Method	Test Fig.	Test Conditions (Pins Under Test)	Limits Min	Limits Max	Unit
1	Functional Test	-	3005	3(b)	Verify Truth Table. V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open Note 1	-	-	-
2	Quiescent Current (Positive)	I_{DD1}	3005	4(a)	V_{IN} (enable) = 4.0V V_{IN} (address) = 0.8V V_{IN} (all channels) = 0V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open (Pin 1)	-	2.0	mA
3	Quiescent Current (Negative)	I_{SS1}	3005	4(a)	V_{IN} (enable) = 4.0V V_{IN} (address) = 0.8V V_{IN} (all channels) = 0V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open (Pin 27)	−1.0	-	mA
4	Quiescent Standby Current (Positive)	I_{DD2}	3005	4(a)	V_{IN} (enable) = 0.8V V_{IN} (address) = 0.8V V_{IN} (all channels) = 0V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open (Pin 1)	-	2.0	mA
5	Quiescent Standby Current (Negative)	I_{SS2}	3005	4(a)	V_{IN} (enable) = 0.8V V_{IN} (address) = 0.8V V_{IN} (all channels) = 0V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open (Pin 27)	−1.0	-	mA
6 to 9	Input Current, Low Level Address or Enable	I_{IL}	3009	4(h)	V_{IN} (under test) = 0.8V V_{IN} (other inputs) = 15V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open Note 3 (Pins 15-16-17-18)	-	1.0	A
10 to 13	Input Current, High Level Address or Enable	I_{IH}	3010	4(c)	V_{IN} (under test) = 4.0V V_{IN} (other inputs) = 0V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open Note 3 (Pins 15-16-17-18)	-	1.0	A

NOTES: See Page 22.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, +125(+0−5) AND −55(+5−0) °C (CONT'D)

No.	Characteristics	Symbol	MIL-STD-883 Test Method	Test Fig.	Test Conditions (Pins Under Test)	Limits		Unit
						Min	Max	
14 to 29	Channel "Off" Input Leakage Current (any Channel)	I_{OFF1}	-	4(d)	V_{IN} (enable) = 0.8V Address Inputs: V_{IL} = 0.8V, V_{IH} = 4.0V Channel Input Conditions: V_{IN} (under test) = 10V V_{IN} (other inputs) = −10V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open Note 3 (Pins 4-2, 5-2, 6-2, 7-2, 8-2, 9-2, 10-2, 11-2, 19-28, 20-28, 21-28, 22-28, 23-28, 24-28, 25-28, 26-28)	-	50	nA
30 to 45	Channel "Off" Input Leakage Current (any Channel)	I_{OFF2}	-	4(d)	V_{IN} (enable) = 0.8V Address Inputs: V_{IL} = 0.8V, V_{IH} = 4.0V Channel Input Conditions: V_{IN} (under test) = −10V V_{IN} (other inputs) = 10V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open Note 3 (Pins 4-2, 5-2, 6-2, 7-2, 8-2, 9-2, 10-2, 11-2, 19-28, 20-28, 21-28, 22-28, 23-28, 24-28, 25-28, 26-28)	-	50	nA
46 to 47	Channel "Off" Output Leakage Current (all Channels)	I_{OFF3}	-	4(e)	V_{IN} (address and enable) = 0.8V Channel Input Conditions: V_{IN} (under test) = −10V V_{IN} (all inputs) = 10V V_{REF} = Open Note 3 (Pins 2 to 4 thru 11, 28 to 19 thru 26)	-	250	nA
48 to 49	Channel "Off" Output Leakage Current (all Channels)	I_{OFF4}	-	4(e)	V_{IN} (address and enable) = 0.8V Channel Input Conditions: V_{IN} (under test) = 10V V_{IN} (all inputs) = −10V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open Note 3 (Pins 2 to 4 thru 11, 28 to 19 thru 26)	-	250	µA

NOTES: See Page 22.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, +125(+0−5) AND −55(+5−0) °C (CONT'D)

No.	Characteristics	Symbol	MIL-STD-883 Test Method	Test Fig.	Test Conditions (Pins Under Test)	Limits		Unit
						Min	Max	
50 to 65	Channel "Off" Output Leakage Current (Overvoltage Applied) (any Channel)	I_{OFF5}	-	4(f)	V_{IN} (enable) = 0.8V Address Inputs: V_{IL} = 0.8V, V_{IH} = 4.0V Channel Input Conditions: V_{IN} (under test) = 33V V_{OUT} (A or B) = 0V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open Note 3 (Pins 4-2, 5-2, 6-2, 7-2, 8-2, 9-2, 10-2, 11-2, 19-28, 20-28, 21-28, 22-28, 23-28, 24-28, 25-28, 26-28)	-	2.0	µA
66 to 81	Channel "Off" Output Leakage Current (Overvoltage Applied) (any Channel)	I_{OFF6}	-	4(f)	V_{IN} (enable) = 0.8V Address Inputs: V_{IL} = 0.8V, V_{IH} = 4.0V Channel Input Conditions: V_{IN} (under test) = −33V V_{OUT} (A or B) = 0V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open Note 3 (Pins 4-2, 5-2, 6-2, 7-2, 8-2, 9-2, 10-2, 11-2, 19-28, 20-28, 21-28, 22-28, 23-28, 24-28, 25-28, 26-28)	-	2.0	µA
82 to 97	Channel "On" Leakage Current	I_{ON1}	-	4(g)	V_{IN} (enable) = 4.0V Address Inputs: V_{IL} = 0.8V, V_{IH} = 4.0V Channel Input Conditions: V_{IN} (input/output under test) = 10V V_{IN} (other inputs) = −10V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open Note 3 (Pins 4 & 2, 5 & 2, 6 & 2, 7 & 2, 8 & 2, 9 & 2, 10 & 2, 11 & 2, 19 & 28, 20 & 28, 21 & 28, 22 & 28, 23 & 28, 24 & 28, 25 & 28, 26 & 28)	-	250	nA

NOTES: See Page 22.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, +125(+0−5) AND −55(+5−0) °C (CONT'D)

No.	Characteristics	Symbol	MIL-STD-883 Test Method	Test Fig.	Test Conditions (Pins Under Test)	Limits		Unit
						Min	Max	
14 to 29	Channel "Off" Input Leakage Current (any Channel)	I_{OFF1}	-	4(d)	V_{IN} (enable) = 0.8V Address Inputs: V_{IL} = 0.8V, V_{IH} = 4.0V Channel Input Conditions: V_{IN} (under test) = 10V V_{IN} (other inputs) = −10V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open Note 3 (Pins 4-2, 5-2, 6-2, 7-2, 8-2, 9-2, 10-2, 11-2, 19-28, 20-28, 21-28, 22-28, 23-28, 24-28, 25-28, 26-28)	-	50	nA
30 to 45	Channel "Off" Input Leakage Current (any Channel)	I_{OFF2}	-	4(d)	V_{IN} (enable) = 0.8V Address Inputs: V_{IL} = 0.8V, V_{IH} = 4.0V Channel Input Conditions: V_{IN} (under test) = −10V V_{IN} (other inputs) = 10V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open Note 3 (Pins 4-2, 5-2, 6-2, 7-2, 8-2, 9-2, 10-2, 11-2, 19-28, 20-28, 21-28, 22-28, 23-28, 24-28, 25-28, 26-28)	-	50	nA
46 to 47	Channel "Off" Output Leakage Current (all Channels)	I_{OFF3}	-	4(e)	V_{IN} (address and enable) = 0.8V Channel Input Conditions: V_{IN} (under test) = −10V V_{IN} (all inputs) = 10V V_{REF} = Open Note 3 (Pins 2 to 4 thru 11, 28 to 19 thru 26)	-	250	nA
48 to 49	Channel "Off" Output Leakage Current (all Channels)	I_{OFF4}	-	4(e)	V_{IN} (address and enable) = 0.8V Channel Input Conditions: V_{IN} (under test) = 10V V_{IN} (all inputs) = −10V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open Note 3 (Pins 2 to 4 thru 11, 28 to 19 thru 26)	-	250	µA

NOTES: See Page 22.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, +125(+0−5) AND −55(+5−0) °C (CONT'D)

No.	Characteristics	Symbol	MIL-STD-883 Test Method	Test Fig.	Test Conditions (Pins Under Test)	Limits		Unit
						Min	Max	
50 to 65	Channel "Off" Output Leakage Current (Overvoltage Applied) (any Channel)	I_{OFF5}	-	4(f)	V_{IN} (enable) = 0.8V Address Inputs: V_{IL} = 0.8V, V_{IH} = 4.0V Channel Input Conditions: V_{IN} (under test) = 33V V_{OUT} (A or B) = 0V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open Note 3 (Pins 4-2, 5-2, 6-2, 7-2, 8-2, 9-2, 10-2, 11-2, 19-28, 20-28, 21-28, 22-28, 23-28, 24-28, 25-28, 26-28)	-	2.0	µA
66 to 81	Channel "Off" Output Leakage Current (Overvoltage Applied) (any Channel)	I_{OFF6}	-	4(f)	V_{IN} (enable) = 0.8V Address Inputs: V_{IL} = 0.8V, V_{IH} = 4.0V Channel Input Conditions: V_{IN} (under test) = −33V V_{OUT} (A or B) = 0V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open Note 3 (Pins 4-2, 5-2, 6-2, 7-2, 8-2, 9-2, 10-2, 11-2, 19-28, 20-28, 21-28, 22-28, 23-28, 24-28, 25-28, 26-28)	-	2.0	µA
82 to 97	Channel "On" Leakage Current	I_{ON1}	-	4(g)	V_{IN} (enable) = 4.0V Address Inputs: V_{IL} = 0.8V, V_{IH} = 4.0V Channel Input Conditions: V_{IN} (input/output under test) = 10V V_{IN} (other inputs) = −10V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open Note 3 (Pins 4 & 2, 5 & 2, 6 & 2, 7 & 2, 8 & 2, 9 & 2, 10 & 2, 11 & 2, 19 & 28, 20 & 28, 21 & 28, 22 & 28, 23 & 28, 24 & 28, 25 & 28, 26 & 28)	-	250	nA

NOTES: See Page 22.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, +125(+0−5) AND −55(+5−0) °C (CONT'D)

No.	Characteristics	Symbol	MIL-STD-883 Test Method	Test Fig.	Test Conditions (Pins Under Test)	Limits		Unit
						Min	Max	
98 to 113	Channel "On" Leakage Current	I_{ON2}	-	4(g)	V_{IN} (enable) = 4.0V Address Inputs: V_{IL} = 0.8V, V_{IH} = 4.0V Channel Input Conditions: V_{IN} (input/output under test) = −10V V_{IN} (other inputs) = 10V V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open Note 3 (Pins 4 & 2, 5 & 2, 6 & 2, 7 & 2, 8 & 2, 9 & 2, 10 & 2, 11 & 2, 19 & 28, 20 & 28, 21 & 28, 22 & 28, 23 & 28, 24 & 28, 25 & 28, 26 & 28)	-	250	nA
114 to 145	Channel "On" Resistance	R_{ON1}	-	4(h)	V_{IN} (enable) = 4.0V Address Inputs: V_{IL} = 0.8V, V_{IH} = 4.0V Channel Input Conditions: V_{IN} (under test) = 10V I_{IN} = 100µA V_{DD} = 15V, V_{SS} = −15V V_{REF} = Open (Pins 2 to 4-5-6-7-8-9-10-11; 28 to 19-20-21-22-23-24-25-26; 4-5-6-7-8-9-10-11 to 2; 19-20-21-22-23-24-25-26 to 28)	-	1.5	kΩ

NOTES: See Page 22.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - QUIESCENT CURRENT

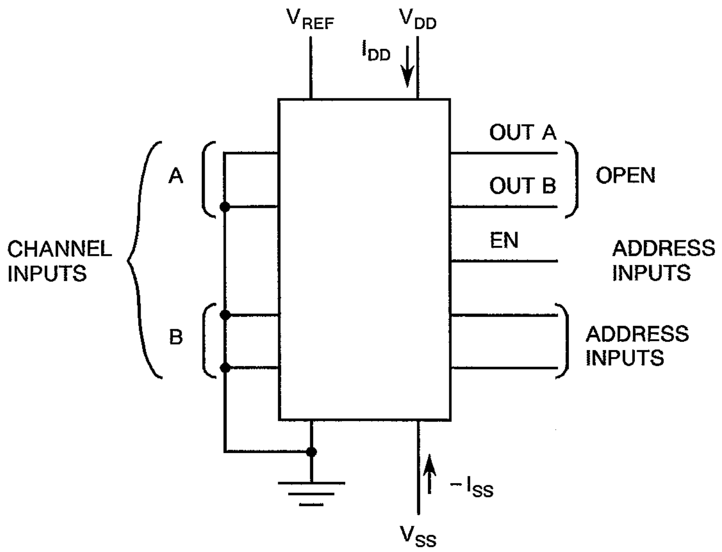
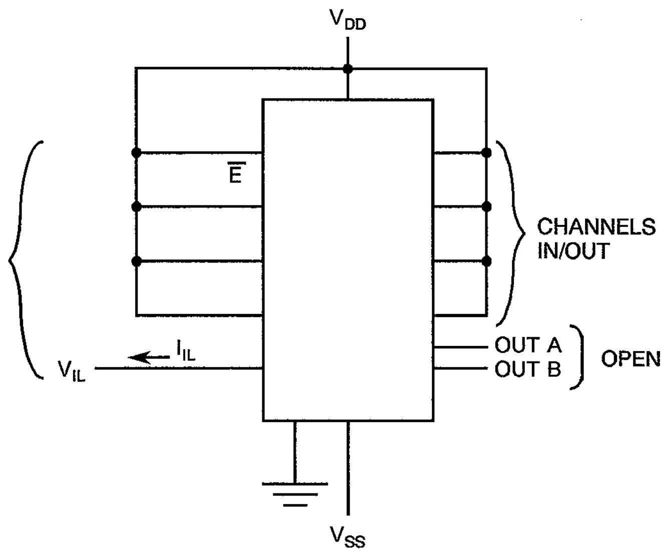
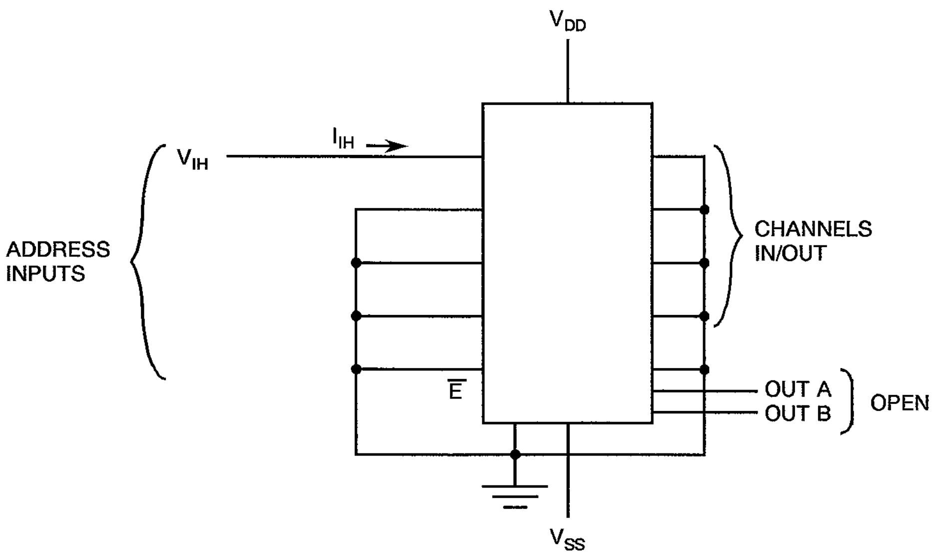


FIGURE 4(b) - INPUT CURRENT LOW LEVEL



NOTES
1. Each input to be tested separately.

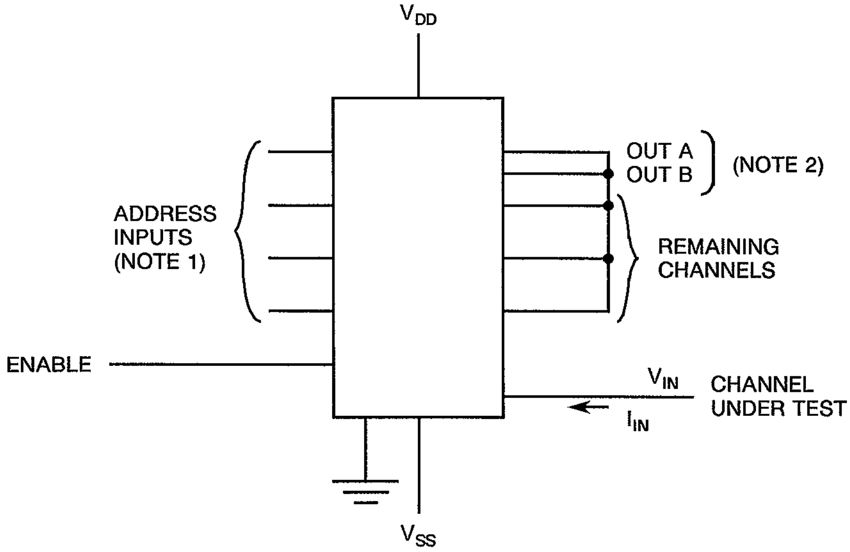
FIGURE 4(c) - INPUT CURRENT HIGH LEVEL



NOTES
1. Each input to be tested separately.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

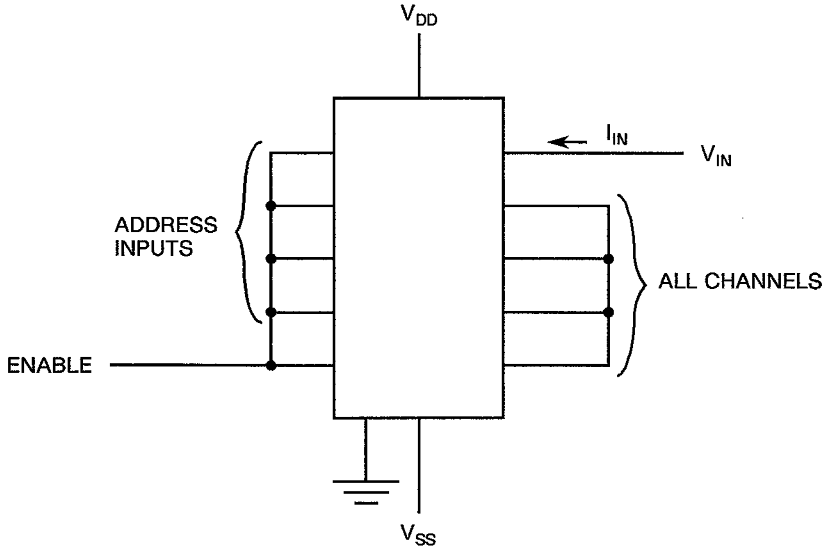
FIGURE 4(d) - CHANNEL "OFF" INPUT LEAKAGE CURRENT



NOTES

1. Select channel under test as per truth table.
2. I_{OFF} is measured at the following conditions:-
   (i) $V_{IN} = 10V$, remaining channel inputs and outputs: $V_{IN} = -10V$.
   (ii) $V_{IN} = -10V$, remaining channel inputs and outputs: $V_{IN} = 10V$.

FIGURE 4(e) - CHANNEL "OFF" OUTPUT LEAKAGE CURRENT

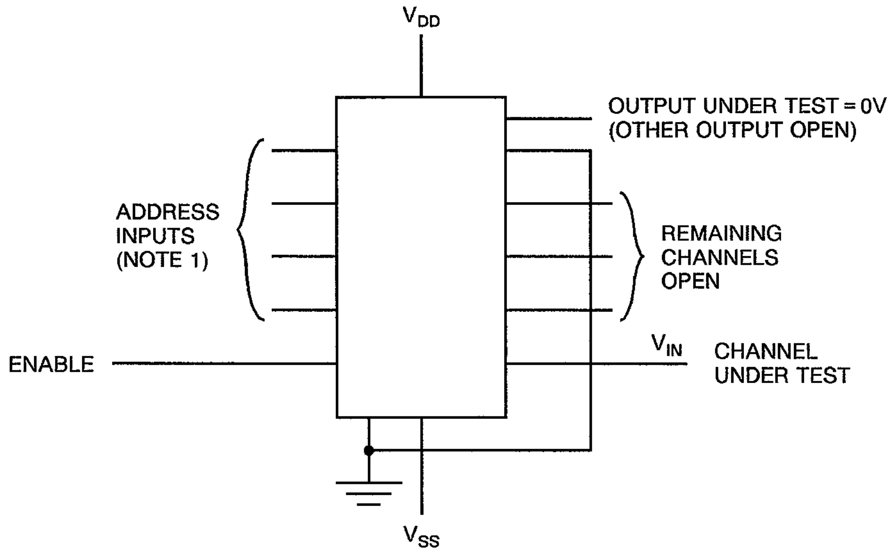


NOTES

1. I_{OFF} is measured at the following conditions:-
   (i) Output under test: $V_{IN} = -10V$, remaining output and all channel inputs: $V_{IN} = 10V$.
   (ii) Output under test: $V_{IN} = 10V$, remaining output and all channel inputs: $V_{IN} = -10V$.

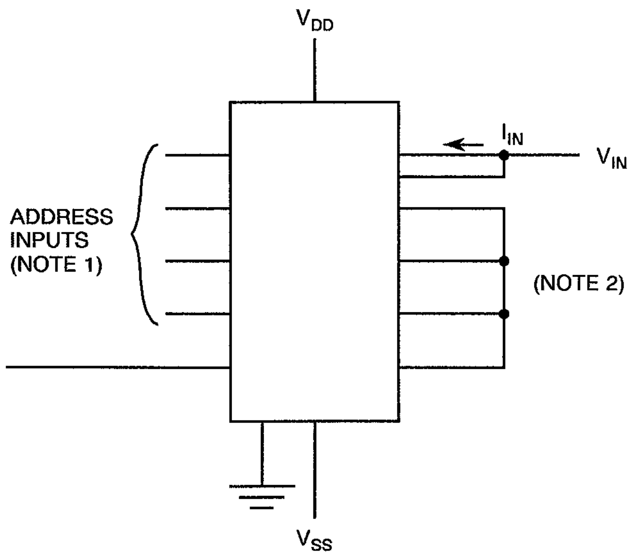
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(f) - CHANNEL "OFF" OUTPUT LEAKAGE CURRENT (OVERVOLTAGE APPLIED)



NOTES
1. Select channel under test as per truth table.
2. I_{OFF} is measured with $V_{IN} = 33V$ and then with $V_{IN} = -33V$.

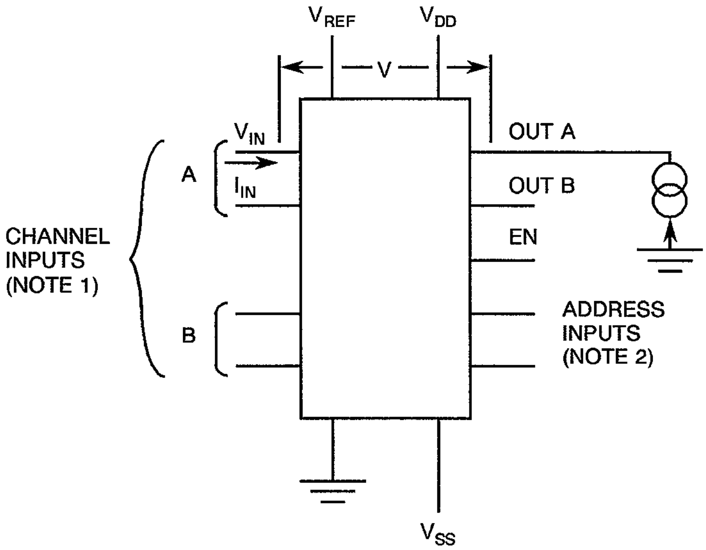
FIGURE 4(g) - CHANNEL "ON" LEAKAGE CURRENT



NOTES
1. Select channel under test as per truth table.
2. I_{ON} is measured with selected channel input and output at $V_{IN} = 10V$.
   Remaining inputs and output $V_{IN} = -10V$ and then with $V_{IN} = -10V$; remaining inputs and output $V_{IN} = 10V$.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

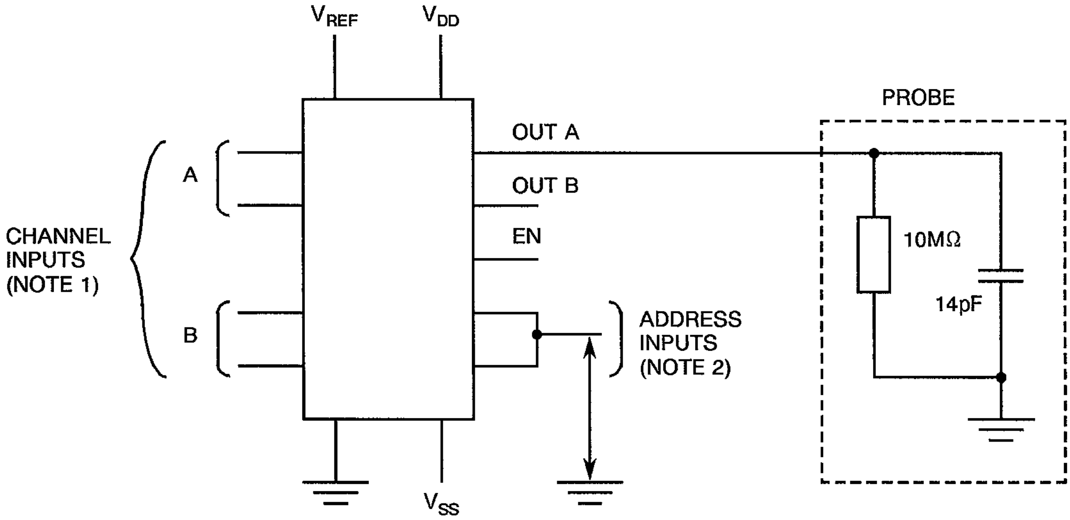
FIGURE 4(h) - CHANNEL "ON" RESISTANCE

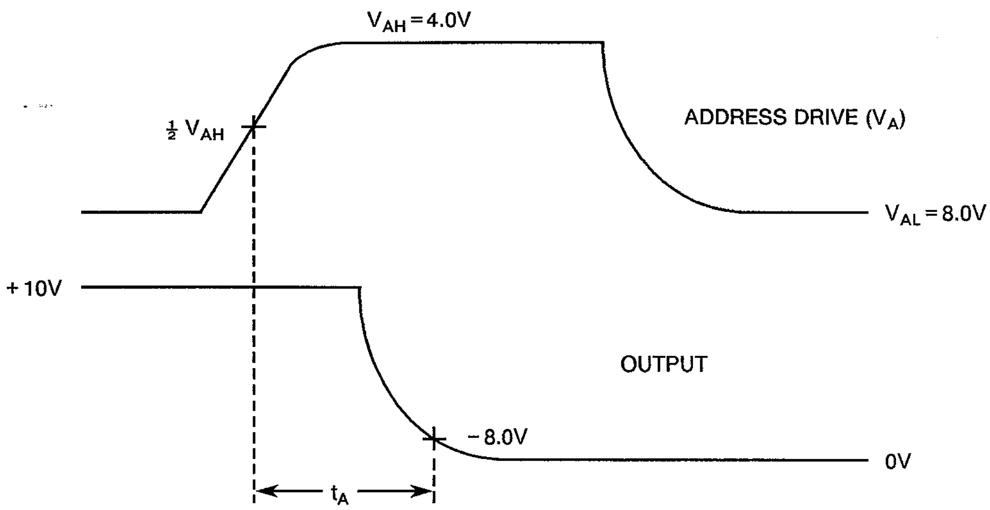


NOTES
1. Each input is tested separately.
2. Test per Truth Table.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - PROPAGATION DELAY ADDRESS INPUTS TO SIGNAL OUT CHANNEL TURNING ON



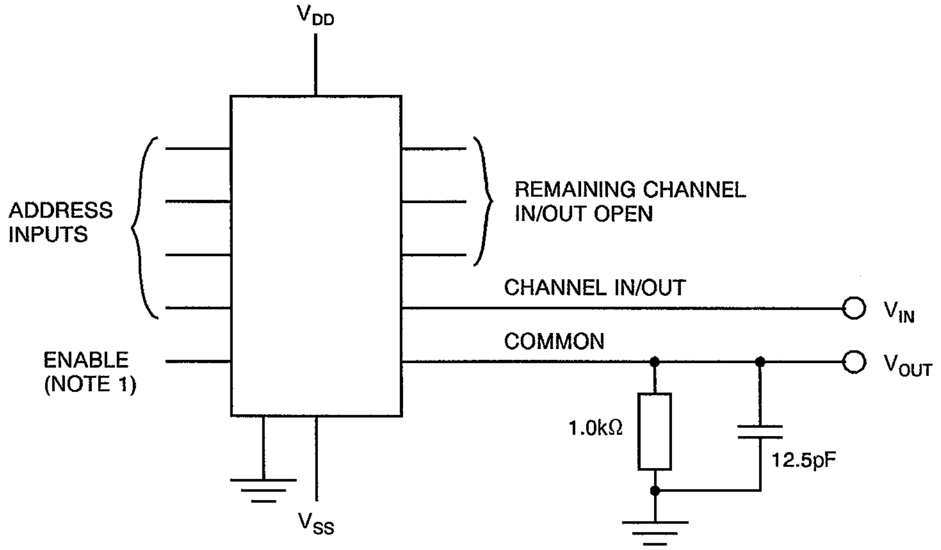


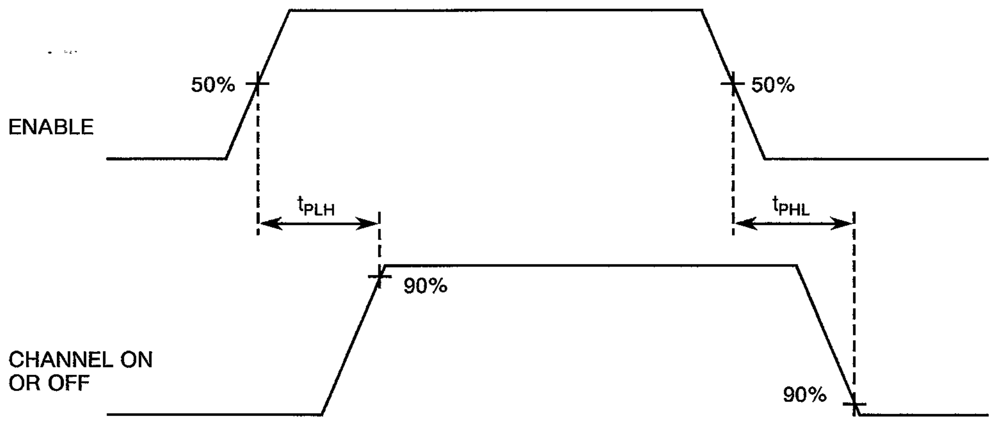
NOTES

1. $V_{INA1} = V_{INB1} = +10V$, $V_{INA8} = V_{INB8} = -10V$.
2. Input waveforms are supplied by a pulse generator having a PPR of 1.0MHz and $Z_{out} = 50\Omega$.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(j) - PROPAGATION DELAY ENABLE TO SIGNAL OUT, CHANNEL "OFF" OR "ON"



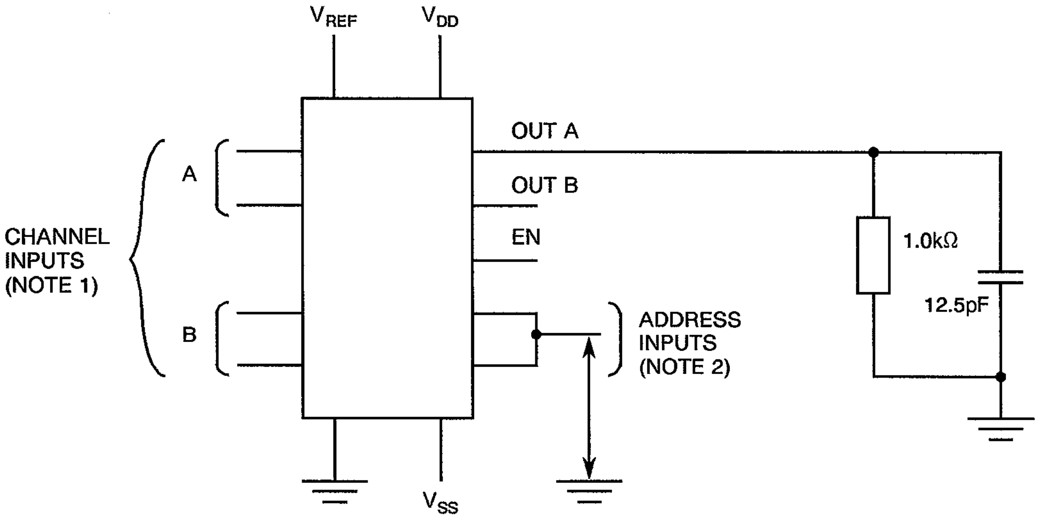


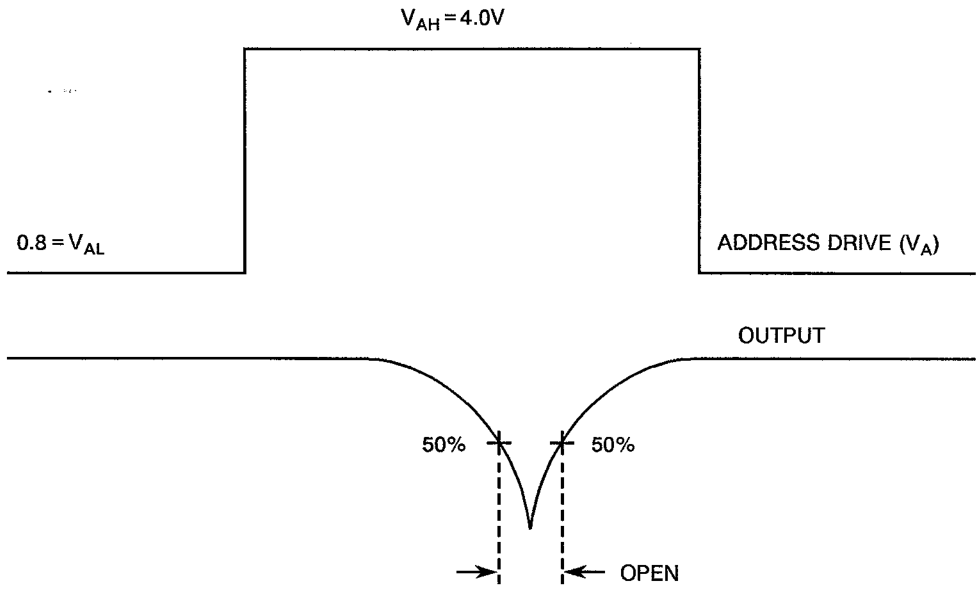
NOTES

1. Input waveforms are supplied by a pulse generator having $V_P = 0.8$ to 4.0V, f = 1.0MHz and $Z_{out} = 50\Omega$.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(k) - BREAK-BEFORE-MAKE DELAY





NOTES

1. $V_{IN} = 5.0V$.
2. Input waveforms are supplied by a pulse generator having a PPR of 1.0MHz and $Z_{out} = 50\Omega$.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(l) - CHANNEL "OFF" INPUT CAPACITANCE AND CHANNEL "OFF" OUTPUT CAPACITANCE

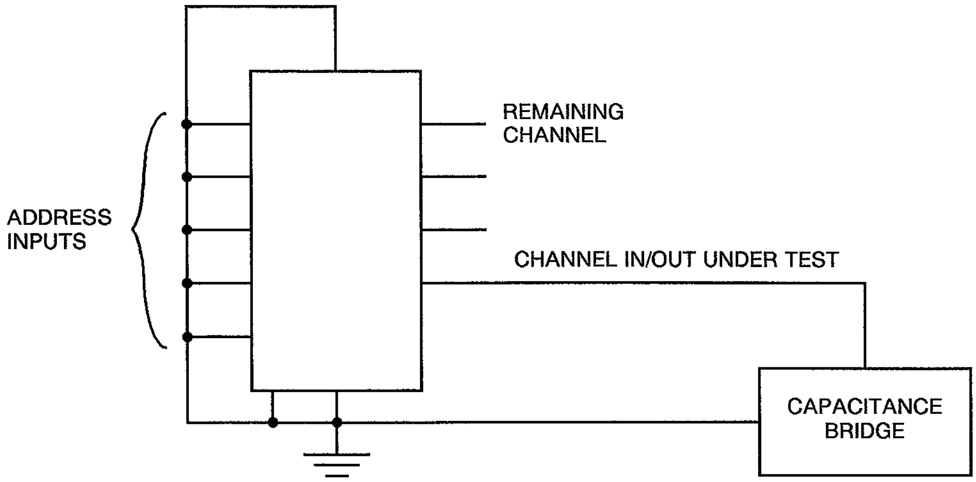


FIGURE 4(m) - INPUT CAPACITANCE ADDRESS OR ENABLE

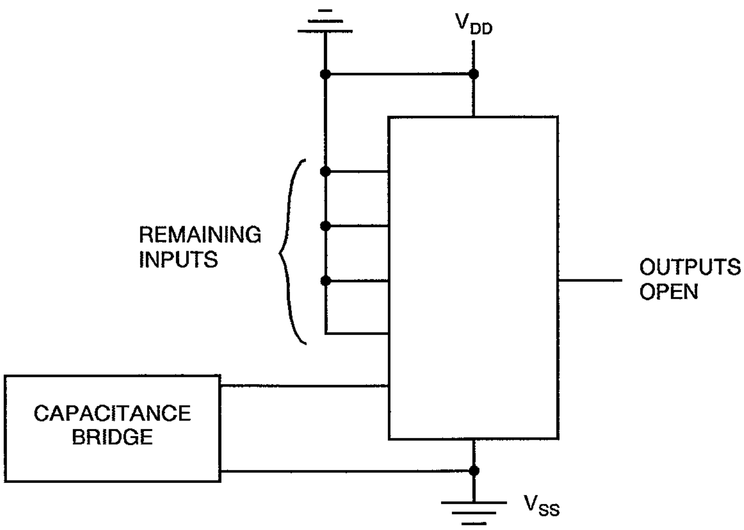


TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
2	Quiescent Current (Positive)	I_{DD1}	As per Table 2	As per Table 2	200	μA
3	Quiescent Current (Negative)	I_{SS1}	As per Table 2	As per Table 2	200	μA
14 to 29	Channel “Off” Input Leakage Current	I_{OFF1}	As per Table 2	As per Table 2	±10	nA
46 to 47	Channel “Off” Output Leakage Current	I_{OFF3}	As per Table 2	As per Table 2	±10	nA
114 to 145	Channel “On” Resistance	R_{ON}	As per Table 2	As per Table 2	±20	%

TABLE 5(a) - CONDITIONS FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, N-CHANNELS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	$+125(+0-5)$	°C
2	Channel Inputs - (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	V_{IN}	V_{SS}	V
3	Channel Out - (Pins 2-28)	V_{IN}	Open	V
4	Address Inputs - (Pins 15-16-17)	V_{IN}	V_{SS}	V
5	Reference Voltage - (Pin 13)	V_{REF}	V_{DD}	V
6	Enable Voltage - (Pin 18)	V_{EN}	V_{DD}	V
7	Positive Supply Voltage - (Pin 1)	V_{DD}	15	V
8	Negative Supply Voltage - (Pin 27)	V_{SS}	-15	V
9	Ground - (Pin 12)	-	Ground	V
10	Duration	t	72	Hours

NOTES

1. Except for V_{DD} and V_{SS}, each terminal connection may, at the Manufacturer's option, be made through a resistor whose value is 47kΩ maximum.

TABLE 5(b) - CONDITIONS FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, P-CHANNELS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	$+125(+0-5)$	°C
2	Channel Inputs - (Pins 5-6-7-8-9-10-11-19-20-21-22-23-24-25)	V_{IN}	V_{DD}	V
3	Channel Input - (Pins 4-26)	V_{IN}	Open	V
4	Channel Out - (Pins 2-28)	V_{IN}	V_{DD}	V
5	Address Inputs - (Pins 15-16-17)	V_{IN}	V_{DD}	V
6	Reference Voltage - (Pin 13)	V_{REF}	V_{DD}	V
7	Enable Voltage - (Pin 18)	V_{EN}	V_{DD}	V
8	Positive Supply Voltage - (Pin 1)	V_{DD}	15	V
9	Negative Supply Voltage - (Pin 27)	V_{SS}	-15	V
10	Ground - (Pin 12)	-	Ground	V
11	Duration	t	72	Hours

NOTES

1. Except for V_{DD} and V_{SS}, each terminal connection may, at the Manufacturer's option, be made through a resistor whose value is 47kΩ maximum.

TABLE 5(c) - CONDITIONS FOR BURN-IN, DYNAMIC AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0−5)	°C
2	Positive Supply Voltage - (Pin 1)	V_{DD}	15	V
3	Negative Supply Voltage - (Pin 27)	V_{SS}	−15	V
4	Enable Voltage - (Pin 18)	V_{EN}	5.0	V
5	Reference Voltage - (Pin 13)	V_{REF}	5.0	V
6	Pulse Voltage	V_{GEN}	0 to 5	V
7	Frequency	f	A_0 = 100 A_1 = 50 A_2 = 25	kHz

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS, N-CHANNELS

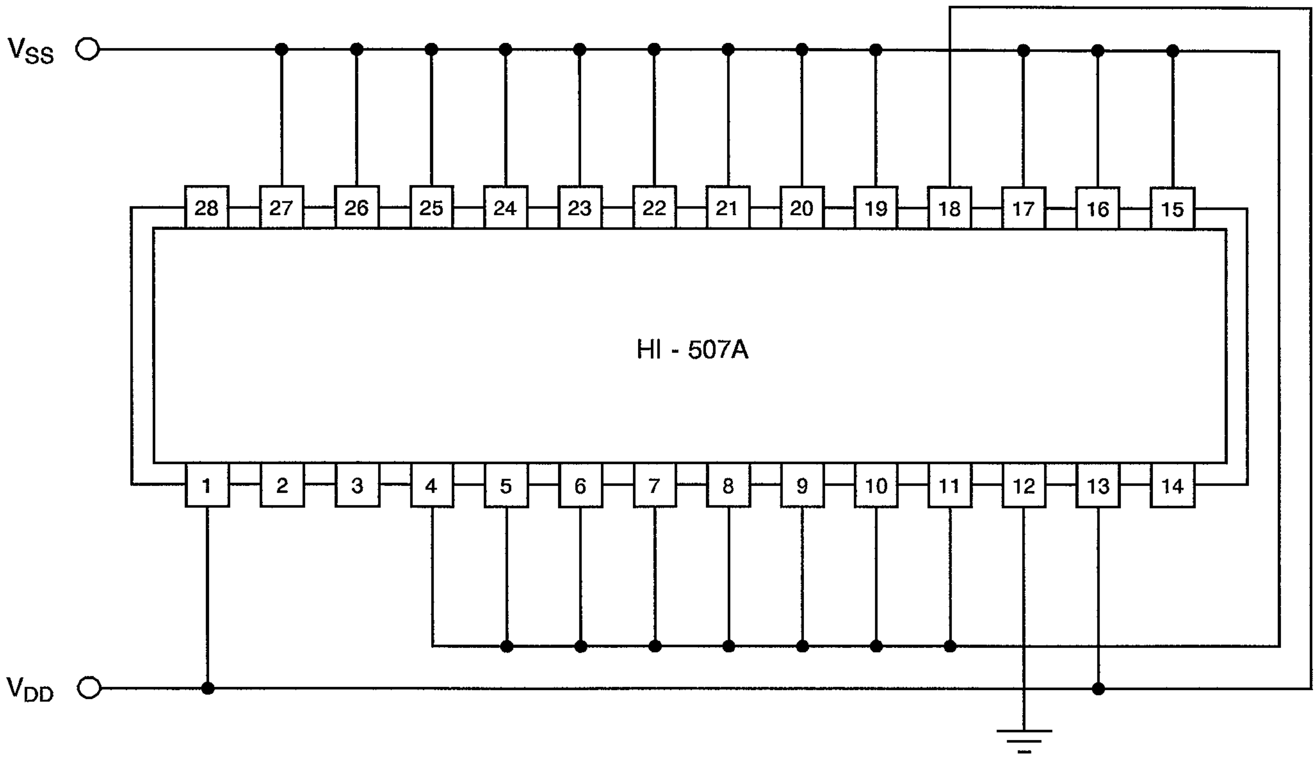


FIGURE 5(b) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS, P-CHANNELS

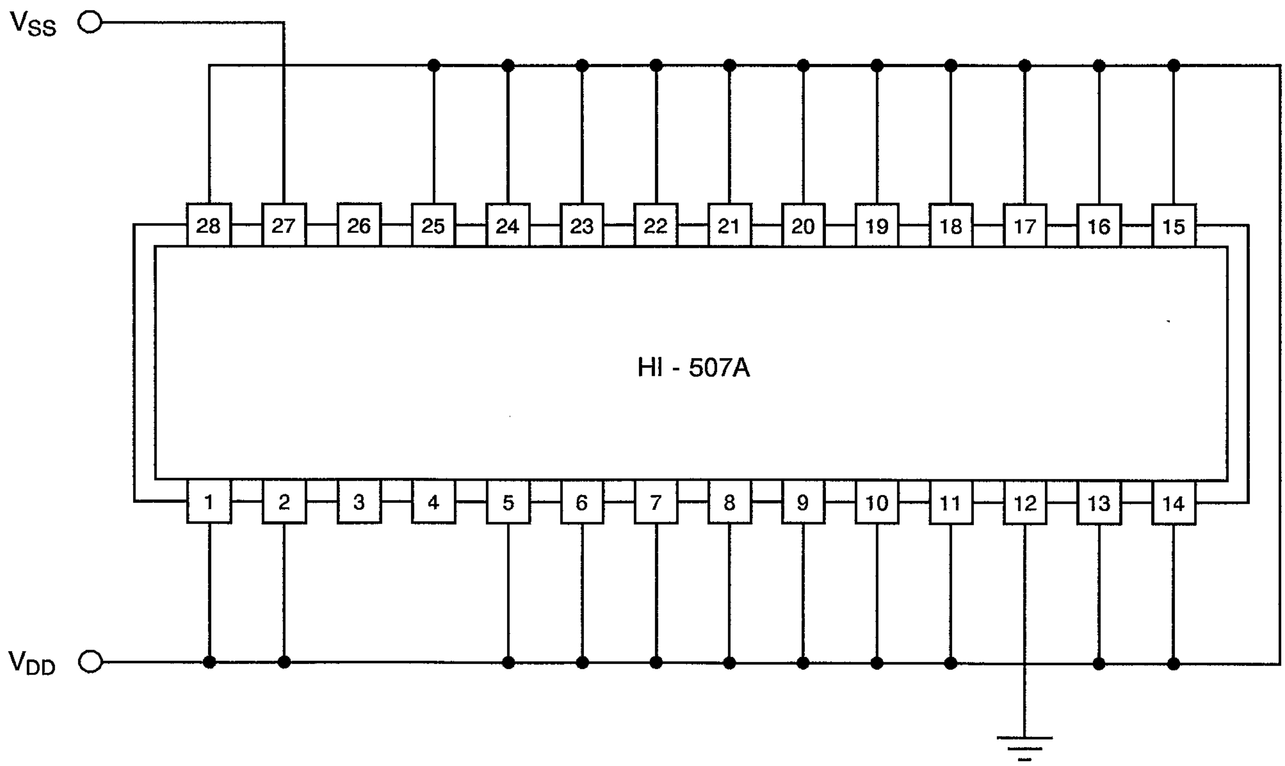
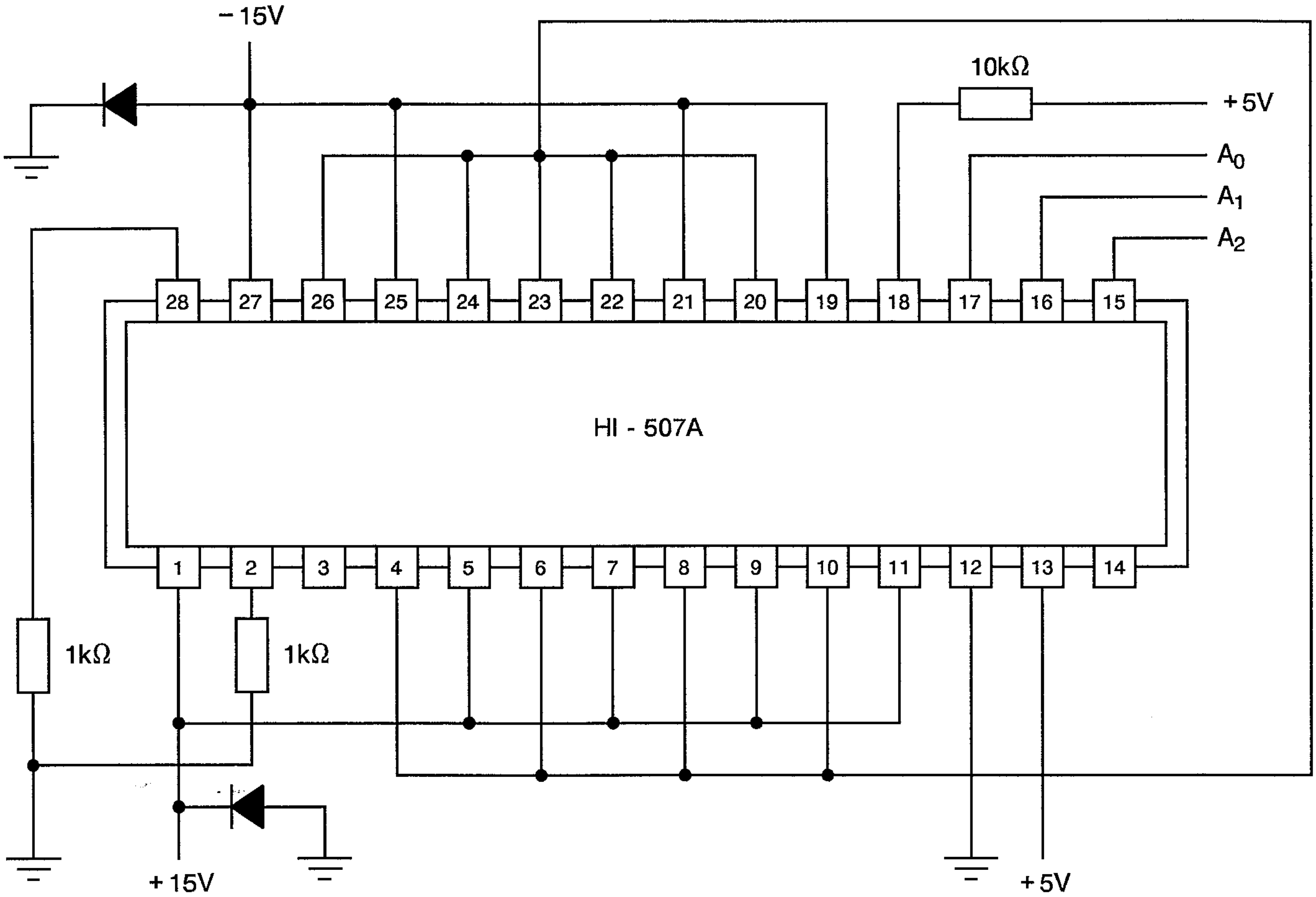


FIGURE 5(c) - ELECTRICAL CIRCUIT FOR BURN-IN, DYNAMIC AND OPERATING LIFE TESTS



4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 2. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(c) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests is shown in Figure 5(c) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The conditions for high temperature storage shall be $T_{amb} = +150(+0-5)$ °C.

TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test	-	As per Table 2	As per Table 2	-	-	-	-
2	Quiescent Current (Positive)	I_{DD1}	As per Table 2	As per Table 2	-	-	2.0	mA
3	Quiescent Current (Negative)	I_{SS1}	As per Table 2	As per Table 2	-	-	2.0	mA
14 to 29	Channel “Off” Input Leakage Current	I_{OFF1}	As per Table 2	As per Table 2	±10	-	-	nA
46 to 47	Channel “Off” Output Leakage Current	I_{OFF3}	As per Table 2	As per Table 2	±10	-	-	nA
114 to 145	Channel “On” Resistance	R_{ON}	As per Table 2	As per Table 2	-	-	1.5	kΩ

APPENDIX 'A'

AGREED DEVIATIONS FOR HARRIS (U.S.)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.1	Deviations from Special In-process Controls (Para. 5.1) (a) Para. 5.1.1, "Scanning Electron Microscope Inspection" (SEM) This shall be performed in accordance with Method 2018 of MIL-STD-883, with the following exceptions:- 1. A SEM lot is defined at the metallisation step. One wafer is selected from the inside row and one from the outside row of the same planet. Sampling condition B_2 (segment, prior to glassivation) is used regardless of the glassivation temperature. 2. All four directional edges of every type of oxide step shall be examined on each wafer. The Manufacturer shall mount each of the wafer's four sample dice 90° out of phase from each other, so that all four edge directions can be properly inspected on each wafer. Questionable steps which are not at the proper viewing angle are inspected by rotating the sample as needed. 3. A lot is unacceptable if the directional edge of any contact window, or other type of oxide step, has a reduced cross-sectional area greater than 50%, or if it is reduced in thickness such that, at worst case specified operating conditions, the current density exceeds the limits specified in MIL-M-38510, Para. 3.5.5 (5×10^5 A/cm^2 for glassivated aluminium products). The current density is determined per Para. 3.5.5(a) of MIL-M-38510. Reduced cross-sectional area due to voids or defects that can be readily observed by Method 2010 of MIL-STD-883, "Visual Inspection of Metallisation", is no cause for SEM lot rejection. 4. A lot is unacceptable if the general metallisation (metallisation at all locations except at oxide steps) shows peeling or lifting as a result of poor adhesion. General metallisation is unacceptable if voiding or undercutting of the metal reduces the cross-sectional area by more than 50% or if it is reduced in thickness such that, at worst case specified operating conditions, the current density exceeds the limits specified in MIL-M-38510, Para. 3.5.5. Voids and defects in the general metallisation that can be readily observed by Method 2010 of MIL-STD-883, "Visual Inspection of Metallisation", are no cause for SEM lot rejection.