INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS, MIXED SIGNAL ASIC

BASED ON A RAD-HARD XH018 IP LIBRARY

ESCC Detail Specification No. 9202/084

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(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
1618	Specification updated to incorporate changes per DCR. .

TABLE OF CONTENTS

1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.

(b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 920208401A####

- Detail Specification Reference: 9202084
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: A (as required)
- Manufacturer Specific ASIC Identification: #### (as applicable, where #### is an individual 4-digit code allocated by the Manufacturer to a specific ASIC design)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Case	Lead Material and Finish (Note 1)	Weight max g	Total Dose Radiation Level Letter (Note 2)
01	CQFN-256	D2	11	Note 3
02	CQFN-132_A	D2	5.5	Note 3

NOTES:

1. The lead material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.
2. The total dose radiation level letter shall be as defined in ESCC Basic Specification No. 22900.
3. The ASICs defined herein have different radiation hardening because some IP elements are guaranteed with a TID of 300krad(Si) and other IP elements are guaranteed with a TID of 100krad(Si). Therefore the applicable Total Dose Radiation Level Letter for a specific ASIC design shall be discussed and agreed between the Orderer and the Manufacturer prior to placing the Purchase Order.

1.4.3 Manufacturer Specific ASIC Identification

An ASIC Datasheet shall be produced by the Manufacturer, after negotiation with the Orderer, that, as a minimum, specifies all the requirements unique to the specific ASIC design that are identified herein as being specified in the ASIC Datasheet. The ASIC Datasheet shall be held under configuration control by the Manufacturer. For identification and traceability purposes the Manufacturer shall allocate a unique Manufacturer Specific ASIC Identification to the ASIC Datasheet and the specific ASIC design as specified in Para. 1.4.1.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
5V Supply Voltage	V_{DD5}	-0.5 to 5.5	V	Note 1
3.3V Supply Voltage	V_{DD3V3}	-0.5 to 3.6	V	Note 1
Substrate Voltage	V_{sub}	-5.5 to V_{SS}+0.5	V	Note 1
Input Voltage Range	V_{INx}	-0.3 to V_{DDx}+0.3	V	Note 1
Device Power Dissipation (Continuous)	P_D	See ASIC Datasheet	W	
Supply Current	I_{DDop}	See ASIC Datasheet	mA	
Operating Temperature Range	T_{op}	-40 to +125	°C	T_{amb} Note 2
Storage Temperature Range	T_{stg}	-55 to +150	°C	
Junction Temperature	T_j	+135	°C	
Thermal Resistance, Junction-to-Case	$R_{th(j-c)}$	See ASIC Datasheet	°C/W	
Soldering Temperature	T_{sol}	+300	°C	Note 3

NOTES:

1. All voltages are with respect to V_{SS}.
2. If the analog level shifter from low to high [IP_7_3] is used, performance at T_{amb} > +85°C may be affected. See Para. 1.7.3, Note 2.
3. Duration 10 seconds maximum at a distance of not less than 1.6mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 500 Volts.

1.7 GENERAL INFORMATION ON THE XH018 PROCESS AND IP LIBRARY

1.7.1 XH018 Modules

The XH018 process offers several modules. The modules used for the IP elements are listed below.

Main module:

- LPMOS: 1.8/3.3V low power CMOS

Other modules:

- DEPL: Depletion module
- DMIM: DMIM capacitor module
- HVMOS: High-voltage module
- HVNMOS: HVNMOS module
- HVPMOS: HVPMOS module
- ISOMOS: Triple well isolated CMOS module
- LP3MOS for Trim OTP
- LVT: 1.8V low Vt module
- LVT: Low Vt module
- MET3: 3-metal module
- MET4: 4-metal module
- MET5: 5-metal module
- METMID: Top metal module
- MIM Capacitors (double)
- TrimOTP

1.7.2 Primitive Devices

Primitive devices are the circuit components provided by the semiconductor foundry. The following primitive devices are used for the IP elements.

- (Isolated) 1.8V, 3.3V LP NMOS/PMOS
- Depletion NMOS
- Bipolar transistors, ESD protected
- MIM Capacitors
- Polysilicon and metal resistors
- Low Vt Transistors

1.7.3 IP Library Elements

For the analog part of the ASIC various IP elements are available. These are summarised in the following table. Detailed descriptions of the IP library elements are available from the Manufacturer.

IP Group	IP Name	Function	IP Identification Number
I/O Pads	pad_analog	Analog input and output pad	[IP_0_1]
	pad_tmr_out	Digital output pad	[IP_0_2]
	pad_tmr_in_out	Digital input and output pad	[IP_0_3]
	pad_lvds_in	LVDS input pad	[IP_0_4]
	pad_lvds_out	LVDS output pad	[IP_0_5]

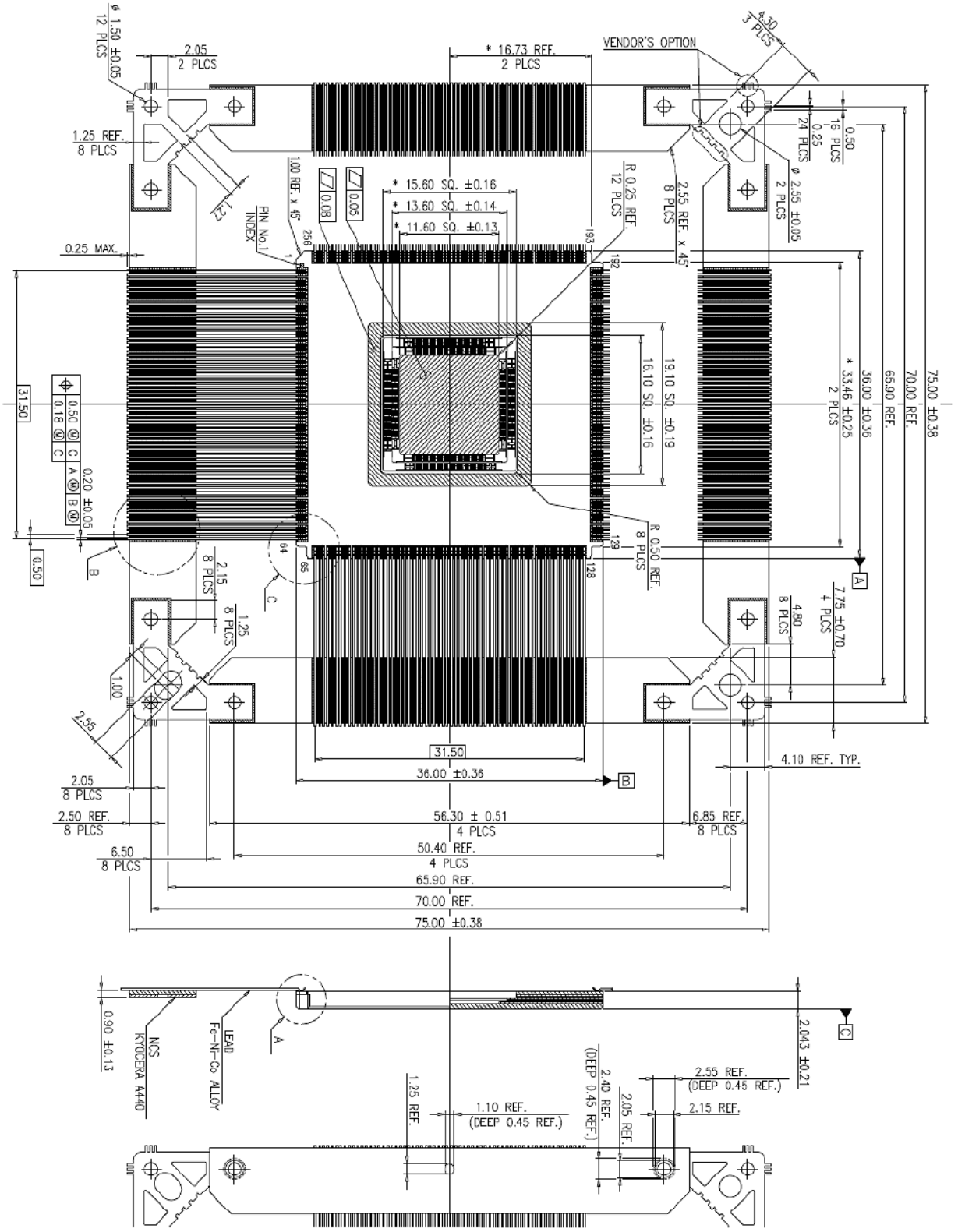
IP Group	IP Name	Function	IP Identification Number
Supply Pads	Pad_vdd_i	1.8V supply pad	[IP_1_1]
	Pad_vdd_o	5V supply pad	[IP_1_2]
	Pad_vdd_or	3.3V supply pad if no 5V is used	[IP_1_3]
	Pad_vdd_r	3.3V supply pad if 5V is used	[IP_1_4]
Ground and Substrate Pads	pad_gnd_all	Ground pad connecting all gnd rails	[IP_2_1]
	pad_gnd_i	Ground pad connecting i-rail	[IP_2_2]
	pad_gnd_or	Ground pad connecting or-rail	[IP_2_3]
	pad_substrate	Substrate pad	[IP_2_4]
Biasing and References	Bg_1v8	Bandgap reference for 1.8V supply	[IP_3_1]
	Bg_3v3	Bandgap reference for 3.3V supply	[IP_3_2]
	Refbiasgen_1v8	Current and voltage reference for 1.8V supply	[IP_3_3]
	refbiasgen_3v3	Current and voltage reference for 3.3V supply	[IP_3_4]
Data converter	Adc_sar_12b_222ks	12 bit analog to digital converter	[IP_5_1]
	Dac_12b_4mhz	12 bit digital to analog converter	[IP_5_2]
Frequency generation	Dcxo_5_50mhz	Crystal oscillator	[IP_6_1]
	Freq_gen_ring_0m6_to_600m	VCO with divider bank	[IP_6_2]
	Pll_frac_n	Fractional-n PLL	[IP_6_3]
	Loop_filter_325k	Integrated loop filter	[IP_6_4]
	Cml2cmos_alone	CML to CMOS converter	[IP_6_5]
	Cmos2cml_400u	CMOS to CML converter	[IP_6_6]
Analog circuits	Ldo_1v8_150m	LDO with 150 mA max. I out	[IP_7_1]
	Lvlshfthl (Note 1)	Analog level shifter from high to low	[IP_7_2]
	Lvlshftlh (Note 2)	Analog level shifter from low to high	[IP_7_3]
	Opv_multi_3v3	Multiple function operational amplifier	[IP_7_4]
	Tempsensor_ana_m40p150	Temperature sensor	[IP_7_5]
	Testmux33x4bit	Test multiplexer	[IP_7_6]
Memory	Otp_top	One time programmable ROM	[IP_8_1]
Control	Spi_shiftreg_tmr_tito	Register bank for SPI controller	[IP_9_1]
	Spi_refresh_tmr_tito	SPI controller	[IP_9_2]
	Lvlshft_tmr_1v8_3v3	Digital level shifter from 1.8V to 3.3V	[IP_9_3]
	Por_10u_porp_3u	Power on reset circuit	[IP_9_4]

NOTES:

1. The level shifter high to low has a parameter drift in the input to output transfer function up to 200mV.
2. The performance of the level shifter low to high at operating temperatures +85°C ≤ T_{amb} ≤ +125°C is not guaranteed.

1.8 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

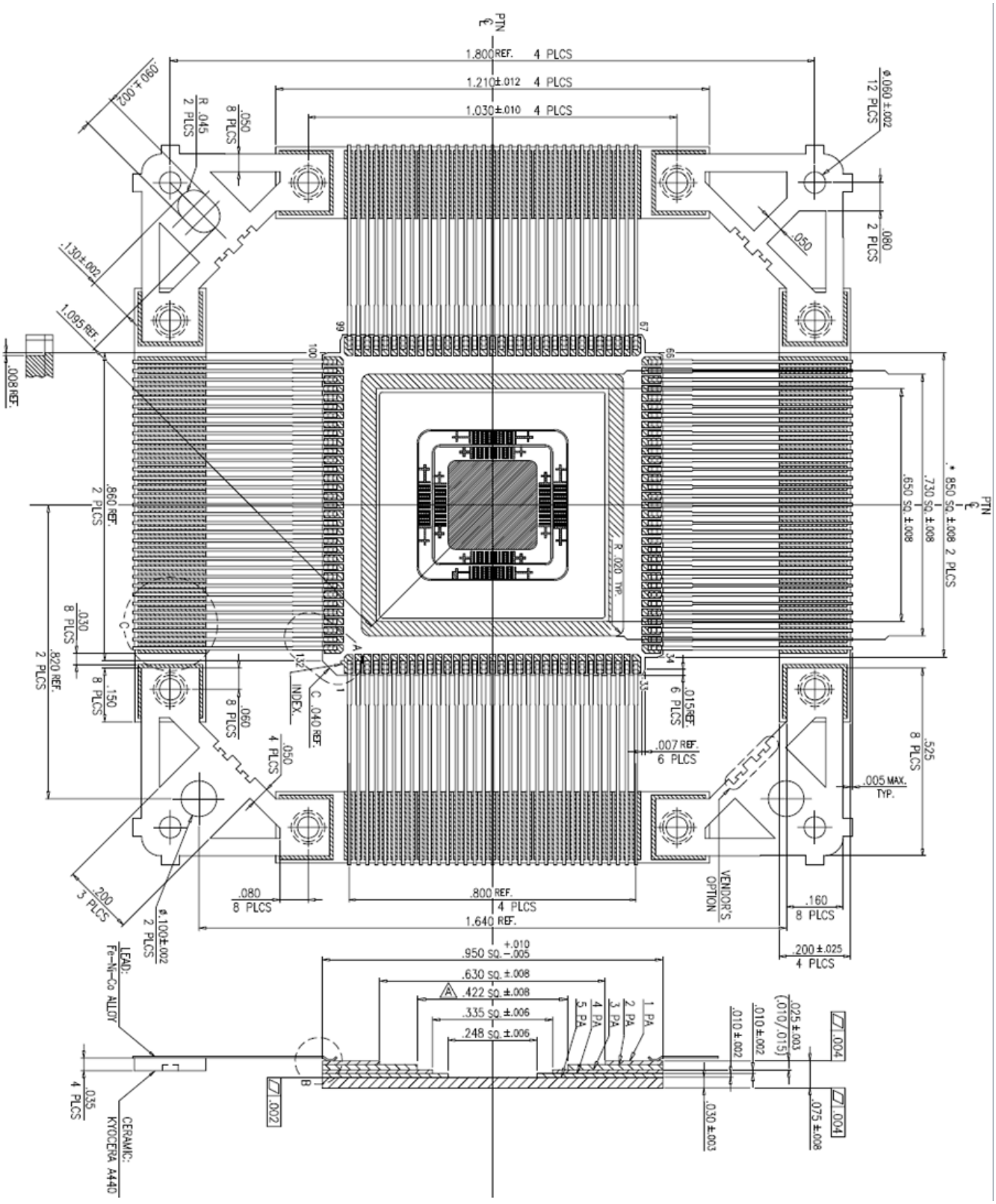
1.8.1 Ceramic Quad Flat Leaded Multilayer Package (CQFN-256) - 256 Leads (Variant 01)



NOTES:

1. Terminal identification is specified by reference to the chamfered corner and Pin No. 1 index as shown.

1.8.2 Ceramic Quad Flat Leaded Multilayer Package (CQFN-132_A) - 132 Leads (Variant 02)



NOTES:

1. Terminal identification is specified by reference to the chamfered corner and Pin No. 1 index as shown.

1.9 FUNCTIONAL DIAGRAM

See ASIC Datasheet.

1.10 PIN ASSIGNMENT

See ASIC Datasheet. Depending on the chosen package (Component Type Variant), the dedicated ground and substrate pins need to be considered as non-free selectable.

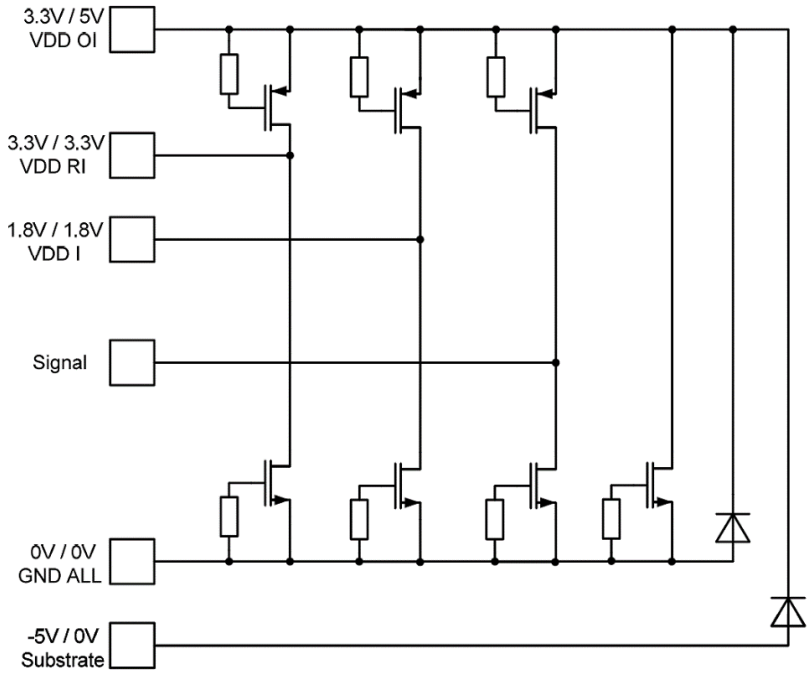
1.11 TRUTH TABLE AND TIMING DIAGRAMS

See ASIC Datasheet. Truth tables and timing diagrams for the IP libraries are also available from the Manufacturer.

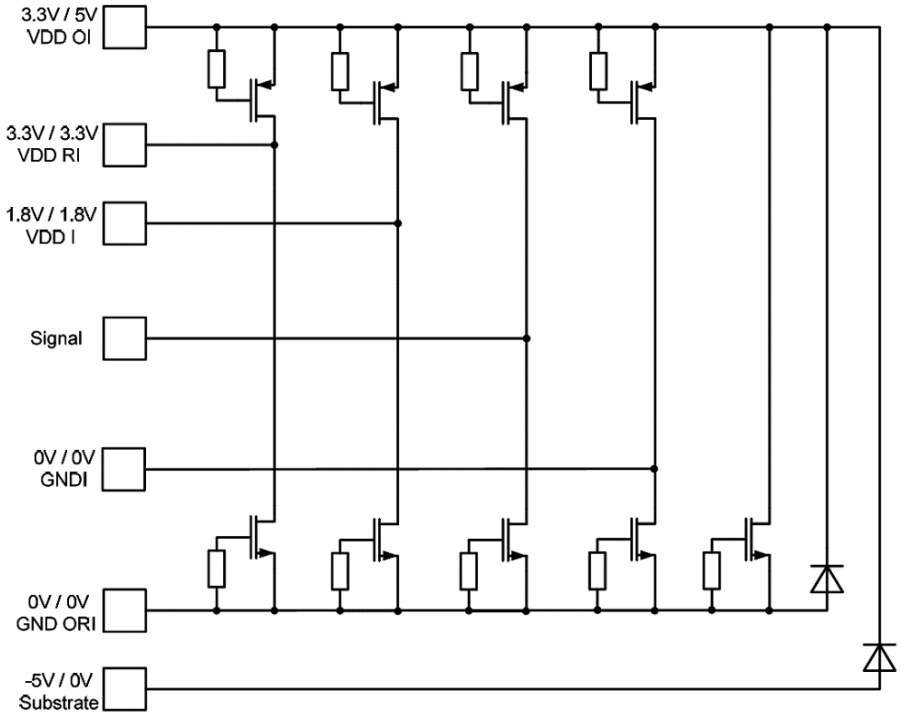
1.12 PROTECTION NETWORKS

Two different protection circuits are applicable: one for a common ground rail and one for an isolated ground between internal core ground and I/O ground. The highest supply voltage is either 3.3V or 5V depending on the I/O IPs used. The substrate can either be connected to ground, or tied to -5V if negative signals are required with respect to ground.

ESD principle in case of one common ground connection



ESD principle in case of isolated core ground to I/O ground



2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Screening Tests - Chart F3

High Temperature Reverse Bias Burn-in shall not be performed.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

As a minimum the information to be marked on the component shall be:

(a) The ESCC qualified components symbol (for ESCC qualified components only).
(b) The ESCC Component Number (see Para. 1.4.1).
(c) Traceability information.

The complete marking shall be as specified in the ASIC Datasheet.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES
Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements
The measurements shall be performed at T_{amb} = +22 ±3°C.

The parameters to be tested shall be specified in the ASIC Datasheet. Internal analogue interfaces will be tested with an integrated test mux in conjunction with a JTAG control of all required digital settings.

2.3.2 High and Low Temperatures Electrical Measurements
Unless otherwise specified the measurements shall be performed at T_{amb} = +125 (+0 -5)°C and T_{amb} = -40 (+5 -0)°C.

Unless otherwise specified the characteristics, test methods, conditions and limits shall be the same as specified for Para. 2.3.1, Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES
Unless otherwise specified, the parameter drift value measurements shall be performed at T_{amb} = +22 ±3°C.

For all intermediate and end-point electrical measurements during Burn-in and Operating Life testing, the tested parameter shall not vary by more than ±10% between initial measurement and the final measurement. Tested values are all parameter specified for the IP blocks as “tested parameters” as defined in the ASIC Datasheet.

The corresponding absolute limit values for all other specific characteristics shall not be exceeded.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS
Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3°C.

The tested values are all parameters specified for the IP blocks as “tested parameters”, or specified as “list of tested parameters for TID test” as a limited number of tests, as defined in the ASIC Datasheet.

2.6 POWER BURN-IN CONDITIONS
See ASIC Datasheet.

2.7 OPERATING LIFE CONDITIONS
Unless otherwise specified the conditions shall be as specified in Para. 2.6 for Power Burn-in.

2.8 TOTAL DOSE RADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing
Continuous bias shall be applied during irradiation testing as specified in the ASIC Datasheet.

The total dose level applied shall be as specified in Para. 1.4.2, in the ASIC Datasheet or in the Purchase Order.

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation testing the devices shall have successfully met Para. 2.3.1, Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at T_{amb} = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1, Room Temperature Electrical Measurements.

The parameters to be measured during and on completion of irradiation testing are specified in the ASIC Datasheet.

APPENDIX A
AGREED DEVIATIONS FOR IMST (D)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 1.2, Applicable Documents	The following IMST proprietary documents also apply: • IMST_SP_005: HARD Library Datasheet • IMST_RD_020: Abstract of Capability Domain
Para. 1.6, Handling Precautions	IMST performs ESD categorisation in accordance with the ESD requirements defined in MIL-STD-883. Therefore these components are categorised to level 1A per MIL-STD-883, Test Method 3015 with a Minimum Critical Path Failure Voltage of 500 Volts HBM.
Para. 2.1.1, Deviations from the Generic Specification: Para. 8.1 Internal Visual Inspection	Internal Visual Inspection shall be performed in accordance with the requirements detailed in the IMST PID including specific requirements of MIL-STD-883, Test Method 2017.

APPENDIX B
IMST ASIC DATASHEET "BOILERPLATE" TEXT FOR POWER BURN-IN AND OPERATING LIFE CONDITIONS

POWER BURN-IN CONDITIONS:
Power burn-in will be done according to MIL-STD-883, Test Method 1015, test condition D: Parallel excitation.

Burn-in is done under bias conditions for the circuit blocks. If possible, the bias condition should drive the ASIC to its maximum operating junction temperature of 135°C. If required, the LDO is loaded with an external resistor in order to drive the ASIC to the maximum junction temperature of +135°C.

Ambient temperature is set to +125°C.

Test duration is 240h with end point measurement within 96h after burn-in. Digital circuits will be stimulated in scan chain mode with scan chain test pattern.

OPERATING LIFE CONDITIONS:
Operating life conditions will be done according to MIL-STD-883, Test Method 1005, test condition D: Parallel excitation.

Test duration is 2000h based on ESCC 9000, Para. 8.25.

At 1000h, one intermediate measurement will be done.

Temperature, bias and stimuli conditions are the same as for Power Burn-in.