INTEGRATED CIRCUITS, SILICON MONOLITHIC, SINGLE PORT GIGABIT ETHERNET COPPER PHY WITH GMII / RGMII / MII / RMII INTERFACES

BASED ON TYPE VSC8541RT

ESCC Detail Specification No. 9405/020

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
1672	Specification updated to incorporate changes per DCR.

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1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.

(b) MIL-STD-883, Test Method Standard for Microcircuits.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 940502001F

- Detail Specification Reference: 9405020
- Component Type Variant Number: 01
- Total Dose Radiation Level Letter: F (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and Finish	Weight max g	Total Dose Radiation Level Letter (Notes 2, 3)
01	VSC8541RT	CQFP-68	D2 (Note 1)	7.5	F [50krad(Si)]

NOTES:

1. The terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.
2. Total dose radiation level letters are defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.
3. The Total Dose Radiation Level Letter (F) shall be validated as follows:
   - Tested up to 100krad(Si)

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage. Functional performance for extended periods at the maximum ratings may adversely affect device reliability.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in the Test Methods and Procedures of the applicable ESCC generic specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltages: Core Analog circuits at 1V Analog circuits at 2.5V Digital I/Os (V_{DDMAC}, V_{DDIO}, V_{DDMDIO})	 $V_{DD1(rated)}$ $V_{DD1A(rated)}$ $V_{DD25A(rated)}$ $V_{CC33(rated)}$	 -0.3 to 1.1 -0.3 to 1.1 -0.3 to 2.75 -0.3 to 3.6	V	Notes 1, 2
Operating Temperature Range	T_{op}	-55 to +125	°C	Note 1 T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	°C	
Junction Temperature	T_j	+175	°C	
Thermal Resistance, Junction-to-Case	$R_{th(j-c)}$	19	°C/W	
Soldering Temperature	T_{sol}	+345	°C	Note 3

NOTES:

1. The following operating conditions also apply. Device performance beyond these operating conditions is not guaranteed:

Characteristics	Symbols	Maximum Rated Operating Conditions		Units	Remarks
		Min	Max		
Supply Voltages: Core Analog circuits at 1V Analog circuits at 2.5V 3.3V Digital I/O's (V_{DDMAC}, V_{DDIO}, V_{DDMDIO}) 2.5V Digital I/O's (V_{DDMAC}, V_{DDIO}, V_{DDMDIO}) 1.8V Digital I/O's (V_{DDMAC}, V_{DDMDIO}) 1.5V Digital I/O's (V_{DDMAC}, V_{DDMDIO}) 1.2V Digital I/O's (V_{DDMDIO})	 V_{DD1} V_{DD1A} V_{DD25A} V_{CC33} V_{CC25} V_{CC18} V_{CC15} V_{CC12}	 0.95 0.95 2.38 3.135 2.38 1.71 1.425 1.14	 1.05 1.05 2.62 3.465 2.62 1.89 1.575 1.26	V	Note 2
Operating Temperature Range	T_{op}	As per Maximum Ratings table			T_{amb}

2. With reference to V_{SS} = 0V (see Para. 1.9).
3. Duration 10 seconds maximum at a distance of not less than 1.6 mm from the device body and the same terminal shall not be re-soldered until 3 minutes have elapsed.

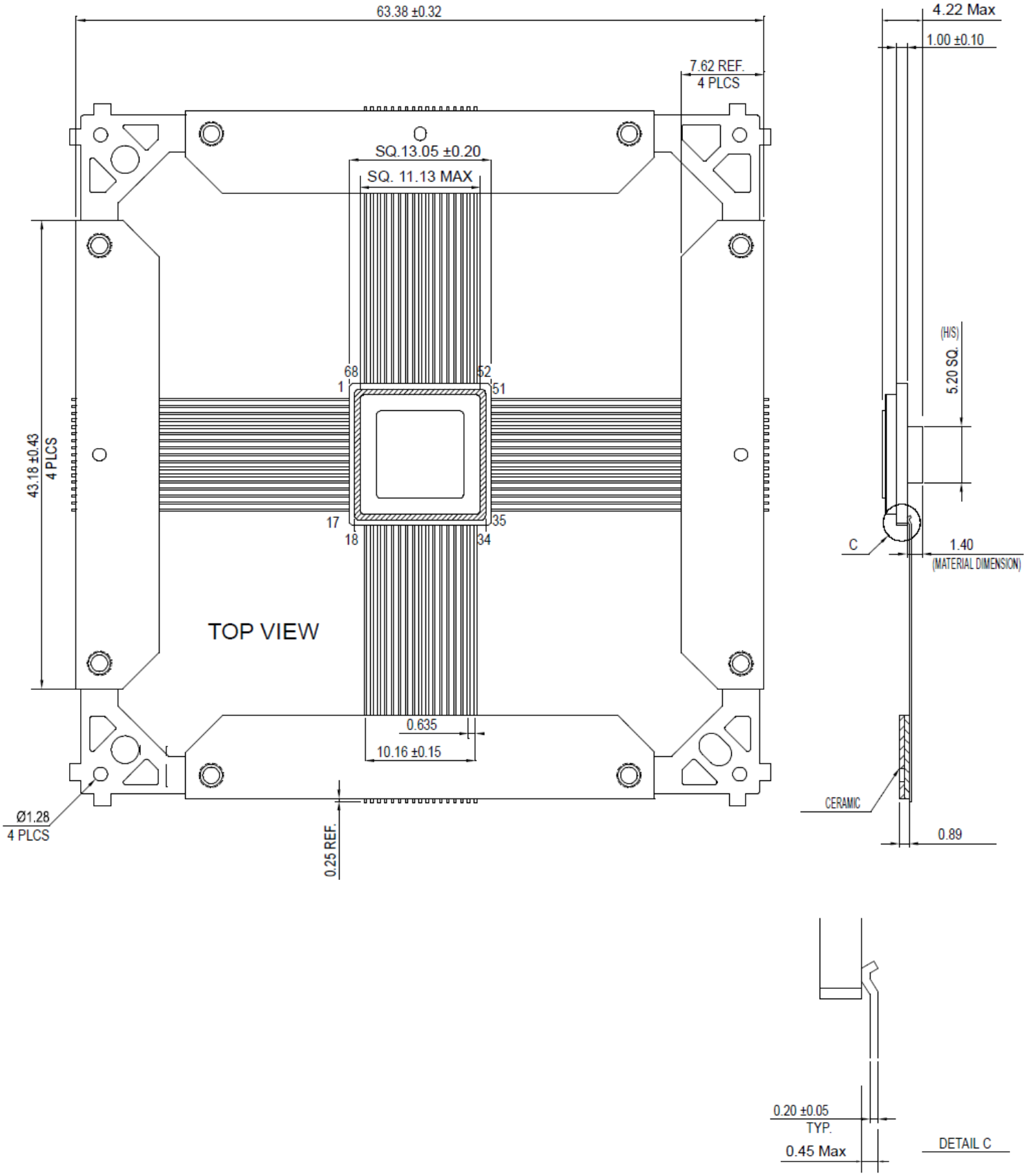
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

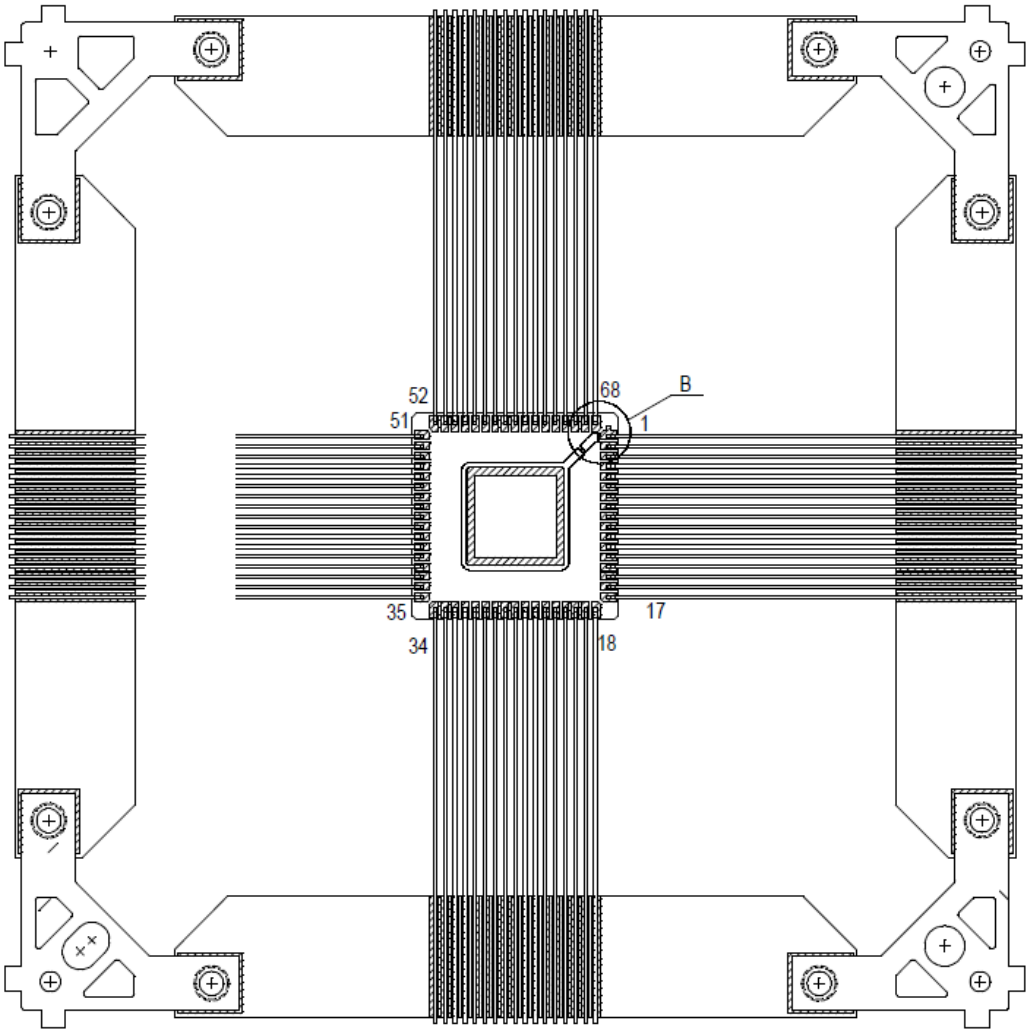
These components are categorised as Class 2 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 2000 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

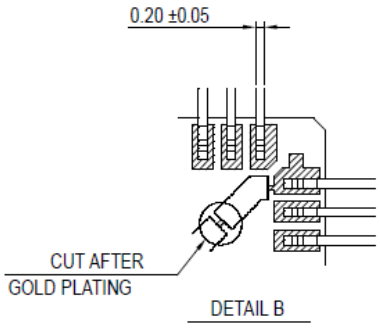
Ceramic Quad Flat Package (CQFP-68) – 68 Tied Leads



Ceramic Quad Flat Package (CQFP-68) – 68 Tied Leads (Cont.)



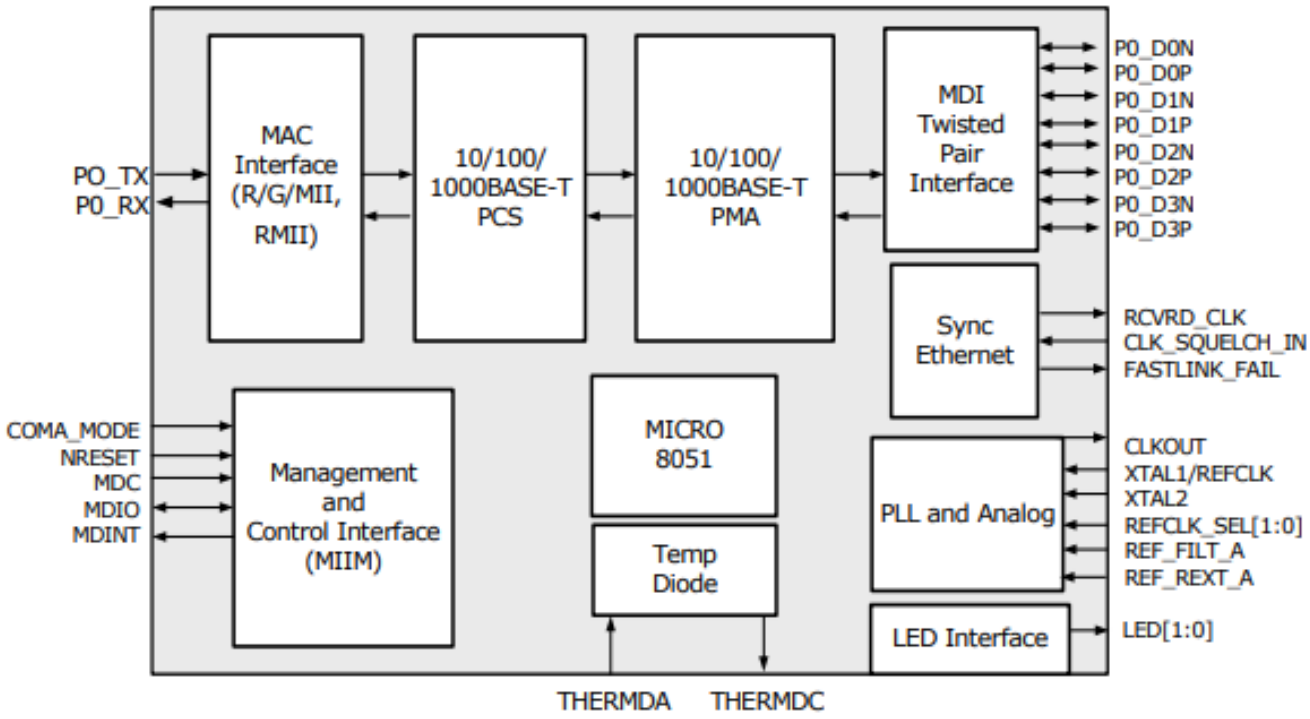
BOTTOM VIEW



NOTES:

1. Terminal identification is specified by reference to the index mark (see detail B).
2. Dimensions in mm.

1.8 FUNCTIONAL DIAGRAM



1.9 PIN ASSIGNMENT

Pin No.	Name	Description	Pin No.	Name	Description
1	REF_REXT	Reference connected via an external 2kΩ (±1%) resistor to analog ground	35	TX_ER	GMII/MII transmit data error input
2	VDD25A	2.5V analog power requiring additional PCB power supply filtering	36	MII_TXCLK	MII transmit clock output. The logic state on this pin is latched on the rising edge of NRESET to configure the device
3	P0_D3N	Tx/Rx channel D negative signal. Unused in 10BASE-T and 100BASE-TX modes, connect to pin 4 via a 100Ω (±5%) resistor	37	GTX_CLK	GMII/RGMII transmit clock input
4	P0_D3P	Tx/Rx channel D positive signal. Unused in 10BASE-T and 100BASE-TX modes, connect to pin 3 via a 100Ω (±5%) resistor	38	TXD0	GMII/MII/RGMII data input
5	VDD1A	1V analog power requiring additional PCB power supply filtering	39	VDDMAC	1.5V, 1.8V, 2.5V or 3.3V GMII/MII/RGMII/RMII MAC power
6	P0_D2N	Tx/Rx channel C negative signal. Unused in 10BASE-T and 100BASE-TX modes, connect to pin 7 via a 100Ω (±5%) resistor	40	TXD1	GMII/MII/RGMII data input

Pin No.	Name	Description	Pin No.	Name	Description
7	P0_D2P	Tx/Rx channel C positive signal. Unused in 10BASE-T and 100BASE-TX modes, connect to pin 6 via a 100Ω (±5%) resistor	41	TXD2	GMII/MII/RGMII data input
8	VDD25A	2.5V analog power requiring additional PCB power supply filtering	42	TXD3	GMII/MII/RGMII data input
9	P0_D1N	Tx/Rx channel B negative signal	43	TXD4	GMII data input
10	P0_D1P	Tx/Rx channel B positive signal	44	VDDMAC	1.5V, 1.8V, 2.5V or 3.3V GMII/MII/RGMII/RMII MAC power
11	VDD25A	2.5V analog power requiring additional PCB power supply filtering	45	TXD5	GMII data input
12	P0_D0N	Tx/Rx channel A negative signal	46	TXD6	GMII data input
13	P0_D0P	Tx/Rx channel A positive signal	47	TXD7	GMII data input
14	VDD1A	1V analog power requiring additional PCB power supply filtering	48	MDC	Management data clock. A 0 MHz to 12.5MHz reference input is used to clock serial MDIO data into and out of the PHY
15	THERMDA	Thermal Diode Anode	49	VDDMDIO	1.2V, 1.5V, 1.8V, 2.5V or 3.3V power for SMI pins
16	THERMDC_VSS	Thermal Diode Cathode connected to device ground. Temperature sensor must be chosen accordingly	50	MDIO	Management data input/output pin. Serial data is written or read form this pin bidirectionally between the PHY and station manager synchronously on the positive edge of MDC. One external pull-up resistor is required at the station manager
17	VDD1	1V digital core power	51	MDINT	Management interrupt signal. These pins can be tied together in a wired-OR configuration with only a single pull-up resistor
18	COL	GMII/MII collision output. The logic state on this pin is latched on the rising edge of NRESET to configure the device	52	FASTLINK_FAIL	Fast link failure indication signal
19	CRS	GMII/MII carrier sense output. The logic state on this pin is latched on the rising edge of NRESET to configure the device	53	NRESET	Device reset. Active low input that powers down the device and sets all register bits to their default state

Pin No.	Name	Description	Pin No.	Name	Description
20	RXD7	GMII data output. The logic state on this pin is latched on the rising edge of NRESET to configure the device	54	CLKOUT	Clock output, can be enabled or disabled. Output a clock based on the local reference clock with programmable frequency. This pin is not active when NRESET is asserted and is disabled by default. When disabled, the pin is held low. The logic state on this pin is latched on the rising edge of NRESET to configure CLKOUT output
21	RXD6	GMII data output. The logic state on this pin is latched on the rising edge of NRESET to configure the device	55	RCVRD_CLK	Recovered clock output, can be enabled or disabled. Output a clock based on the selected active media with programmable frequency. This pin is not active when NRESET is asserted. When disabled, the pin is held low
22	VDDMAC	1.5V, 1.8V, 2.5V or 3.3V GMII/MII/RGMII/RMII MAC power	56	COMA_MODE	When this pin is asserted high, PHY is held in a powered down state. When deasserted low, PHY is powered up and resumes normal operation. This signal is also used to synchronize the operation of multiple chips on the same PCB to provide visual synchronization for LEDs driven by separate chips
23	RXD5	GMII data output. The logic state on this pin is latched on the rising edge of NRESET to configure the device	57	CLK_SQUELCH_IN	Input control to squelch recovered clock
24	RXD4	GMII data output. The logic state on this pin is latched on the rising edge of NRESET to configure the device	58	VDDIO	2.5V or 3.3V general I/O power
25	RXD3	GMII/MII/RGMII data output. The logic state on this pin is latched on the rising edge of NRESET to configure the device	59	LED1	LED direct drive outputs. All LED pins are active low. LED_CLK output in serial LED mode
26	RXD2	GMII/MII/RGMII data output. The logic state on this pin is latched on the rising edge of NRESET to configure the device	60	LED0	LED direct drive outputs. All LED pins are active low. LED_DATA output in serial LED mode

Pin No.	Name	Description	Pin No.	Name	Description
27	RXD1	GMII/MII/RGMII data output. The logic state on this pin is latched on the rising edge of NRESET to configure the device	61	REFCLK_SEL_1	Reference clock mode/frequency select signal
28	VDDMAC	1.5V, 1.8V, 2.5V or 3.3V GMII/MII/RGMII/RMII MAC power	62	REFCLK_SEL_0	Reference clock mode/frequency select signal
29	RXD0	GMII/MII/RGMII data output. The logic state on this pin is latched on the rising edge of NRESET to configure the device	63	XTAL1	Crystal/single ended reference clock input
30	RX_DV/RX_CTL	GMII/MII receive data valid output/RGMII receive control output. The logic state on this pin is latched on the rising edge of NRESET to configure the device	64	XTAL2	Crystal output, leave unconnected when using single ended reference clock
31	RX_ER	GMII/MII receive data error output. The logic state on this pin is latched on the rising edge of NRESET to configure the device	65	RESERVED_1	Reserved signal, leave unconnected
32	RX_CLK	GMII/MII receive clock output. The logic state on this pin is latched on the rising edge of NRESET to configure the device	66	RESERVED_0	Reserved signal, leave unconnected
33	TX_EN/TX_CTL	GMII/MII transmit data enable input/RGMII transmit data control input	67	REF_FILT	Reference filter connected via an external 0.01µF (±20%) capacitor to analog ground
34	VDD1	1V digital core power	68	VDD1A	1V analog power requiring additional PCB power supply filtering

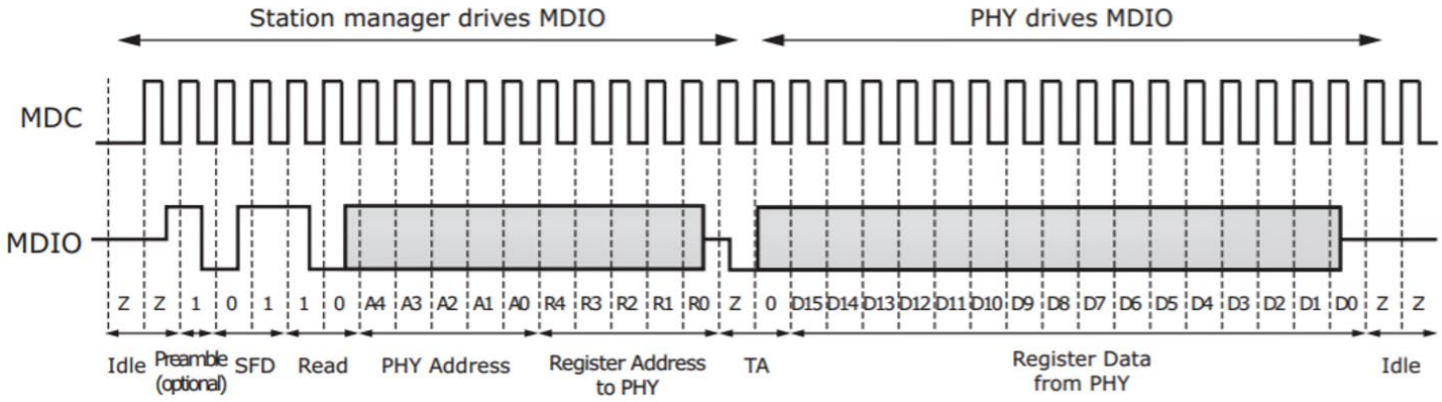
NOTES:

1. Internal V_{SS} is connected to the package heat sink which shall be connected to GND.

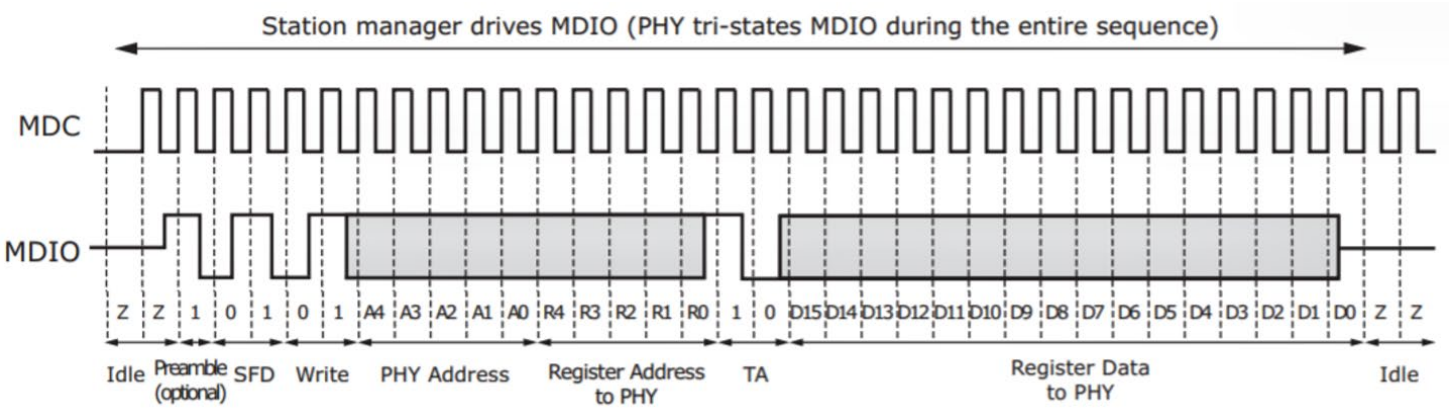
1.10 INSTRUCTION SET AND TIMING DIAGRAMS

Ethernet timings are verified through functional tests in loopback mode (1000Mb/s and 100Mb/s). Serial management interface (SMI) timing is tested through a specific test, SMI timing of 85x1 micro. These diagrams are shown below:

SMI READ FRAME



SMI WRITE FRAME



1.11 PROTECTION NETWORK

Pads are protected with standard I/O protection, wafer manufacturer proprietary and confidential.

2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirements and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviations from Production Control for Packaged Components – Chart F2A

(a) Paras. 5.3.2(a), 8.1, Internal Visual Inspection (MIL-STD-883 Test Method 2010 Condition A): The minimum separation between 2 internal wires shall be one wire diameter or 25.4µm, whichever is greater.

2.1.1.2 Deviations from Screening Tests for Packaged Components – Chart F3A

(a) Para. 8.15, High Temperature Reverse Bias Burn-in: Shall not be performed.

2.1.1.3 Deviations from Qualification and Periodic Tests for Packaged Components – Chart F4A

(a) The following additional tests shall be performed as part of the Assembly Capability Subgroup:

Test Description	Test Method	Test Quantity
Bond pull test	MIL-STD-883, TM 2011	4 components, 100% of wires
Ball shear test	JESD22-B116	50% of balls over 4 components
Bond pull test after bake: 1h/300°C	MIL-STD-883, TM 2011	4 components, 100% of wires
Ball shear test after bake: 1h/300°C	JESD22-B116	50% of balls over 4 components

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification (see Para. 1.7).
(b) The ESCC qualified components symbol (for ESCC qualified component only).
(c) The ESCC Component Number (see Para. 1.4.1).
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{case} = +25(+3 -5)°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Functional Tests	-	3014	Self-tests (ATPG, BIST, DLOOP100, DLOOP1000, GMII, RGMII)	-	-	-
High Level Output Voltage	V_{OH}	3006	Outputs @2.5V drive 24mA: CLKOUT, COMA_MODE, FASTLINK_Fail, LED0, LED1, RCVRD_CLK, MDC, MDINT, MDIO	1.9	-	V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Low Level Output Voltage	V_{OL}	3007	Outputs @2.5V drive 24mA: CLKOUT, COMA_MODE, FASTLINK_Fail, LED0, LED1, RCVRD_CLK, MDC, MDINT, MDIO	-	420	mV
Low Level Input Current	I_{IL}	3009	Bi Dir2 = MDINT	-1	1	µA
			Input = XTAL1	-2	2	
Low Level Input Current with Pull-down	I_{ILPD}	3009	Bi Dir2 = CLKOUT	-2	2	µA
			Bi Dir = RXD0 to 7, TXD0 to 7, TX_CLK, TX_ER, TX_EN_TX_CTL CRS, GTX_CLK, RX_CLK, RX_DV_RX_CTL, RX_ER, RCVRD_CLK, LED1, LED0, COL, FASTLINK_Fail, MDIO, MDC	-2	2	
			Input = NRESET, MODE_SEL1_TANA1, MODE_SEL0_TANA0, CLK_SQUELCH_IN	-2	2	
Low Level Input Current with Pull-up	I_{ILPU}	3009	Input = REFCLK_SEL1, REFCLK_SEL0	-74	-30	µA
			Bi Dir = COMA_MODE	-73.4	-30	
High Level Input Current	I_{IH}	3010	Bi Dir2 = MDINT	-1	1	µA
			Bi Dir = COMA_MODE, MDC, MDIO	-1	1	
			Input = REFCLK_SEL1, REFCLK_SEL0	-1	1	
High Level Input Current with Pull-down	I_{IHPD}	3010	Bi Dir2 = CLKOUT	25	68	µA
			Bi Dir = RXD0 to 7, TXD0 to 7, TX_CLK, TX_ER, TX_EN_TX_CTL CRS, GTX_CLK, RX_CLK, RX_DV_RX_CTL, RX_ER, RCVRD_CLK, LED1, LED0, COL, FASTLINK_Fail	25	68	
			Input = XTAL1	-2	2	
High Level Input Current with Pull-down	I_{IHPD}	3010	Input Pull Down = NRESET, MODE_SEL1_TANA1, MODE_SEL0_TANA0, CLK_SQUELCH_IN	22	68	µA
Reference Voltage 1	REF_FILT	-	-	1.164	1.24	V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Reference Voltage 2	REF_REXT	-	-	0.976	1.03	V
Static Current Consumption	$IDD1_S$	3005	V_{DD1max}, Note 2	-	40	mA
	$IDD1A_S$	3005	$V_{DD1Amax}$, Note 2	-	5	mA
	$IDD25A_S$	3005	$V_{DD25Amax}$, Note 2	-	2	mA
	$IDDIO_S$	3005	$V_{CC33max}$, Note 2	-	0.5	mA
	$IDDMAC_S$	3005	$V_{CC33max}$, Note 2	-	0.3	mA
	$IDDMDIO_S$	3005	$V_{CC33max}$, Note 2	-	1	mA
Static Power	P_{STATIC}	-	-	-	20	mW
Dynamic Current Consumption (Note 1)	$IDD1_D$	3005	V_{DD1max}, Note 2	-	110	mA
	$IDD1A_D$	3005	$V_{DD1Amax}$, Note 2	-	35	mA
	$IDD25A_D$	3005	$V_{DD25Amax}$, Note 2	-	190	mA
	$IDDIO_D$	3005	$V_{CC33max}$, Note 2	-	30	mA
	$IDDMAC_D$	3005	$V_{CC33max}$, Note 2	-	90	mA
	$IDDMDIO_D$	3005	$V_{CC33max}$, Note 2	-	2	mA
Dynamic Power (Note 1)	$P_{DYNAMIC}$	-	-	-	750	mW
ADC (Cal Lower and Cal Upper)	ADC_{CalL}, ADC_{CalU}	-	-	0	9	-
AFE10, DC Threshold	$AFE10_1$	-	-	-3	2.5	-
AFE10, Threshold	$AFE10_2$	-	-	0	2	-
AFE10, Error (Min or Max)	$AFE10_3$	-	-	0	1	-
AFE10, Zcal (Min or Max)	$AFE10_4$	-	-	0.95	1.05	-
AFE1000, DC Threshold	$AFE1000_1$	-	-	0	5	-
AFE1000, Error Threshold	$AFE1000_2$	-	-	0	2.5	-
AFE1000, Gain Error	$AFE1000_3$	-	-	0	0.12	-
AFE1000, STD Error	$AFE1000_4$	-	-	0	0.8	-
ALOOP Slicer	$ALOOP_S$	-	-	-37.8	-25	-
Clock Out	CLK125a	-	XTAL_125MHz_ClkOut_125MHz	124.95	125.05	MHz
	CLK025	-	XTAL_125MHz_ClkOut_25MHz	24.99	25.01	MHz
	CLK050	-	XTAL_125MHz_ClkOut_50MHz	49.98	50.02	MHz
	CLK125b	-	XTAL_25MHz_ClkOut_125MHz	124.95	125.05	MHz
	CLK125c	-	XTAL_50MHz_ClkOut_125MHz	124.95	125.05	MHz

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
TANA0	$TANA0_1$	-	ADC Ref Voltage	0.15	0.45	V
	$TANA0_2$	-	Com Ref Current	-55	-12.2	µA
	$TANA0_3$	-	TX Ref Current	-53.5	-12.2	µA
	$TANA0_4$	-	Mirror Ref Current	-45	-12.2	µA
TANA1	$TANA1_1$	-	ADC Ref Voltage	0.65	1.25	V
	$TANA1_2$	-	Com Ref Current	-53.5	-12.2	µA
	$TANA1_3$	-	TX Ref Current	-53.3	-12.2	µA
	$TANA1_4$	-	Mirror Ref Current	-53.5	-13	µA
TXV Vocm	TXV	-	Pin Diff	1.175	1.235	V

NOTES:
1. Tested GO-NO-GO only.
2. See Para. 1.5, Note 1.

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{case} = +125 ±3°C and T_{case} = -55 ±3°C.

The characteristics, test methods, conditions and limits shall be the same as specified in Para. 2.3.1, Room Temperature Electrical Measurements, except for the parameters shown in the tables below:

HIGH TEMPERATURE ELECTRICAL MEASUREMENTS (T_{case} = +125 ±3°C)

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
Static Current Consumption	$IDD1_S$	3005	V_{DD1max}, Note 2	-	90	mA
	$IDD1A_S$	3005	$V_{DD1Amax}$, Note 2	-	18	mA
Dynamic Current Consumption (Note 1)	$IDD1_D$	3005	V_{DD1max}, Note 2	-	200	mA
	$IDD1A_D$	3005	$V_{DD1Amax}$, Note 2	-	50	mA
	$IDD25A_D$	3005	$V_{DD25Amax}$, Note 2	-	200	mA

NOTES:
1. Tested GO-NO-GO only.
2. See Para. 1.5, Note 1.

LOW TEMPERATURE ELECTRICAL MEASUREMENTS (T_{case} = -55 ±3°C)

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions	Limits		Units
				Min	Max	
AFE1000, Gain Error	$AFE1000_3$	-	-	0	0.14	-

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{case} = +25(+3 -5)°C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1, Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Low Level Input Current	I_{IL}	±0.1	-1	1	µA
High Level Input Current	I_{IH}	±0.1	-1	1	µA
Static Current Consumption	$IDD1_S$	±5	-	40	mA
	$IDD1A_S$	±500	-	5000	µA
	$IDD25A_S$	±50	-	2000	µA
Low Level Output Voltage	V_{OL}	±100	-	420	mV
High Level Output Voltage	V_{OH}	±100	1900	-	mV

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{case} = +25(+3 -5)°C.

The characteristics, test methods, conditions and limits shall be the same as specified in Para. 2.3.1, Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125(+8 -0)	°C
Core Supply Voltage	V_{Test1}	1.1	V
I/O Supply Voltage	V_{Test2}	3.6	V
1V Analog Supply Voltage	V_{Test3}	1.1	V
2.5V Analog Supply Voltage	V_{Test4}	2.75	V
Forcing Inputs	Clock1	125	MHz
Programmed inputs (Note 1)	Clock2/Clock3	Special pattern generator	-

NOTES:

1. The code sent through MDIO and MDC pins set the chip in connector loopback mode at 1000Mb/s RGMII mode with 125MHz clkout. It runs Ethernet Packet Generator (EPG) in continuous, 64B and random payload. Therefore, the VSC8541RT is run at its maximum speed and activity.

2. Pin connections shall be as follows, where N/A = not applicable and NC = not connected:

Pin	Name	Serial R or C	Wired To	Pin	Name	Serial R or C	Wired To
1	REF_REXT	2kΩ	GND	35	TX_ER	40Ω	RX_ER
2	VDD25A	N/A	V_{Test4}	36	MII_TXCLK	-	NC
3	P0_D3N	100nF	P0_D2N	37	GTX_CLK	40Ω	RX_CLK
4	P0_D3P	100nF	P0_D2P	38	TXD0	40Ω	RXD0
5	VDD1A	N/A	V_{Test3}	39	VDDMAC	N/A	V_{Test2}
6	P0_D2N	100nF	P0_D3N	40	TXD1	40Ω	RXD
7	P0_D2P	100nF	P0_D3P	41	TXD2	40Ω	RXD
8	VDD25A	N/A	V_{Test4}	42	TXD3	40Ω	RXD
9	P0_D1N	100nF	P0_D0N	43	TXD4	40Ω	RXD
10	P0_D1P	100nF	P0_D0P	44	VDDMAC	N/A	V_{Test2}
11	VDD25A	N/A	V_{Test4}	45	TXD5	40Ω	RXD
12	P0_D0N	100nF	P0_D1N	46	TXD6	40Ω	RXD
13	P0_D0P	100nF	P0_D1P	47	TXD7	40Ω	RXD
14	VDD1A	N/A	V_{Test1}	48	MDC	N/A	Clock2
15	THERMDA	-	NC	49	VDDMDIO	N/A	V_{Test2}
16	THERMDC_VSS	-	GND	50	MDIO	N/A	Clock3
17	VDD1A	N/A	V_{Test1}	51	MDINT	10kΩ	V_{Test2}
18	COL	-	NC	52	FASTLINK_FAIL	-	NC
19	CRS	-	NC	53	NRESET	10kΩ	V_{Test2}
20	RXD7	40Ω	TXD7	54	CLKOUT	5pF	GND
21	RXD6	40Ω	TXD6	55	RCVRD_CLK	10kΩ	GND
22	VDDMAC	N/A	V_{Test2}	56	COMA_MODE	10kΩ	GND
23	RXD5	40Ω	TXD5	57	CLK_SQUELCH_IN	10kΩ	GND
24	RXD4	40Ω	TXD4	58	VDDIO	N/A	V_{Test2}
25	RXD3	40Ω	TXD3	59	LED1	1kΩ	LED1
26	RXD2	40Ω	TXD2	60	LED0	1kΩ	LED0
27	RXD1	40Ω	TXD1	61	REFCLK_SEL_1	10kΩ	V_{Test2}
28	VDDMAC	N/A	V_{Test2}	62	REFCLK_SEL_0	10kΩ	V_{Test2}
29	RXD0	40Ω	TXD0	63	XTAL1	N/A	Clock1
30	RX_DV/RX_CTL	40Ω	TX_EN	64	XTAL2	-	NC
31	RX_ER	40Ω	TX_ER	65	RESERVED_1	-	NC
32	RX_CLK	40Ω	GTX_CLK	66	RESERVED_0	-	NC
33	TX_EN/TX_CTL	40Ω	RX_DV	67	REF_FILT	10nF	GND
34	VDD1	N/A	V_{Test1}	68	VDD1A	N/A	V_{Test3}

3. All differential pairs have 100Ω terminations between P0_D1N & P0D1P, P0_D2N & P0D2P P0_D3N & P0D3P, P0_D3N & P0D3P

2.7 OPERATING LIFE CONDITIONS

The conditions shall be as specified in Para. 2.6, Power Burn-in Conditions.

2.8 TOTAL DOSE IRRADIATION TESTING

2.8.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified below.

Unless otherwise specified the total dose level applied shall be as specified in Para. 1.4.2 or in the Purchase Order.

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+25(+3 -5)	°C
Core Supply Voltage	V_{Test1}	1.1	V
I/O Supply Voltage	V_{Test2}	3.6	V
1V Analog Supply Voltage	V_{Test3}	1.1	V
2.5V Analog Supply Voltage	V_{Test4}	2.75	V

NOTES:

1. Pin connections shall be as follows, where N/A = not applicable and NC = not connected:

Pin	Name	Serial R or C	Wired To	Pin	Name	Serial R or C	Wired To
1	REF_REXT	2kΩ	GND	35	TX_ER	1kΩ	V_{Test2}
2	VDD25A	N/A	V_{Test4}	36	MII_TXCLK	-	NC
3	P0_D3N	-	NC	37	GTX_CLK	1kΩ	V_{Test2}
4	P0_D3P	-	NC	38	TXD0	1kΩ	V_{Test2}
5	VDD1A	N/A	V_{Test3}	39	VDDMAC	N/A	V_{Test2}
6	P0_D2N	-	NC	40	TXD1	1kΩ	V_{Test2}
7	P0_D2P	-	NC	41	TXD2	1kΩ	V_{Test2}
8	VDD25A	N/A	V_{Test4}	42	TXD3	1kΩ	V_{Test2}
9	P0_D1N	-	NC	43	TXD4	1kΩ	V_{Test2}
10	P0_D1P	-	NC	44	VDDMAC	N/A	V_{Test2}
11	VDD25A	N/A	V_{Test4}	45	TXD5	1kΩ	V_{Test2}
12	P0_D0N	-	NC	46	TXD6	1kΩ	V_{Test2}
13	P0_D0P	-	NC	47	TXD7	1kΩ	V_{Test2}
14	VDD1A	N/A	V_{Test3}	48	MDC	10kΩ	GND
15	THERMDA	-	GND	49	VDDMDIO	N/A	V_{Test2}
16	THERMDC_VSS	-	GND	50	MDIO	10kΩ	V_{Test2}
17	VDD1	N/A	V_{Test1}	51	MDINT	10kΩ	V_{Test2}
18	COL	1kΩ	V_{Test2}	52	FASTLINK_FAIL	N/A	$V_{Test2}/2$
19	CRS	1kΩ	V_{Test2}	53	NRESET	10kΩ	GND
20	RXD7	1kΩ	V_{Test2}	54	CLKOUT	N/A	$V_{Test2}/2$

Pin	Name	Serial R or C	Wired To	Pin	Name	Serial R or C	Wired To
21	RXD6	1kΩ	V_{Test2}	55	RCVRD_CLK	N/A	$V_{Test2}/2$
22	VDDMAC	N/A	V_{Test2}	56	COMA_MODE	N/A	$V_{Test2}/2$
23	RXD5	1kΩ	V_{Test2}	57	CLK_SQUELCH_IN	1kΩ	V_{Test2}
24	RXD4	1kΩ	V_{Test2}	58	VDDIO	N/A	V_{Test2}
25	RXD3	1kΩ	V_{Test2}	59	LED1	N/A	$V_{Test2}/2$
26	RXD2	1kΩ	V_{Test2}	60	LED0	N/A	$V_{Test2}/2$
27	RXD1	1kΩ	V_{Test2}	61	REFCLK_SEL_1	10kΩ	V_{Test2}
28	VDDMAC	N/A	V_{Test2}	62	REFCLK_SEL_0	10kΩ	V_{Test2}
29	RXD0	1kΩ	V_{Test2}	63	XTAL1	-	GND
30	RX_DV/RX_CTL	1kΩ	V_{Test2}	64	XTAL2	N/A	$V_{Test2}/2$
31	RX_ER	1kΩ	V_{Test2}	65	RESERVED_1	-	NC
32	RX_CLK	1kΩ	V_{Test2}	66	RESERVED_0	-	NC
33	TX_EN/TX_CTL	1kΩ	V_{Test2}	67	REF_FILT	1µF	GND
34	VDD	N/A	V_{Test1}	68	VDD1A	N/A	V_{Test3}

2. $V_{Test2}/2$ is High Z state (using one 5.6kΩ at GND and another 5.6kΩ at V_{Test2})

2.8.2 Electrical Measurements for Total Dose Radiation Testing

Prior to, during and on completion of irradiation testing the devices shall have successfully met the Room Temperature Electrical Measurements specified in Para. 2.3.1.

Unless otherwise stated the measurements shall be performed at T_{case} = +25(+3 -5)°C.

The characteristics, test methods, conditions and limits shall be as per the corresponding test defined in Para. 2.3.1, Room Temperature Electrical Measurements.