TRANSISTORS, MATCHED DUAL, NPN

BASED ON TYPE 2N2919, 2N2920 AND 2N2920A

ESCC Detail Specification No. 5207/002

Issue 11	November 2024

Document Custodian: European Space Agency – see https://escies.org

LEGAL DISCLAIMER AND COPYRIGHT

DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
1684	Specification updated to incorporate changes per DCR.

TABLE OF CONTENTS

1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 5000
(b) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 520700210

- Detail Specification Reference: 5207002
- Component Type Variant Number: 10 (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Lead/Terminal Material and/or Finish (Note 1)	Weight max g
10	2N2919	CCP	2	0.2
11	2N2920	CCP	2	0.2
12	2N2920A	CCP	2	0.2
13	2N2919	CCP	4	0.2
14	2N2920	CCP	4	0.2
15	2N2920A	CCP	4	0.2
16	2N2920A	FP	G2	0.7
17	2N2920A	FP	G4	0.7
18	2N2920A	Die (Note 2)	N/A	N/A

NOTES:

1. The lead/terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.
2. Variant 18 is a single transistor die; this Variant shall be ordered, tested and delivered in matched pairs. See Para. 1.6.3.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

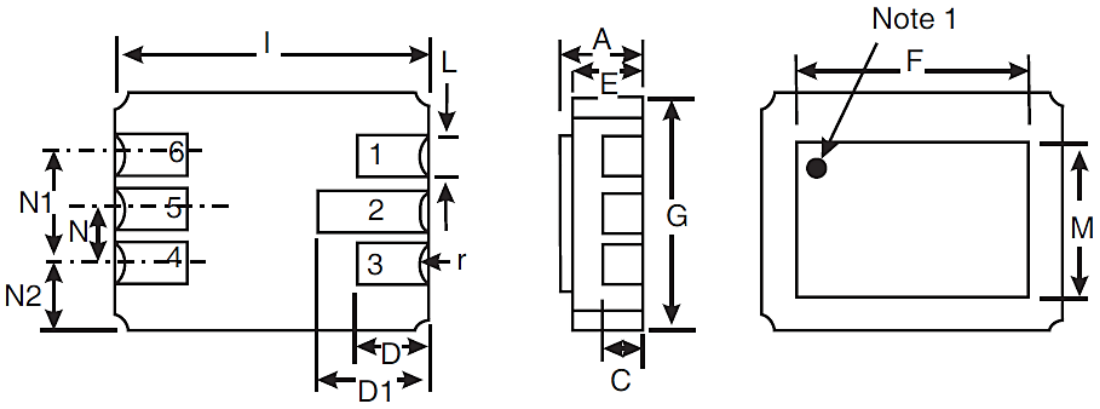
Characteristics	Symbols	Maximum Ratings	Unit	Remarks
Collector-Base Voltage	V_{CBO}	60	V	Over entire operating temperature range
Collector-Emitter Voltage	V_{CEO}	60	V	
Emitter-Base Voltage	V_{EBO}	6	V	
Collector Current	I_C	30	mA	Continuous
Power Dissipation (One Section)	P_{totO}	0.3	W	At $T_{amb} \leq +25°C$
Power Dissipation (Both Sections)	P_{totB}	0.5	W	At $T_{amb} \leq +25°C$
Thermal Resistance, Junction-to-Ambient For one section: For both sections:	$R_{th(j-a)}$	 583.3 350	°C/W	
Operating Temperature Range	T_{op}	-55 to +200	°C	Note 1
Storage Temperature Range	T_{stg}	-65 to +200	°C	Note 1
Soldering Temperature For CCP (Variants 10 to 15): For FP (Variants 16, 17):	T_{sol}	 +245 +265	°C	 Note 2 Note 3

NOTES:

1. For Variants 13, 14, 15, 17 with hot solder dip lead finish, all testing, and any handling, performed at $T_{amb} > +125°C$ shall be carried out in a 100% inert atmosphere.
2. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.
3. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

1.6 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

1.6.1 Chip Carrier Package (CCP) - 6 terminal (Variants 10, 11, 12, 13, 14, 15)

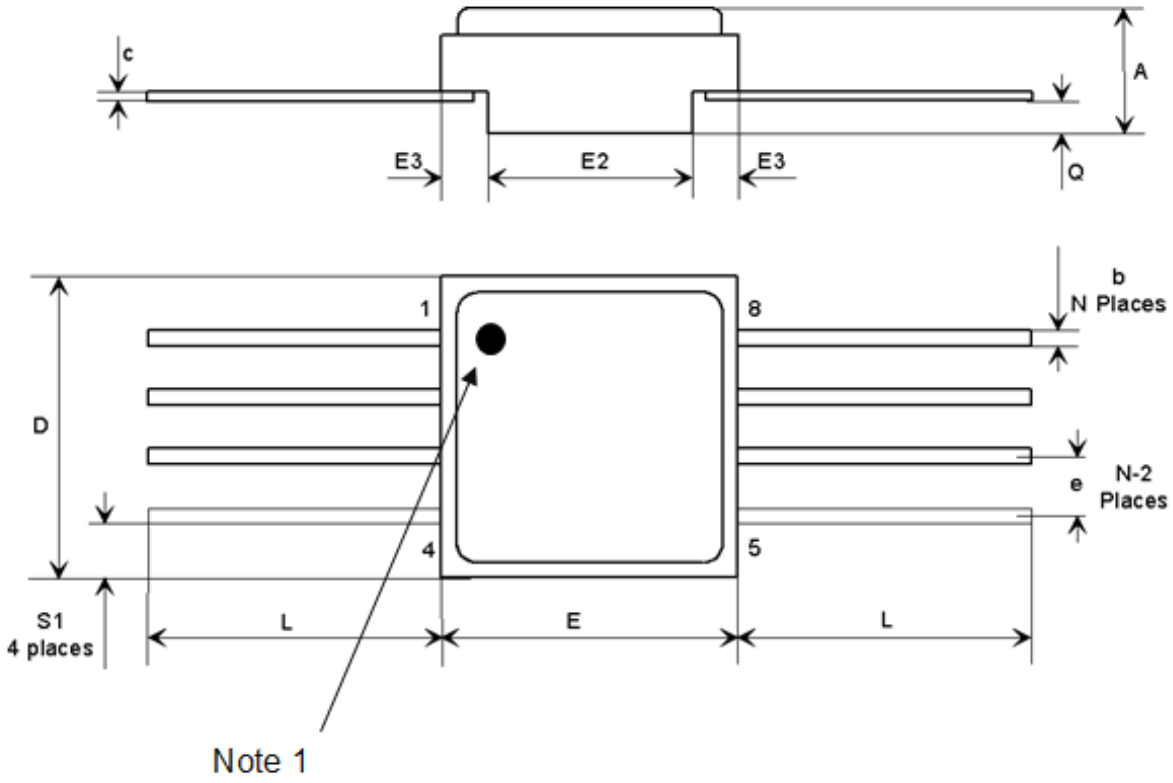


Symbols	Dimensions mm		Notes
	Min	Max	
A	1.53	1.96	
C	0.89 TYPICAL		2
D	1.52	1.78	
D1	2.08	2.49	
E	1.24	1.55	
F	5.76	5.92	
G	4.19	4.45	
I	6.1	6.35	
L	0.55	0.71	2
M	3.86	4.01	
N	1.14	1.4	
N1	2.41	2.67	
N2	0.89 TYPICAL		
r	0.23 TYPICAL		2

NOTES:

1. Terminal identification is specified, when viewing the top side of the package, by reference to a black ink dot adjacent to terminal 1 = base 2. Terminal 2 = collector 2, terminal 3 = emitter 2, terminal 4 = emitter 1, terminal 5 = collector 1 and terminal 6 = base 1.
2. Applies to all terminals.

1.6.2 Flat Package (FP) - 8 Pin (Variants 16, 17)



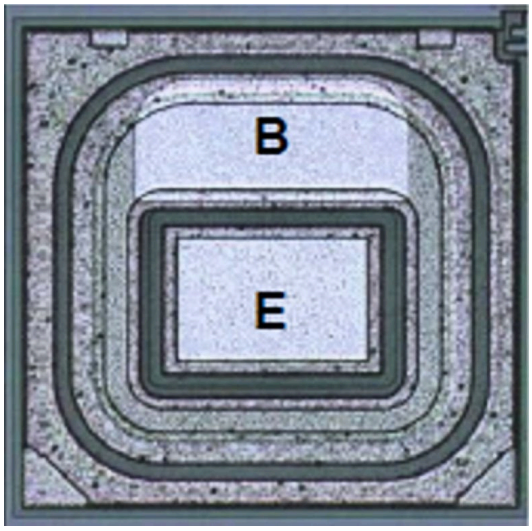
Symbols	Dimensions mm		Notes
	Min	Max	
A	2.24	2.64	
b	0.38	0.48	2
c	0.10	0.16	2
D	6.35	6.61	
E	6.35	6.61	
E2	4.32	4.58	
E3	0.88	1.14	
e	1.27 TYPICAL		4
L	3 TYPICAL		2
Q	0.66	0.92	
S1	0.92	1.32	3

NOTES:

1. Terminal identification is specified, when viewing the top side of the package, by reference to a black ink dot adjacent to terminal 1 = collector 1, terminal 2 = base 1, terminal 3 = emitter 1, terminal 6 = emitter 2 terminal 7 = base 2, terminal 8 = collector 2, terminals 4 and 5 are connected to seal ring and lid.
2. Applies to all pins.
3. 4 places.
4. 6 places.

1.6.3 Die (Variant 18)

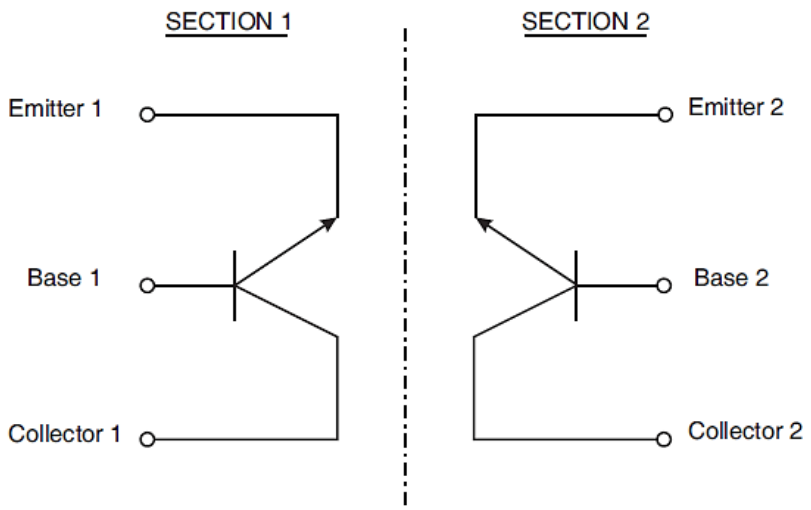
Single Transistor Die Shown



NOTES:

1. Variant 18 shall be ordered, tested and delivered in matched pairs. For delivery, each matched pair shall be identifiable by their location within the primary package.
2. Die materials and dimensions:
   - Die substrate: Silicon
   - Die length: 457 µm
   - Die width: 457 µm
   - Die thickness: 230 ±20µm
   - Top Glassivation:
     - P-Vapox with thickness 720 ±80nm and
     - Nitride with thickness 540 ±60nm
   - Top metallisation: Al/Si (1%) with thickness: 2 ±0.2µm (Typ.)
   - Backside metallisation: Au/As with thickness: 1.485 ±0.165µm
   - Emitter pad dimensions: 100 × 160 µm
   - Base pad dimensions: 70 × 220 µm
3. Terminal identification: B = Base, E = Emitter
4. Bias details: backside contact = Collector

1.7 FUNCTIONAL DIAGRAM



NOTES:

1. For CCP (Variants 10, 11, 12, 13, 14, 15), the lid is not connected to any terminal.
2. For FP (Variants 16, 17), the seal ring and the lid are connected to terminals 4 and 5.
3. For Die (Variant 18), each Section as shown is a single die of each matched pair.

1.8 MATERIALS AND FINISHES

1.8.1 Materials and Finishes of Packaged Components

For Variants 10 to 17, the materials and finishes shall be as follows:

(a) Case
For the chip carrier package (Variants 10 to 15) and the flat package (Variants 16, 17), the case shall be hermetically sealed and have a ceramic body with a Kovar lid.

(b) Leads/Terminals
As specified in Para. 1.4.2, Component Type Variants.

1.8.2 Materials and Finishes of Die Components

For Variant 18, the materials and finishes shall be as specified in Para. 1.6.3.

2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

2.1.1.1 Deviation from Production Control – Chart F2

(a) For Special In-Process Controls: assembly of the packaged test sublot: For Variant 18, each packaged test sublot sample shall contain two dice in a matched pair.

For procurement, the quantity of matched pairs of dice to be assembled, n, shall be selected at the Manufacturer's discretion from one of the four specified sampling plans (a), (b), (c) or (d).

For Qualification and Maintenance of Qualification: the quantity of matched pairs of dice to be assembled, n, shall be selected at the Manufacturer's discretion from one of the specified sampling plans (c) or (d).

2.1.1.2 Deviation from Screening Tests – Chart F3

(a) High Temperature Reverse Bias Burn-in and the subsequent Final Measurements for HTRB shall be omitted.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component or its primary package shall be:

(a) Terminal identification (see Para. 1.6).
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number (see Para. 1.4.1).
(d) Traceability information.

2.3 TERMINAL STRENGTH

The test conditions for terminal strength, tested as specified in the ESCC Generic Specification, shall be as follows:

- For FP (Variants 16, 17), Test Condition: E, lead fatigue. The applied weight shall be 3 ounces (85g), with three bends of 15°.

2.4 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

2.4.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb} = +22 ±3°C.

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	3001	I_C = 10µA, Bias condition D	60	-	V
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	3011	I_C = 10mA, Bias condition D, Note 1	60	-	V
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	3026	I_E = 10µA, Bias condition D	6	-	V
Collector-Emitter Cut-off Current	I_{CEO}	3041	V_{CE} = 5V, Bias condition D	-	2	nA

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Collector-Base Cut-off Current	I_{CBO}	3036	V_{CB} = 45V, Bias condition D	-	2	nA
Emitter-Base Cut-off Current	I_{EBO}	3061	V_{EB} = 5V, Bias condition D	-	2	nA
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	3071	I_C = 1mA, I_B = 0.1mA Note 1	-	350	mV
Base-Emitter Saturation Voltage	$V_{BE(sat)}$	3066	I_C = 1mA, I_B = 0.1mA Test Condition A Note 1	0.5	1	V
Forward-Current Transfer Ratio	h_{FE1}	3076	V_{CE} = 5V, I_C = 10µA Variants 10, 13: Variants 11, 12, 14, 15, 16, 17, 18:	 60 150	 240 600	-
	h_{FE2}	3076	VCE = 5V, I_C = 100µA Variants 10, 13: Variants 11, 12, 14, 15, 16, 17, 18:	 100 225	 - -	-
	h_{FE3}	3076	VCE = 5V, I_C = 1mA Variants 10, 13: Variants 11, 12, 14, 15, 16, 17, 18:	 150 300	 - -	-
Forward-Current Transfer Ratio Comparison	h_{FE2-1}/ h_{FE2-2}	3076	V_{CE} = 5V, I_C = 100µA	0.9	1	-
Base-Emitter Voltage Differential	$\|V_{BE1}-V_{BE2}\|1$	3066	V_{CE} = 5V ; I_C = 10µA Test Condition B Variants 10, 11, 13, 14: Variants 12, 15, 16, 17, 18: Note 2	 - -	 5 2	mV
	$\|V_{BE1}-V_{BE2}\|2$	3066	V_{CE} = 5V ; I_C = 100µA Test Condition B Variants 10, 11, 13, 14: Variants 12, 15, 16, 17, 18: Note 2	 - -	 3 1.5	mV
	$\|V_{BE1}-V_{BE2}\|3$	3066	V_{CE} = 5V ; I_C = 1mA Test Condition B Variants 10, 11, 13, 14: Variants 12, 15, 16, 17, 18: Note 2	 - -	 5 2	mV
Leakage Current Between Sections	$I_{LS(e-e)}$	-	50V to Emitter 2, 0V to Emitter 1	-	5	µA
	$I_{LS(b-b)}$	-	50V to Base 2 0V to Base 1	-	5	µA
	$I_{LS(c-c)}$	-	50V to Collector 2 0V to Collector 1	-	5	µA

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions	Limits		Units
				Min	Max	
Current Gain Bandwidth Product	f_T	3206	V_{CE} = 5V, I_C = 500µA f = 20MHz Notes 3, 4	60	-	MHz
Small-Signal Output Admittance	h_{oe}	3216	V_{CE} = 5V, I_C = 1mA, f = 1kHz Notes 3, 4	-	1	µmho
Spot Noise Figure	NF_s	3246	V_{CE} = 5V, I_C = 10µA R_s = 10kΩ, f = 1kHz BW = 200Hz Notes 3, 4	-	3	dB
Wide-Band Noise Figure	NF_w	3246	V_{CE} = 5V, I_C = 10µA, R_s = 10kΩ 10Hz ≤ f ≤ 15.7kHz BW = 10kHz Notes 3, 4	-	3	dB
Output Capacitance	C_{obo}	3236	V_{CB} = 5V, I_E = 0A 100kHz ≤ f ≤ 1MHz Notes 3, 4	-	6	pF
Small-Signal Input Impedance	h_{ib}	3201	V_{CB} = 5V, I_C = 1mA, f = 1kHz Notes 3, 4	25	32	Ω

NOTES:

1. Pulsed measurement: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
2. Any device whose measurement values exceed the specified limits shall be removed from the lot, but only count for PDA when such values exceed twice the specified limits (e.g. for Base-Emitter Voltage Differential 1: 10mV max or 4mV max).
3. For Variants 10 to 17, all AC characteristics read and record measurements shall be performed on a sample of 32 components with 0 failures allowed. Alternatively, a 100% inspection may be performed.
4. For Variant 18, all AC characteristics read and record measurements shall be performed on either a sample of 32 matched pairs (64 dice) or 100% of the Packaged Test Sublot, whichever is less, with 0 failures allowed.

2.4.2 High and Low Temperatures Electrical Measurements

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Collector-Base Cut-off Current	I_{CBO}	3036	T_{amb} = +150 (+0 -5)°C V_{CB} = 45V, Bias Condition D	-	10	µA
Forward-Current Transfer Ratio	h_{FE1}	3076	T_{amb} = -55 (+5 -0)°C V_{CE} = 5V, I_C = 10µA Variants 10, 13: Variants 11, 12, 14, 15, 16, 17, 18:	 20 50	 - -	-
Forward-Current Transfer Ratio Comparison	h_{FE2-1}/h_{FE2-2}	3076	T_{amb} = -55 to +125°C V_{CE} = 5V, I_C = 100µA	0.85	1.18	-

Characteristics	Symbols	MIL-STD-750 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Base-Emitter Voltage Differential Change	$\|\Delta(V_{BE1}-V_{BE2})\Delta T_{amb}\|1$	3066	T_{amb} = -55 (+5 -0)°C to +25 ±3°C V_{CE} = 5V, I_C = 100µA Test condition B			mV
			Variants 10, 11, 13, 14:	-	0.8	
			Variants 12, 15, 16, 17, 18:	-	0.4	
	$\|\Delta(V_{BE1}-V_{BE2})\Delta T_{amb}\|2$	3066	T_{amb} = +25 ±3°C to +125 (+0 -5)°C V_{CE} = 5V, I_C = 100µA Test condition B			mV
			Variants 10, 11, 13, 14:	-	1	
			Variants 12, 15, 16, 17, 18:	-	0.5	

NOTES:
1. Measurements shall be performed on a sample basis as specified in the Generic Specification.

2.5 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.4.1, Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Collector-Base Cut-off Current	I_{CBO}	±1 or (1) ±100%	-	2	nA
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	±15 or (1) ±10%	-	350	mV
Forward-Current Transfer Ratio 2	h_{FE2}	±15%			
Variants 10, 13:			100	-	
Variants 11, 12, 14, 15, 16, 17, 18:			225	-	

NOTES:
1. Whichever is greater, referred to the initial value.

2.6 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in either Para. 2.4.1, Room Temperature Electrical Measurements or Para. 2.4.2, High and Low Temperatures Electrical Measurements, as applicable.

The limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits		Units
		Min	Max	
Collector-Base Cut-off Current	I_{CBO}	-	2	nA
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	-	350	mV
Forward-Current Transfer Ratio 2	h_{FE2}			-
Variants 10, 13:		100	-	
Variants 11, 12, 14, 15, 16, 17, 18:		225	-	
Forward-Current Transfer Ratio Comparison	h_{FE2-1}/h_{FE2-2}	0.85	1.18	-
Base-Emitter Voltage Differential 2	$\lvert V_{BE1}-V_{BE2}\rvert 2$			mV
Variants 10, 11, 13, 14:		-	3	
Variants 12, 15, 16, 17, 18:		-	1.5	
Base-Emitter Voltage Differential Change 1 (Note 1)	$\lvert\Delta(V_{BE1}-V_{BE2})\Delta T_{amb}\rvert 1$			mV
Variants 10, 11, 13, 14:		-	0.96	
Variants 12, 15, 16, 17, 18:		-	0.48	
Base-Emitter Voltage Differential Change 2 (Note 1)	$\lvert\Delta(V_{BE1}-V_{BE2})\Delta T_{amb}\rvert 2$			mV
Variants 10, 11, 13, 14:		-	1.2	
Variants 12, 15, 16, 17, 18:		-	0.6	

NOTES:

1. To be measured after Operating Life test only.

2.7 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+25 to +50	°C
Power Dissipation (Both Sections)	P_{totB}	As per Para. 1.5, Maximum Ratings. Derate P_{totB1} at the chosen T_{amb} using the specified $R_{th(j-a)}$.	W
Collector-Base Voltage	V_{CB}	40	V

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified in Para. 2.7, Power Burn-in Conditions.

APPENDIX A
AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 2.1.1, Deviations from the Generic Specification: Para. 8, Test Methods and Procedures	For qualification and qualification maintenance, or procurement of qualified or unqualified components, the following replacement test method specifications shall be used instead of the following ESCC Basic Specifications: No. 20400, Internal Visual Inspection: replaced by MIL-STD-750 Test Method 2072. No. 20500, External Visual Inspection: replaced by MIL-STD-750 Test Method 2071. No. 20900, Radiographic Inspection of Electronic Components: replaced by MIL-STD-750 Test Method 2076.
Para. 2.1.1.1, Deviations from the Generic Specification: Deviations from Production Control - Chart F2	Special In-Process Controls - Internal Visual Inspection. For CCP packages (Variants 10 to 15), the criteria specified for voids in the fillet and minimum die mounting material around the visible die perimeter for die mounting defects may be omitted providing that a radiographic inspection to verify the die-attach process is performed on a sample basis in accordance with STMicroelectronics procedure 0076637.
Para. 2.1.1.2, Deviations from the Generic Specification: Deviations from Screening Tests - Chart F3	Solderability is not applicable unless specifically stipulated in the Purchase Order.
Para. 2.4.1, Room Temperature Electrical Measurements	All AC characteristics (Para. 2.4.1, Notes 3 and 4) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Para. 2.4.2, High and Low Temperatures Electrical Measurements	All characteristics specified may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes characteristic measurements at high and low temperatures per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.