INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS 4-BIT LATCH / 4-LINE TO 16-LINE DECODER WITH FULLY BUFFERED OUTPUTS

BASED ON TYPE 4514B

ESCC Detail Specification No. 9408/012

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DCR No.	CHANGE DESCRIPTION
1733	Specification upissued to incorporate changes per DCR.

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1 GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 940801201

- Detail Specification Reference: 9408012
- Component Type Variant Number: 01 (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and Finish	Weight max g
01	4514B	FP	G2	1.7
02	4514B	FP	G4	1.7
03	4514B	DIP	G2	5.2
04	4514B	DIP	G4	5.2

The terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.5 to 18	V	Note 1
Input Voltage	V_{IN}	-0.5 to V_{DD}+0.5	V	Note 1 Power on
Input Current	I_{IN}	±10	mA	-
Device Power Dissipation (Continuous)	P_D	200	mW	-
Power Dissipation per Output	P_{DSO}	100	mW	-
Operating Temperature Range	T_{op}	-55 to +125	°C	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	°C	-
Soldering Temperature	T_{sol}	+265	°C	Note 2

NOTES:

1. Device is functional for $3V \leq V_{DD} \leq 15V$.
2. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.

1.6 HANDLING PRECAUTIONS

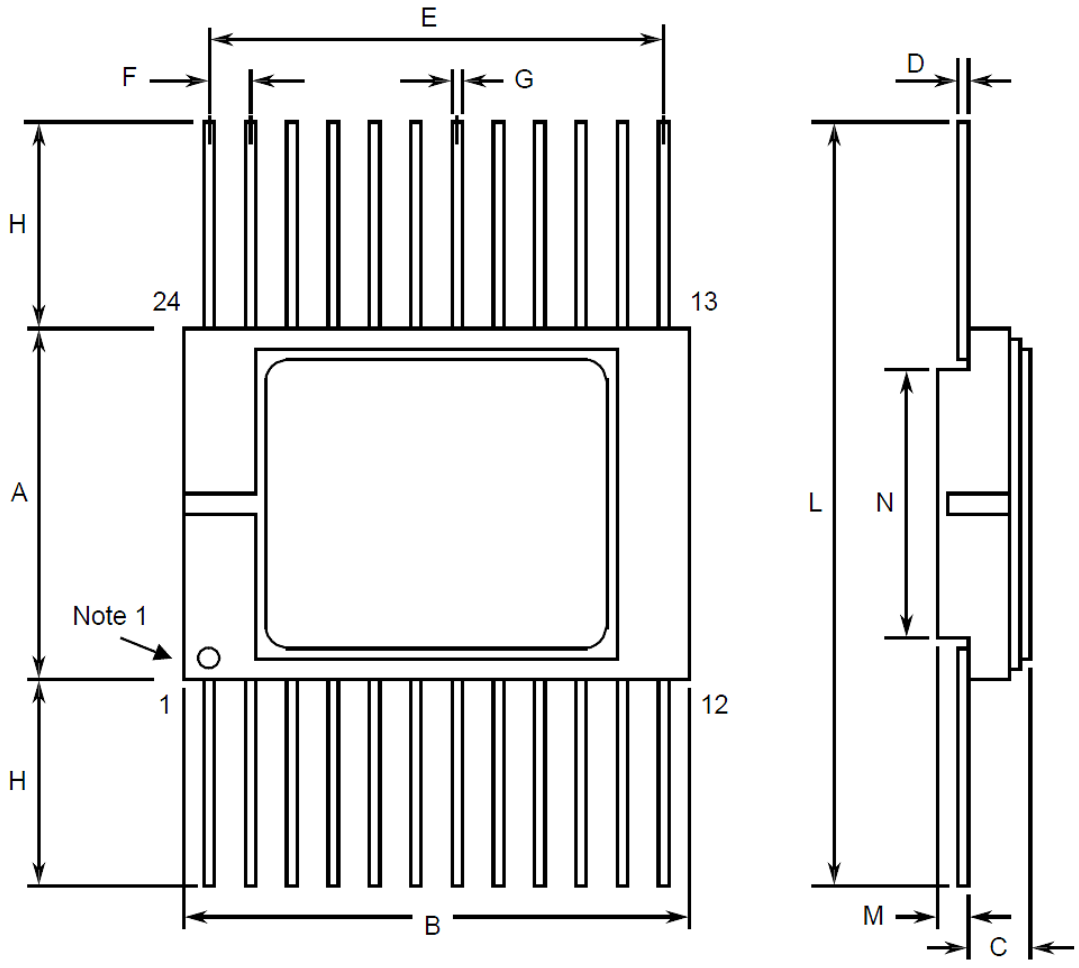
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a minimum Critical Path Failure Voltage of 400 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

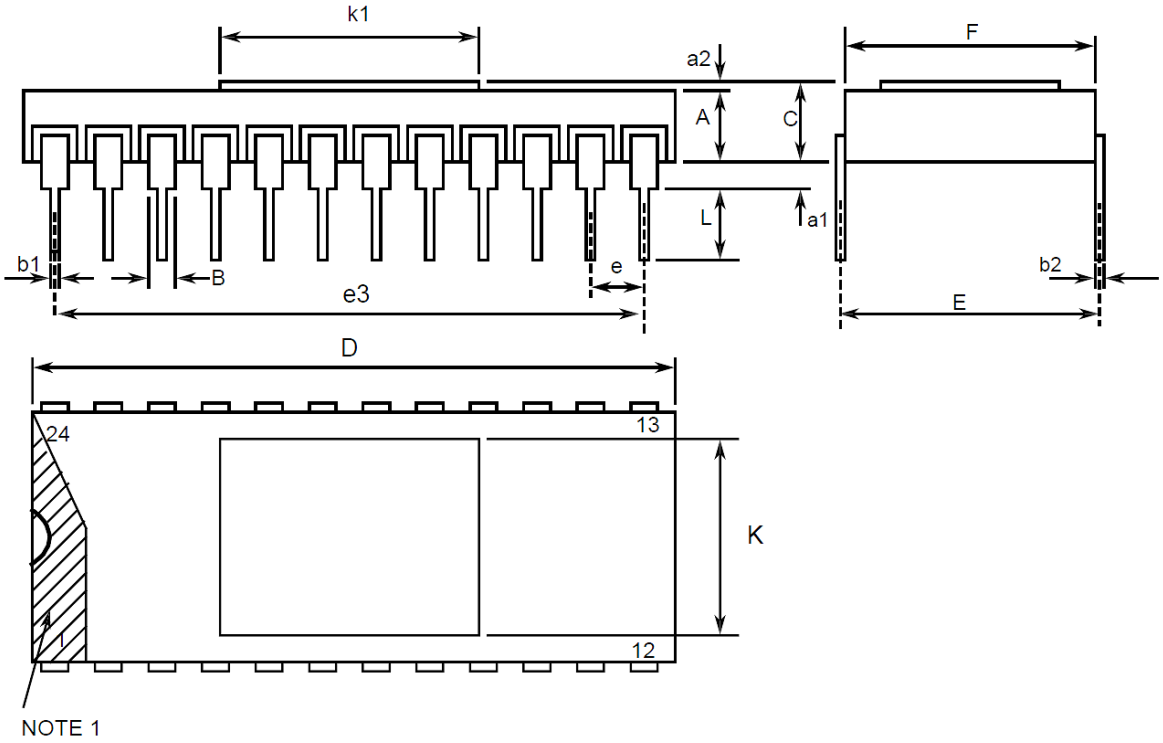
Consolidated Notes are given in Para. 1.7.3.

1.7.1 Flat Package (FP) - 24 Pin (Variants 01, 02)



Symbols	Dimensions mm		Notes
	Min	Max	
A	10.7	11.3	
B	15.3	15.7	
C	1.45	1.9	
D	0.23	0.3	5
E	13.84	14.1	
F	1.22	1.32	3, 6
G	0.45	0.55	5
H	7.25	8.25	5
L	25	28	
M	0.45	0.55	
N	7 TYPICAL		

1.7.2 Dual-in-line Package (DIP) - 24 Pin (Variants 03, 04)

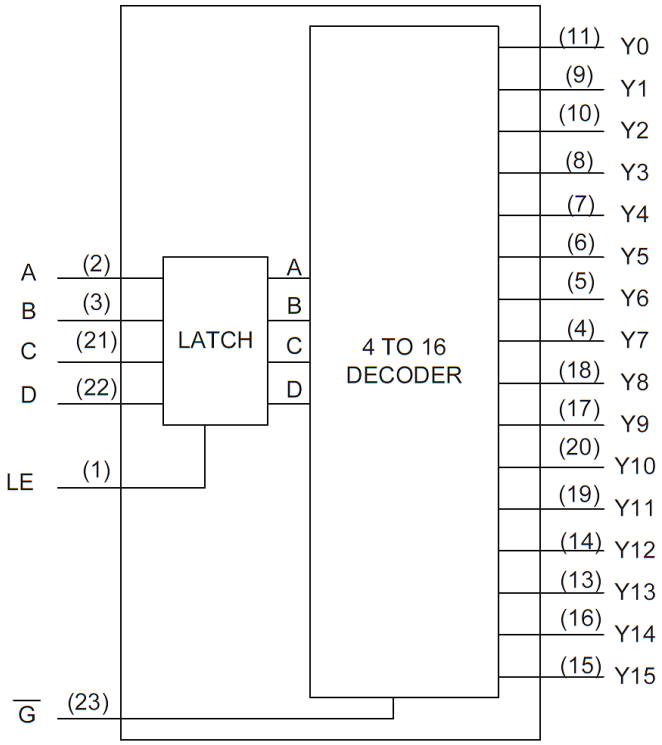


Symbols	Dimensions mm		Notes
	Min	Max	
A	1.931	2.387	
a1	1.016	1.524	2
a2	0.274	0.34	
B	1.274 TYPICAL		5
b1	0.407	0.507	5
b2	0.229	0.304	5
C	2.205	2.727	
D	30.176	30.784	
E	14.986	15.494	
e	2.413	2.667	4, 6
e3	27.813	28.067	
F	14.859	15.367	
L	3	3.8	
K	12.6	13	
k1	12.6	13	

1.7.3 Notes to Physical Dimensions and Terminal Identification

1. Index area: a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown.
2. The dimension shall be measured from the seating plane to the base plane.
3. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ±0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
4. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.
5. All terminals.
6. 22 spaces.

1.8 FUNCTIONAL DIAGRAM



NOTES:

1. The package lid for all packages is not connected to any terminal.

1.9 PIN ASSIGNMENT

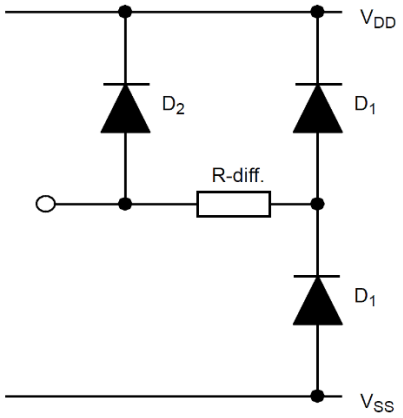
Pin	Function	Pin	Function
1	LE Input (Latch Enable)	13	Y13 Output
2	A Input (Data)	14	Y12 Output
3	B Input (Data)	15	Y15 Output
4	Y7 Output	16	Y14 Output
5	Y6 Output	17	Y9 Output
6	Y5 Output	18	Y8 Output
7	Y4 Output	19	Y11 Output
8	Y3 Output	20	Y10 Output
9	Y1 Output	21	C Input (Data)
10	Y2 Output	22	D Input (Data)
11	Y0 Output	23	$\overline{G}$ Input (Enable)
12	V_{SS}	24	V_{DD}

1.10 TRUTH TABLE

1. Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant.
2. ↓ = Transition, High to Low.

Inputs						Output(s) selected	State of Outputs
LE	$\overline{G}$	D	C	B	A		
H	L	L	L	L	L	Y0	Selected Output = H ; All other Outputs = L
H	L	L	L	L	H	Y1	Selected Output = H ; All other Outputs = L
H	L	L	L	H	L	Y2	Selected Output = H ; All other Outputs = L
H	L	L	L	H	H	Y3	Selected Output = H ; All other Outputs = L
H	L	L	H	L	L	Y4	Selected Output = H ; All other Outputs = L
H	L	L	H	L	H	Y5	Selected Output = H ; All other Outputs = L
H	L	L	H	H	L	Y6	Selected Output = H ; All other Outputs = L
H	L	L	H	H	H	Y7	Selected Output = H ; All other Outputs = L
H	L	H	L	L	L	Y8	Selected Output = H ; All other Outputs = L
H	L	H	L	L	H	Y9	Selected Output = H ; All other Outputs = L
H	L	H	L	H	L	Y10	Selected Output = H ; All other Outputs = L
H	L	H	L	H	H	Y11	Selected Output = H ; All other Outputs = L
H	L	H	H	L	L	Y12	Selected Output = H ; All other Outputs = L
H	L	H	H	L	H	Y13	Selected Output = H ; All other Outputs = L
H	L	H	H	H	L	Y14	Selected Output = H ; All other Outputs = L
H	L	H	H	H	H	Y15	Selected Output = H ; All other Outputs = L
X	H	X	X	X	X	All	L
L	L	X	X	X	X	All	Remain in state existing before LE ↓

1.11 INPUT PROTECTION NETWORK



2 REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

None.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification (see Para. 1.7).

(b) The ESCC qualified components symbol (for ESCC qualified components only).

(c) The ESCC Component Number (see Para. 1.4.1).

(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated Notes are given in Para. 2.3.3.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb} = +22 ±3°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table without Load V_{IL} = 0V, V_{IH} = 3V V_{DD} = 3V, V_{SS} = 0V Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table without Load V_{IL} = 0V, V_{IH} = 15V V_{DD} = 15V, V_{SS} = 0V Note 2	-	-	-
Quiescent Current	I_{DD}	3005	V_{IL} = 0V, V_{IH} = 15V V_{DD} = 15V, V_{SS} = 0V Note 3	-	1	µA
Low Level Input Current	I_{IL}	3009	V_{IN} (Under Test) = 0V V_{DD} = 15V, V_{SS} = 0V	-	-50	nA
High Level Input Current	I_{IH}	3010	V_{IN} (Under Test) = 15V V_{DD} = 15V, V_{SS} = 0V	-	50	nA
Low Level Output Voltage 1	V_{OL1}	3007	V_{IL} = 0V, V_{IH} = 15V, I_{OL} = 0A V_{DD} = 15V, V_{SS} = 0V	-	50	mV
Low Level Output Voltage 2 (Noise Immunity)	V_{OL2}	3007	V_{IL} = 1.5V, V_{IH} = 3.5V, I_{OL} = 0A V_{DD} = 5V, V_{SS} = 0V	-	500	mV
Low Level Output Voltage 3 (Noise Immunity)	V_{OL3}	3007	V_{IL} = 4V, V_{IH} = 11V, I_{OL} = 0A V_{DD} = 15V, V_{SS} = 0V	-	1.5	V
High Level Output Voltage 1	V_{OH1}	3006	V_{IL} = 0V, V_{IH} = 15V, I_{OH} = 0A V_{DD} = 15V, V_{SS} = 0V	14.95	-	V
High Level Output Voltage 2 (Noise Immunity)	V_{OH2}	3006	V_{IL} = 1.5V, V_{IH} = 3.5V, I_{OH} = 0A V_{DD} = 5V, V_{SS} = 0V	4.5	-	V
High Level Output Voltage 3 (Noise Immunity)	V_{OH3}	3006	V_{IL} = 4V, V_{IH} = 11V, I_{OH} = 0A V_{DD} = 15V, V_{SS} = 0V	13.5	-	V
Low Level Output Current 1	I_{OL1}	-	V_{IL} = 0V, V_{IH} = 5V, V_{OL} = 0.4V V_{DD} = 5V, V_{SS} = 0V Note 4	400	-	µA
Low Level Output Current 2	I_{OL2}	-	V_{IL} = 0V, V_{IH} = 15V, V_{OL} = 1.5V V_{DD} = 15V, V_{SS} = 0V Note 4	3.4	-	mA
High Level Output Current 1	I_{OH1}	-	V_{IL} = 0V, V_{IH} = 5V, V_{OH} = 4.6V V_{DD} = 5V, V_{SS} = 0V Note 4	-510	-	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
High Level Output Current 2	I_{OH2}	-	V_{IL} = 0V, V_{IH} = 15V, V_{OH} = 13.5V V_{DD} = 15V, V_{SS} = 0V Note 4	-3.4	-	mA
Threshold Voltage N-Channel	V_{THN}	-	LE Input at Ground All Other Inputs: V_{IN} = 5V V_{DD} = 5V, I_{SS} = -10µA	-0.7	-3	V
Threshold Voltage P-Channel	V_{THP}	-	LE Input at Ground All Other Inputs: V_{IN} = -5V V_{SS} = -5V, I_{DD} = 10µA	0.7	3	V
Input Clamp Voltage 1, to V_{SS}	V_{IC1}	-	I_{IN} (Under Test) = -100µA V_{DD} = Open, V_{SS} = 0V All Other Pins Open	-	-2	V
Input Clamp Voltage 2, to V_{DD}	V_{IC2}	-	V_{IN} (Under Test) = 6V R = 30kΩ, V_{SS} = Open All Other Pins Open Note 5	3	-	V
Input Capacitance	C_{IN}	3012	V_{IN} (Not Under Test) = 0V V_{DD} = V_{SS} = 0V f = 100kHz to 1MHz Note 6	-	7.5	pF
Propagation Delay Low to High 1, A to Y0	t_{PLH1}	3003	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Truth Table V_{IL} = 0V, V_{IH} = 5V, V_{DD} = 5V, V_{SS} = 0V Note 7	-	920	ns
Propagation Delay High to Low 1, A to Y0	t_{PHL1}	3003	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Truth Table V_{IL} = 0V, V_{IH} = 5V, V_{DD} = 5V, V_{SS} = 0V Note 7	-	1750	ns
Propagation Delay Low to High 2, $\overline{G}$ to Y0	t_{PLH2}	3003	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Truth Table V_{IL} = 0V, V_{IH} = 5V, V_{DD} = 5V, V_{SS} = 0V Note 7	-	450	ns

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Propagation Delay High to Low 2, $\overline{G}$ to Y0	t_{PHL2}	3003	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Truth Table V_{IL} = 0V, V_{IH} = 5V, V_{DD} = 5V, V_{SS} = 0V Note 7	-	850	ns
Transition Time Low to High, Y0	t_{TLH}	3004	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Truth Table V_{IL} = 0V, V_{IH} = 5V, V_{DD} = 5V, V_{SS} = 0V Note 7	-	150	ns
Transition Time High to Low, Y0	t_{THL}	3004	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Truth Table V_{IL} = 0V, V_{IH} = 5V, V_{DD} = 5V, V_{SS} = 0V Note 7	-	150	ns

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb} = +125 (+0 -5)°C and T_{amb} = -55 (+5 -0)°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table without Load V_{IL} = 0V, V_{IH} = 3V V_{DD} = 3V, V_{SS} = 0V Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table without Load V_{IL} = 0V, V_{IH} = 15V V_{DD} = 15V, V_{SS} = 0V Note 2	-	-	-
Quiescent Current	I_{DD}	3005	V_{IL} = 0V, V_{IH} = 15V V_{DD} = 15V, V_{SS} = 0V Note 3 T_{amb} = +125°C T_{amb} = -55°C	 - -	 3 1	µA
Low Level Input Current	I_{IL}	3009	V_{IN} (Under Test) = 0V V_{DD} = 15V, V_{SS} = 0V T_{amb} = +125°C T_{amb} = -55°C	 - -	 -100 -50	nA
High Level Input Current	I_{IH}	3010	V_{IN} (Under Test) = 15V V_{DD} = 15V, V_{SS} = 0V T_{amb} = +125°C T_{amb} = -55°C	 - -	 100 50	nA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Low Level Output Voltage 1	V_{OL1}	3007	V_{IL} = 0V, V_{IH} = 15V, I_{OL} = 0A V_{DD} = 15V, V_{SS} = 0V	-	50	mV
Low Level Output Voltage 2 (Noise Immunity)	V_{OL2}	3007	V_{IL} = 1.5V, V_{IH} = 3.5V, I_{OL} = 0A V_{DD} = 5V, V_{SS} = 0V	-	500	mV
Low Level Output Voltage 3 (Noise Immunity)	V_{OL3}	3007	V_{IL} = 4V, V_{IH} = 11V, I_{OL} = 0A V_{DD} = 15V, V_{SS} = 0V	-	1.5	V
High Level Output Voltage 1	V_{OH1}	3006	V_{IL} = 0V, V_{IH} = 15V, I_{OH} = 0A V_{DD} = 15V, V_{SS} = 0V	14.95	-	V
High Level Output Voltage 2 (Noise Immunity)	V_{OH2}	3006	V_{IL} = 1.5V, V_{IH} = 3.5V, I_{OH} = 0A V_{DD} = 5V, V_{SS} = 0V	4.5	-	V
High Level Output Voltage 3 (Noise Immunity)	V_{OH3}	3006	V_{IL} = 4V, V_{IH} = 11V, I_{OH} = 0A V_{DD} = 15V, V_{SS} = 0V	13.5	-	V
Low Level Output Current 1	I_{OL1}	-	V_{IL} = 0V, V_{IH} = 5V, V_{OL} = 0.4V V_{DD} = 5V, V_{SS} = 0V Note 4 T_{amb} = +125°C T_{amb} = -55°C	 360 640	 - -	µA
Low Level Output Current 2	I_{OL2}	-	V_{IL} = 0V, V_{IH} = 15V, V_{OL} = 1.5V V_{DD} = 15V, V_{SS} = 0V Note 4 T_{amb} = +125°C T_{amb} = -55°C	 2.4 4.2	 - -	mA
High Level Output Current 1	I_{OH1}	-	V_{IL} = 0V, V_{IH} = 5V, V_{OH} = 4.6V V_{DD} = 5V, V_{SS} = 0V Note 4 T_{amb} = +125°C T_{amb} = -55°C	 -360 -640	 - -	µA
High Level Output Current 2	I_{OH2}	-	V_{IL} = 0V, V_{IH} = 15V, V_{OH} = 13.5V V_{DD} = 15V, V_{SS} = 0V Note 4 T_{amb} = +125°C T_{amb} = -55°C	 -2.4 -4.2	 - -	mA
Threshold Voltage N-Channel	V_{THN}	-	LE Input at Ground All Other Inputs: V_{IN} = 5V V_{DD} = 5V, I_{SS} = -10µA T_{amb} = +125°C T_{amb} = -55°C	 -0.3 -0.7	 -3.5 -3.5	V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Threshold Voltage P-Channel	V_{THP}	-	LE Input at Ground All Other Inputs: V_{IN} = -5V V_{SS} = -5V, I_{DD} = 10µA T_{amb} = +125°C T_{amb} = -55°C	 0.3 0.7	 3.5 3.5	V

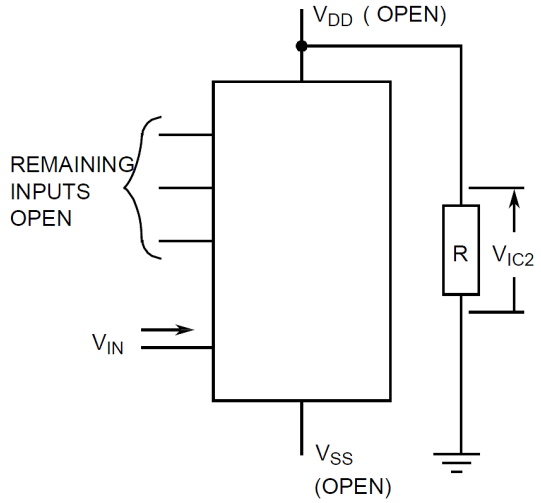
2.3.3 Notes to Electrical Measurement Tables

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not under test shall be V_{IN} = V_{SS} or V_{DD} and outputs not under test shall be open.
2. Functional tests shall be performed to verify Truth Table with $V_{OH} \geq V_{DD}$-0.5V, $V_{OL} \leq$ 0.5V. The maximum time to output comparator strobe = 300µs.
3. Quiescent Current shall be tested using the following input conditions, with 1 = V_{IH} = V_{DD} and 0 = V_{IL} = V_{SS}:

I_{DD} TEST	INPUT CONDITIONS					
	LE	A	B	C	D	$\overline{G}$
(a)	1	0	0	0	0	0
(b)	1	1	0	0	0	0
(c)	1	0	1	0	0	0
(d)	1	1	1	0	0	0
(e)	1	0	0	1	0	0
(f)	1	1	0	1	0	0
(g)	1	0	1	1	0	0
(h)	1	1	1	1	0	0
(i)	1	0	0	0	1	0
(j)	1	1	0	0	1	0
(k)	1	0	1	0	1	0
(l)	1	1	1	0	1	0
(m)	1	0	0	1	1	0
(n)	1	1	0	1	1	0
(o)	1	0	1	1	1	0
(p)	1	1	1	1	1	0
(q)	1	1	1	1	1	1
(r)	1	0	0	0	0	1
(s)	0	0	0	0	0	0
(t)	0	1	1	1	1	0
(u)	0	0	0	0	0	0

4. Interchange of forcing and measuring parameters is permitted.

5. Input Clamp Voltage 2 to V_{DD}, V_{IC2}, shall be tested on each input as follows:



6. Guaranteed but not tested.

7. Read and record measurements shall be performed on a sample of 32 components with 0 failures permitted.

   The pulse generator shall have the following characteristics:

   V_{GEN} = 0 to V_{DD}; f_{GEN} = 500kHz; t_r and t_f ≤ 15ns (10% to 90%); duty cycle = 50%; Z_{out} = 50Ω. Output load capacitance C_L = 50pF ±5% including scope probe, wiring and stray capacitance without component in the test fixture. Output load resistance R_L = 200kΩ ±5%.

   Propagation delay shall be measured referenced to the 50% input and output voltages.

   Transition time shall be measured referenced to the 10% and 90% output voltage.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1, Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Quiescent Current	I_{DD}	±0.15	-	1	µA
Low Level Output Current 1	I_{OL1}	±15% (2)	510	-	µA
High Level Output Current 1	I_{OH1}	±15% (2)	-510	-	µA
Threshold Voltage N-Channel	V_{THN}	±0.3	-0.7	-3	V
Threshold Voltage P-Channel	V_{THP}	±0.3	0.7	3	V

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. Percentage of limit value if voltage is the measuring parameter.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb} = +22 ±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1, Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic where specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Functional Test 1	-	-	-	-	-
Quiescent Current	I_{DD}	±0.15	-	1	µA
Low Level Input Current	I_{IL}	-	-	-50	nA
High Level Input Current	I_{IH}	-	-	50	nA
Low Level Output Voltage 1	V_{OL1}	-	-	50	mV
Low Level Output Voltage 2 (Noise Immunity)	V_{OL2}	-	-	500	mV
High Level Output Voltage 1	V_{OH1}	-	14.95	-	V
High Level Output Voltage 2 (Noise Immunity)	V_{OH2}	-	4.5	-	V
Low Level Output Current 1	I_{OL1}	±15% (3)	510	-	µA
Low Level Output Current 2	I_{OL2}	±15% (3)	3.4	-	mA
High Level Output Current 1	I_{OH1}	±15% (3)	-510	-	µA
High Level Output Current 2	I_{OH2}	±15% (3)	-3.4	-	mA
Threshold Voltage N-Channel	V_{THN}	±0.3	-0.7	-3	V
Threshold Voltage P-Channel	V_{THP}	±0.3	0.7	3	V

NOTES:

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. The drift values (Δ) are applicable to the Operating Life test only.
3. Percentage of limit value if voltage is the measuring parameter.

2.6 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

2.6.1 N-Channel HTRB

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	°C
Outputs Yn	V_{OUT}	Open	V
Inputs B, D, $\overline{G}$	V_{IN}	V_{SS}	V
Inputs LE, A, C	V_{IN}	V_{DD}	V
Positive Supply Voltage	V_{DD}	15 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V
Duration	t	72	Hours

NOTES:
1. Input Protection Resistor = 2kΩ min to 47kΩ max.

2.6.2 P-Channel HTRB

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	°C
Outputs Yn	V_{OUT}	Open	V
Inputs B, D, $\overline{G}$	V_{IN}	V_{DD}	V
Inputs LE, A, C	V_{IN}	V_{SS}	V
Positive Supply Voltage	V_{DD}	15 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V
Duration	t	72	Hours

NOTES:
1. Input Protection Resistor = 2kΩ min to 47kΩ max.

2.7 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	°C
Outputs Yn	V_{OUT}	V_{SS}	V
Input LE	V_{IN}	V_{DD}	V
Input $\overline{G}$	V_{IN}	V_{GEN1}	V
Inputs A, B, C, D	V_{IN}	V_{GEN2}	V
Pulse Voltage	V_{GEN}	0V to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN1} f_{GEN2}	50k 25k 50% Duty Cycle	Hz
Positive Supply Voltage	V_{DD}	15 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:
1. Input Protection Resistor = Output Load = 2kΩ min to 47kΩ max.

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified in Para. 2.7, Power Burn-in Conditions.

APPENDIX A

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 2.1.1 Deviations from the Generic Specification: Deviations from Screening Tests - Chart F3	External Visual Inspection: The criteria applicable to chip-outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a). High Temperature Reverse Bias Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used. Power Burn-in test is performed using STMicroelectronics Specification Ref: 0019255. Solderability is not applicable unless specifically stipulated in the Purchase Order.
Para. 2.1.1 Deviations from the Generic Specification: Deviations from Qualification and Periodic Tests - Chart F4	External Visual Inspection: The criteria applicable to chip-outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a). Operating Life: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.
Para. 2.3.1 Room Temperature Electrical Measurements	All AC characteristics (Capacitance and Timings) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Para. 2.3.2 High and Low Temperatures Electrical Measurements	High and Low Temperatures Electrical Measurements may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes High and Low Temperatures Electrical Measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.