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**INTEGRATED CIRCUITS, SILICON MONOLITHIC,
BIPOLAR, ADVANCED LOW POWER SCHOTTKY,
TRIPLE, 3-INPUT, POSITIVE-NAND GATES,
BASED ON TYPES 54ALS10 AND 54ALS10A
ESCC Detail Specification No. 9201/093**

**ISSUE 1
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space components
coordination group

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DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Reference CHANGE Item	Approved DCR No.
		This Issue supersedes Issue 2 and incorporates all modifications defined in Revision 'A' to Issue 2 and the following DCR's:- Cover Page : Title amended to include Type 54ALS10A DCN Para. 1.1 : Amended to incorporate Type 54ALS10A Table 1(a) : Expanded to incorporate Type 54ALS10A : Lead material and/or finish amended Figures 2 : Imperial dimensions and references deleted Figure 2(c) : In drawing, Note 6 corrected to "10" Notes to Figures : Title amended : Note 1, amended to read "...Figure 2(b)" Figure 3(a) : Comparison Table added Figure 3(b) : Note 2 added Para. 4.2.2 : Deviation deleted, "None." added Para. 4.4.2 : Paragraph amended Para. 4.5.2 : Amended to read "...Figure 2(b)" Para. 4.5.3 : "Type Variant, as applicable" amended to refer to Table 1(a) Para. 4.6.3 : Reference to functional test sequence deleted Para. 4.7.1 : Expanded to identify the stated temperature as T _{amb} Table 2 : Nos. 64 to 81, amended to incorporate test limits for Type 54ALS10A Variants : Nos. 82 to 99, amended to incorporate test limits for Type 54ALS10A Variants Figure 5 : Type 54ALS10A added to drawing Para. 4.8 : Title expanded	22816 None 22816 22816 22881 22881 23456 22881 22881 22881 23456 21048 22881 22881 23455 23455 23455 22816 22816 22816 23455
'A'	Feb.'92	Cover Page DCN P13. Para. 4.2.4 : Deviation deleted, "None" added P14. Para. 4.2.5 : Deviation deleted, "None" added	None None 22919 22919
'B'	June '94	P1. Cover Page P2. DCN P14. Para. 4.3.2 : Weights amended	None None 221047



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1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, bipolar, advanced low power Schottky, Triple, 3-Input, Positive-NAND Gate, based on Types 54ALS10 and 54ALS10A. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the integrated circuits specified herein are shown in Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

As per Figure 3(b).

1.8 CIRCUIT SCHEMATIC

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).



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TABLE 1(a) - TYPE VARIANTS

VARIANT	BASED ON TYPE	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
01	54ALS10	FLAT	2(a)	D7
02	54ALS10	FLAT	2(a)	G4
03	54ALS10	CCP	2(b)	7
04	54ALS10	CCP	2(b)	4
05	54ALS10	DIL	2(c)	D7
06	54ALS10	DIL	2(c)	G4
07	54ALS10A	FLAT	2(a)	D7
08	54ALS10A	FLAT	2(a)	G4
09	54ALS10A	CCP	2(b)	7
10	54ALS10A	CCP	2(b)	4
11	54ALS10A	DIL	2(c)	D7
12	54ALS10A	DIL	2(c)	G4

TABLE 1(b) - MAXIMUM RATINGS

NO.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage	V_{CC}	– 0.5 to 7.0	V	-
2	Input Voltage	V_{IN}	– 0.5 to 7.0	V	Note 1
3	Device Dissipation	P_D	12.1	mWdc	Note 2
4	Operating Temperature Range	T_{op}	– 55 to + 125	°C	-
5	Storage Temperature Range	T_{stg}	– 65 to + 150	°C	-
6	Soldering Temperature For FP and DIP For CCP	T_{sol}	+ 265 + 245	°C	Note 3 Note 4

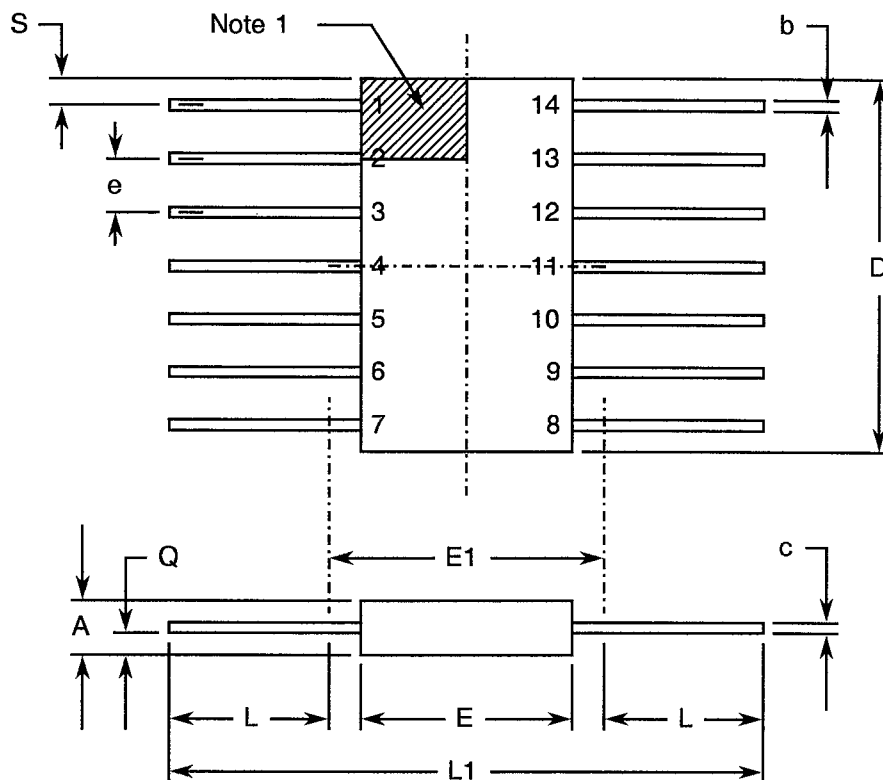
NOTES

1. Input Current limited to – 18mA.
2. Must withstand added P_D due to short circuit conditions (i.e. I_{OS}) at 1 output for 5 seconds.
3. Duration 10 seconds maximum at a distance of not less than 1.5mm from the package and the same lead shall not be resoldered until 3 minutes have elapsed.
4. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.



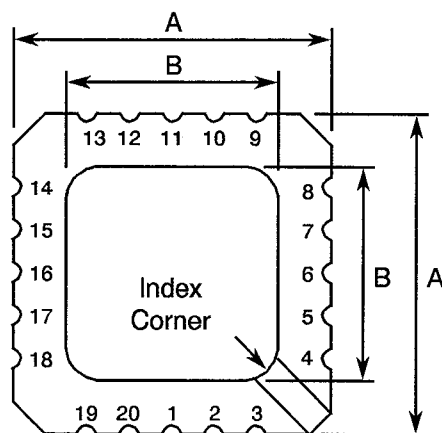
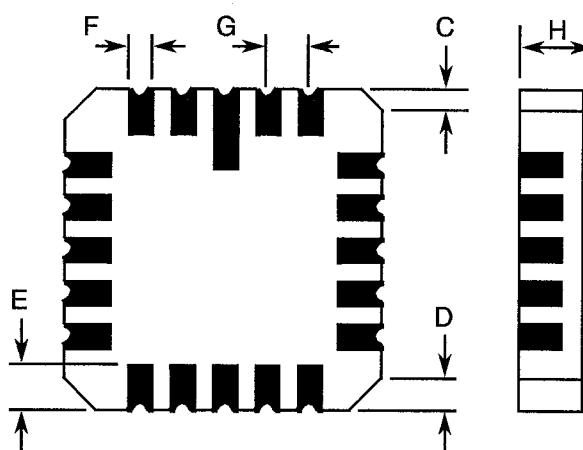
FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - FLAT PACKAGE



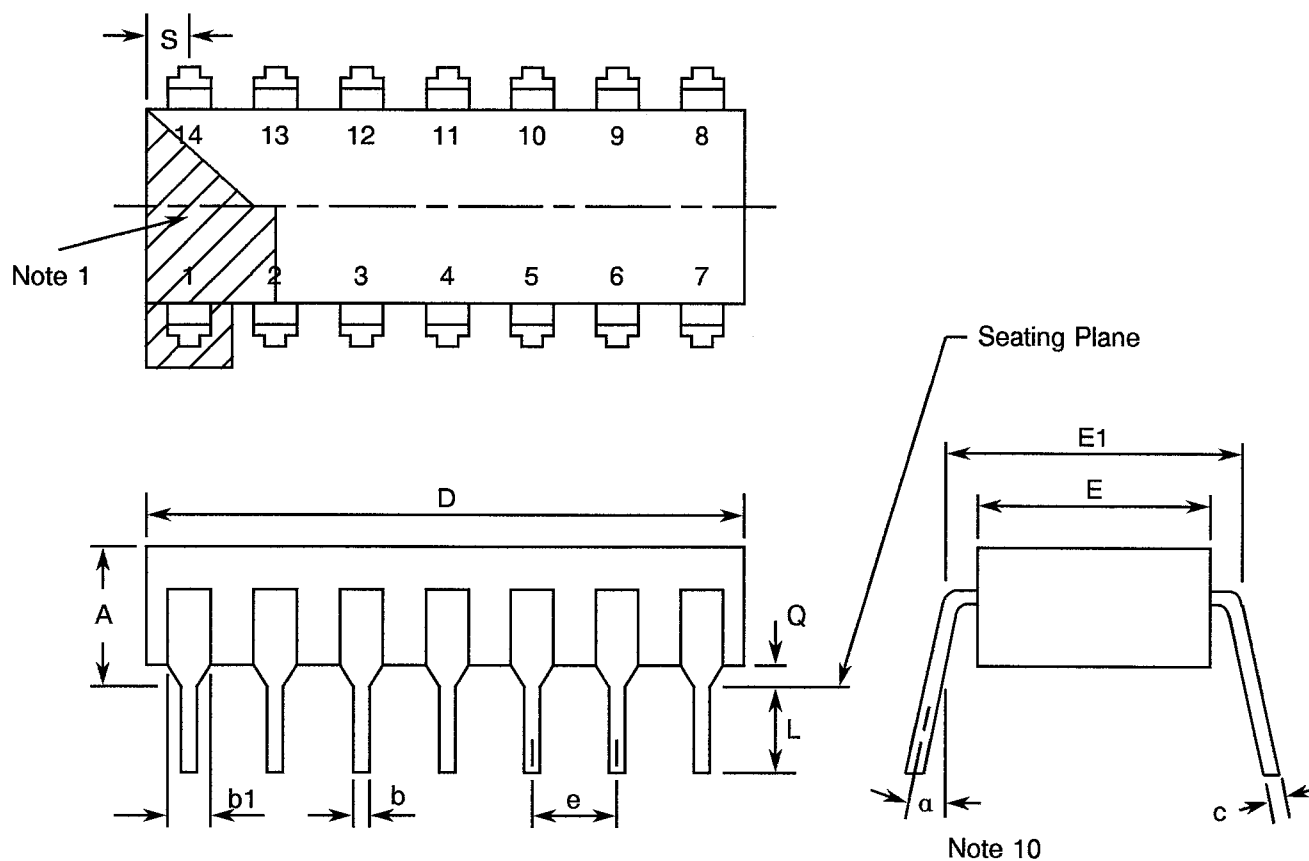
SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	1.24	2.03	
b	0.38	0.48	8
c	0.08	0.15	8
D	8.56	8.89	
E	5.97	6.73	
E1	-	7.11	4
e	1.27 TYPICAL		5, 9
L	6.85	8.00	
L1	21.30	21.90	
Q	0.51	1.02	2
S	0.25	0.64	7

NOTES: See Page 10.

**FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)****FIGURE 2(b) - SQUARE CHIP CARRIER PACKAGE (3 LAYER BASE)**20 Terminal

SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	8.687	9.093	
B	7.798	9.093	
C	0.250	0.510	11
D	0.889	1.143	12
E	1.140	1.400	8
F	0.559	0.712	8
G	1.27 TYPICAL		5, 9
H	1.630	2.540	

NOTES: See Page 10.

**FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)****FIGURE 2(c) - DUAL-IN-LINE PACKAGE**

SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	-	5.08	
b	0.38	0.58	8
b1	-	1.78	8
c	0.20	0.36	8
D	19.18	19.94	
E	6.22	7.11	
E1	7.37	7.87	4
e	2.54 TYPICAL		6, 9
L	3.30	5.08	
Q	0.51	2.03	3
S	1.78	2.54	7
a	0°	15°	10

NOTES: See Page 10.



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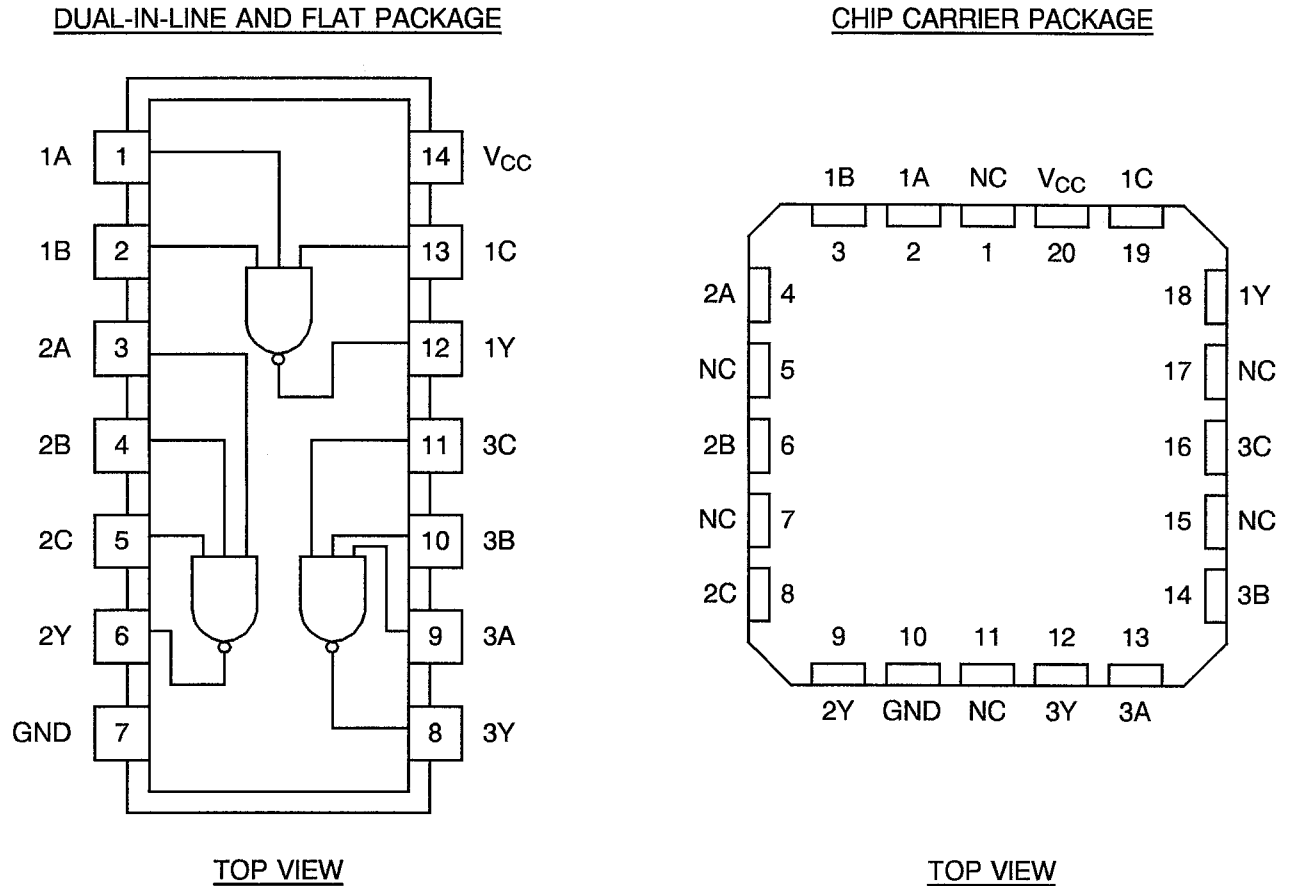
FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURES 2(a) TO 2(c) INCLUSIVE

1. Index area; a notch or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages the index shall be as defined in Figure 2(b).
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-centre lids, meniscus and glass overrun.
5. The true position pin or terminal spacing is 1.27mm between centrelines. Each pin or terminal centreline shall be located within $\pm 0.13\text{mm}$ of its true longitudinal position relative to Pins 1 and the highest pin number.
6. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within $\pm 0.25\text{mm}$ of its true longitudinal position relative to Pins 1 and the highest pin number.
7. Applies to all 4 corners.
8. All leads or terminals.
9. 12 spaces for flat and dual-in-line packages.
16 spaces for chip carrier packages.
10. Lead centre when α is 0° .
11. Index corner only - 2 dimensions.
12. 3 non-index corners - 6 dimensions.



FIGURE 3(a) - PIN ASSIGNMENT



FLAT PACKAGE AND DUAL-IN-LINE TO CHIP CARRIER PIN ASSIGNMENT

FLAT PACKAGE AND DUAL-IN-LINE PIN OUTS	1	2	3	4	5	6	7	8	9	10	11	12	13	14
CHIP CARRIER PIN OUTS	2	3	4	6	8	9	10	12	13	14	16	18	19	20

FIGURE 3(b) - TRUTH TABLE

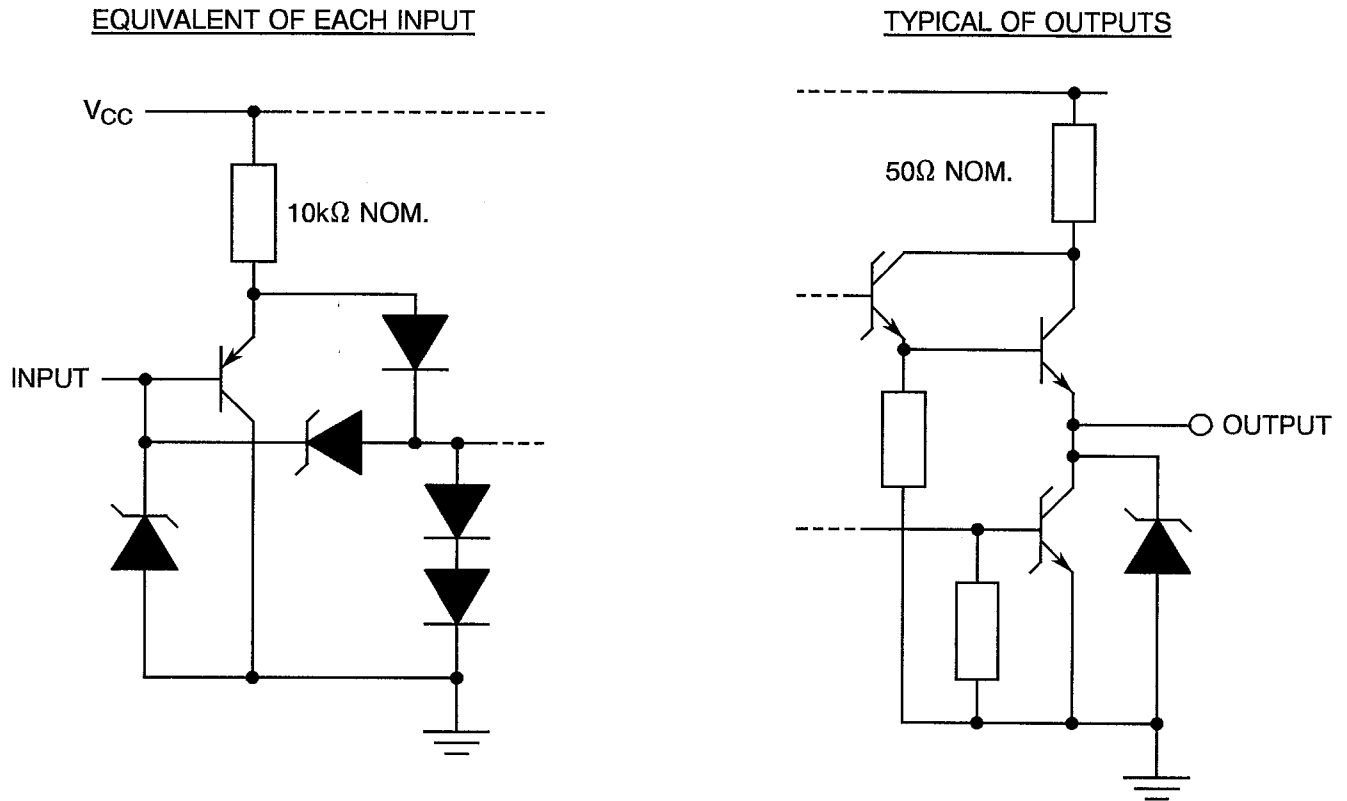
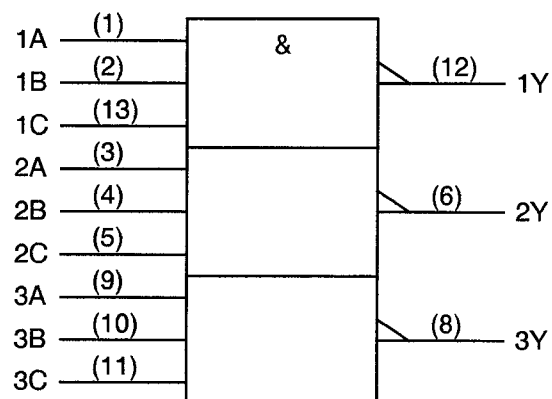
(EACH GATE)

INPUTS			OUTPUT Y
A	B	C	
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

NOTES

1. Positive Logic: $Y = \overline{A \cdot B \cdot C}$

2. Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant.

**FIGURE 3(c) - CIRCUIT SCHEMATIC****FIGURE 3(d) - FUNCTIONAL DIAGRAM****NOTES**

1. Pin numbers shown are for flat and dual-in-line packages; for chip carrier pins, see Figure 3(a).

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2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

- (a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.
- (b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviation is used:-

$I_{OS/2}$ - One half of the true output short circuit current.

4. REQUIREMENTS**4.1 GENERAL**

The complete requirements for procurement of the integrated circuits specified herein shall be as stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION**4.2.1 Deviations from Special In-process Controls**

None.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

- (a) Para. 7.1.1(a), "High Temperature Reverse Bias" tests and subsequent electrical measurements related to this test shall be omitted.
- (b) Para. 9.9.2, "Electrical Measurements at High and Low Temperatures": Only a test result summary, based on go-no-go tests and presented in histogram form is required.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.



4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 0.7 grammes for the flat package, 0.6 grammes for the chip carrier package and 2.2 grammes for the dual-in-line package.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body and the lids shall be welded, brazed, preform-soldered or glass frit-sealed.

4.4.2 Lead Material and Finish

For dual-in-line and flat packages, the material shall be either Type 'D' or Type 'G' with either Type '4' or Type '7' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. For chip carrier packages, the finish shall be either Type '4' or Type '7' in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING



4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

- (a) Lead Identification.
- (b) The SCC Component Number.
- (c) Traceability Information.

4.5.2 Lead Identification

For dual-in-line and flat packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side. For chip carrier packages, the index shall be as defined by Figure 2(b).

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4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:

920109302B

Detail Specification Number _____

Type Variant (see Table 1(a)) _____

Testing Level (B or C, as applicable) _____

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ °C and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for power burn-in shall be as specified in Table 5 of this specification.

4.7.3 Electrical Circuits for Power Burn-in

Circuits for use in performing the power burn-in tests are shown in Figure 5 of this specification.



TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test	-	-	3(b)	Verify Truth Table with Load. Note 1	-	-	-
2 to 10	Input Current High Level 1	I_{IH1}	3010	4(a)	$V_{CC} = 5.5V$, $V_{IN} = 2.7V$ (Pins D/F 1-2-3-4-5-9-10-11-13) (Pins C 2-3-4-6-8-13-14-16-19)	-	20	μA
11 to 19	Input Current High Level 2 (Max. Input Voltage)	I_{IH2}	3010	4(a)	$V_{CC} = 5.5V$, $V_{IN} = 7.0V$ (Pins D/F 1-2-3-4-5-9-10-11-13) (Pins C 2-3-4-6-8-13-14-16-19)	-	100	μA
20 to 28	Input Clamp Voltage	V_{IC}	3008	4(b)	$V_{CC} = 4.5V$, $I_{IN} = -18mA$ Note 2 (Pins D/F 1-2-3-4-5-9-10-11-13) (Pins C 2-3-4-6-8-13-14-16-19)	-	-1.5	V
29 to 37	Input Current Low Level	I_{IL}	3009	4(c)	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$ (Pins D/F 1-2-3-4-5-9-10-11-13) (Pins C 2-3-4-6-8-13-14-16-19)	-	-100	μA
38 to 40	Output Voltage Low Level	V_{OL}	3007	4(d)	$V_{CC} = 4.5V$, $V_{IH} = 2.0V$ $I_{OL} = 4mA$ (Pins D/F 6-8-12) (Pins C 9-12-18)	-	0.4	V
41 to 49	Output Voltage High Level 1	V_{OH1}	3006	4(e)	$V_{CC} = 4.5V$, $V_{IH} = 2.0V$ $V_{IL} = 0.7V$, $I_{OH} = -400\mu A$ (Pins D/F 6-8-12) (Pins C 9-12-18)	2.5	-	V
50 to 58	Output Voltage High Level 2	V_{OH2}	3006	4(e)	$V_{CC} = 5.5V$, $V_{IH} = 2.0V$ $V_{IL} = 0.7V$, $I_{OH} = -400\mu A$ (Pins D/F 6-8-12) (Pins C 9-12-18)	3.5	-	V

NOTES: See Page 18.



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TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
59 to 61	One Half of the True Output Short Circuit Current	$I_{OS/2}$	3011	4(f)	$V_{CC} = 5.5V$, $V_{OUT} = 2.25V$ Note 3 (Pins D/F 6-8-12) (Pins C 9-12-18)	-30	-112	mA
62	Supply Current Outputs High	I_{CCH}	3005	4(g)	$V_{CC} = 5.5V$ All Inputs at Ground (Pin D/F 14) (Pin C 20)	-	0.6	mA
63	Supply Current Outputs Low	I_{CCL}	3005	4(g)	$V_{CC} = 5.5V$ All Inputs at 4.5V (Pin D/F 14) (Pin C 20)	-	2.2	mA

NOTES: See Page 18.



TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP) (NOTE 4)	LIMITS		UNIT																				
						MIN	MAX																					
64 to 81	Propagation Delay Low to High A or B or C to Y	t _{PLH}	3003	4(h)	V _{CC} = 4.5 and 5.5V C _L = 50pF, R _L = 500Ω Variants 01 to 06 Variants 07 to 12 <table><tr><td><u>Pins D/F</u></td><td><u>Pins C</u></td></tr><tr><td>1 to 12</td><td>2 to 18</td></tr><tr><td>2 to 12</td><td>3 to 18</td></tr><tr><td>13 to 12</td><td>19 to 18</td></tr><tr><td>3 to 6</td><td>4 to 9</td></tr><tr><td>4 to 6</td><td>6 to 9</td></tr><tr><td>5 to 6</td><td>8 to 9</td></tr><tr><td>9 to 8</td><td>13 to 12</td></tr><tr><td>10 to 8</td><td>14 to 12</td></tr><tr><td>11 to 8</td><td>16 to 12</td></tr></table>	<u>Pins D/F</u>	<u>Pins C</u>	1 to 12	2 to 18	2 to 12	3 to 18	13 to 12	19 to 18	3 to 6	4 to 9	4 to 6	6 to 9	5 to 6	8 to 9	9 to 8	13 to 12	10 to 8	14 to 12	11 to 8	16 to 12	3 2	14 11	ns
<u>Pins D/F</u>	<u>Pins C</u>																											
1 to 12	2 to 18																											
2 to 12	3 to 18																											
13 to 12	19 to 18																											
3 to 6	4 to 9																											
4 to 6	6 to 9																											
5 to 6	8 to 9																											
9 to 8	13 to 12																											
10 to 8	14 to 12																											
11 to 8	16 to 12																											
82 to 99	Propagation Delay High to Low A or B or C to Y	t _{PHL}	3003	4(h)	V _{CC} = 4.5 and 5.5V C _L = 50pF, R _L = 500Ω Variants 01 to 06 Variants 07 to 12 <table><tr><td><u>Pins D/F</u></td><td><u>Pins C</u></td></tr><tr><td>1 to 12</td><td>2 to 18</td></tr><tr><td>2 to 12</td><td>3 to 18</td></tr><tr><td>13 to 12</td><td>19 to 18</td></tr><tr><td>3 to 6</td><td>4 to 9</td></tr><tr><td>4 to 6</td><td>6 to 9</td></tr><tr><td>5 to 6</td><td>8 to 9</td></tr><tr><td>9 to 8</td><td>13 to 12</td></tr><tr><td>10 to 8</td><td>14 to 12</td></tr><tr><td>11 to 8</td><td>16 to 12</td></tr></table>	<u>Pins D/F</u>	<u>Pins C</u>	1 to 12	2 to 18	2 to 12	3 to 18	13 to 12	19 to 18	3 to 6	4 to 9	4 to 6	6 to 9	5 to 6	8 to 9	9 to 8	13 to 12	10 to 8	14 to 12	11 to 8	16 to 12	4 2	21 10	ns
<u>Pins D/F</u>	<u>Pins C</u>																											
1 to 12	2 to 18																											
2 to 12	3 to 18																											
13 to 12	19 to 18																											
3 to 6	4 to 9																											
4 to 6	6 to 9																											
5 to 6	8 to 9																											
9 to 8	13 to 12																											
10 to 8	14 to 12																											
11 to 8	16 to 12																											

NOTES



- Go-no-go test with $V_{IL} = 0.3V$, $V_{IH} = 3.0V$, trip point $1.5V$.
- All inputs and outputs not under test shall be open.
- No more than 1 output should be tested at a time.
- Propagation delay measurements shall be performed as a go-no-go test on a 100% basis. Read-and-record measurements shall be performed on an LTPD7 sample basis following the Chart III burn-in test.



**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES,
+ 125(+ 0 – 5) °C AND – 55(+ 5 – 0) °C**

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test	-	-	3(b)	Verify Truth Table with Load. Note 1	-	-	-
2 to 10	Input Current High Level 1	I_{IH1}	3010	4(a)	$V_{CC} = 5.5V$, $V_{IN} = 2.7V$ (Pins D/F 1-2-3-4-5-9-10-11-13) (Pins C 2-3-4-6-8-13-14-16-19)	-	20	μA
11 to 19	Input Current High Level 2 (Max. Input Voltage)	I_{IH2}	3010	4(a)	$V_{CC} = 5.5V$, $V_{IN} = 7.0V$ (Pins D/F 1-2-3-4-5-9-10-11-13) (Pins C 2-3-4-6-8-13-14-16-19)	-	100	μA
20 to 28	Input Clamp Voltage	V_{IC}	3008	4(b)	$V_{CC} = 4.5V$, $I_{IN} = -18mA$ Note 2 (Pins D/F 1-2-3-4-5-9-10-11-13) (Pins C 2-3-4-6-8-13-14-16-19)	-	-1.5	V
29 to 37	Input Current Low Level	I_{IL}	3009	4(c)	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$ (Pins D/F 1-2-3-4-5-9-10-11-13) (Pins C 2-3-4-6-8-13-14-16-19)	-	-100	μA
38 to 40	Output Voltage Low Level	V_{OL}	3007	4(d)	$V_{CC} = 4.5V$, $V_{IH} = 2.0V$ $I_{OL} = 4mA$ (Pins D/F 6-8-12) (Pins C 9-12-18)	-	0.4	V
41 to 49	Output Voltage High Level 1	V_{OH1}	3006	4(e)	$V_{CC} = 4.5V$, $V_{IH} = 2.0V$ $V_{IL} = 0.7V$, $I_{OH} = -400\mu A$ (Pins D/F 6-8-12) (Pins C 9-12-18)	2.5	-	V
50 to 58	Output Voltage High Level 2	V_{OH2}	3006	4(e)	$V_{CC} = 5.5V$, $V_{IH} = 2.0V$ $V_{IL} = 0.7V$, $I_{OH} = -400\mu A$ (Pins D/F 6-8-12) (Pins C 9-12-18)	3.5	-	V

NOTES: See Page 18.

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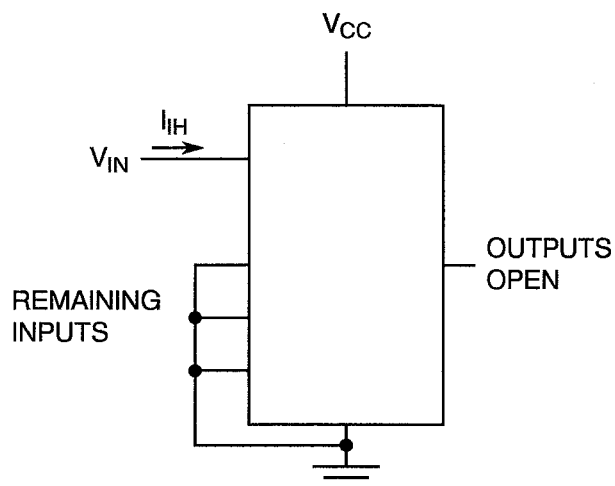
**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES,
+ 125(+ 0 – 5) °C AND – 55(+ 5 – 0) °C (CONT'D)**

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
59 to 61	One Half of the True Output Short Circuit Current	$I_{OS/2}$	3011	4(f)	$V_{CC} = 5.5V$, $V_{OUT} = 2.25V$ Note 3 (Pins D/F 6-8-12) (Pins C 9-12-18)	– 30	– 112	mA
62	Supply Current Outputs High	I_{CCH}	3005	4(g)	$V_{CC} = 5.5V$ All Inputs at Ground (Pin D/F 14) (Pin C 20)	-	0.6	mA
63	Supply Current Outputs Low	I_{CCL}	3005	4(g)	$V_{CC} = 5.5V$ All Inputs at 4.5V (Pin D/F 14) (Pin C 20)	-	2.2	mA

NOTES: See Page 18.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

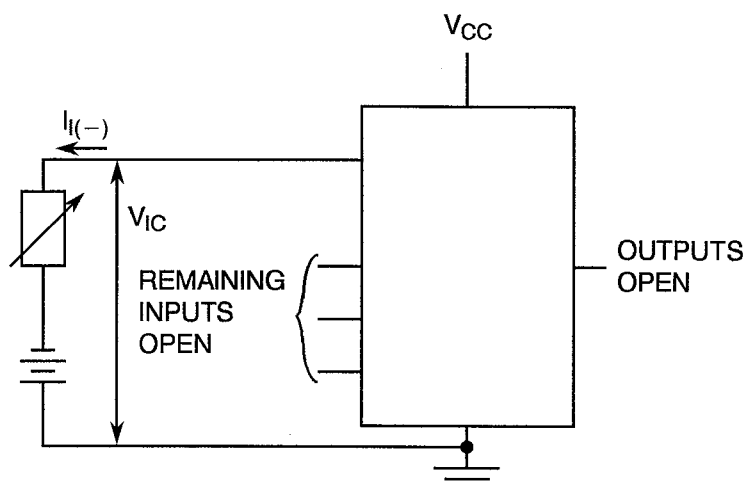
FIGURE 4(a) - INPUT CURRENT HIGH LEVEL



NOTES

1. Each input to be tested separately.

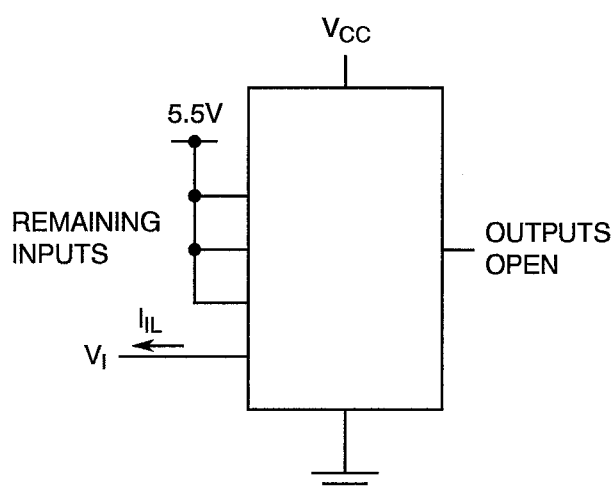
FIGURE 4(b) - INPUT CLAMP VOLTAGE



NOTES

1. Each input to be tested separately.

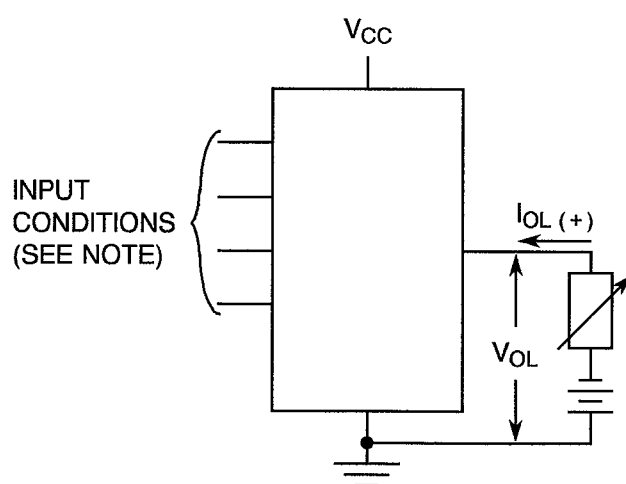
FIGURE 4(c) - LOW LEVEL INPUT CURRENT



NOTES

1. Each input to be tested separately.

FIGURE 4(d) - LOW LEVEL OUTPUT VOLTAGE

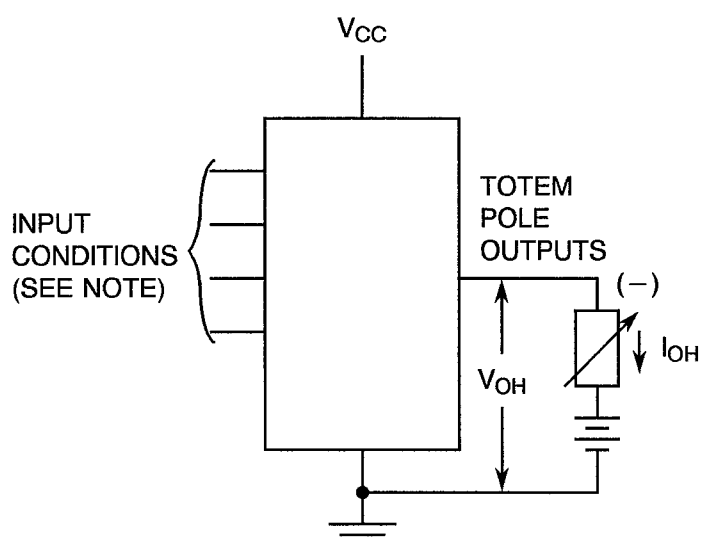


NOTES

1. All inputs at V_{IH} min.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

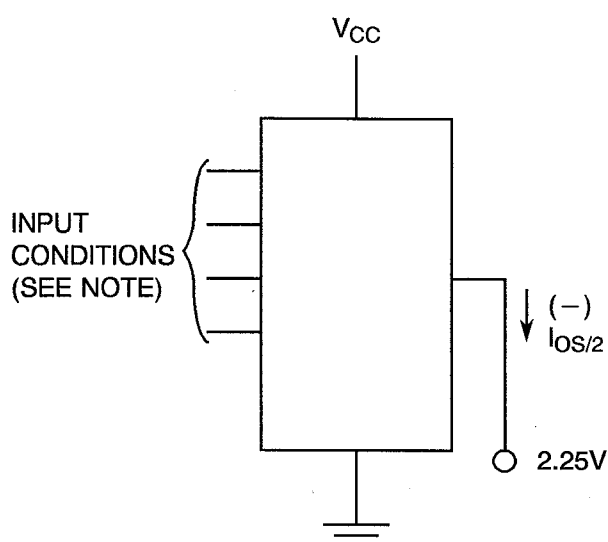
FIGURE 4(e) - HIGH LEVEL OUTPUT VOLTAGE



NOTES

1. Each input in turn at V_{IL} with all other inputs at V_{IH} .

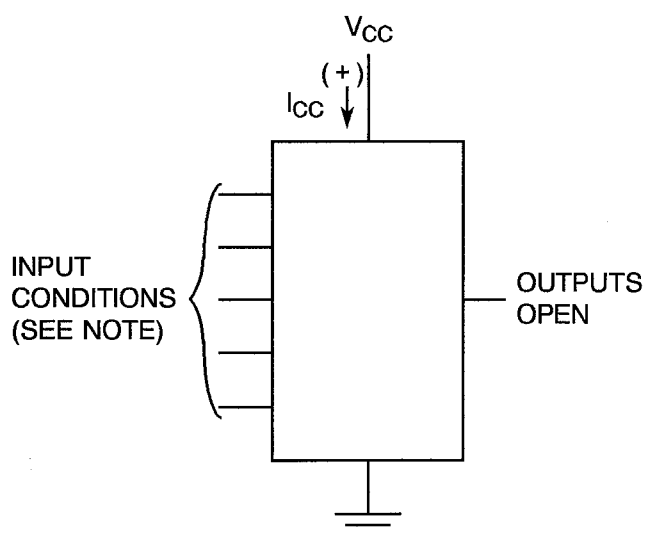
FIGURE 4(f) - ONE HALF SHORT CIRCUIT OUTPUT CURRENT



NOTES

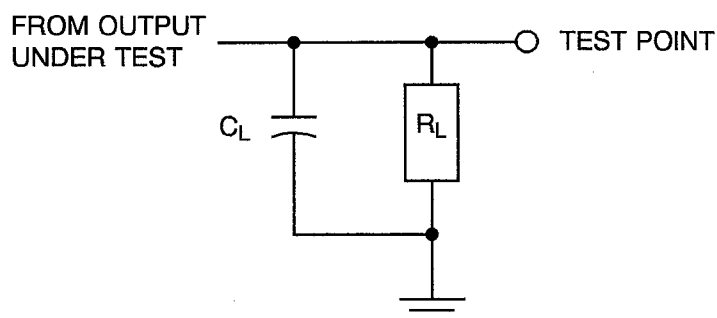
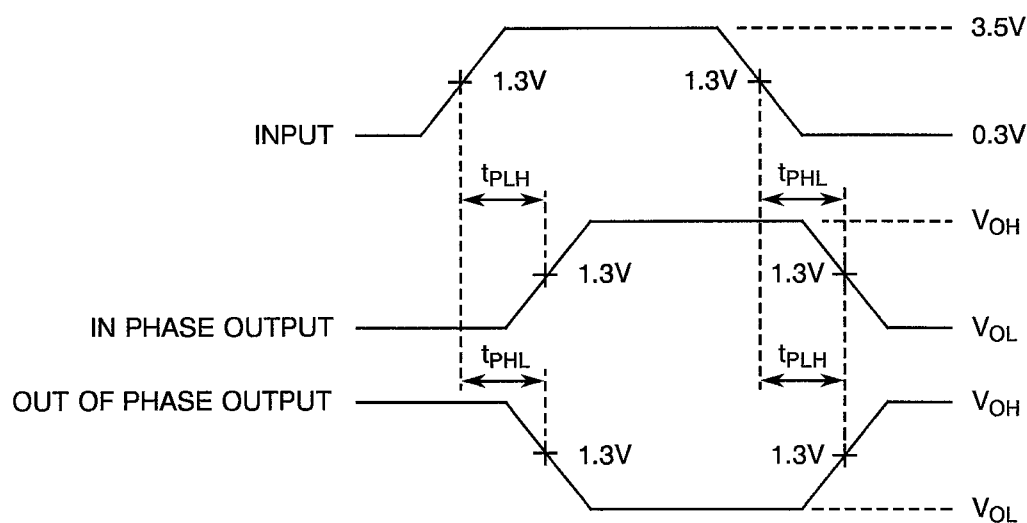
1. All inputs at Ground.
2. Each gate to be tested separately.

FIGURE 4(g) - SUPPLY CURRENT



NOTES

1. For I_{CCH} all inputs at Ground.
For I_{CCL} all inputs at 4.5V.

**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)**FIGURE 4(h) - DYNAMIC TEST AND SWITCHING WAVEFORMSVOLTAGE WAVEFORMS - PROPAGATION DELAY TIMES**NOTES**

1. The generator has the following characteristics: $t_r = t_f = 2\text{ns}$, $\text{PRR} = 1\text{MHz}$, $Z_{\text{out}} = 50\Omega$, Duty Cycle = 50%.
2. $C_L = 50\text{pF} \pm 5\%$ including scope probe, wiring and stray capacitance without package in test fixture.
3. Each gate tested separately.
4. $R_L = 500\Omega \pm 5\%$.



TABLE 4 - PARAMETER DRIFT VALUES

NO.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
2 to 10	Input Current High Level 1	I_{IH1}	As per Table 2	As per Table 2	± 20 or (1) ± 0.5	% μA
29 to 37	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	± 10	μA
38 to 40	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	± 60	mV
41 to 49	Output Voltage High Level 1	V_{OH1}	As per Table 2	As per Table 2	± 200	mV
50 to 58	Output Voltage High Level 2	V_{OH2}	As per Table 2	As per Table 2	± 200	mV

NOTES

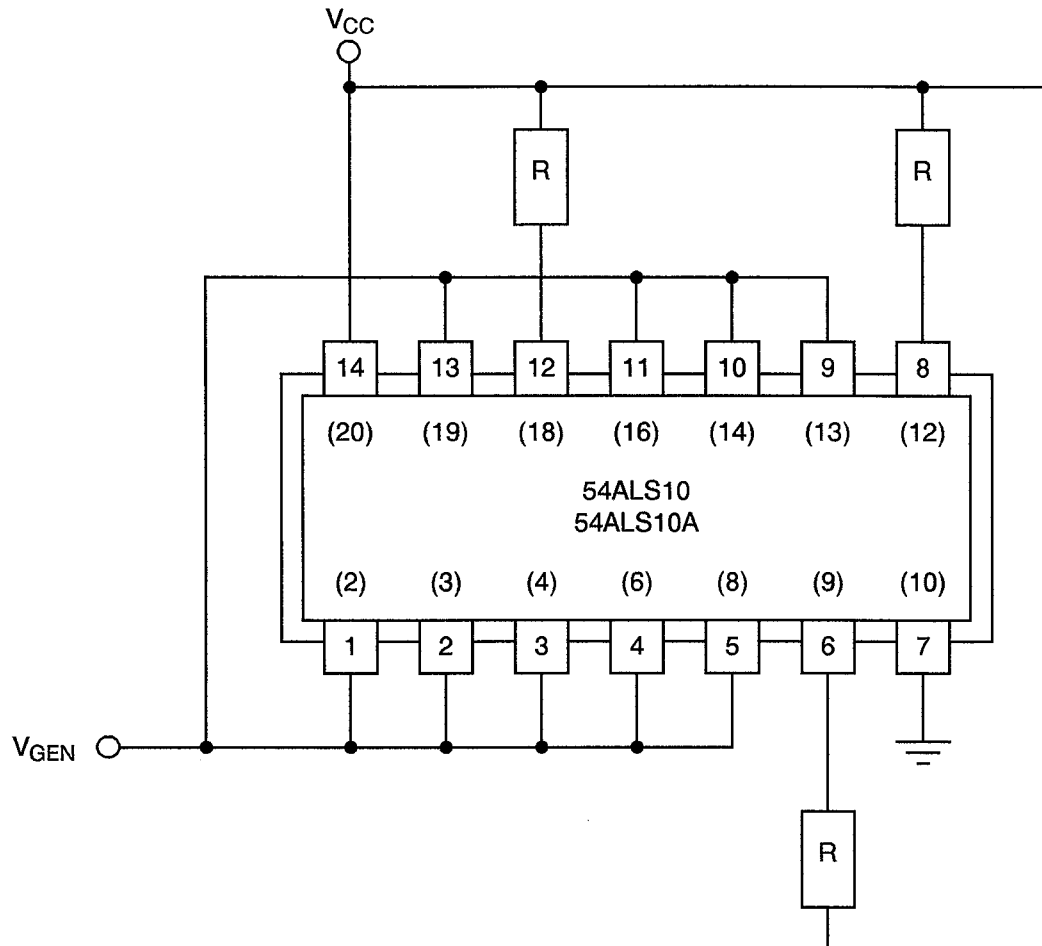
1. Whichever is greater referred to the initial value.

TABLE 5 - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TEST



NO.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+ 125(+ 0 – 5)	$^{\circ}C$
2	Power Supply Voltage	V_{CC}	+ 5(+ 0.5 – 0)	V
3	Pulse Voltage	V_{GEN}	0.5 max. to 3.0 min.	V
4	Frequency	f	100 (See Note 1)	Hz
5	Fan-out	-	10	-
6	Rise Time	t_r	50 max.	μs
7	Fall Time	t_f	50 max.	μs
8	Duty Cycle	-	20 min.	%

NOTES

1. Tolerance $\pm 10\%$.

**FIGURE 5 - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TEST****NOTES**

1. Pin numbers in parenthesis are for the chip carrier package.
2. $R = 1.2k\Omega$.

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4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5 of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5.


4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The conditions for high temperature storage shall be $T_{amb} = +150(+0-5)$ °C.



TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTS

NO.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS		UNIT
					(Δ)	ABSOLUTE	
2 to 10	Input Current High Level 1	I_{IH1}	As per Table 2	As per Table 2	± 1	-	μA
11 to 19	Input Current High Level 2 (Max. Input Voltage)	I_{IH2}	As per Table 2	As per Table 2	-	100	μA
29 to 37	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	± 10	-	μA
38 to 40	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	± 60	-	mV
41 to 49	Output Voltage High Level 1	V_{OH1}	As per Table 2	As per Table 2	± 200	-	mV
50 to 58	Output Voltage High Level 2	V_{OH2}	As per Table 2	As per Table 2	± 200	-	mV
62	Supply Current Outputs High	I_{CCH}	As per Table 2	As per Table 2	± 20	-	%
63	Supply Current Outputs Low	I_{CCL}	As per Table 2	As per Table 2	± 20	-	%

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APPENDIX 'A'

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AGREED DEVIATIONS FOR TEXAS INSTRUMENTS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.1	Scanning Electron Microscope (SEM) Inspection may be performed using TIF document TIF 3.61.610.001.
Para. 4.2.2	Prior to Die Shear Test TIF may perform a Radiographic Inspection on the randomly chosen samples to be subjected to this test, using TIF document TIF 50.42-3002.
Para. 4.2.3	Radiographic Inspection may be performed using TIF document TIF 50.42-3002.