CHARGE COUPLED DEVICES,

SILICON, PHOTOSENSITIVE, AREA ARRAY,

IMAGE SENSOR, 286 LINES×382 PIXELS,

BASED ON TYPE TH7863D

ESCC Detail Specification No. 9610/003

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Pages 1 to 52

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space components
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TABLE OF CONTENTS

		Page
1.	**GENERAL**	5
1.1	Scope	5
1.2	Component Type Variants	5
1.3	Maximum Ratings	5
1.4	Parameter Derating Information	5
1.5	Physical Dimensions and Geometrical Characteristics	5
1.6	Pin Assignment	5
1.7	Timing Diagrams	5
1.8	Functional Diagram	5
1.9	Handling Precautions	5
1.10	Input Protection Networks	5
2.	**APPLICABLE DOCUMENTS**	22
3.	**TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS**	22
4.	**REQUIREMENTS**	22
4.1	General	22
4.2	Deviations from Generic Specification	22
4.2.1	Deviations from Special In-process Controls	22
4.2.2	Deviations from Final Production Tests	22
4.2.3	Deviations from Burn-in Tests	22
4.2.4	Deviations from Qualification Tests	23
4.2.5	Deviations from Lot Acceptance Tests	23
4.3	Mechanical Requirements	23
4.3.1	Dimension Check	23
4.3.2	Geometrical Characteristics	23
4.3.3	Weight	23
4.3.4	Terminal Strength	23
4.4	Materials and Finishes	23
4.4.1	Case	23
4.4.2	Lead Material and Finish	23
4.4.3	Window	23
4.5	Marking	24
4.5.1	General	24
4.5.2	Lead Identification	24
4.5.3	The SCC Component Number	24
4.5.4	Traceability Information	25
4.6	Electrical and Electro-optical Measurements	25
4.6.1	Electrical and Electro-optical Measurements at Reference Temperature	25
4.6.2	Electrical and Electro-optical Measurements at High and Low Temperatures	25
4.6.3	Circuits for Electrical and Electro-optical Measurements	25
4.7	Burn-in Tests	25
4.7.1	Parameter Drift Values	25
4.7.2	Conditions for High Temperature Reverse Bias Burn-in	25
4.7.3	Conditions for Power Burn-in	25
4.7.4	Electrical Circuits for High Temperature Reverse Bias Burn-in	25
4.7.5	Electrical Circuits for Power Burn-in	25
4.8	Environmental and Endurance Tests	43
4.8.1	Electrical and Electro-optical Measurements on Completion of Environmental Tests	43
4.8.2	Electrical and Electro-optical Measurements at Intermediate Points during Endurance Tests	43

		Page
4.8.3	Electrical and Electro-optical Measurements on Completion of Endurance Tests	43
4.8.4	Conditions for Operating Life Tests	43
4.8.5	Electrical Circuits for Operating Life Tests	43
4.8.6	Conditions for High Temperature Storage Test	43
4.9	Total Dose Irradiation Testing	43
4.9.1	Application	43
4.9.2	Bias Conditions	43
4.9.3	Electrical and Electro-optical Measurements	43

TABLES

1(a)	Type Variant Summary	6
	Type Variant Detailed Information	47
1(b)	Maximum Ratings	6
1(c)	Format for individual Tables 1(a)	7
2	Electrical and Electro-optical Measurements at Reference Temperature	26
3	Electrical and Electro-optical Measurements at High and Low Temperatures	33
4	Parameter Drift Values	40
5(a)	Conditions for High Temperature Reverse Bias Burn-in	41
5(b)	Conditions for Power Burn-in and Operating Life Tests	41
6	Electrical and Electro-optical Measurements on Completion of Environmental Tests and at Intermediate Points and on Completion of Endurance Testing	44
7	Electrical and Electro-optical Measurements During and on Completion of Irradiation Testing	46

FIGURES

1	Parameter Derating Information	6
2	Physical Dimensions	11
3(a)	Pin Assignment	14
3(b)	Timing Diagrams	15
3(c)	Functional Diagram	21
3(d)	Input Protection Networks	21
4	Circuits for Electrical and Electro-optical Measurements	34
5(a)	Electrical Circuit for High Temperature Reverse Bias Burn-in	42
5(b)	Electrical Circuit for Power Burn-in and Operating Life Tests	42
6	Bias Conditions for Irradiation Testing	45

APPENDICES (Applicable to specific Manufacturers only)
None.

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical, geometrical, electrical and electro-optical characteristics, test and inspection data for a silicon Photosensitive Area Array CCD Image Sensor, 286 Lines × 382 Pixels, based on Type TH7863D. It shall be read in conjunction with ESA/SCC Generic Specification No. 9020, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

A list of the type variants of the basic area array CCD image sensor specified herein, which are also covered by this specification, are given in "Table 1(a) - Type Variant Summary".

For each type variant, the full electro-optical, electrical and geometrical characteristics are given in individual "Tables 1(a) - Type Variant Detailed Information" at the end of this specification.

The contents of the individual Tables 1(a) shall be as shown in Table 1(c).

The specific characteristics shall be negotiated between the Manufacturer and the Orderer. The Manufacturer shall then apply to the ESA/SCC Secretariat for a type variant number for each individual basic area array CCD image sensor concerned, by sending a finalised Table 1(a) which shall also be copied to the Qualifying Space Agency (QSA).

For information concerning Variant 01, see ESA/SCC Generic Specification No. 9020, Para. 4.1.1.

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the components specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS AND GEOMETRICAL CHARACTERISTICS

The physical dimensions and geometrical characteristics of the components specified herein are shown in Figures 2(a) and 2(b).

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TIMING DIAGRAMS

As per Figure 3(b).

1.8 FUNCTIONAL DIAGRAM

As per Figure 3(c).

1.9 HANDLING PRECAUTIONS

The component is susceptible to damage by electro-static discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 with a Minimum Critical Path Failure Voltage of 400 Volts.

1.10 INPUT PROTECTION NETWORKS

Protection networks shall be incorporated into each input as shown in Figure 3(d).

TABLE 1(a) - TYPE VARIANT SUMMARY

VARIANT	REFERENCE TEMPERATURE (T_{ref} °C)	OPERATING TEMPERATURE RANGE (T_{op} °C)	TIMING DIAGRAM (FIGURE 3(b)) (TD)	SPECTRAL RANGE FOR WINDOW OPTICAL COATING WOC (nm)
01	+25 ± 3	−20 to +85	TD1	N/A
02	+35 ± 3	−20 to +85	TD2	450 to 900

NOTES

1. Full electrical and electro-optical characteristics are given in the individual Tables 1(a) at the end of this specification.

TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNITS	REMARKS
1	Range of applied voltages	-	−0.3 to +19	V	Note 1
2	Range of applied voltages	-	−0.3 to +16	V	Note 2
3	Range of applied voltages	-	−5.0 to 0	V	Note 3
4	Input Current	I_{IN}	200	mA	-
5	Device Dissipation (Continuous)	P_D	Note 4	mW	-
6	Operating Temperature Range	T_{op}	Note 5	°C	T_{amb} Note 6
7	Storage Temperature Range	T_{stg}	−55 to +150	°C	-
8	Soldering Temperature	T_{sol}	+260	°C	Note 7

NOTES

1. On pins 5, 15, 18 with respect to pins 1, 10.
2. On pins 2, 3, 4, 6, 7, 8, 9, 11, 12, 13, 14, 19, 20 with respect to pins 1, 10.
3. On pins 1, 10, 17.
4. The maximum device dissipation is determined by $19V \times I_{DD(T_{op})}$ max. (mA) (see individual Tables 1(a)).
5. See Table 1(a).
6. Shall not exceed the Storage Temperature Range.
7. Duration 10 seconds maximum at a distance of not less than 3.0mm from the package and the same lead shall not be resoldered until 3.0 minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION

Not applicable.

TABLE 1(c) - FORMAT FOR INDIVIDUAL TABLES 1(a)

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION

TYPE VARIANT No.

No.	CHARACTERISTICS	SYMBOL	LIMITS		UNITS	REMARKS
			MIN.	MAX.		
1	Operating Temperature Range	T_{op}			°C	
2	Reference Temperature	T_{ref}			°C	
3	Flatness of Image Area	P			µm	
4	Spectral Range for Optical Coating on Window	WOC			nm	Note 1
5	Timing Diagram	TD			-	Note 2
6	Power Supply Current 1	I_{DD1}			mA	Note 3
7	Power Supply Current 2	I_{DD2}			mA	Note 3
8	Power Supply Current 1 over T_{op}	I_{DD1} (T_{op})			mA	Note 3
9	DC Output Level	V_{Ref}			V	
10	Output Impedance	Z_S			Ω	Note 4
11	Saturation Voltage for the Image Area	V_{SAT}			mV	
12	Vertical Charge Transfer Inefficiency	VCTI			%	Note 5
13	Horizontal Charge Transfer Inefficiency	HCTI			%	Note 5
14	Average Dark Signal (Image Area)	VDS1			mV	Note 6
15	Average Dark Signal (Image Area + Storage Area)	VDS2			mV	Note 6
16	Average Dark Signal (Image Area + Storage Area) over T_{op}	VDS2(T_{op})			mV	Note 6
17	Dark Signal Non-uniformity, standard deviation σ	DSNU(σ)			mV	Note 7
18	Number of Dark Signal Defects beyond a3 limit	Ndef3			-	Note 7

NOTES: See Page 10.

TABLE 1(c) - FORMAT FOR INDIVIDUAL TABLES 1(a) (CONTINUED)

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION (CONTINUED)

TYPE VARIANT No.

No.	CHARACTERISTICS	SYMBOL	LIMITS		UNITS	REMARKS
			MIN.	MAX.		
19	Number of Dark Signal Defects beyond a4 limit	Ndef4			-	Note 7
20	DSNU Limit for Ndef3	a3			mV	Note 7
21	DSNU Limit for Ndef4	a4			mV	Note 7
22	Responsivity	R			V/μJ/cm²	Note 8
23	Responsivity over T_{op}	$R(T_{op})$			V/μJ/cm²	
24	Photoresponse Non-uniformity, standard deviation σ	PRNU(σ)			%	Note 9
25	Number of PRNU Defects beyond a1 Limit	Ndef1			-	Note 9
26	Number of PRNU Defects beyond a2 Limit	Ndef2			-	Note 9
27	PRNU Limit for Ndef1	a1			%	Note 9
28	PRNU Limit for Ndef2	a2			%	Note 9
29	Spectral Responsivity in Optical Band B1	R(B1)			V/μJ/cm²	Note 10
30	Spectral Responsivity in Optical Band B2	R(B2)			V/μJ/cm²	Note 10
31	Spectral Responsivity in Optical Band B3	R(B3)			V/μJ/cm²	Note 10
32	Spectral Responsivity in Optical Band B4	R(B4)			V/μJ/cm²	Note 10
33	Spectral Responsivity in Optical Band B5	R(B5)			V/μJ/cm²	Note 10
34	Spectral Responsivity in Optical Band B6	R(B6)			V/μJ/cm²	Note 10
35	Spectral Responsivity in Optical Band B7	R(B7)			V/μJ/cm²	Note 10
36	Linearity Error	LE			%	Note 11

NOTES: See Page 10.

TABLE 1(c) - FORMAT FOR INDIVIDUAL TABLES 1(a) (CONTINUED)

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION (CONTINUED)

TYPE VARIANT No.

No.	CHARACTERISTICS	SYMBOL	LIMITS		UNITS	REMARKS
			MIN.	MAX.		
37	Temporal Noise	V_N			µV	Note 12
38	Offset Voltage	V_{Offset}			mV	
39	Amplitude of Reset Feedthrough	V_{Reset}			mV	
40	Reference Level Settling Time	$t_{D\text{-}Ref}$			ns	Note 13
41	Reference Level Duration	$t_{U\text{-}Ref}$			ns	Note 13
42	Reference Level Error Band	ΔU_{Ref}			mV	Note 13
43	Signal Level Settling Time	$t_{D\text{-}Signal}$			ns	Note 13
44	Signal Level Duration	$t_{U\text{-}Signal}$			ns	Note 13
45	Signal Level Error Band	ΔU_{Signal}			mV	Note 13
46	Electrode Capacitance	$C\phi P$			pF	Note 14
47	Electrode Capacitance	$C\phi M$			pF	Note 14
48	Electrode Capacitance	$C\phi L$			pF	Note 14
49	Electrode Capacitance	$C\phi R$			pF	Note 14
50	Electrode Capacitance with respect to another Clock	$C\phi Po$			pF	Note 15
51	Electrode Capacitance with respect to another Clock	$C\phi Mo$			pF	Note 15
52	Electrode Capacitance with respect to another Clock	$C\phi Lo$			pF	Note 15
53	Charge to Voltage Conversion Factor	CVF			µV/e	Note 16

NOTES: See Page 10.

TABLE 1(c) - FORMAT FOR INDIVIDUAL TABLES 1(a) (CONTINUED)

NOTES

1. The reflectance for each side of the window shall be specified inside the spectral range for optical coating.
2. The timing diagram TD1 or TD2, as specified in Table 1(a), shall be used for all measurements.
3. I_{DD1} measurement shall be static, I_{DD2} measurement shall be dynamic, $I_{DD1(T_{op})}$ measurement shall be static and all shall be specified in Table 1(a).
4. The values of R and C used for output impedance measurement shall be defined in Table 1(a).
5. The measurement is based on uniform illumination - ESA/SCC Basic Specification No. 25000, Para. 6.12.2(a).
6. VDS1 is measured on the first lines or on the whole area if the integration time induces a negligible slope effect.

   VDS2 is measured on the last lines.
7. The slope effect is removed.
8. The responsivity is measured under uniform illumination with BG38 optical filter.
9. Optical bands used for PRNU calculation shall be defined in Table 1(a).
10. The optical bands shall be specified in terms of centre wavelength and bandwidth at 50% of transmission peak.
11. The measurement is made under uniform illumination with a BG38 optical filter. The output signal range used for linearity error calculation shall be defined in Table 1(a).
12. The measurement is based on two successive acquisitions of the same row.
13. For output signal waveform measurements, the error bands for reference and signal levels are defined by ΔU_{Ref} and ΔU_{Signal}. Settling times can be referenced either to ϕR or ϕL2 edges (to be specified in Table 1(a)).
14. Boonton Bridge. Load voltage is typically DC = 10V
    AC = 50mV, 1.0MHz

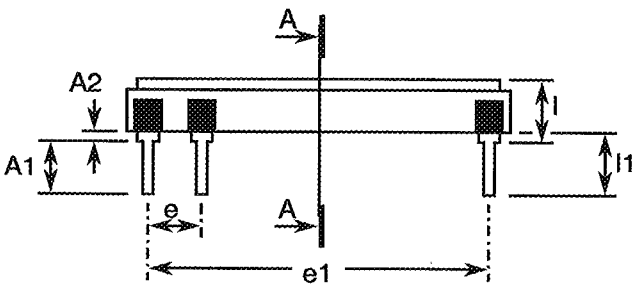
    This parameter is measured by sampling on 3 devices per wafer lot but not on deliverable items.
15. Standard capacitance bridge (1.0kHz).

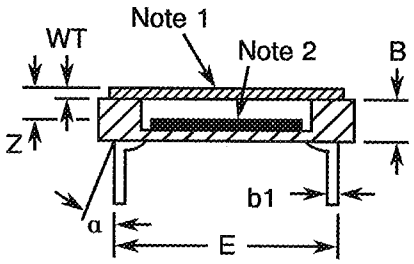
    This parameter is measured by sampling on 3 devices per wafer lot but not on deliverable items.
16. The CVF is measured by sampling on 5 devices per wafer lot, but not on deliverable devices.

N.B.
BG38 Optical Filter = Filter BP492/399 of DIN3140, thickness 2.0mm.

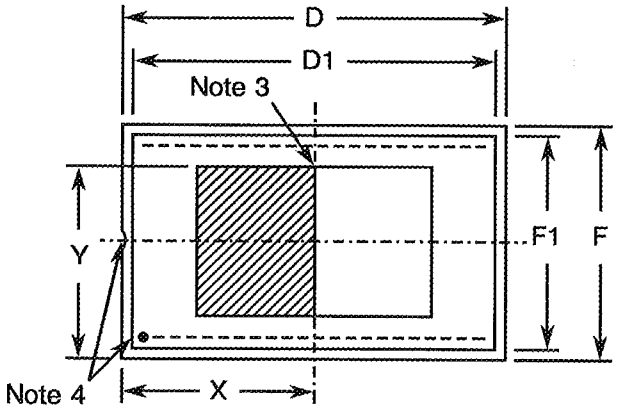
FIGURE 2 - PHYSICAL DIMENSIONS

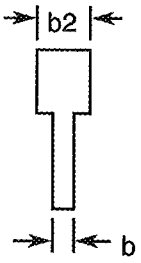
FIGURE 2(a) - PHYSICAL DIMENSIONS





AA CROSS SECTION





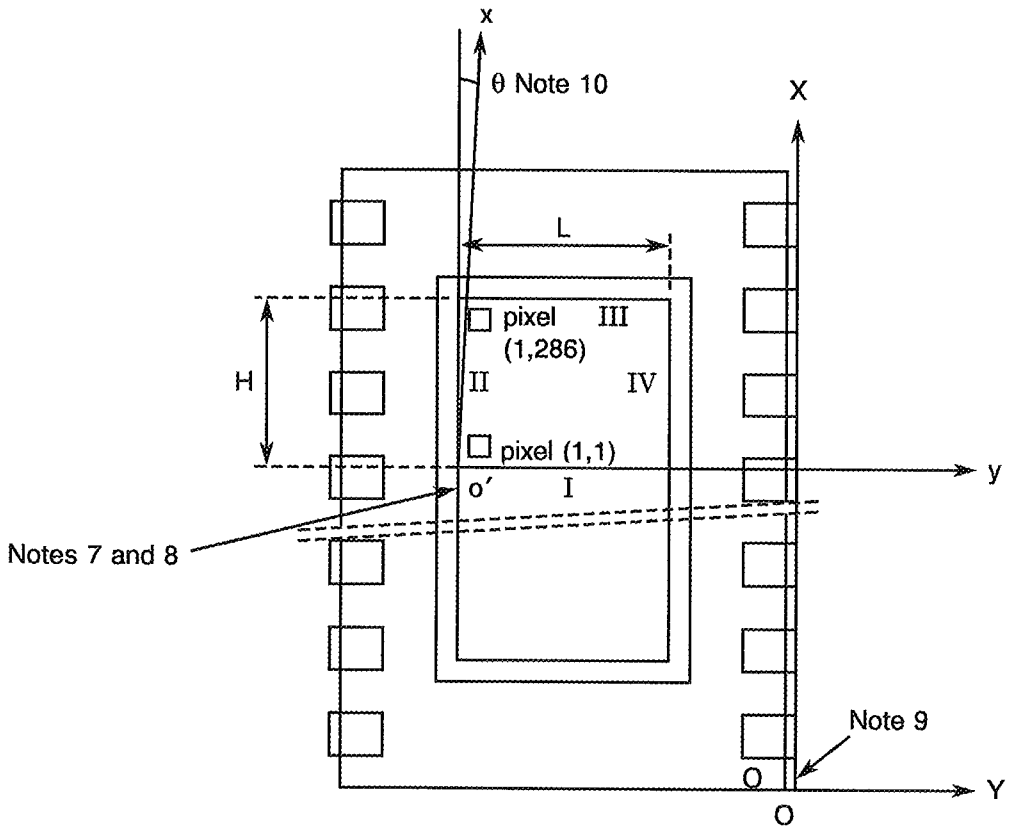
PIN DETAIL

SYMBOL	MILLIMETRES		REMARKS
	MIN	MAX	
A1	2.50	3.90	
A2	1.00	-	
b	0.38	0.51	
b1	0.20	0.30	
b2	-	1.77	
B	2.55 TYPICAL		Note 5
D	25.50	26.10	
D1	23.90	24.10	Note 5
e	2.54 TYPICAL		
e1	22.86 TYPICAL		
E	15.24	15.87	
F	17.40	18.00	
F1	15.90	16.10	Note 5
l	-	5.58	
l1	4.00	4.60	
WT	1.00	1.20	Note 5
Z	-	-	Note 6
α	-	15°	

NOTES: See Page 13.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - GEOMETRICAL CHARACTERISTICS



No.	CHARACTERISTIC	ESA/SCC 9020 TEST METHOD PARA. 9.12 OR NOTE	SYMBOL	LIMITS		UNIT	REMARKS
				MIN.	MAX.		
1	Flatness of Image Area		P	Table 1(a) Item 3		µm	Note 11
2 to 3	Position of the First Pixel		X Y	12800 13250	13000 13450	µm	Notes 11, 13, 14
4	Image Plane Orientation		θ	−0.5	+0.5	°	Notes 10, 12
5	Optical Distance between Image Plane and Window		Z	1.54	1.94	mm	Note 12
6	Parallelism between Image Plane and Window		TILT	−100	+100	µm	Note 12
7 to 8	Image Plane Dimensions		L W	8797 6589	8837 6629	µm	Notes 12, 13, 15

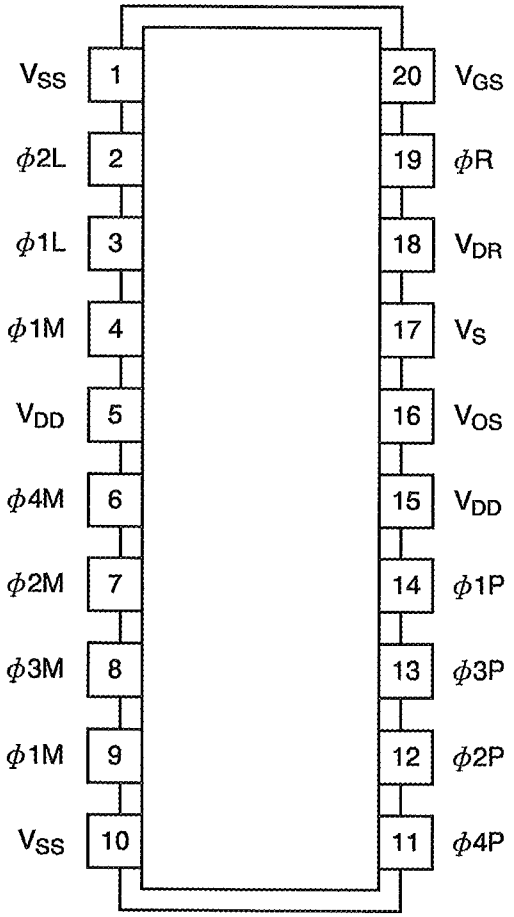
NOTES: See Page 13.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURES 2(a) AND 2(b)

1. Window.
2. Photosensitive area.
3. First pixel of first line (X, Y, Z coordinates).
4. Index (notch or dot).
5. Measured by sampling during Material Incoming Inspection.
6. Optical distance between external face of window and photosensitive area.
7. I, II, III and IV = Aluminium edges.
8. x, o', y = Die referential.
9. X, O, Y = Case referential.
10. θ = Site angle (skew).
11. Measured on a 100% basis.
12. Measured by sampling on 5 devices per assembly lot.
13. Measured with aluminium edges as references.
14. The first useful pixel (1,1) is located at a distance:
    X + (23µm) from aluminium edge I.
    Y − $\frac{2}{3}$(23µm) from aluminium edge II.
15. The pixels are square and the size of any pixel is equal to 23µm × 23µm.

FIGURE 3(a) - PIN ASSIGNMENT

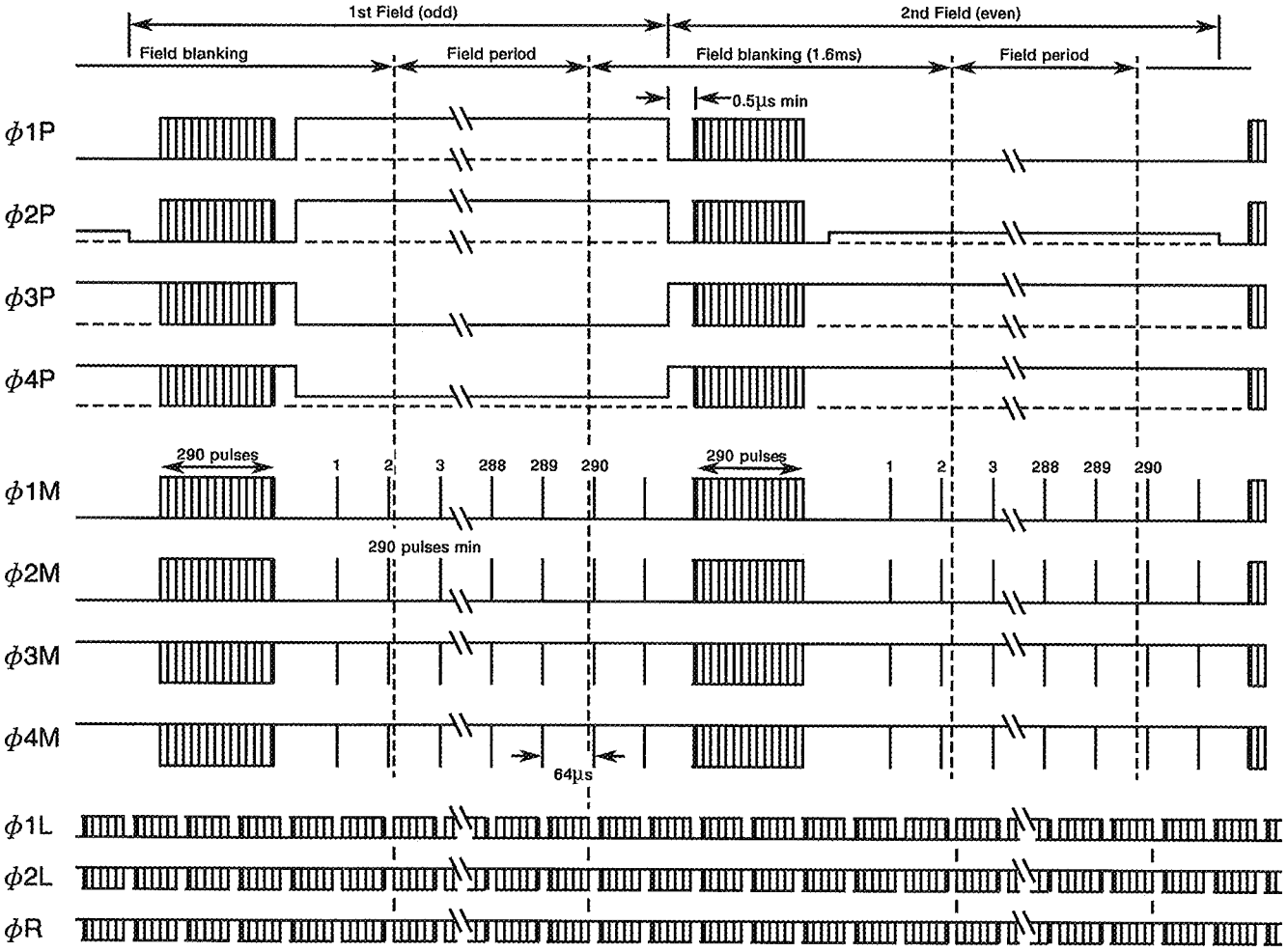


TOP VIEW

DESIGNATION	SYMBOL	PIN No.
Substrate Bias	V_{SS}	1-10
Readout Register Clocks	ϕ1L, ϕ2L	3-2
Memory-Zone Clocks	ϕ1M → ϕ4M	(4,9)-7-8-6
Output Amplifier Drain Supply	V_{DD}	5-15
Image-Zone Clocks	ϕ1P → ϕ4P	14-12-13-11
Video Output Signal	V_{OS}	16
Output Amplifier Source Bias	V_S	17
Reset Bias	V_{DR}	18
Reset Clock	ϕR	19
Register Output Gate Bias	V_{GS}	20

FIGURE 3(b) - TIMING DIAGRAM TD1

FRAME TIMING DIAGRAM



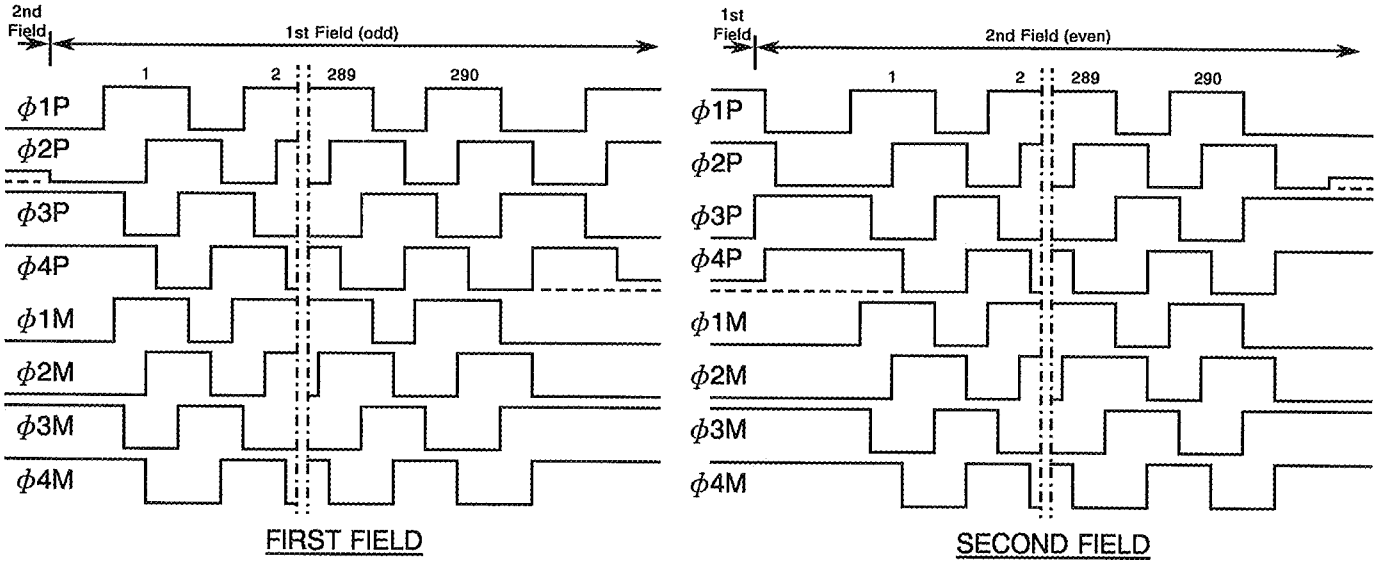
NOTES

1. Repartition of lines:

First	:	shielded.
2nd	:	partially shielded.
3 to 288	:	useful lines.
289	:	partially shielded.
290	:	shielded.

FIGURE 3(b) - TIMING DIAGRAM TD1 (CONTINUED)

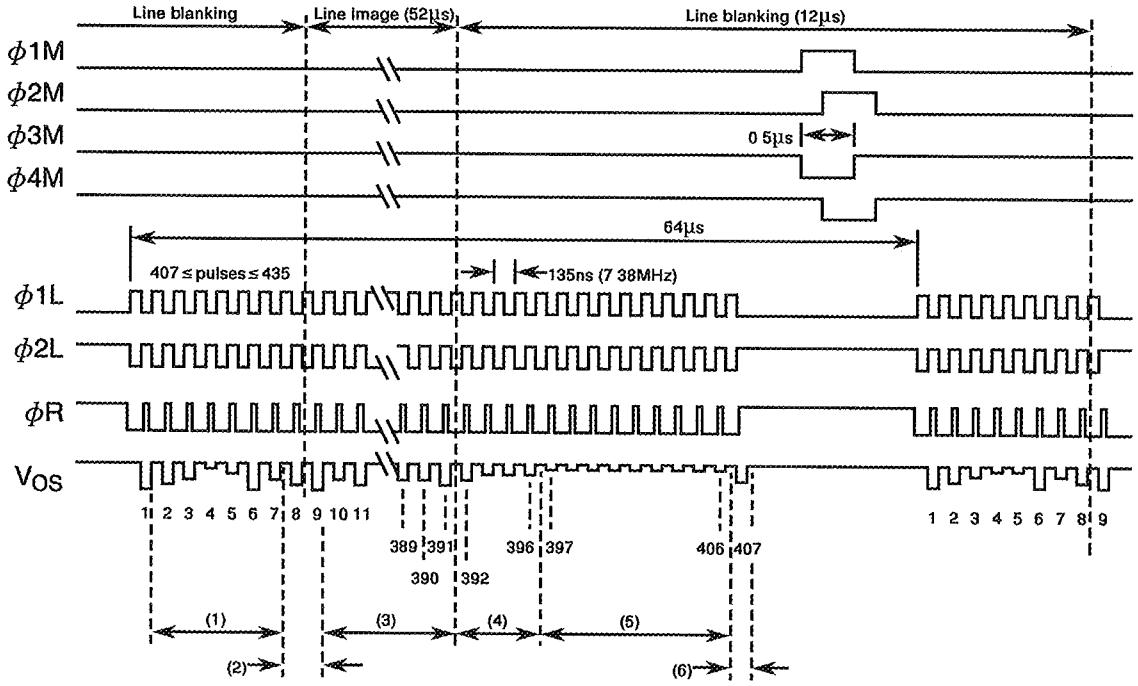
VERTICAL TRANSFERS DURING FIELD BLANKING



FIRST FIELD

SECOND FIELD

LINE TIMING DIAGRAM



NOTES

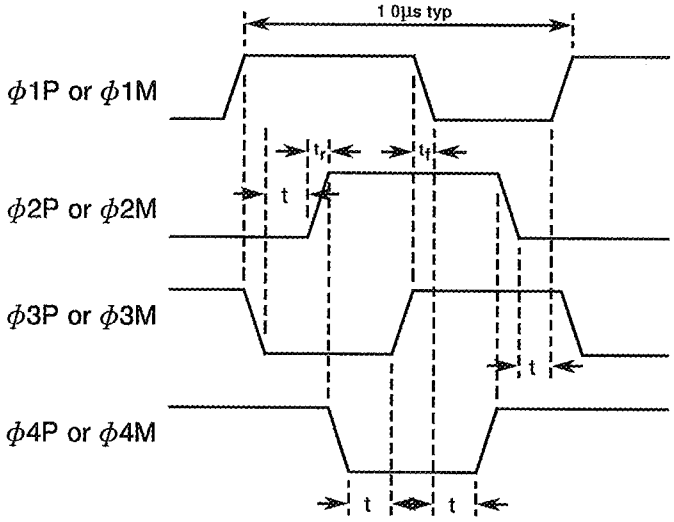
The video line comprises:

1. 7 inactive "pre-scan" elements = zero reference level.
2. 2 isolation elements (the second one is partially shielded).
3. 382 useful video pixels.
4. 5 isolation elements (the first one is partially shielded).
5. 10 dark reference elements (elements 397 to 406).
6. 1 isolation element.

FIGURE 3(b) - TIMING DIAGRAM TD1 (CONTINUED)

OUTPUT TIMING DIAGRAM FOR ϕ_P AND ϕ_M CLOCKS DURING TRANSFER

STANDARD CONFIGURATION

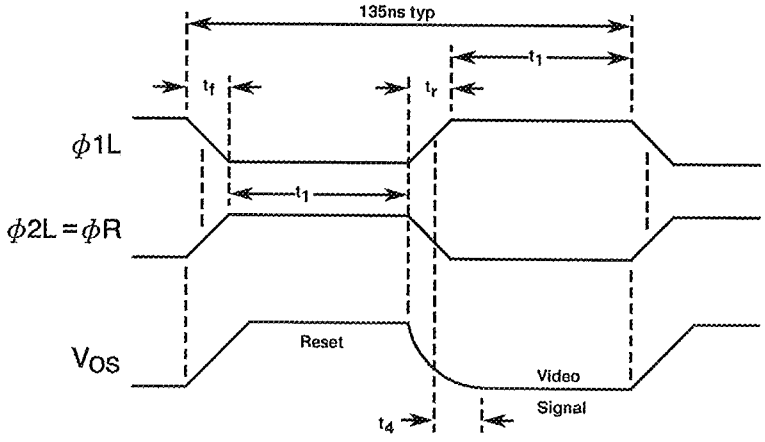


NOTES

1. $30ns \leq t_r \leq 80ns$; $30ns \leq t_f \leq 80ns$; $t \geq 50ns$.

2. Crossover of complementary clocks ($\phi 1$ and $\phi 3$, $\phi 2$ and $\phi 4$) in the high state (above 90% of max. amplitude).

OUTPUT TIMING DIAGRAM FOR READOUT REGISTER AND RESET CLOCKS



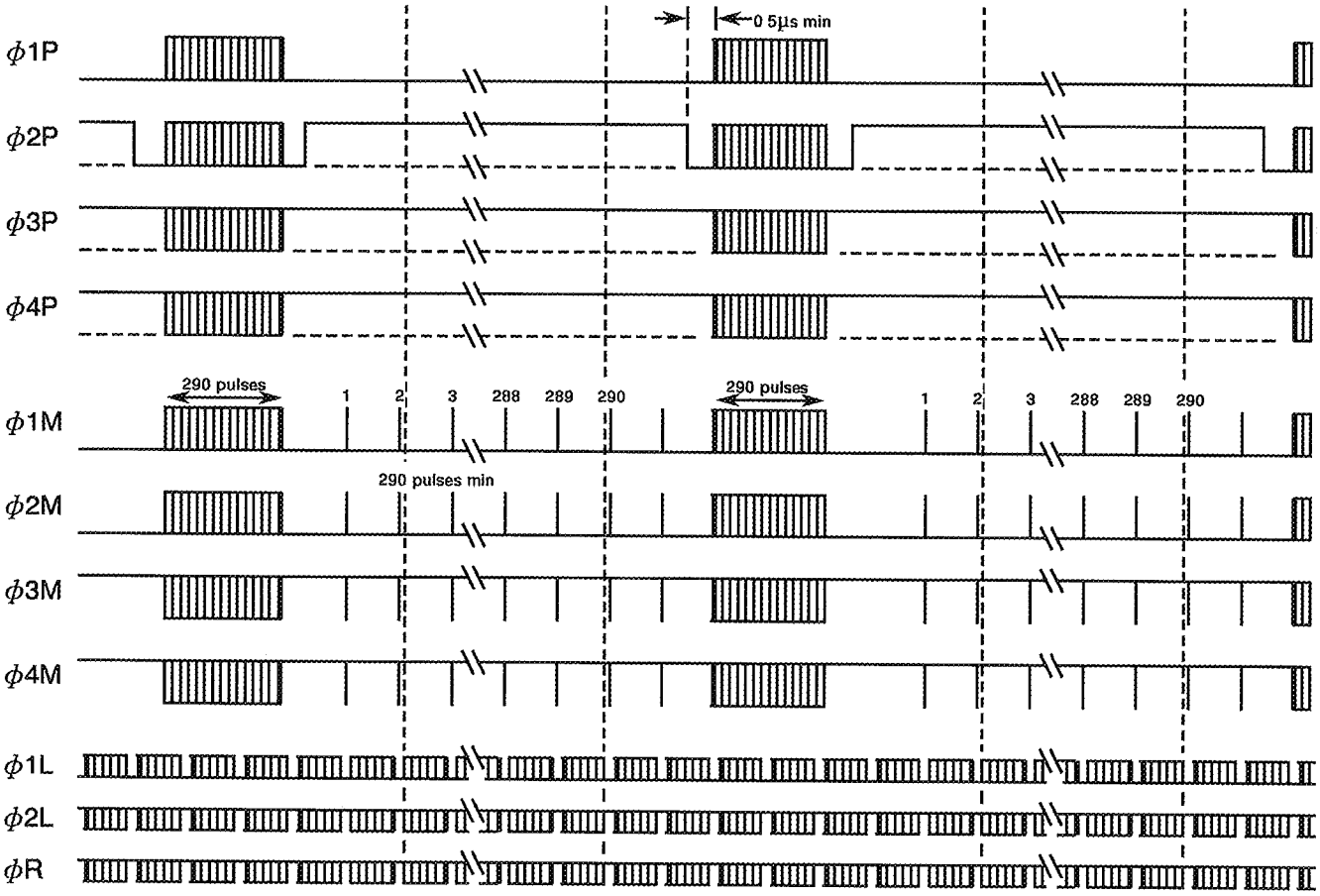
NOTES

1. $10ns \leq t_r \leq 20ns$; $10ns \leq t_f \leq 20ns$; $t_1 \geq 40ns$; typical $t_4 = 20ns$.

2. Crossover of complementary clocks ($\phi 1L$ and $\phi 2L$) preferably 50% of their amplitude.

FIGURE 3(b) - TIMING DIAGRAM TD2

FRAME TIMING DIAGRAM



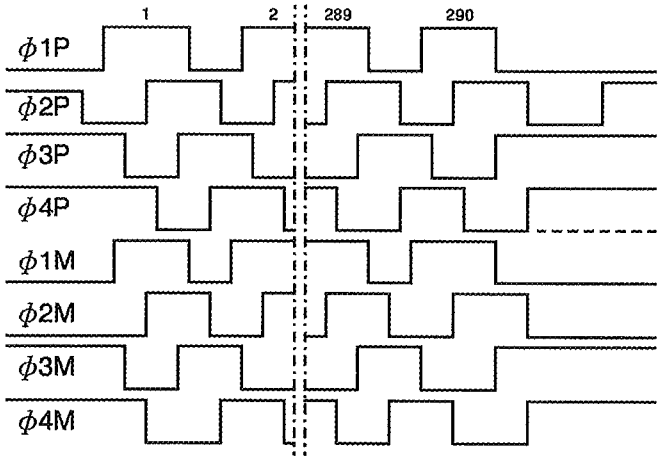
NOTES

1. Repartition of lines:

First	:	shielded.
2nd	:	partially shielded.
3 to 288	:	useful lines.
289	:	partially shielded.
290	:	shielded.

FIGURE 3(b) - TIMING DIAGRAM TD2 (CONTINUED)

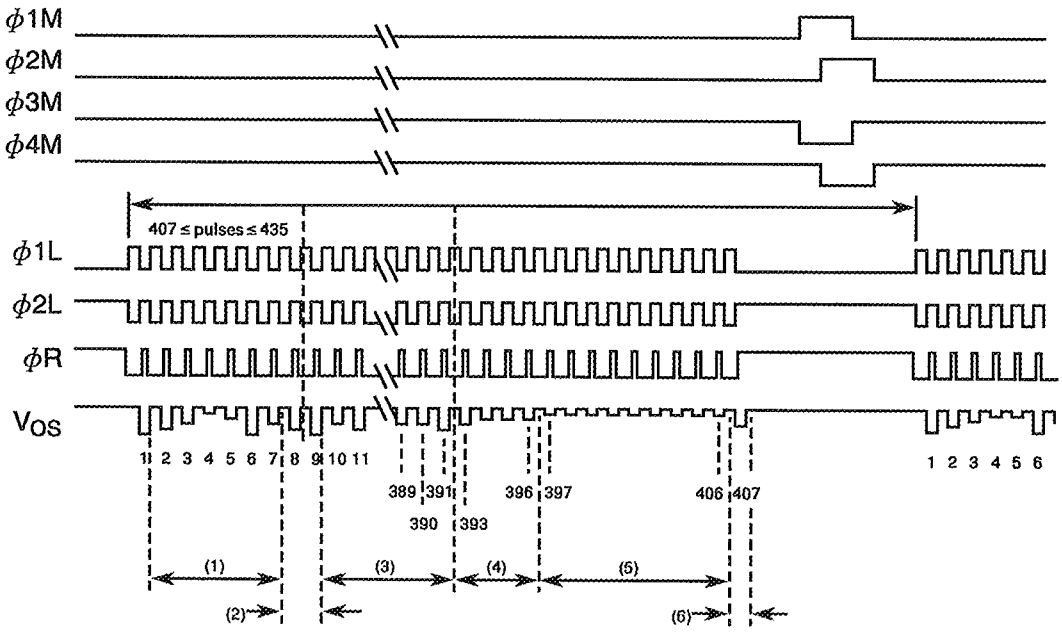
VERTICAL TRANSFERS TIMING DIAGRAM



NOTES

1. Fl = 1.0MHz; FL = 4.0MHz; Typical Ti = 31ms.

LINE TIMING DIAGRAM



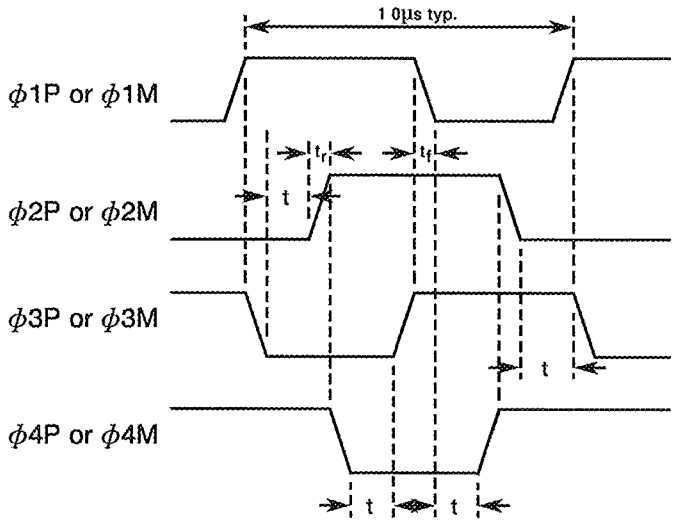
NOTES

The video line comprises:

1. 7 inactive "pre-scan" elements = zero reference level.
2. 2 isolation elements (the second one is partially shielded).
3. 382 useful video pixels.
4. 5 isolation elements (the first one is partially shielded).
5. 10 dark reference elements (elements 397 to 406).
6. 1 isolation element.

FIGURE 3(b) - TIMING DIAGRAM TD2 (CONTINUED)

OUTPUT TIMING DIAGRAM FOR ϕ_P AND ϕ_M CLOCKS DURING TRANSFER

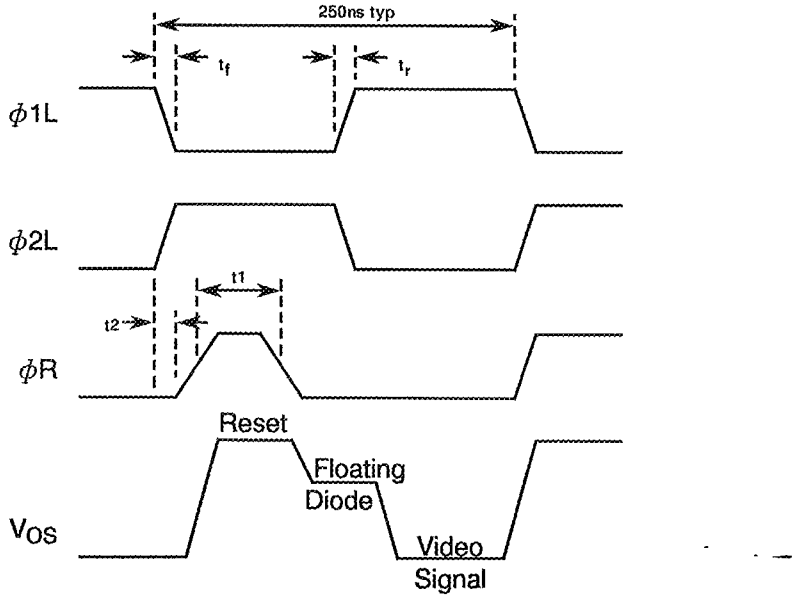


NOTES

1. $30ns \leq t_r \leq 80ns$; $30ns \leq t_f \leq 80ns$; $t \geq 50ns$.

2. Crossover of complementary clocks ($\phi 1$ and $\phi 3$, $\phi 2$ and $\phi 4$) in the high state (above 90% of max. amplitude).

OUTPUT TIMING DIAGRAM FOR READOUT REGISTER AND RESET CLOCKS



NOTES

1. $10ns \leq t_r \leq 30ns$; $10ns \leq t_f \leq 30ns$; $t_1 \geq 30ns$; $t_2 \geq 0ns$.

FIGURE 3(c) - FUNCTIONAL DIAGRAM

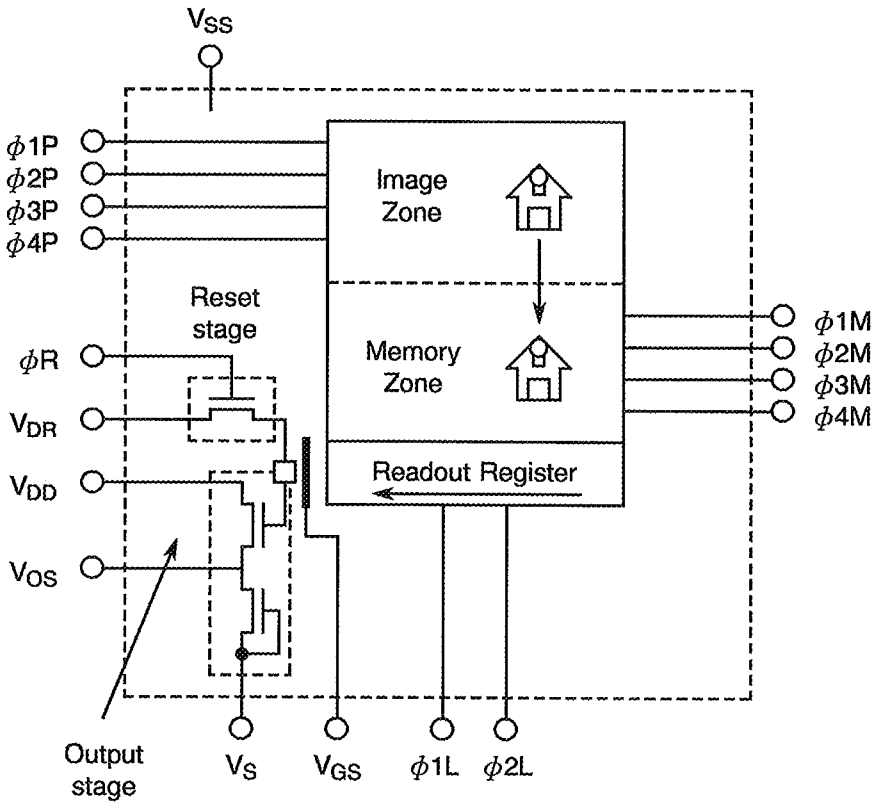
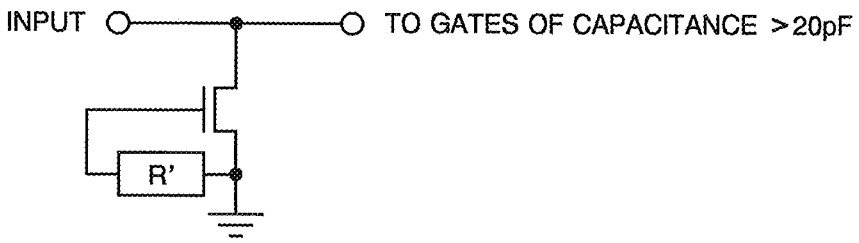
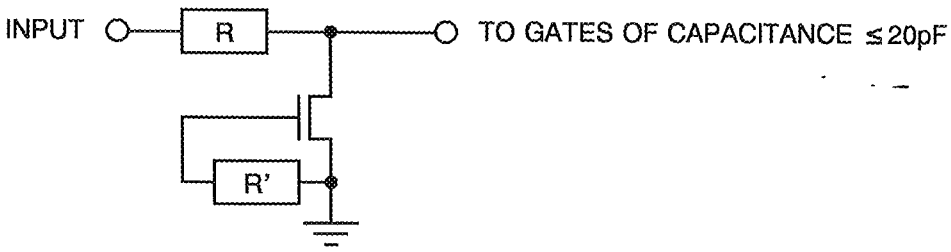


FIGURE 3(d) - INPUT PROTECTION NETWORKS

PINS 2-3-6-7-8-9-11-12-13-14-18



PINS 4-19-20



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9020 for Charge Coupled Devices, Silicon Photosensitive.

(b) DIN3140, "MAβ-und Toleranzangaben für Optikeinzelteile; oberflächenbeschichtungen" (Inscription of dimensions and tolerances for optical components; indication for coatings).

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the components specified herein are stated in this specification and ESA/SCC Generic Specification No. 9020 for Charge Coupled Devices. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

(a) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during qualification and maintenance of qualification.

(b) Para. 5.2.2, Total Dose Irradiation Testing: If specified in a Purchase Order, shall be performed during procurement on a lot acceptance basis at the total dose irradiation level specified in the Purchase Order.

(c) CϕPo, CϕMo, CϕLo, CϕP, CϕM, CϕL and CϕR are measured by sampling 3 devices per wafer lot, but not on deliverable devices.

(d) CVF is measured by sampling 5 devices per wafer lot, but not on deliverable devices.

4.2.2 Deviations from Final Production Tests (Chart II)

(a) Para. 9.8, the pressure during seal test shall not exceed 3kg/cm^2.

(b) Para. 9.8.1, Leak Rate: 5×10^{-7} atm/cm^3/sec.

4.2.3 Deviations from Burn-in Tests (Chart III)

(a) Para. 7.1.1(a), "High Temperature Reverse Bias (H.T.R.B.)" test and subsequent electrical measurements related to this test shall not be performed.

(b) Para. 9.8, the pressure during seal test shall not exceed 3kg/cm^2.

(c) Para. 9.8.1, Leak Rate: 5×10^{-7} atm/cm^3/sec.

4.2.4 Deviations from Qualification Tests (Chart IV)

(a) Para. 9.8, the pressure during seal test shall not exceed 3kg/cm^2.

(b) Para. 9.8.1, Leak Rate: 5×10^{-7} atm/cm^3/sec.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

(a) Para. 9.8, the pressure during seal test shall not exceed 3kg/cm^2.

(b) Para. 9.8.1, Leak Rate: 5×10^{-7} atm/cm^3/sec.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the components specified herein shall be checked. They shall conform to those shown in Figure 2(a).

4.3.2 Geometrical Characteristics

The geometrical characteristics of the components specified herein shall be checked. They shall conform to those shown in Figure 2(b).

4.3.3 Weight

The maximum weight of the components specified herein shall be 5.0 grammes.

4.3.4 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESA/SCC Generic Specification No. 9020. The test conditions shall be as follows:

Applied Force: 1.0 ± 0.1 Newtons, 3 bends at $45(+5-0)°$.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the components specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

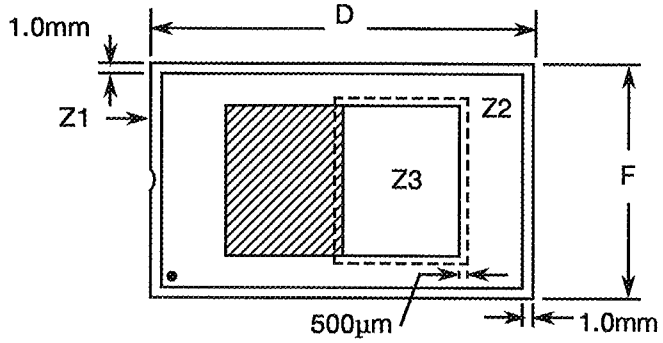
The case shall be hermetically sealed and have a ceramic body and glass window. The flatness of the underside of package shall be better than 0.01mm/cm, measured between edges, across the complete surface.

4.4.2 Lead Material and Finish

For lead material shall be Type 'D' with Type '7' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500.

4.4.3 Window

Window material shall be ZKN7 glass. The optical quality of the window including coating, if required for both sides, shall be better than as defined in DIN3140.



- Surface Defects:

Z1 (Peripheral Zone)	:	No specification.
Z2 (Zone between Z1 and Z3)	:	0 defect larger than 10 000µm².
Z3 (Image Zone + Surround)	:	0 defect longer than 25µm.
	:	0 scratch wider than 10µm.

- Inclusions:

Z3 (Image Zone + Surround)	:	0 inclusion larger than 25µm.

- Chips and Cracks : No chips or cracks crossing Z1 and coming into Z2.

- Window form error before mounting : Surface flatness shall be better than 6 fringes measured by interferometry at a wavelength $\lambda \approx 633$nm.

- Parallelism : ±10µm max.

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700, and the following paragraphs. When the component is too small to accommodate all of the marking specified, as much as space permits shall be marked and the marking information, in full, shall accompany the component in its primary package.

The information to be marked and the order of precedence, shall be as follows:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

4.5.2 Lead Identification

An index shall be located at the top of the package in the position defined in Note 1 to Figure 2(a). The pin numbering must be read with the index on the left-hand side.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:

961000301BE

Detail Specification Number
Type Variant (see Table 1(a))
Testing Level (B or C, as applicable)
Total Dose Irradiation Level (if applicable)

The Total Dose Irradiation Level designation shall be added for those devices for which a sample has been successfully tested to the level in question. For these devices, a code letter shall be added in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS

4.6.1 Electrical and Electro-optical Measurements at Reference Temperature

The parameters to be measured in respect of electrical and electro-optical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at T_{ref} ±3 °C.

4.6.2 Electrical and Electro-optical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. Unless otherwise specified, the measurements shall be performed at −20(+5−0) and +85(+0−5) °C respectively.

4.6.3 Circuits for Electrical and Electro-optical Measurements

Circuits for use in performing electrical and electro-optical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to H.T.R.B. and Power Burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at T_{ref} ±3 °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-in

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9020. The conditions for power burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for High Temperature Reverse Bias Burn-in

Not applicable.

4.7.5 Electrical Circuits for Power Burn-in

Circuits for use in performing the power burn-in test are shown in Figure 5(b) of this specification.

TABLE 2 - ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT REFERENCE TEMPERATURE

No.	CHARACTERISTICS	SYMBOL	TEST METHOD ESA/SCC 25000	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
1	Leakage Current on Input Gates	I_L	Para. 5.1	4(b)	V_{IH} = 15V Note 1	-	300	pA
2 to 15	Input Clamp Voltage (to V_{SS})	V_{IC}	-	4(c)	I_{IN} (Under Test) = −500μA at $V_{IN} \leq -3.5V$ V_{IN} (Remaining Pins) = 0V (Pins 2-3-4-6-7-8-9-11-12-13-14-18-19-20)	−1.5	-	V
16 to 29	Insulation Leakage Current between Pins (Input Current)	I_E	Para. 5.2	4(d)	V_{IH} = 15V Note 1 (Pins 2-3-4-6-7-8-9-11-12-13-14-18-19-20) (Pin 18) Note 2	-	10	nA
30	Power Supply Current 1	I_{DD1}	Para. 5.3	4(e)	STATIC $V_{DR} = \phi R$ (High Level) = Table 1(a) V_{IN} (Remaining Pins) = 0V V_{OS} = Open V_{DD} = Table 1(a) V_{SS} = 0V (Pins 5 and 15)	Table 1(a) Item 6		mA
31	Power Supply Current 2	I_{DD2}	Para. 5.3	4(g)	DYNAMIC V_{IN} (Remaining Pins) = Figure 4(a) V_{DD} = 15.5V, V_{SS} = −2.0V (Pins 5 and 15)	Table 1(a) Item 7		mA
32	DC Output Level	V_{ref}	Para. 5.4	4(e)	STATIC V_{DR} = 13.3V or Table 1(a) ϕR (High Level) = 10V or Table 1(a) V_{IN} (Remaining Pins) = 0V V_{OS} = Open V_{DD} = 15.5V or Table 1(a) V_{SS} = 0V or Table 1(a) (Pin 16)	Table 1(a) Item 9		V
33	Output Impedance	Z_S	Para. 6.1	4(f)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 10		Ω

NOTES: See Page 32.

TABLE 2 - ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT REFERENCE TEMPERATURE (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD ESA/SCC 25000	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
34	Saturation Voltage for the Image Area	V_{SAT}	Para. 6.7 Method (a)	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 11		mV
35	Vertical Charge Transfer Inefficiency	VCTI	Para. 6.12	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 12		%
36	Horizontal Charge Transfer Inefficiency	HCTI	Para. 6.12	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 13		%
37	Average Dark Signal (Image Area)	VDS1	Para. 6.20	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 14		mV
38	Average Dark Signal (Image Area + Storage Area)	VDS2	Para. 6.20	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 15		mV
39	Dark Signal Non-uniformity, standard deviation σ	DSNU(σ)	Para. 6.21	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 17		mV
40	Number of Dark Signal Defects beyond a3 Limit	Ndef3	Para. 6.21	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 18		-
41	Number of Dark Signal Defects beyond a4 Limit	Ndef4	Para. 6.21	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 19		-

NOTES: See Page 32.

TABLE 2 - ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT REFERENCE TEMPERATURE (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD ESA/SCC 25000	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
42	DSNU Limit for Ndef3	a3	Para. 6.21	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 20		mV
43	DSNU Limit for Ndef4	a4	Para. 6.21	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 21		mV
44	Responsivity	R	Para. 6.17	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 22		V/μJ/cm²
45	Photoresponse Non-uniformity, standard deviation σ	PRNU(σ)	Para. 6.14	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 24		%
46	Number of PRNU Defects beyond a1 Limit	Ndef1	Para. 6.14	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 25		-
47	Number of PRNU Defects beyond a2 Limit	Ndef2	Para. 6.14	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 26		-
48	PRNU Limit for Ndef1	a1	Para. 6.14	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 27		%
49	PRNU Limit for Ndef2	a2	Para. 6.14	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 28		%

NOTES: See Page 32.

TABLE 2 - ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT REFERENCE TEMPERATURE (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD ESA/SCC 25000	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
50	Spectral Responsivity in Optical Band B1	R(B1)	Para. 6.15	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 29		V/μJ/cm²
51	Spectral Responsivity in Optical Band B2	R(B2)	Para. 6.15	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 30		V/μJ/cm²
52	Spectral Responsivity in Optical Band B3	R(B3)	Para. 6.15	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 31		V/μJ/cm²
53	Spectral Responsivity in Optical Band B4	R(B4)	Para. 6.15	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 32		V/μJ/cm²
54	Spectral Responsivity in Optical Band B5	R(B5)	Para. 6.15	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 33		V/μJ/cm²
55	Spectral Responsivity in Optical Band B6	R(B6)	Para. 6.15	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 34		V/μJ/cm²
56	Spectral Responsivity in Optical Band B7	R(B7)	Para. 6.15	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 35		V/μJ/cm²
57	Linearity Error	LE	Para. 6.6	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 36		%

NOTES: See Page 32.

TABLE 2 - ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT REFERENCE TEMPERATURE (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD ESA/SCC 25000	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
58	Temporal Noise	V_N	Para. 6.4	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 37		µV
59	Offset Voltage	V_{Offset}	Para. 6.5	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 38		mV
60	Amplitude of Reset Feedthrough	V_{Reset}	Para. 5.5	4(h)	V_{IN} (Remaining Pins) = Figure 4(a) V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 39		mV
61	Reference Level Settling Time	$t_{D\text{-}Ref}$	Para. 6.3	4(h)	V_{IN} (Remaining Pins) = Figure 4(a) V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 40		ns
62	Reference Level Duration	$t_{U\text{-}Ref}$	Para. 6.3	4(h)	V_{IN} (Remaining Pins) = Figure 4(a) V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 41		ns
63	Reference Level Error Band	ΔU_{Ref}	Para. 6.3	4(h)	V_{IN} (Remaining Pins) = Figure 4(a) V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 42		mV
64	Signal Level Settling Time	$t_{D\text{-}Signal}$	Para. 6.3	4(h)	V_{IN} (Remaining Pins) = Figure 4(a) V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 43		ns
65	Signal Level Duration	$t_{U\text{-}Signal}$	Para. 6.3	4(h)	V_{IN} (Remaining Pins) = Figure 4(a) V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 44		ns

NOTES: See Page 32.

TABLE 2 - ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT REFERENCE TEMPERATURE (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD ESA/SCC 25000	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
66	Signal Level Error Band	ΔU_{Signal}	Para. 6.3	4(h)	V_{IN} (Remaining Pins) = Figure 4(a) V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 45		mV
67 to 70	Electrode Capacitance	CϕP	Para. 6.2	4(i)	V_{DR} = 13.3V or Table 1(a) V_{IN} (Not Under Test) = 15V or Table 1(a) Load Voltage = 10V plus 50mV, 1.0MHz or Table 1(a) (Pins 11-12-13-14)	Table 1(a) Item 46		pF
71 to 74	Electrode Capacitance	CϕM	Para. 6.2	4(i)	V_{DR} = 13.3V or Table 1(a) V_{IN} (Not Under Test) = 15V or Table 1(a) Load Voltage = 10V plus 50mV, 1.0MHz or Table 1(a) (Pins 6-7-8-9)	Table 1(a) Item 47		pF
75 to 76	Electrode Capacitance	CϕL	Para. 6.2	4(i)	V_{DR} = 13.3V or Table 1(a) V_{IN} (Not Under Test) = 15V or Table 1(a) Load Voltage = 10V plus 50mV, 1.0MHz or Table 1(a) (Pins 2-3)	Table 1(a) Item 48		pF
77	Electrode Capacitance	CϕR	Para. 6.2	4(i)	V_{DR} = 13.3V or Table 1(a) V_{IN} (Not Under Test) = 15V or Table 1(a) Load Voltage = 10V plus 50mV, 1.0MHz or Table 1(a) (Pin 19)	Table 1(a) Item 49		pF
78 to 81	Electrode Capacitance	CϕPo	Para. 6.3	4(j)	V_{DR} = 13.3V or Table 1(a) V_{IN} (Not Under Test) = Open Load Voltage = 10V plus 50mV, 1.0MHz or Table 1(a) (Pins 11-12-13-14)	Table 1(a) Item 50		pF

NOTES: See Page 32.

TABLE 2 - ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT REFERENCE TEMPERATURE (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD ESA/SCC 25000	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
82 to 85	Electrode Capacitance	$C\phi Mo$	Para. 6.3	4(j)	V_{DR} = 13.3V or Table 1(a) V_{IN} (Not Under Test) = Open Load Voltage = 10V plus 50mV, 1.0MHz or Table 1(a) (Pins 6-7-8-9)	Table 1(a) Item 51		pF
86 to 88	Electrode Capacitance	$C\phi Lo$	Para. 6.3	4(j)	V_{DR} = 13.3V or Table 1(a) V_{IN} (Not Under Test) = Open Load Voltage = 10V plus 50mV, 1.0MHz or Table 1(a) (Pins 2-3)	Table 1(a) Item 52		pF
89	Charge to Voltage Conversion Factor	CVF	Para. 6.18	4(g)	V_{IN} (Remaining Pins) = Figure 4(a) V_{OS} = Open V_{DD} = 15.5V, V_{SS} = −2.0V (Pin 16)	Table 1(a) Item 53		μV/e

NOTES

1. T_{amb} = +25 ± 3 °C.
2. See Note 1 of Figure 4(d).

TABLE 3 - ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES

No.	CHARACTERISTICS	SYMBOL	TEST METHOD ESA/SCC 25000	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
1	Leakage Current on Input Gates over T_{op}	I_L	Para. 5.1	4(b)	V_{IH} = 15V Note 1	-	1.0	µA
16 to 29	Insulation Leakage Current between Pins (Input Current)	I_E	Para. 5.2	4(d)	V_{IH} = 15V (Pins 2-3-4-6-7-8-9-11-12-13-14-19-20) (Pin 18) Note 2	-	1.0	µA
30	Power Supply Current 1 over T_{op}	I_{DD1} (T_{op})	Para. 5.3	4(e)	STATIC V_{DR} = ϕR (High Level) = Table 1(a) V_{IN} (Remaining Pins) = 0V V_{OS} = Open V_{DD} = Table 1(a) V_{SS} = 0V (Pins 5 and 15)	Table 1(a) Item 8		mA
38	Average Dark Signal (Image Area + Storage Area) over T_{op}	VDS2 (T_{op})	Para. 6.20	4(g)	Timing Diagram TD1	Table 1(a) Item 16		mV
44	Responsivity over T_{op}	R (T_{op})	Para. 6.17	4(g)	Timing Diagram TD1 Uniform illumination BG38 optical filter	Table 1(a) Item 23		V/µJ/cm²

NOTES

1. Measurements performed on 100% basis go-no-go.
2. See Note 1 of Figure 4(d).

FIGURE 4 - CIRCUITS FOR ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS

FIGURE 4(a) - BIASING VOLTAGE LEVELS

PARAMETER	SYMBOL	CONDITIONS	UNIT
Output Amplifier Drain Supply	V_{DD}	15.5 (+0.5 −0.5)	V
Reset Bias	V_{DR}	13.3 (+0.2 −0.3)	V
Register Output Gate Bias	V_{GS}	2.5 (+0.5 −0.5)	V
Output Amplifier Gate Bias	V_S	0 (+0 −2.0)	V
Substrate Bias	V_{SS}	−2.0 (+2.0 −0)	V
Image Zone Clocks during Integration Period	ϕ1P low ϕ2P, ϕ3P, ϕ4P high	0.3 (+0.2 −0.3) 10 (+1.0 −1.0)	V
Image Zone Clocks during Transfer Period	ϕP low ϕP high	0.3 (+0.2 −0.3) 10 (+1.0 −1.0)	V
Memory Zone Clocks, Output Register Clocks and Reset Clock	ϕM, ϕL, ϕR low ϕM, ϕL, ϕR high	0.3 (+0.2 −0.3) 10 (+1.0 −1.0)	V

FIGURE 4(b) - LEAKAGE CURRENT ON INPUT GATES

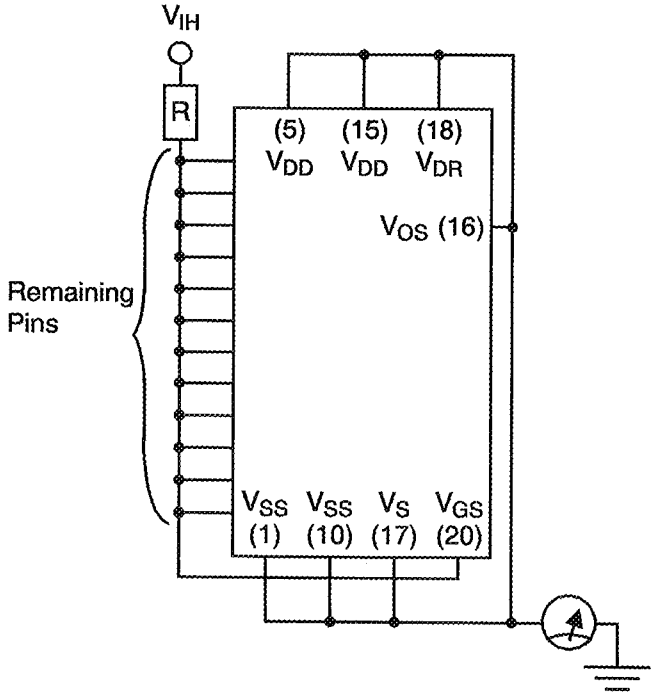
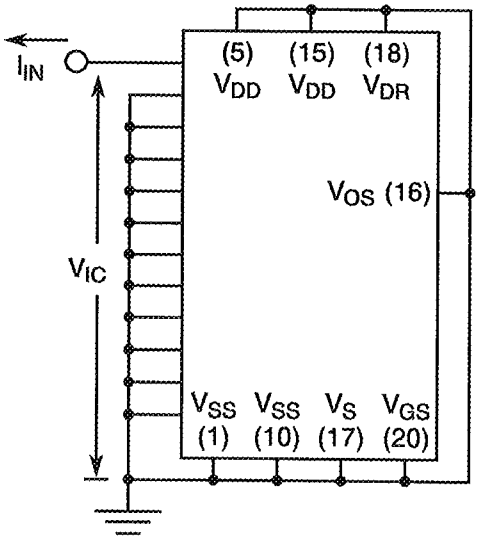


FIGURE 4(c) - INPUT CLAMP VOLTAGE

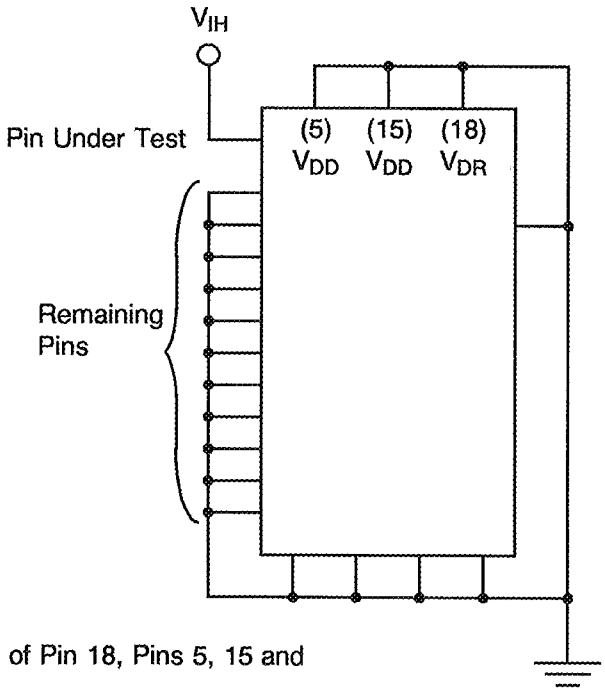


NOTES

1. R = 1.0MΩ.

FIGURE 4 - CIRCUITS FOR ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS (CONTINUED)

FIGURE 4(d) - INSULATION LEAKAGE CURRENT BETWEEN PINS



NOTES

1. For the measurement of Pin 18, Pins 5, 15 and 16 must be open.

FIGURE 4(e) - POWER SUPPLY CURRENT AND D.C. OUTPUT LEVEL

STATIC

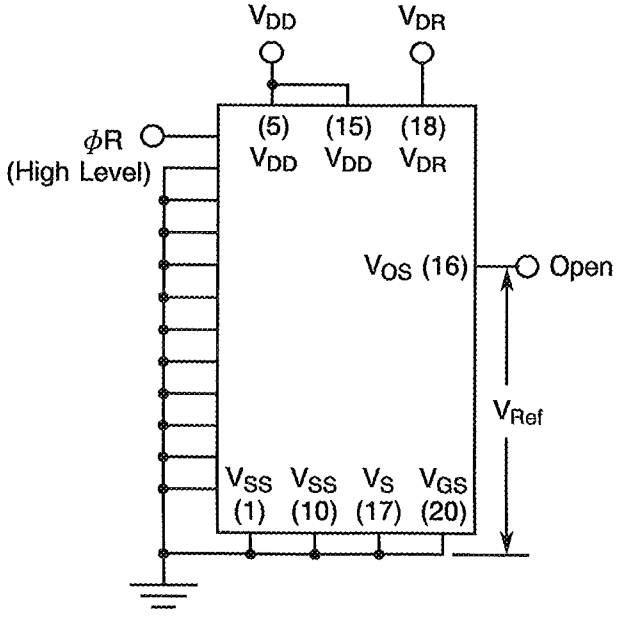
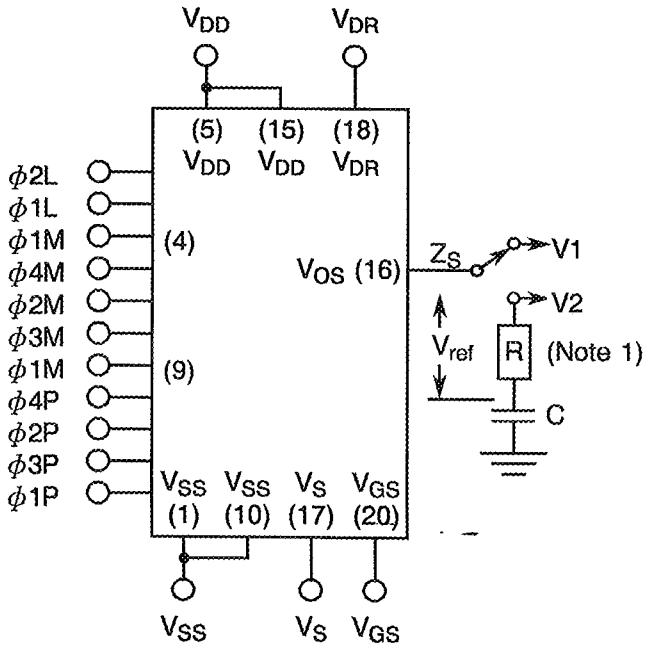


FIGURE 4(f) - OUTPUT IMPEDANCE

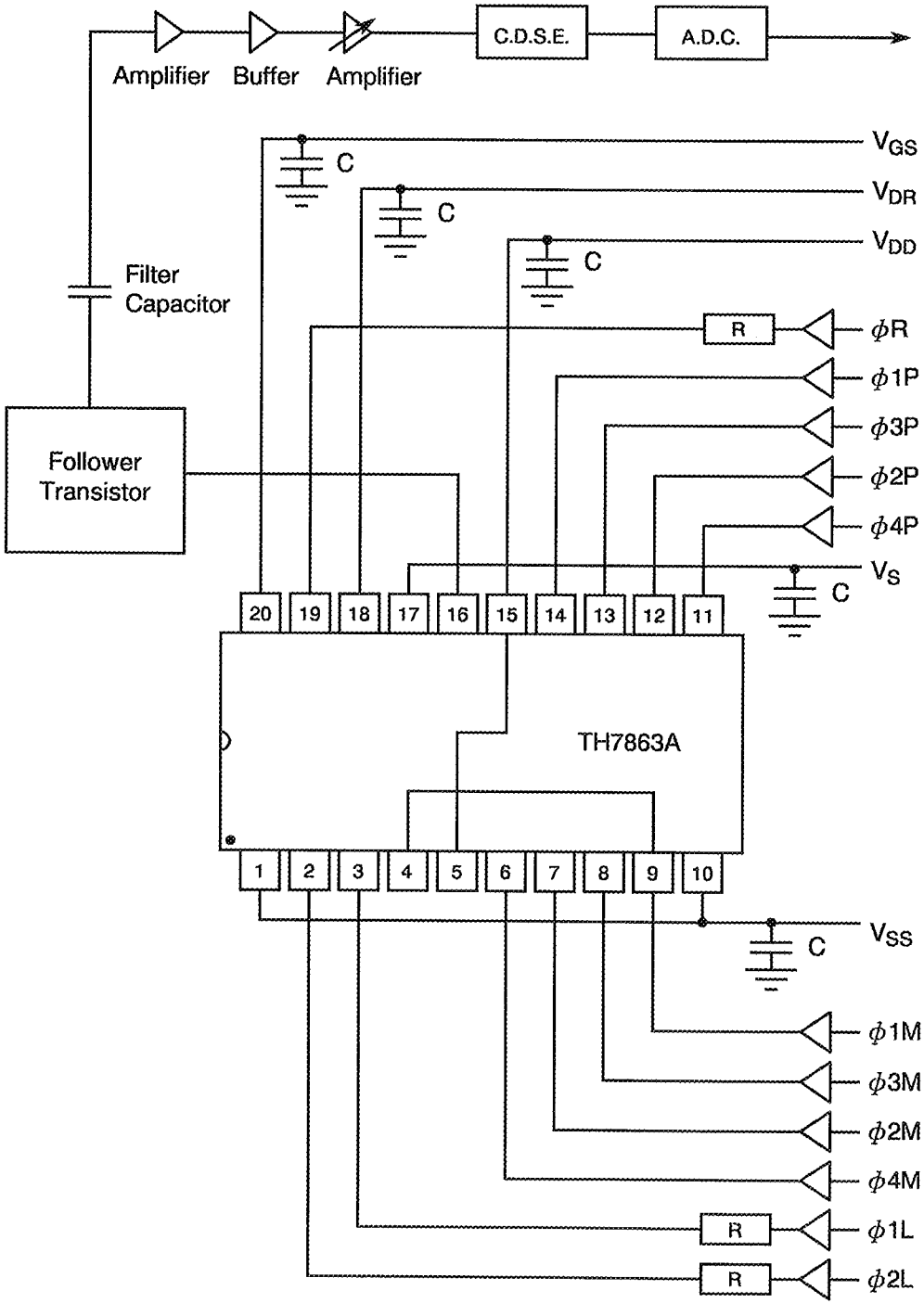


NOTES

1. See individual Tables 1(a).

FIGURE 4 - CIRCUITS FOR ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS (CONTINUED)

FIGURE 4(g) - DRIVING CIRCUIT

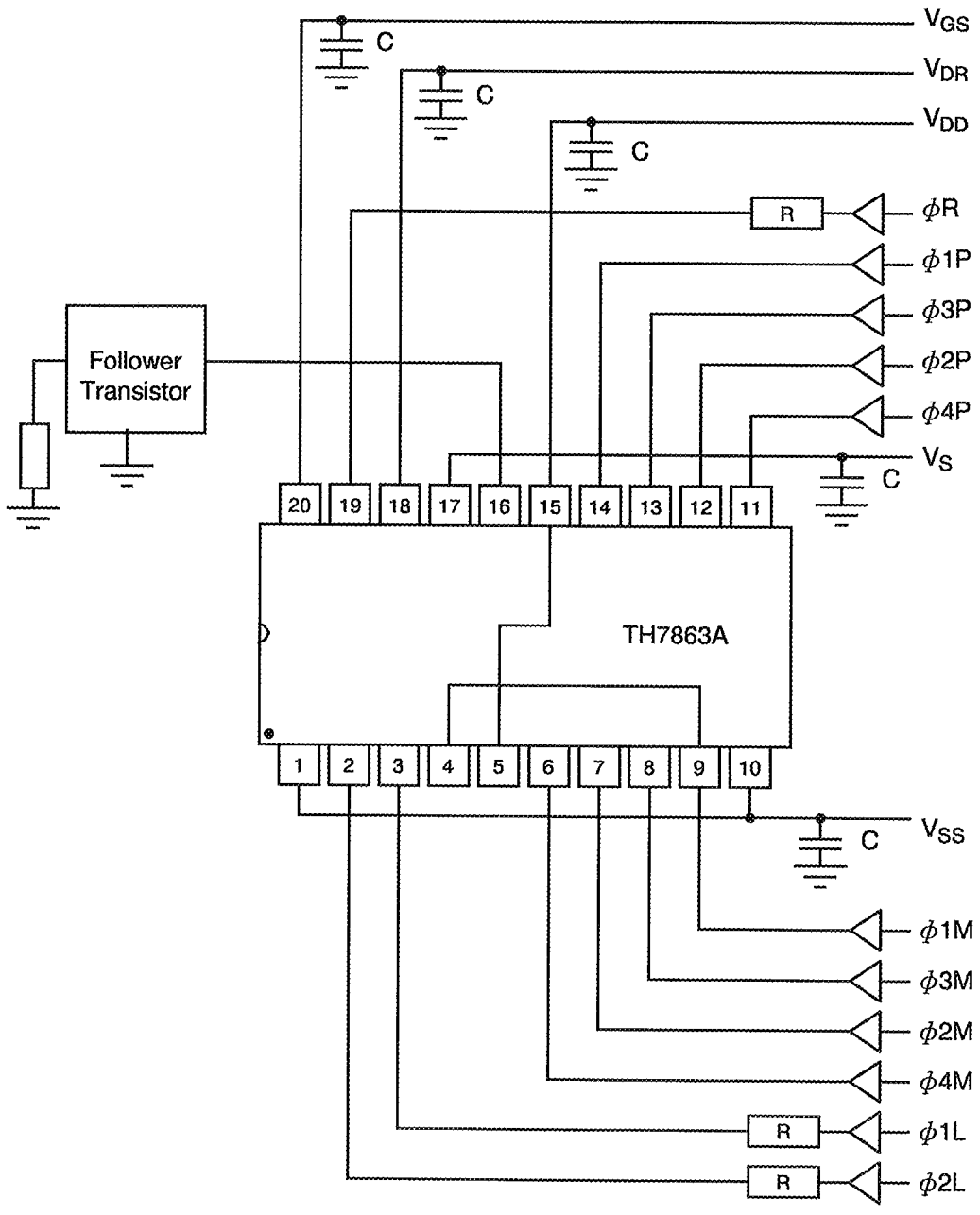


NOTES

1. R = Serial resistors to be adjusted to obtain a rise time compatible with the appropriate timing diagram.
2. C = Decoupling capacitors to be adjusted to adequately decouple.
3. For TD1: FI = 1.0MHz, FL = 7.4MHz.
4. For TD2: FI = 1.0MHz, FL = FP = 4.0MHz.

FIGURE 4 - CIRCUITS FOR ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS (CONTINUED)

FIGURE 4(h) - VIDEO SIGNAL



NOTES

1. R = Serial resistors to be adjusted to obtain a rise time compatible with the appropriate timing diagram.
2. C = Decoupling capacitors to be adjusted to adequately decouple.
3. For TD1: FI = 1.0MHz, FL = 7.4MHz.
4. For TD2: FI = 1.0MHz, FL = FP = 4.0MHz.

FIGURE 4 - CIRCUITS FOR ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS (CONTINUED)

OUTPUT WAVEFORM FEATURES

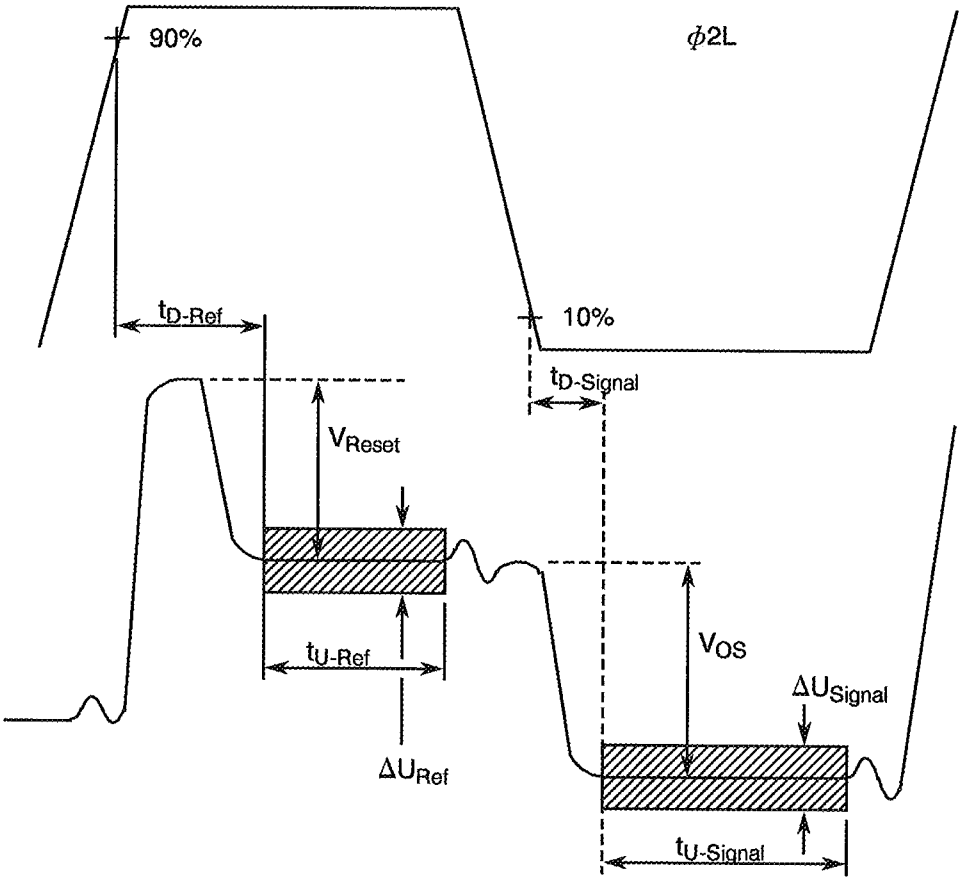


FIGURE 4 - CIRCUITS FOR ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - ELECTRODE CAPACITANCE

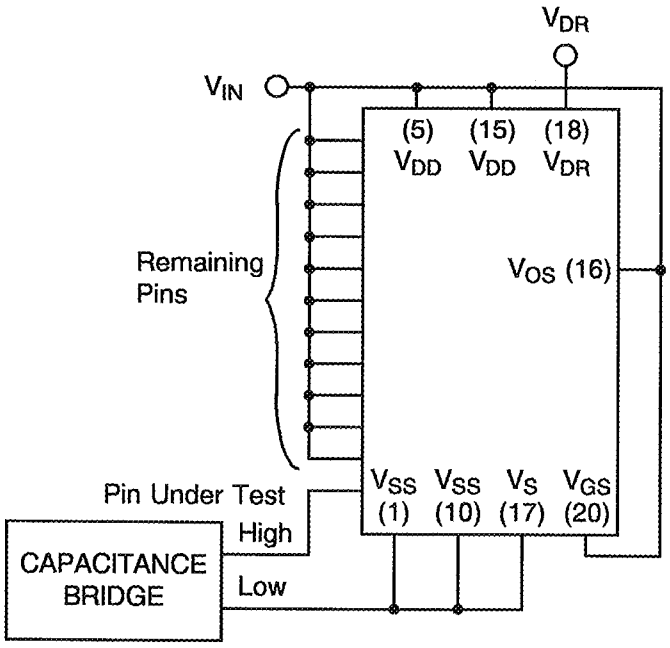
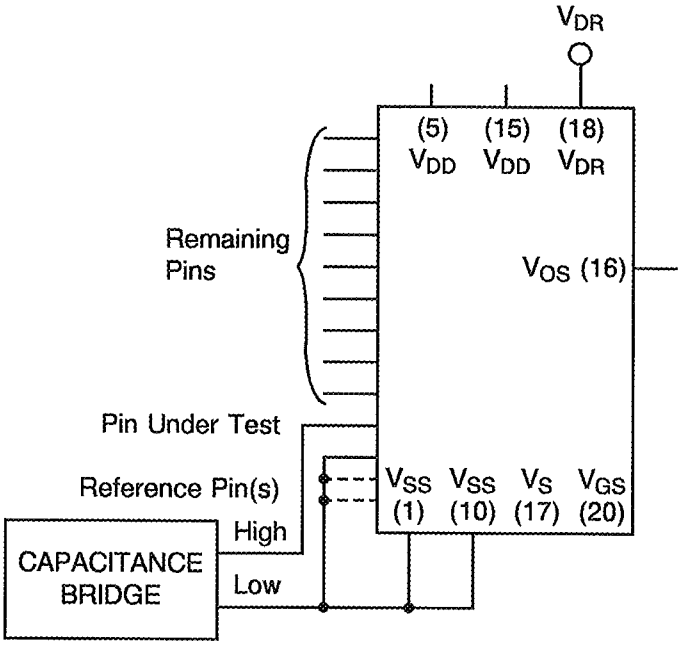


FIGURE 4(j) - ELECTRODE CAPACITANCE WITH RESPECT TO ANOTHER CLOCK



NOTES

1. Pins 4 and 9 must be connected together when either is measured.

TABLE FOR FIGURE 4(j)

MEASUREMENT	CϕPo		CϕMo		CϕLo	
	Ref. Pin	Test Pin	Ref. Pin	Test Pin	Ref. Pin	Test Pin
M1	11, 12, 13	14	6, 7, 8	9	2	3
M2	11, 13, 14	12	6, 8, 9	7	3	2
M3	-	11, 12, 13, 14	-	6, 7, 8, 9	-	2, 3
M4	12, 14	11, 13	7, 9	6, 8	-	-

NOTES

1. $C\phi Po$ or $C\phi Mo$ max. $= MAX\left[\frac{1}{2}(M1+M2-M4) \bullet \frac{1}{2}(M4-\frac{M3}{2})\right]$.

   $C\phi Lo = \frac{1}{2}(M1+M2-M3)$.

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
1	Leakage Current on Input Gates	I_L	As per Table 2	As per Table 2	±50 or (1) ±100	pA %
16 to 29	Insulation Leakage Current between Pins (Input Current)	I_E	As per Table 2	As per Table 2	±1.0 or (1) ±100	nA %
30	Power Supply Current 1	I_{DD1}	As per Table 2	As per Table 2	±10	%
31	Power Supply Current 2	I_{DD2}	As per Table 2	As per Table 2	±10	%
37	Average Dark Signal (Image Area)	VDS1	As per Table 2	As per Table 2	±30	%
38	Average Dark Signal (Image Area + Storage Area)	VDS2	As per Table 2	As per Table 2	±30	%

NOTES

1. Whichever is the greater, referred to the initial value.

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

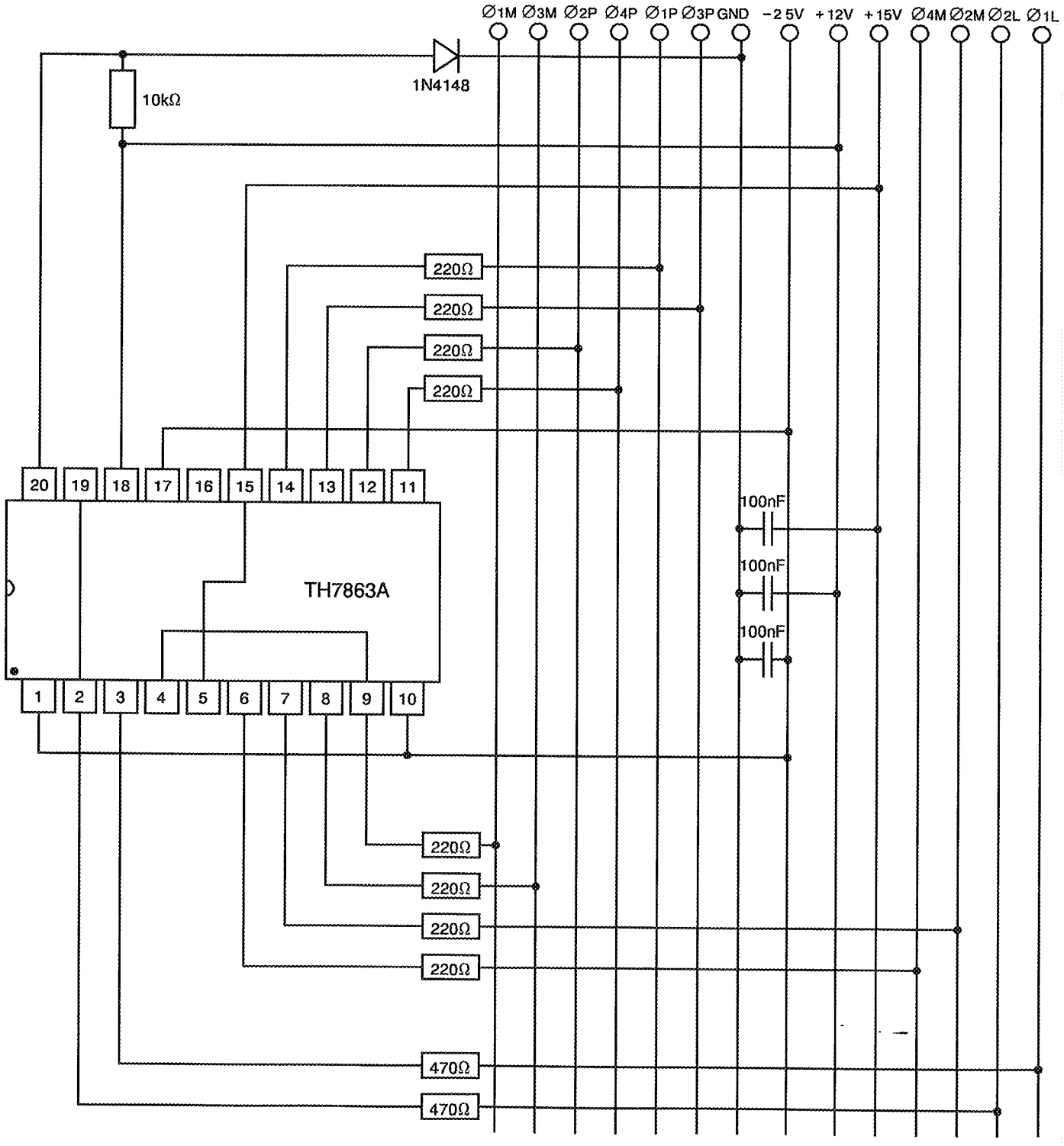
TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS		SYMBOL	CONDITIONS	UNIT
1	Ambient Temperature		T_{amb}	+125(+0−5)	°C
2	Output Amplifier Drain Supply	(Pins 5-15)	V_{DD}	15	V
3	Reset Bias	(Pin 18)	V_{DR}	13	V
4	Register Output Gate Bias	(Pin 20)	V_{GS}	0.6	V
5	Output Amplifier Gate Bias	(Pin 17)	V_S	−2.5	V
6	Substrate Bias	(Pins 1-10)	V_{SS}	−2.5	V
7	Image Zone Clocks	(Pins 11-12-13-14)	ϕP	High 11 Low 0.3	Vac
8	Memory Zone Clocks	(Pins 4-6-7-8-9)	ϕM	High 11 Low 0.3	Vac
9	Output Register Clocks	(Pins 2-3)	ϕL	High 11 Low 0.3	Vac
10	Reset Clock	(Pin 19)	ϕR	High 11 Low 0.3	Vac
11	Image Zone to Memory Zone and Memory Zone to Output Register Frequency		F_I	125k	Hz
12	Output Register and Reset Frequency		F_L	1.0M	Hz

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9020)

4.8.1 Electrical and Electro-optical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{ref} \pm 3$ °C.

4.8.2 Electrical and Electro-optical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{ref} \pm 3$ °C.

4.8.3 Electrical and Electro-optical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{ref} \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9020. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(b) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9020. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

4.9 TOTAL DOSE IRRADIATION TESTING

4.9.1 Application

If specified in Para. 4.2.1 of this specification, total dose irradiation testing shall be performed in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.9.2 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6 of this specification.

4.9.3 Electrical and Electro-optical Measurements

For all Variants, the parameters to be measured prior to irradiation exposure are I_L in accordance with Table 2 and those parameters scheduled in the individual Table 1(a) for Variant 01, with the Conditions and Limits as specified in the individual Table 1(a) for the Variant in question. Only devices which meet these requirements shall be included in the test sample.

The parameters to be measured during and on completion of irradiation testing are scheduled in Table 7 of this specification.

TABLE 6 - ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	ABSOLUTE		UNIT
						MIN.	MAX.	
1	Leakage Current on Input Gates	I_L	As per Table 2	As per Table 2	±50 or (1) ±100	-	300	pA %
16 to 29	Insulation Leakage Current between Pins (Input Current)	I_E	As per Table 2	As per Table 2	±1.0 or (1) ±100	-	-	nA %
30	Power Supply Current 1	I_{DD1}	As per Table 2	As per Table 2	±10	-	-	%
31	Power Supply Current 2	I_{DD2}	As per Table 2	As per Table 2	±10	-	-	%
34	Saturation Voltage for the Image Area	V_{SAT}	As per Table 2	As per Table 2	±15	-	-	%
37	Average Dark Signal (Image Area)	VDS1	As per Table 2	As per Table 2	±30	-	-	%
38	Average Dark Signal (Image Area + Storage Area)	VDS2	As per Table 2	As per Table 2	±30	-	-	%
39	Dark Signal Non-uniformity, standard deviation σ	DSNU(σ)	As per Table 2	As per Table 2	-	As per Table 2		mV
40	Number of DSNU Defects beyond a3 Limit	Ndef3	As per Table 2	As per Table 2	-	As per Table 2		-
41	Number of DSNU Defects beyond a4 Limit	Ndef4	As per Table 2	As per Table 2	-	As per Table 2		-
44	Responsivity	R	As per Table 2	As per Table 2	±5.0	-	-	%
45	Photoresponse Non-uniformity, standard deviation σ	PRNU(σ)	As per Table 2	As per Table 2	-	As per Table 2		%
46	Number of PRNU Defects beyond a1 Limit	Ndef1	As per Table 2	As per Table 2	-	As per Table 2		-
47	Number of PRNU Defects beyond a2 Limit	Ndef2	As per Table 2	As per Table 2	-	As per Table 2		-

NOTES

1. Whichever is the greater, referred to the initial value.

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING

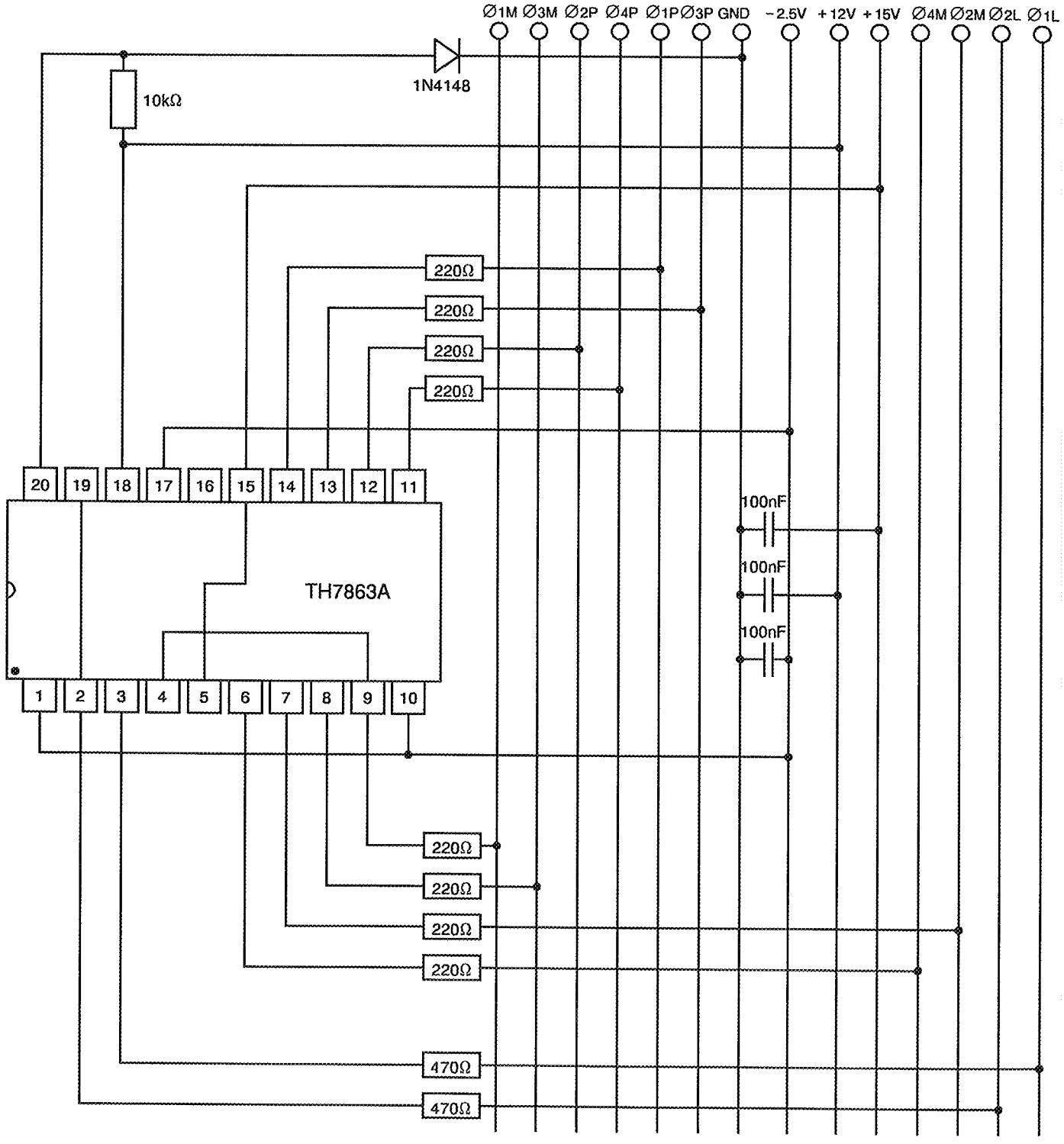


TABLE 7 - ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	ABSOL. (MAX) t0 (1)	ABSOL. (MAX) t1 (1)	ABSOL. (MAX) t2 (1)	UNIT
1	Leakage Current on Input Gates	I_L	As per Table 2	As per Table 2	300	300	300	pA
31	Power Supply Current 1	I_{DD1}	As per Table 2	As per Table 2	13 -	- ±15	- ±15	mA %
37	Average Dark Signal (Image Area)	VDS1	As per Table 2	ti = 10s T_{amb} = −20°C Timing Diagram TD2 (Note 3)	30	120	400	mV
90	Average Dark Signal (Storage Area)	VDS3	-	ti = 180ms T_{amb} = −20°C Timing Diagram TD2 Notes 3 and 4	1.0	10	30	mV

NOTES

1. t0 = Initial Measurements, t1 = Measurements during and on completion of Irradiation Testing, t2 = Measurements after annealing, (see ESA/SCC Basic Specification No. 22900, Figure II).
2. Whichever is the greater, referred to the initial value.
3. Measurements are performed at −20°C in order to separate image area and storage area dark signal contributions at t0, t1, t2 steps.
4. This parameter is derived as a difference in measurements between VDS2 and VDS1.

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION

TYPE VARIANT No. 01

No.	CHARACTERISTICS	SYMBOL	LIMITS		UNITS	REMARKS
			MIN.	MAX.		
1	Operating Temperature Range	T_{op}	−20	+85	°C	
2	Reference Temperature	T_{ref}	+22	+28	°C	
3	Flatness of Image Area	P	-	10	µm	At +25 ± 3 °C
4	Spectral Range for Optical Coating on Window	WOC	N/A		nm	
5	Timing Diagram	TD	TD1 (Figure 3(b))		-	
6	Power Supply Current 1	I_{DD1}	-	10	mA	Static V_{DD} = 15V V_{DR} = ϕR = 10V
7	Power Supply Current 2	I_{DD2}	N/A		mA	Dynamic
8	Power Supply Current 1 over T_{op}	I_{DD1} (T_{op})	-	13	mA	Static V_{DD} = 15V V_{DR} = ϕR = 10V
9	DC Output Level	V_{Ref}	N/A		V	
10	Output Impedance	Z_S	N/A		Ω	
11	Saturation Voltage for the Image Area	V_{SAT}	900	-	mV	
12	Vertical Charge Transfer Inefficiency	VCTI	-	7.0	%	
13	Horizontal Charge Transfer Inefficiency	HCTI	-	5.0	%	
14	Average Dark Signal (Image Area)	VDS1	-	4.0	mV	ti = 20ms
15	Average Dark Signal (Image Area + Storage Area)	VDS2	-	8.0	mV	ti = 20ms
16	Average Dark Signal (Image Area + Storage Area) over T_{OP}	VDS2(T_{op})	-	220	mV	Timing diagram TD1
17	Dark Signal Non-uniformity, standard deviation σ	DSNU(σ)	-	0.5	mV	Slope effect removed
18	Number of Dark Signal Defects beyond a3 limit	Ndef3	-	0	-	Slope effect removed

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION (CONTINUED)

TYPE VARIANT No. 01

No.	CHARACTERISTICS	SYMBOL	LIMITS		UNITS	REMARKS
			MIN.	MAX.		
19	Number of Dark Signal Defects beyond a4 limit	Ndef4	N/A		-	
20	DSNU Limit for Ndef3	a3	-	2.0	mV	Slope effect removed
21	DSNU Limit for Ndef4	a4	N/A		mV	
22	Responsivity	R	7.0	-	V/μJ/cm²	BG38 optical filter
23	Responsivity over T_{op}	$R(T_{op})$	6.0	-	V/μJ/cm²	BG38 optical filter
24	Photoresponse Non-uniformity, standard deviation σ	PRNU(σ)	-	2.5	%	BG38 optical filter
25	Number of PRNU defects beyond a1 limit	Ndef1	-	10	-	BG38 optical filter
26	Number of PRNU defects beyond a2 limit	Ndef2	-	0	-	BG38 optical filter
27	PRNU limit for Ndef1	a1	−20	-	%	BG38 optical filter
28	PRNU limit for Ndef2	a2	−30	+15	%	BG38 optical filter Black defects (dips) area max. = 2 pixels
29	Spectral Responsivity in Optical Band B1	R(B1)	N/A		V/μJ/cm²	
30	Spectral Responsivity in Optical Band B2	R(B2)	N/A		V/μJ/cm²	
31	Spectral Responsivity in Optical Band B3	R(B3)	N/A		V/μJ/cm²	
32	Spectral Responsivity in Optical Band B4	R(B4)	N/A		V/μJ/cm²	
33	Spectral Responsivity in Optical Band B5	R(B5)	N/A		V/μJ/cm²	
34	Spectral Responsivity in Optical Band B6	R(B6)	N/A		V/μJ/cm²	
35	Spectral Responsivity in Optical Band B7	R(B7)	N/A		V/μJ/cm²	
36	Linearity Error	LE	N/A		%	
37	Temporal Noise	V_N	N/A		μV	
38	Offset Voltage	V_{Offset}	N/A		mV	

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION (CONTINUED)

TYPE VARIANT No. 01

No.	CHARACTERISTICS	SYMBOL	LIMITS		UNITS	REMARKS
			MIN.	MAX.		
39	Amplitude of Reset Feedthrough	V_{Reset}	N/A		mV	
40	Reference Level Settling Time	$t_{D\text{-}Ref}$	N/A		ns	
41	Reference Level Duration	$t_{U\text{-}Ref}$	N/A		ns	
42	Reference Level Error Band	ΔU_{Ref}	N/A		mV	
43	Signal Level Settling Time	$t_{D\text{-}Signal}$	N/A		ns	
44	Signal Level Duration	$t_{U\text{-}Signal}$	N/A		ns	
45	Signal Level Error Band	ΔU_{Signal}	N/A		mV	
46	Electrode Capacitance	$C\phi P$	N/A		pF	
47	Electrode Capacitance	$C\phi M$	N/A		pF	
48	Electrode Capacitance	$C\phi L$	N/A		pF	
49	Electrode Capacitance	$C\phi R$	N/A		pF	
50	Electrode Capacitance with respect to another Clock	$C\phi Po$	N/A		pF	
51	Electrode Capacitance with respect to another Clock	$C\phi Mo$	N/A		pF	
52	Electrode Capacitance with respect to another Clock	$C\phi Lo$	N/A		pF	
53	Charge to Voltage Conversion Factor	CVF	N/A		µV/e	

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION

TYPE VARIANT No. 02

No.	CHARACTERISTICS	SYMBOL	LIMITS		UNITS	REMARKS
			MIN.	MAX.		
1	Operating Temperature Range	T_{op}	−20	+85	°C	
2	Reference Temperature	T_{ref}	+32	+38	°C	
3	Flatness of Image Area	P	-	10	µm	At +25±3 °C
4	Spectral Range for Optical Coating on Window	WOC	450	900	nm	Reflectance < 1.0% for each side
5	Timing Diagram	TD	TD2 (Figure 3(b))		-	
6	Power Supply Current 1	I_{DD1}	-	10	mA	Static V_{DD} = 15V V_{DR} = ϕR = 10V
7	Power Supply Current 2	I_{DD2}	-	10	mA	Dynamic
8	Power Supply Current 1 over T_{op}	I_{DD1} (T_{op})	-	13	mA	Static V_{DD} = 15V V_{DR} = ϕR = 10V
9	DC Output Level	V_{Ref}	10	13	V	
10	Output Impedance	Z_S	-	500	Ω	R = 1000Ω C = 200nF
11	Saturation Voltage for the Image Area	V_{SAT}	900	-	mV	
12	Vertical Charge Transfer Inefficiency	VCTI	-	7.0	%	
13	Horizontal Charge Transfer Inefficiency	HCTI	-	5.0	%	
14	Average Dark Signal (Image Area)	VDS1	-	270	mV	ti = 1.0s
15	Average Dark Signal (Image Area + Storage Area)	VDS2	-	270	mV	ti = 1.0s
16	Average Dark Signal (Image Area + Storage Area) over T_{op}	VDS2(T_{op})	-	220	mV	Timing diagram TD1
17	Dark Signal Non-uniformity, standard deviation σ	DSNU(σ)	-	17	mV	ti = 1.0s
18	Number of Dark Signal Defects beyond a3 limit	Ndef3	-	10	-	ti = 1.0s

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION (CONTINUED)

TYPE VARIANT No. 02

No.	CHARACTERISTICS	SYMBOL	LIMITS		UNITS	REMARKS
			MIN.	MAX.		
19	Number of Dark Signal Defects beyond a4 limit	Ndef4	-	0	-	ti = 1.0s
20	DSNU Limit for Ndef3	a3	-	68	mV	ti = 1.0s
21	DSNU Limit for Ndef4	a4	-	95	mV	ti = 1.0s
22	Responsivity	R	7.0	-	V/μJ/cm²	BG38 optical filter
23	Responsivity over T_{op}	$R(T_{op})$	6.0	-	V/μJ/cm²	BG38 optical filter Timing diagram TD1
24	Photoresponse Non-uniformity, standard deviation σ	PRNU(σ)	-	2.5	%	B5, B6 optical filters
25	Number of PRNU defects beyond a1 limit	Ndef1	-	10	-	B5, B6 optical filters
26	Number of PRNU defects beyond a2 limit	Ndef2	-	0	-	B5, B6 optical filters
27	PRNU limit for Ndef1	a1	−10	+10	%	B5, B6 optical filters
28	PRNU limit for Ndef2	a2	−20	+20	%	B5, B6 optical filters
29	Spectral Responsivity in Optical Band B1	R(B1)	N/A		V/μJ/cm²	
30	Spectral Responsivity in Optical Band B2	R(B2)	6.3	-	V/μJ/cm²	517/81 nm
31	Spectral Responsivity in Optical Band B3	R(B3)	10	-	V/μJ/cm²	610/98 nm
32	Spectral Responsivity in Optical Band B4	R(B4)	12.2	-	V/μJ/cm²	703/94 nm
33	Spectral Responsivity in Optical band B5	R(B5)	10.9	-	V/μJ/cm²	827/98 nm
34	Spectral Responsivity in Optical band B6	R(B6)	7.0	-	V/μJ/cm²	900/105 nm
35	Spectral Responsivity in Optical band B7	R(B7)	N/A		V/μJ/cm²	
36	Linearity Error	LE	-	3.0	%	Signal amplitude = 45 to 850mV
37	Temporal Noise	V_N	-	200	μV	

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION (CONTINUED)

TYPE VARIANT No. 02

No.	CHARACTERISTICS	SYMBOL	LIMITS		UNITS	REMARKS
			MIN.	MAX.		
38	Offset Voltage	V_{Offset}	-	15	mV	
39	Amplitude of Reset Feedthrough	V_{Reset}	-	250	mV	
40	Reference Level Settling Time	$t_{D\text{-}Ref}$	-	70	ns	ϕ2L rising edge (90%) = reference
41	Reference Level Duration	$t_{U\text{-}Ref}$	45	-	ns	
42	Reference Level Error Band	ΔU_{Ref}	-	9.0	mV	
43	Signal Level Settling Time	$t_{D\text{-}Signal}$	-	40	ns	ϕ2L falling edge (10%) = reference V_{OS} = 400mV
44	Signal Level Duration	$t_{U\text{-}Signal}$	60	-	ns	V_{OS} = 400mV
45	Signal Level Error Band	ΔU_{Signal}	-	9.0	mV	V_{OS} = 400mV
46	Electrode Capacitance	CϕP	-	2000	pF	T_{amb} = +25 ± 3 °C
47	Electrode Capacitance	CϕM	-	2500	pF	T_{amb} = +25 ± 3 °C
48	Electrode Capacitance	CϕL	-	200	pF	T_{amb} = +25 ± 3 °C
49	Electrode Capacitance	CϕR	-	10	pF	T_{amb} = +25 ± 3 °C
50	Electrode Capacitance with respect to another Clock	CϕPo	-	2000	pF	T_{amb} = +25 ± 3 °C
51	Electrode Capacitance with respect to another Clock	CϕMo	-	2500	pF	T_{amb} = +25 ± 3 °C
52	Electrode Capacitance with respect to another Clock	CϕLo	-	200	pF	T_{amb} = +25 ± 3 °C
53	Charge to Voltage Conversion Factor	CVF	1.7	2.2	µV/e	5 devices/lot (not deliverable devices)