TRANSISTORS, MOSFET, P-CHANNEL POWER,

BASED ON TYPE IRF9140

ESCC Detail Specification No. 5206/006

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BASED ON TYPE IRF9140

ESA/SCC Detail Specification No. 5206/006

space components
coordination group

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DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE Reference	CHANGE Item	Approved DCR No.
		This Issue supersedes Issue 1 and incorporates all modifications defined in the following DCR's:-		
		Cover Page		None
		DCN		None
		Table 1(a)	: Values amended	22939
		Figure 2	: Values in Table aligned to those of Table 2 in ESA/SCC Detail Specification No. 5206/004	22939
		Para. 2	: Reference to ESA/SCC Basic Specification No. 21400 added	22939
		Para. 4.2.1	: Para. rewritten	22939
		Para. 4.2.2	: Reference to Bond Strength and Die-Shear Tests deleted	23499
			: Reference to PIND Test deleted	21043
		Para. 4.2.3	: Reference to radiographic Inspection deleted	21049
		Para. 4.2.4	: Reference to Bond Strength and Die-Shear Tests deleted	23499
		Table 2	: Limits of items Nos. 9, 14 and 16 amended	22939
		Table 3	: Notes from Tables 2 brought at the bottom of Table 3 except sampling Note	21047

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1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for Transistors, MOSFET, P-Channel, Power, based on Type IRF9140. It shall be read in conjunction with ESA/SCC Generic Specification No. 5000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type transistors specified herein, which are also covered by this specification, are listed in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the transistors specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The parameter derating information applicable to the transistors specified herein is shown in Figure 1(a).

1.5 SAFE OPERATING AREA

The safe operating area information applicable to the transistors specified herein is shown in Figure 1(b).

1.6 PHYSICAL DIMENSIONS

The physical dimensions of the transistors specified herein are shown in Figure 2.

1.7 FUNCTIONAL DIAGRAM

The functional diagram, showing lead identification, of the transistors specified herein, is shown in Figure 3.

1.8 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be taken for protection during all phases of manufacture, testing, packaging, shipment and any handling. These components are categorised as Class 1, with a Minimum Critical Path Failure Voltage of 30Volts.

TABLE 1(a) - TYPE VARIANTS

Variant	(1) Lead Material and Finish	(2) Based on Type	(3) V_{DS}Max (V)	(4) I_DMax (A) (Note 1)	(5) I_DMax (A) (Note 2)	(6) I_s (A) (Note 1)	(7) V_{DS} (80%) (V)	(8) I_{DM}Max (Apk)	(9) V_{DG} (V)
01	D3 or D4	IRF9140	-100	-19	-12	-19	-80	-76	-100

NOTES
1. At T_C = +25°C
2. At T_C = +100°C

TABLE 1(b) - MAXIMUM RATINGS

NO	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Drain Source Voltage	V_{DS}	Table 1(a) Column 3	V	
2	Gate Source Voltage	V_{GS}	±20	V	
3	Drain Gate Voltage	V_{DG}	Table 1(a) Column 9	V	
4	Drain Current, (Continuous)	I_D	Table 1(a) Column 4	A	At T_C = +25°C Note 1
5	Drain Current, (Continuous)	I_D	Table 1(a) Column 5	A	At T_C = +100°C Note 1
6	Source Current, (Continuous)	I_S	Table 1(a) Column 6	A	At T_C = +25°C Note 1
7	Drain Current Pulsed (Peak)	I_{DM}	Table1(a) Column 8	Apk	
8	Total Power Dissipation	P_{tot}	125	W	Note 2
9	Operating Temperature Range	T_{op}	-55 to +150	°C	T_{amb}
10	Storage Temperature Range	T_{stg}	-55 to +150	°C	
11	Soldering Temperature	T_{sol}	+300	°C	Time: ≤10 Sec. Distance to Case: ≥1.5mm
12	Thermal Resistance Junction to Case	$R_{\theta JC}$	1.0	°C/W	

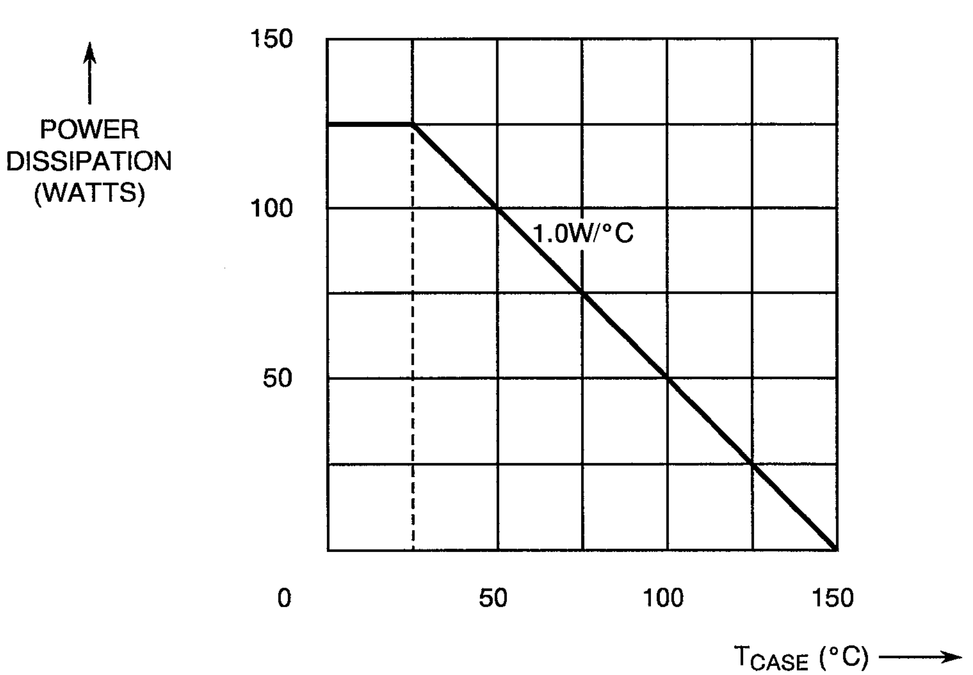
NOTES
1. For T_C > + 25°C derated as follows:-

$$I_D = \frac{\sqrt{P(rated)}}{K} \quad \text{where : } P(rated) = 125 - (T_C-25)(1.0) \text{ Watts.}$$

: K = rated $r_{DS(ON)}$ at T_j = +150°C.

2. At T_C < +25°C. For derating at T_C > +25°C, see Figure 1(a).

FIGURE 1(a) - PARAMETER DERATING INFORMATION



Power Dissipation Versus Temperature

FIGURE 1(b) - MAXIMUM SAFE OPERATING AREA

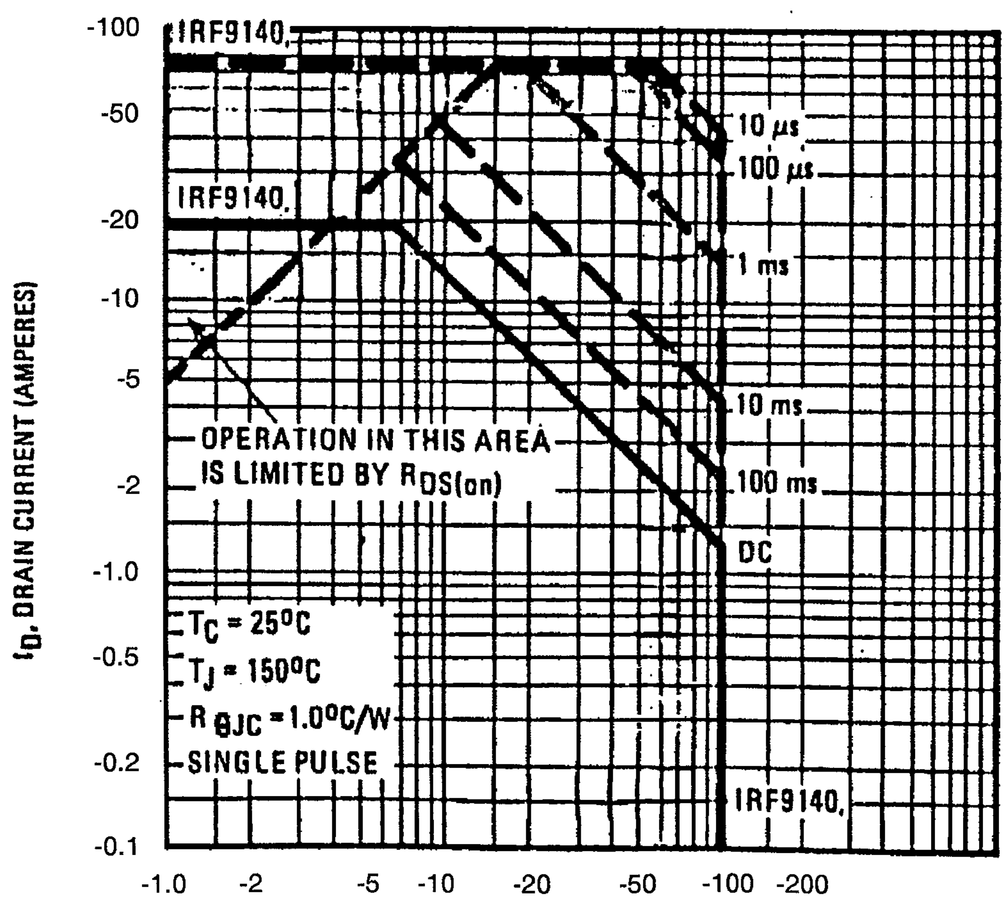
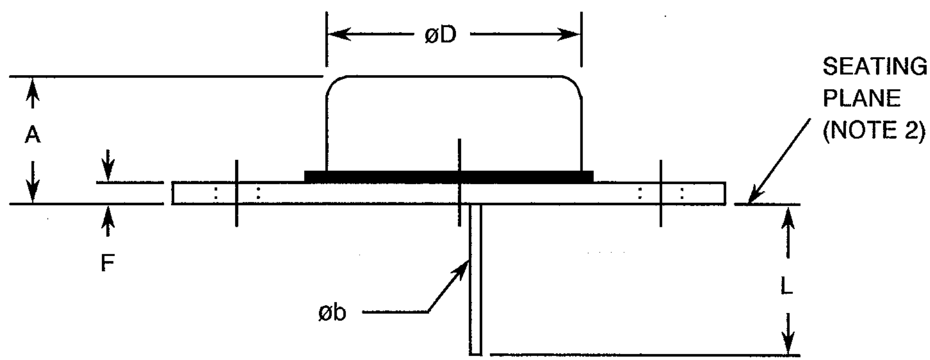
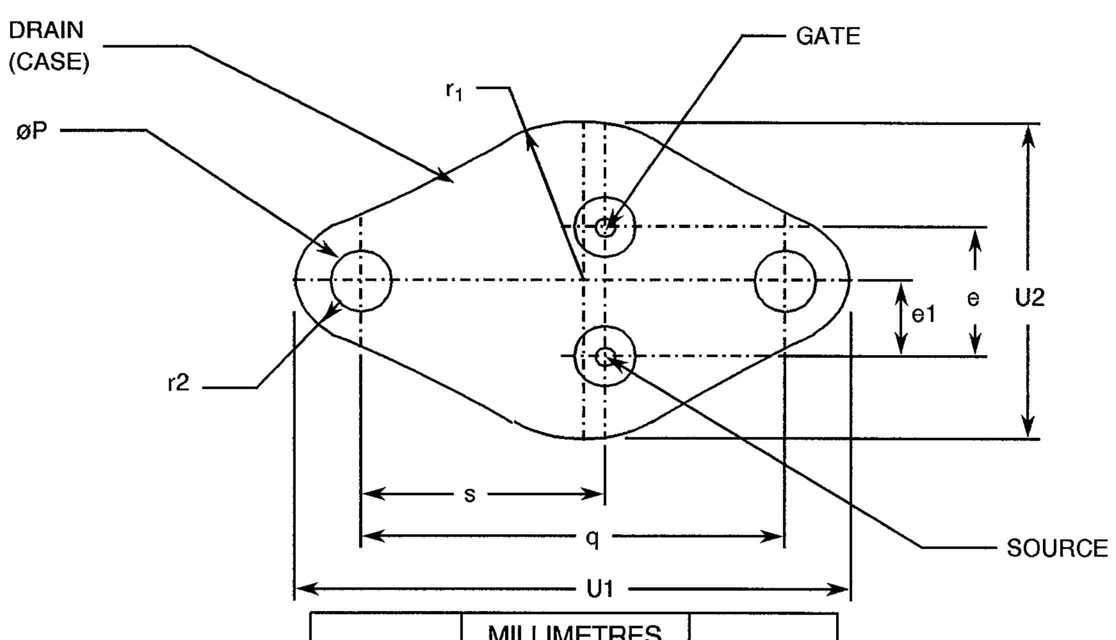


FIGURE 2 - PHYSICAL DIMENSIONS



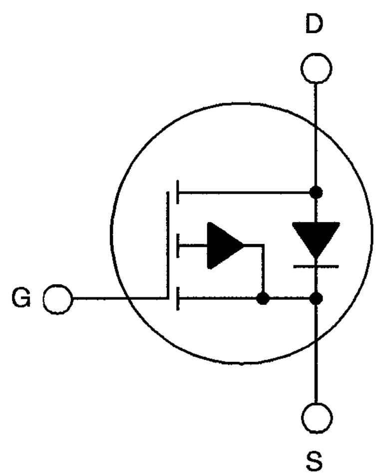


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	6.86	9.15	
øb	0.97	1.10	
øD	-	22.23	
e	10.67	11.18	1
e1	5.21	5.72	1
F	1.52	3.43	
L	7.92	12.7	
øP	3.84	4.09	
q	29.9	30.4	
r1	12.57	13.34	
r2	3.33	4.78	
s	16.64	17.15	
U1	-	40.13	
U2	-	27.17	

NOTES

1. These dimensions should be measured at points 1.27mm, 1.40mm below the seating plane. When a gauge is not used, the measurements will be made at the seating plane.
2. The seating plane of the header shall be flat within 0.03mm concave to 0.10mm convex inside a 23.62mm diameter circle on the centre of the header and flat within 0.03mm concave to 0.15mm convex overall.

FIGURE 3 - FUNCTIONAL DIAGRAM



NOTES

1. The drain is electrically connected to the case.

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 5000 for Discrete Semiconductors.

(c) ESA/SCC Basic Specification No. 21400, Scanning Electron Microscope (SEM) Inspection of Semiconductor Dice.

(c) MIL-STD-750, Test Methods and Procedures for Semiconductor Devices.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition the following abbreviations are used:-

I_{GSS} = Gate to Source Leakage Current

B_{VGSS} = Gate to Source Breakdown Voltage

$V_{GS(th)}$ = Gate Threshold Voltage

V_{GS} = Gate to Source Voltage

V_{DG} = Drain to Gate Voltage

V_{DS} = Drain to Source Voltage

V_{SD} = Source to Drain Diode Forward Voltage

gfs = Forward Transfer Conductance

C_{iss} = Common Source Input Capacitance

C_{oss} = Common Source Output Capacitance

C_{rss} = Common Source Reverse Transfer Capacitance

I_s = Source Current

I_D = Drain Current

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the transistors specified herein shall be as stated in this specification and ESA/SCC Generic Specification No. 5000 for Discrete Semiconductors. Deviations from the Generic Specification, applicable to this Detail Specification only, are listed in Para 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

(a) For testing levels 'B' and 'C', a Scanning Electron Microscope (SEM) inspection shall be performed on samples from each metallisation lot in accordance with ESA/SCC Basic Specification No. 21400. The SEM inspection shall include the gate finger area plus 3 randomly selected transistor cells, magnification X2000 viewed from above and with the die tilted about 60°.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

(a) Para. 7.1.1(a), High Temperature Reverse Bias (H.T.R.B.) Burn-in: Prior to operating power burn-in, a high temperature reverse bias screen at +150°C shall be performed in accordance with Table 5(a) of this specification. The exposure to H.T.R.B. shall be 72 hours and Table 4 Parameter Drift Values shall be applied at 0 and 72 hours.

(b) Para. 7.1.1(b), Power Burn-in: The duration shall be 240 hours.

(c) The following test shall be added to the Electrical Measurements at Room Temperature; to be performed after the power burn-in only:-

Verification of Safe Operating Area (See Figure 4(a))

Test 'A' Condition

T_{case} = +25 ±10 °C. Duration = 1.0s.

V_{DS} = -80V. I_D = -1.5A.

Test 'B' Condition

T_{case} = +25 ±10 °C. Duration = 1.0s.

V_{DS} = -7.0V. I_D = -17.8A.

Test Method for Both Tests

Using a 1.0 second pulse width with a minimum of 1 minute between pulses, increase V_{GS} and the Drain Supply Voltage until the specified value of I_D and V_{DS} are obtained. A load resistor, R_L, shall be used and shall be selected such the $I_D \times R_L$ = 2.5 ± 1.0V.

Electrical Measurements

After performing both tests, the electrical measurements Nos. 1 to 8 inclusive of Table 2 shall be repeated.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the transistors specified herein shall be checked; they shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the transistors specified herein shall be 20 grammes.

4.3.3 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESA/SCC Generic Specification No. 5000. The test conditions shall be as follows:-

Test Condition : 'A', Tension

Applied Force : 10 Newtons

Duration : 10 Seconds

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the transistors specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals and the lids shall be welded, brazed or pre-form soldered.

4.4.2 Lead Material and Finish

The lead material shall be Type 'D' with Type '3 or 4' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500.

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Terminal Identification.

(b) The SCC Component Number.

(c) Traceability information.

4.5.2 Lead Identification

Lead identification shall be as shown in Figures 2 and 3.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:-

520600601B

Detail Specification Number — 5206006

Type Variant, (see Table 1(a)) — 01

Testing Level (B or C, as applicable) — B

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. The measurements shall be performed at T_{amb} = +22 ± 3 °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at T_{amb} = +125 (+0-5) and -55 (+5-0) °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Tables 2 and 3 are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at T_{amb} = +22 ± 3°C. The parameter drift values (Δ) applicable to the parameters scheduled shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified in Table 2 shall not be exceeded.

4.7.2 Conditions for H.T.R.B. and Power Burn-in

The requirements for H.T.R.B. and Power Burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 5000. The conditions for H.T.R.B. and Power Burn-in shall be as specified in Tables 5(a) and 5(b) of this specification.

4.7.3 Electrical Circuits for H.T.R.B. and Power Burn-in

Circuits for use in performing the H.T.R.B. and Power Burn-in tests are shown in Figures 5(a) and 5(b) of this specification .

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE, d.c. PARAMETERS

NO	CHARACTERISTICS	SYMBOL	MIL-STD-750 TEST METHOD	TEST CONDITION	LIMITS		UNIT
					MIN	MAX	
1	Breakdown Voltage Drain to Source	BV_{DSS}	3407 Bias Cond. C	$V_{GS} = 0$ $I_D = -0.25mA$	-100	-	V
2	Gate Threshold Voltage	$V_{GS(th)}$	3403	$V_{DS} \geq V_{GS}$ $I_D = -0.25mA$	-2.0	-4.0	V
3 to 4	Gate to Source Leakage Current	I_{GSS}	3411 Bias Cond. C	$V_{GS} = -20V$ $V_{GS} = +20V$ $V_{DS} = 0$	- -	-100 -100	nA
5	Drain Current	I_{DSS}	3413 Bias Cond C	$V_{DS} = -100V$ $V_{GS} = 0$	-	-0.25	mA
6	Drain to Source ON Resistance	$r_{DS(ON)}$	3421	$V_{GS} = -10V$ $I_D = -10A$ Notes 1 and 2	-	0.20	Ω
7	Drain to Source ON Voltage	$V_{DS(ON)}$	3405	$V_{GS} = -10V$ $I_D = -10A$ Notes 1 and 2	-	-2.0	V
8	Source to Drain Diode Forward Voltage	V_{SD}	4011	$I_S = -19A$ Note 1	-2.4	-4.2	V

NOTES

1. Pulsed Measurement: Pulse Width ≤ 300ns, Duty Cycle ≤ 2%.
2. Measured within 2mm of case.
3 Measurement to be performed on a sample basis, LTPD 7 or less.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE, a.c. PARAMETERS

NO	CHARACTERISTICS	SYMBOL	MIL-STD-750 TEST METHOD	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
9	Foward Trans-conductance	gfs	3455	-	V_{DS} = -5V I_D = -10A Note 1	5.0	11	s
10	Turn-on Delay Time	$t_{D(ON)}$	3459	4(b)	V_{DD} = -50V I_D = -10A	-	30	ns
11	Rise Time	t_r	3251	4(b)	V_{DD} = -50V I_D = -10A	-	100	ns
12	Turn-off Delay Time	$t_{D(OFF)}$	3251	4(b)	V_{DD} = -50V I_D = -10A	-	100	ns
13	Fall Time	t_f	3251	4(b)	V_{DD} = -50V I_D = -10A	-	50	ns
14	Common Source Input Capacitance	C_{iss}	3431	-	V_{DS} = -25V V_{GS} = 0A f = 1MHz	900	1600	pF
15	Common Source Output Capacitance	C_{oss}	3453	4(c)	V_{DS} = - 25V f = 1MHz	400	700	pF
16	Common Source Reverse Transfer Capacitance	C_{rss}	3433	-	V_{DS} = -25V V_{GS} = 0 f = 1MHz	60	400	pF

NOTES: See Page 14.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125 (+0-5) °C

NO	CHARACTERISTICS	SYMBOL	MIL-STD-750 TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
2	Gate Threshold Voltage	$V_{GS(th)}$	3403	$V_{DS} \geq V_{GS}$ $I_D = -0.25mA$	-1.0	-	V
3 to 4	Gate to Source Leakage Current	I_{GSS}	3411 Bias Cond. C	$V_{GS} = -20V$ $V_{GS} = +20V$ $V_{DS} = 0$	- -	-200 -200	nA
5	Drain Current	I_{DSS}	3413 Bias Cond. C	$V_{DS} = -80V$ $V_{GS} = 0$	-	-1.0	mA
6	Drain to Source ON Resistance	$r_{DS(ON)}$	3421	$V_{GS} = -10V$ $I_D = -10A$ Notes 1 and 2	-	0.55	Ω

NOTES
1. Pulsed Measurement: Pulse Width ≤ 300ns, Duty Cycle ≤ 2%.
2. Measured within 2mm of case.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, -55 (+5-0) °C

NO	CHARACTERISTICS	SYMBOL	MIL-STD-750 TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
2	Gate Threshold Voltage	$V_{GS(th)}$	3403	$V_{DS} \geq V_{GS}$ $I_D = -0.25mA$	-	-5.0	V

NOTES
1. Pulsed Measurement: Pulse Width ≤ 300ns, Duty Cycle ≤ 2%.
2. Measured within 2mm of case.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - SAFE OPERATING AREA TEST CIRCUIT

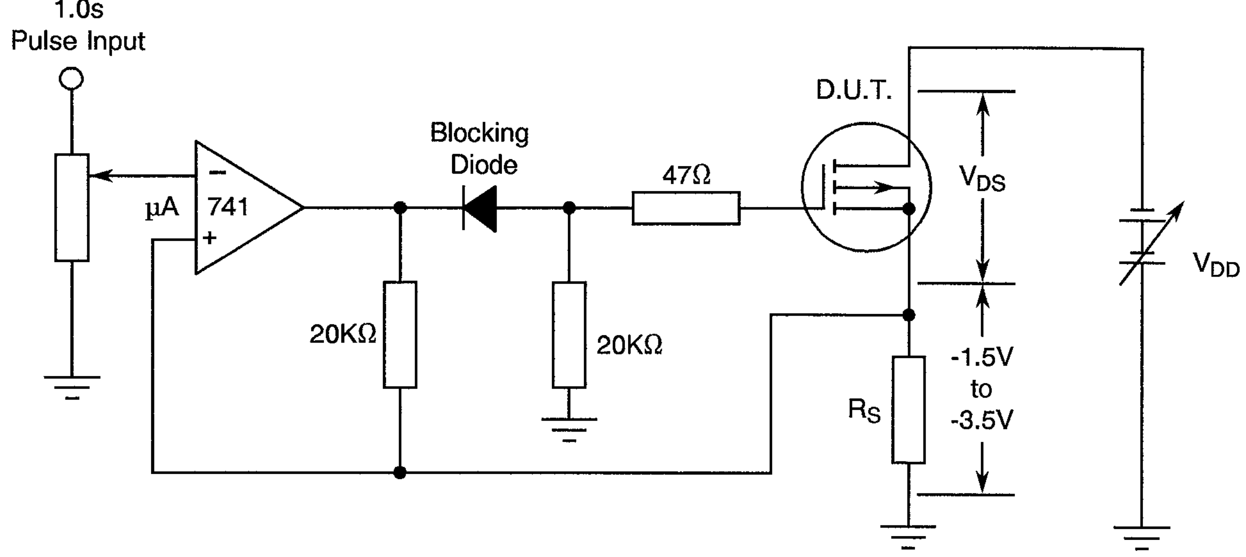
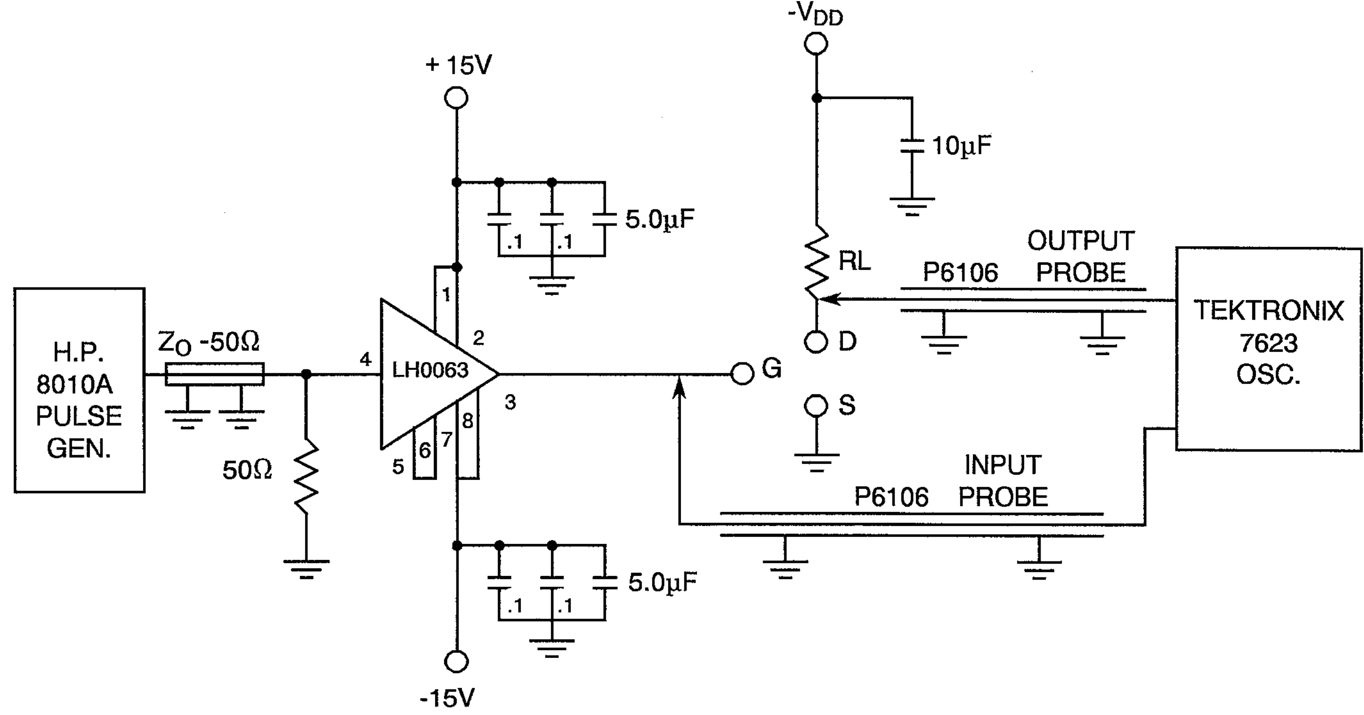
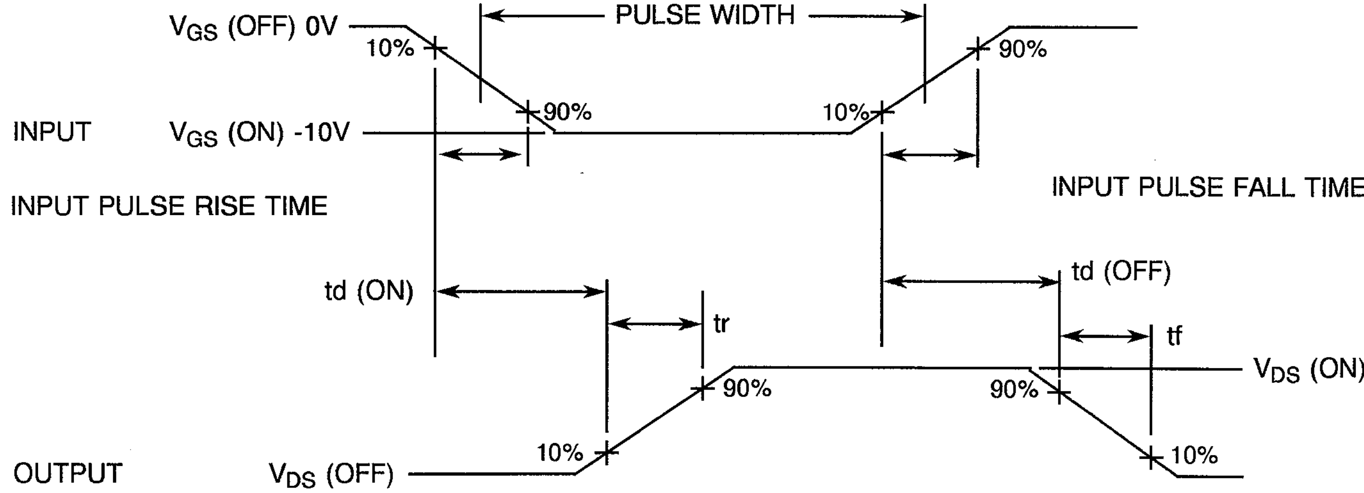


FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONT'D)

FIGURE 4(b) - SWITCHING TIME TESTS CIRCUIT



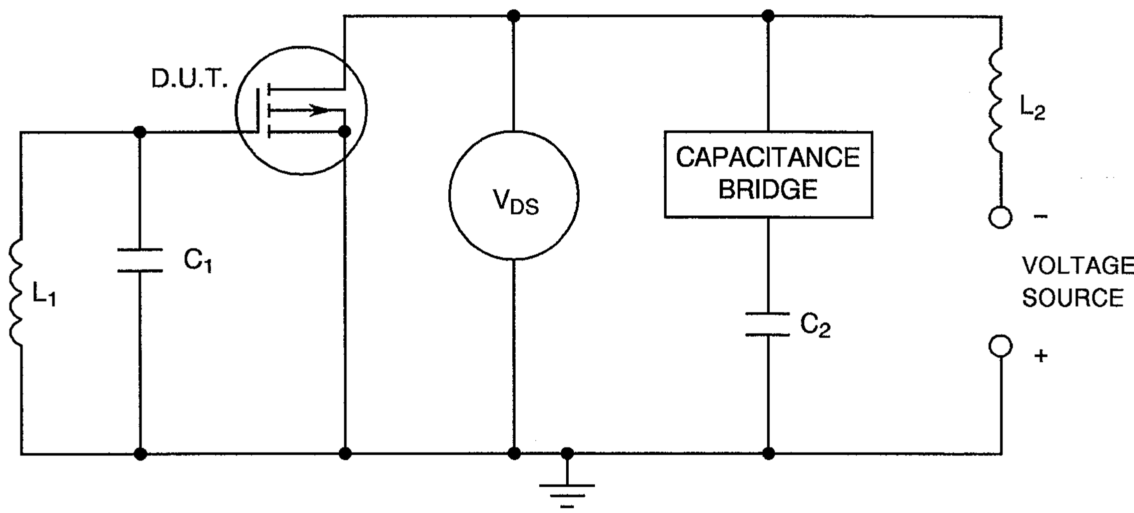
NOTES
1. LH0063 case grounded.
2. Grounded connections common to ground plane on board.
3. Pulse width ≤ 3.0s, Period ≤ 1.0ms, Amplitude = 0V to -10V.



NOTES
1. When measuring rise time, V_{GS} (on) shall be as specified on the input waveform.
2. When measuring fall time, V_{GS} (off) shall be as specified on the input waveform.
3. The input transition and drain voltage response detector shall have rise and fall response times such that doubling these responses will not affect the results greater than the precision of measurement.
4. The current shall be sufficiently small so that doubling it does not affect test results greater than the precision of measurement.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONT'D)

FIGURE 4(c) - COMMON SOURCE OUTPUT CAPACITANCE



PROCEDURE

The capacitors C_1 and C_2 shall present short circuits at the test frequency. L_1 and L_2 shall present a high ac impedance at the test frequency for isolation. The bridge shall have low dc resistance between its output terminals and should be capable of carrying the test current without affecting the desired accuracy of measurement.

TABLE 4 - PARAMETER DRIFT VALUES

NO	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
2	Gate Threshold Voltage	$V_{GS(th)}$	As per Table 2	As per Table 2	±20	%
3 to 4	Gate to Source Leakage Current	I_{GSS}	As per Table 2	As per Table 2	±20 or (1) ±100	nA %
5	Drain Current	I_{DSS}	As per Table 2	As per Table 2	±25 or (1) ±100	µA %
6	Drain to Source ON Resistance	$r_{DS(ON)}$	As per Table 2	As per Table 2	±20	%

NOTES
1. Whichever is greater referred to the initial value.

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

NO	CHARACTERISTIC	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+150(+0-5)	°C
2	Drain-Source Voltage	V_{DS}	-80	V
3	Gate-Source Voltage	V_{GS}	0	V
4	Duration	t	72	h

TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

NO	CHARACTERISTIC	SYMBOL	CONDITION	UNIT
1	Junction Temperature	T_j	+140 ± 10 (1)	°C
2	Drain-Source Voltage	V_{DS}	-10	V
3	Gate-Source Voltage	V_{GS}	-1.0 to -16	V
4	Duration	t	240	h

NOTES

1. Using the circuit shown in Figure 5(b), power shall be applied to the device to achieve the specified junction temperature. The junction temperature (T_j) should be determined as follows:
   - T_j = $(P_T)\ (R_{\theta JC}) + T_C$
   - P_T = $(V_{DS})\ (I_D)$
   - $R_{\theta JC}$ = 1.0°C/W
   - T_C = Measured value at the hottest point on case.

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

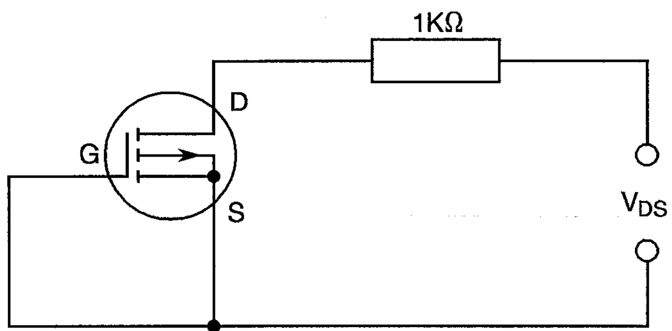
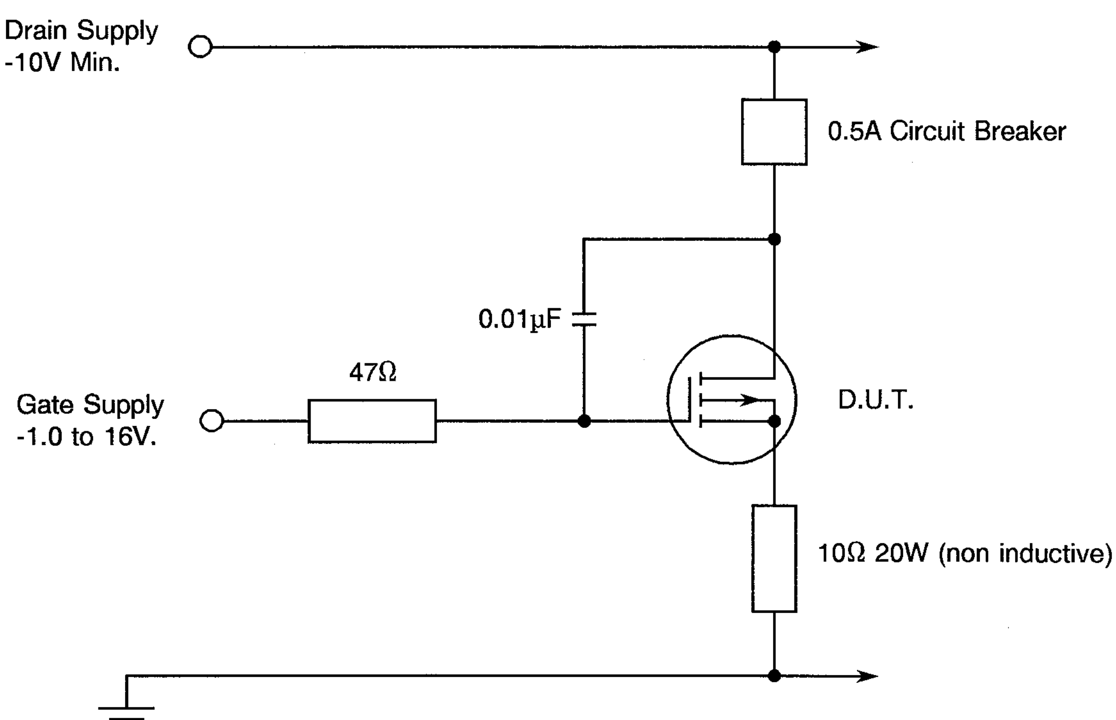


FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 5000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 2 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests

The parameters to be measured at intermediate points and on completion of endurance tests are scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Conditions for Operation Life Tests (Part of Endurance Testing)

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 5000. The conditions for operating life testing shall be the same as specified in Table 5(b) for the burn-in test.

4.8.4 Electrical Circuits for Operating Life Tests

The circuit to be used for performance of the operating life tests shall be the same as shown in Figure 5(b) for burn-in.

4.8.5 Conditions for High Temperature Storage Test (Part of Endurance Testing)

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 5000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

NO	CHARACTERISTIC	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
2	Gate Threshold Voltage	$V_{GS(th)}$	As per Table 2	As per Table 2	-2.0	-4.0	V
3 to 4	Gate to Source Leakage Current	I_{GSS}	As per Table 2	As per Table 2	-	-100	nA
5	Drain Current	I_{DSS}	As per Table 2	As per Table 2	-	-0.25	mA