



Pages 1 to 25

**INTEGRATED CIRCUITS, SILICON MONOLITHIC, HCMOS  
DUAL POSITIVE OR NEGATIVE EDGE  
SCHMITT-RETRIGGERABLE MONOSTABLE  
MULTIVIBRATOR WITH CLEAR AND FULLY BUFFERED  
OUTPUTS**

**BASED ON TYPE 54HC4538**

**ESCC Detail Specification No. 9207/008**

Issue 3	April 2010
---------	------------



**LEGAL DISCLAIMER AND COPYRIGHT**

European Space Agency, Copyright © 2010. All rights reserved.

The European Space Agency disclaims any liability or responsibility, to any person or entity, with respect to any loss or damage caused, or alleged to be caused, directly or indirectly by the use and application of this ESCC publication.

This publication, without the prior permission of the European Space Agency and provided that it is not used for a commercial purpose, may be:

- copied in whole, in any medium, without alteration or modification.
- copied in part, in any medium, provided that the ESCC document identification, comprising the ESCC symbol, document number and document issue, is removed.

**DOCUMENTATION CHANGE NOTICE**

(Refer to <https://escies.org> for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
245, 447, 551	Specification upissued to incorporate editorial and technical changes per DCR.

**TABLE OF CONTENTS**

<b>1.</b>	<b><u>GENERAL</u></b>	<b><u>5</u></b>
1.1	Scope	5
1.2	Applicable Documents	5
1.3	Terms, Definitions, Abbreviations, Symbols and Units	5
1.4	The ESCC Component Number and Component Type Variants	5
1.4.1	The ESCC Component Number	5
1.4.2	Component Type Variants	5
1.5	Maximum Ratings	6
1.6	Handling Precautions	6
1.7	Physical Dimensions and Terminal Identification	6
1.7.1	Flat Package (FP) - 16 Pin	7
1.7.2	Dual-in-line Package (DIP) - 16 Pin	8
1.7.3	Chip Carrier Package (CCP) - 20 Terminal	9
1.7.4	Small Outline Ceramic Package (SO) - 16 Pin	11
1.7.5	Notes to Physical Dimensions and Terminal Identification	12
1.8	Functional Diagram	12
1.9	Pin Assignment	13
1.10	Truth Table and Timing Chart	13
1.11	Protection Networks	14
<b>2.</b>	<b><u>REQUIREMENTS</u></b>	<b><u>15</u></b>
2.1	General	15
2.1.1	Deviations from the Generic Specification	15
2.2	Marking	15
2.3	Electrical Measurements at Room, High and Low Temperatures	15
2.3.1	Room Temperature Electrical Measurements	15
2.3.2	High and Low Temperatures Electrical Measurements	18
2.3.3	Notes to Electrical Measurement Tables	20
2.4	Parameter Drift Values	21
2.5	Intermediate and End-Point Electrical Measurements	22
2.6	High Temperature Reverse Bias Burn-in Conditions	23
2.6.1	N-Channel HTRB	23
2.6.2	P-Channel HTRB	23
2.7	Power Burn-in Conditions	24
2.8	Operating Life Conditions	24
APPENDIX 'A'		25

## 1. GENERAL

### 1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

### 1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

- (a) ESCC Generic Specification No. 9000.
- (b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

### 1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

### 1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

#### 1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 920700801

- Detail Specification Reference: 9207008
- Component Type Variant Number: 01 (as required)

#### 1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and /or Finish	Weight max g
01	54HC4538	FP	G2	0.7
02	54HC4538	FP	G4	0.7
05	54HC4538	CCP	2	0.6
10	54HC4538	DIP	G2	2.2
11	54HC4538	DIP	G4	2.2
12	54HC4538	SO	G2	0.7
13	54HC4538	SO	G4	0.7

The terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	$V_{DD}$	-0.5 to 7	V	Note 1
Input Voltage	$V_{IN}$	-0.5 to $V_{DD} + 0.5$	V	Notes 1, 2
Output Voltage	$V_{OUT}$	-0.5 to $V_{DD} + 0.5$	V	Notes 1, 3
Device Power Dissipation (Continuous)	$P_D$	300	mW	Note 4
Supply Current	$I_{DDop}$	50	mA	
Operating Temperature Range	$T_{op}$	-55 to +125	°C	$T_{amb}$
Storage Temperature Range	$T_{stg}$	-65 to +150	°C	
Soldering Temperature For FP, DIP and SO For CCP	$T_{sol}$	+265 +245	°C	Note 5 Note 6
External Resistor	$R_{ext}$	$V_{DD}=2V$ : 5k to 1M $V_{DD}\geq 3V$ : 1k to 1M	$\Omega$	FP, DIP, SO Pins: 2,14 CCP Pins: 3,18

**NOTES:**

1. Device is functional for  $2V \leq V_{DD} \leq 6V$ .
2. Input current limited to  $I_{IC} = \pm 20mA$ .
3. Output current limited to  $I_{OUT} = \pm 25mA$ .
4. The maximum device dissipation is determined by  $I_{DDop} \max (50mA) \times 6V$ .
5. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.
6. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 2500 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

Consolidated Notes are given following the case drawings and dimensions.

1.7.1 Flat Package (FP) - 16 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	6.75	7.06	
B	9.76	10.14	
C	1.49	1.95	
D	0.1	0.15	5
E	8.76	9.01	
F	1.27 BSC		3, 6
G	0.38	0.48	5
H	6	-	5
L	18.75	22	
M	0.33	0.43	
N	4.32 TYPICAL		

1.7.2 Dual-in-line Package (DIP) - 16 Pin

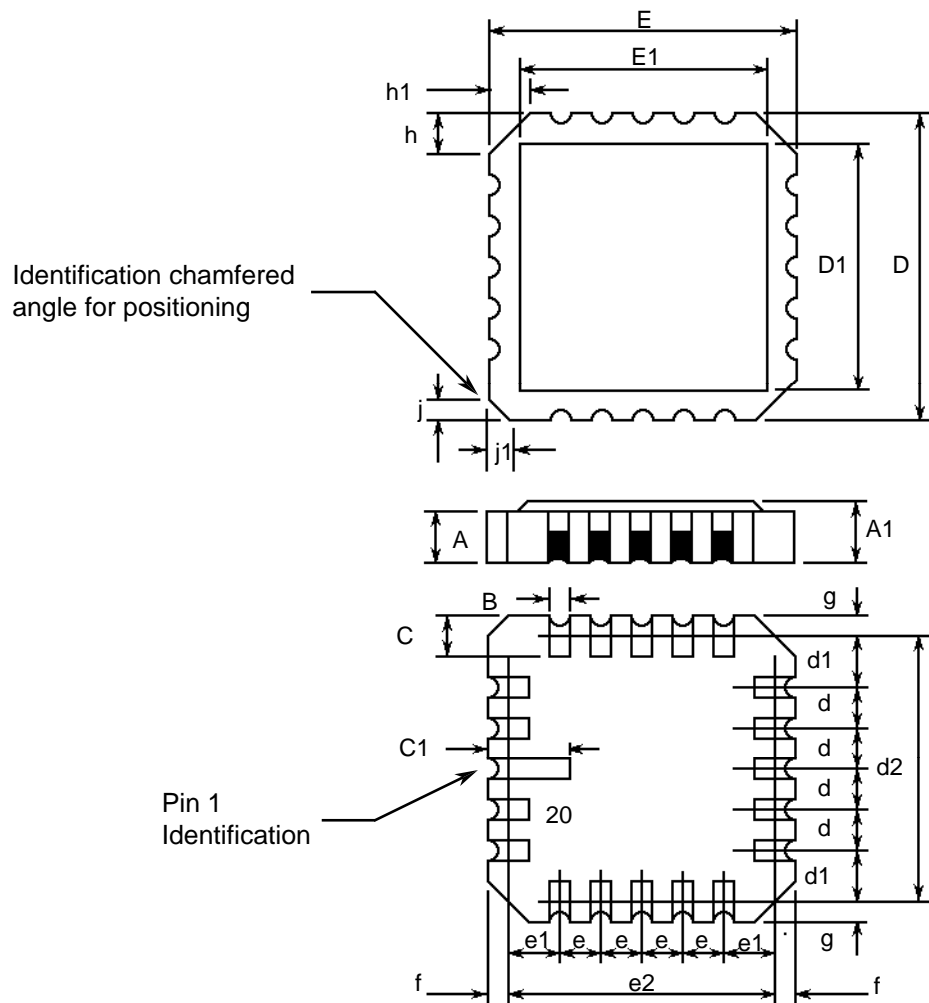


Symbols	Dimensions mm		Notes
	Min	Max	
A	2.1	2.71	
a1	3	3.7	
a2	0.63	1.14	2
B	1.82	2.39	
b	0.4	0.5	5
b1	1.14	1.5	5
c	0.2	0.3	5
D	20.06	20.58	
E	7.36	7.87	
e	2.54 BSC		4, 6
e1	17.65	17.9	
e2	7.62	8.12	
F	7.29	7.7	
l	-	3.83	



Symbols	Dimensions mm		Notes
	Min	Max	
K	10.9	12.1	

1.7.3 Chip Carrier Package (CCP) - 20 Terminal



Symbols	Dimensions mm		Notes
	Min	Max	
A	1.14	1.95	
A1	1.63	2.36	
B	0.55	0.72	5
C	1.06	1.47	5
C1	1.91	2.41	

Symbols	Dimensions mm		Notes
	Min	Max	
D	8.67	9.09	
D1	7.21	7.52	
d, d1	1.27 BSC		3
d2	7.62 BSC		
E	8.67	9.09	
E1	7.21	7.52	
e, e1	1.27 BSC		3
e2	7.62 BSC		
f, g	-	0.76	
h, h1	1.01 TYPICAL		8
j, j1	0.51 TYPICAL		7

1.7.4 Small Outline Ceramic Package (SO) - 16 Pin



Symbols	Dimensions mm		Notes
	Min	Max	
A	6.75	7.06	
B	9.76	10.14	
C	1.49	1.95	
D	0.1	0.15	5
E	8.76	9.01	
F	1.27 BSC		3, 6
G	0.38	0.48	5
H	0.6	0.9	5

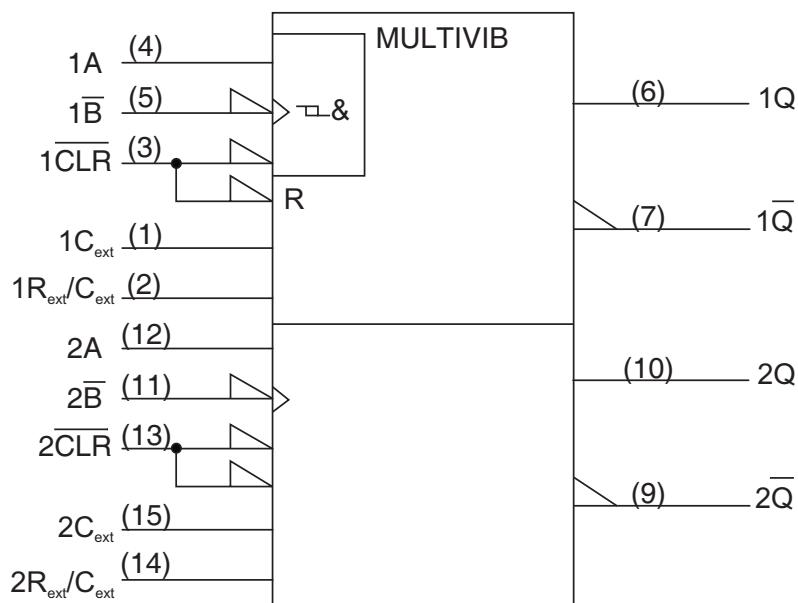
Symbols	Dimensions mm		Notes
	Min	Max	
K	9 TYPICAL		
L	10	10.65	
M	0.33	0.43	
N	4.31 TYPICAL		

1.7.5 Notes to Physical Dimensions and Terminal Identification

1. Index area; a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown.
2. The dimension shall be measured from the seating plane to the base plane.
3. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within  $\pm 0.13\text{mm}$  of its true longitudinal position relative to Pin 1 and the highest pin number.
4. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within  $\pm 0.25\text{mm}$  of its true longitudinal position relative to Pin 1 and the highest pin number.
5. All terminals.
6. 14 spaces.
7. Index corner only - 2 dimensions.
8. 3 non-index corners - 6 dimensions.
9. For all pins, either pin shape may be supplied.

1.8 FUNCTIONAL DIAGRAM

Pin numbers relate to FP, DIP and SO packages only.



1.9 PIN ASSIGNMENT

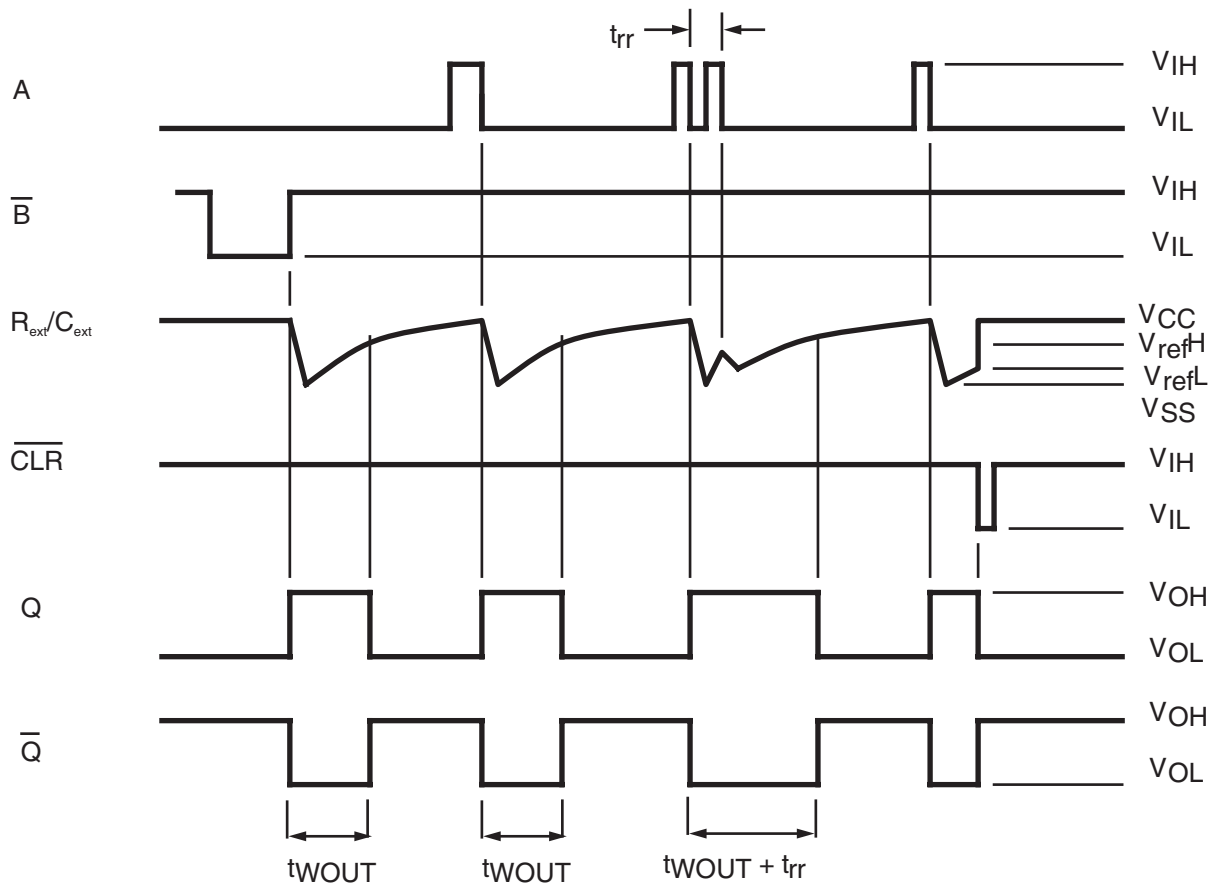
Pin	Function		Pin	Function	
	FP, DIP and SO	CCP		FP, DIP and SO	CCP
1	1C <sub>ext</sub>	-	11	2 $\bar{B}$ Input	-
2	1R <sub>ext</sub> /C <sub>ext</sub>	1C <sub>ext</sub>	12	2A Input	2 $\bar{Q}$ Output
3	1 $\bar{CLR}$ Input (Clear)	1R <sub>ext</sub> /C <sub>ext</sub>	13	2 $\bar{CLR}$ Input (Clear)	2Q Output
4	1A Input	1 $\bar{CLR}$ Input (Clear)	14	2R <sub>ext</sub> /C <sub>ext</sub>	2 $\bar{B}$ Input
5	1 $\bar{B}$ Input	1A Input	15	2C <sub>ext</sub>	2A Input
6	1Q Output	-	16	V <sub>DD</sub>	-
7	1 $\bar{Q}$ Output	1 $\bar{B}$ Input	17	-	2 $\bar{CLR}$ Input (Clear)
8	V <sub>SS</sub>	1Q Output	18	-	2R <sub>ext</sub> /C <sub>ext</sub>
9	2 $\bar{Q}$ Output	1 $\bar{Q}$ Output	19	-	2C <sub>ext</sub>
10	2Q Output	V <sub>SS</sub>	20	-	V <sub>DD</sub>

1.10 TRUTH TABLE AND TIMING CHART

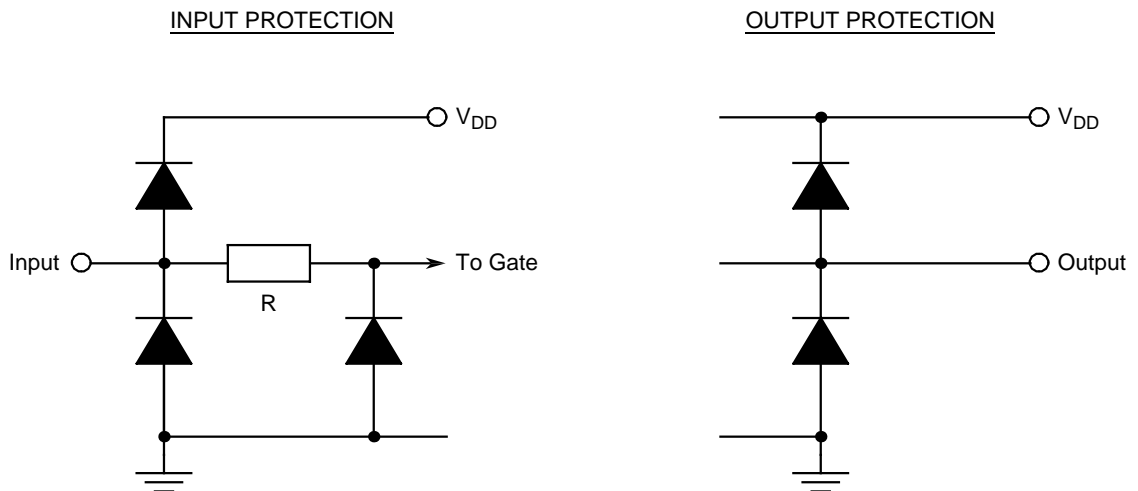
1. Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant.
2.  $\uparrow$  = Transition, Low to High;  $\downarrow$  = Transition, High to Low.
3. + = High level pulse for time period determined by R<sub>ext</sub>, C<sub>ext</sub>.
4. - = Low level pulse for time period determined by R<sub>ext</sub>, C<sub>ext</sub>.

EACH MULTIVIBRATOR

INPUTS			OUTPUTS	
A	$\bar{B}$	$\bar{CLR}$	Q	$\bar{Q}$
X	X	L	L	H
H	X	H	L	H
X	L	H	L	H
L	$\downarrow$	H	+	-
$\uparrow$	H	H	+	-



1.11 PROTECTION NETWORKS



**2. REQUIREMENTS**

**2.1 GENERAL**

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

**2.1.1 Deviations from the Generic Specification**

None.

**2.2 MARKING**

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

- (a) Terminal identification.
- (b) The ESCC qualified components symbol (for ESCC qualified components only).
- (c) The ESCC Component Number.
- (d) Traceability information.

**2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES**

Electrical measurements shall be performed at room, high and low temperatures. Consolidated Notes are given after the tables.

**2.3.1 Room Temperature Electrical Measurements**

The measurements shall be performed at  $T_{amb}=+22 \pm 3^{\circ}C$ .

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table without Load $V_{IL}=0.3V, V_{IH}=1.5V$ $V_{DD}=2V, V_{SS}=0V$ $t_r=t_f < 1\mu s$ (CLR only) Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table without Load $V_{IL}=0.9V, V_{IH}=3.15V$ $V_{DD}=4.5V, V_{SS}=0V$ $t_r=t_f < 500ns$ (CLR only) Note 2	-	-	-

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 3	-	3014	Verify Truth Table without Load $V_{IL}=1.2V, V_{IH}=4.2V$ $V_{DD}=6V, V_{SS}=0V$ $t_r=t_f < 400ns$ (CLR only) Note 2	-	-	-
Quiescent Current	$I_{DD}$	3005	$V_{IL}=0V, V_{IH}=6V$ $V_{DD}=6V, V_{SS}=0V$ All Outputs Open Note 3	-	400	nA
Active Supply Current 1	$I_{DD(S1)}$	3005	$V_{IL}=0V, V_{IH}=2V,$ $V_{DD}=2V, V_{SS}=0V$ All Outputs Open Note 3	-	200	$\mu A$
Active Supply Current 2	$I_{DD(S2)}$	3005	$V_{IL}=0V, V_{IH}=4.5V,$ $V_{DD}=4.5V, V_{SS}=0V$ All Outputs Open Note 3	-	600	$\mu A$
Active Supply Current 3	$I_{DD(S3)}$	3005	$V_{IL}=0V, V_{IH}=6V,$ $V_{DD}=6V, V_{SS}=0V$ All Outputs Open Note 3	-	1	mA
Low Level Input Current 1 (A, $\bar{B}$ , $\overline{CLR}$ )	$I_{IL1}$	3009	$V_{IN}$ (Under Test)=0V $V_{IN}$ (Remaining Inputs)=6V $V_{DD}=6V, V_{SS}=0V$	-	-50	nA
Low Level Input Current 2 ( $R_{ext}/C_{ext}$ )	$I_{IL2}$	3009	$V_{IN}$ (Under Test)=0V $V_{IN}$ (Remaining Inputs)=6V $V_{DD}=6V, V_{SS}=0V$	-	-500	nA
High Level Input Current 1 (A, $\bar{B}$ , $\overline{CLR}$ )	$I_{IH1}$	3010	$V_{IN}$ (Under Test)=6V $V_{IN}$ (Remaining Inputs)=0V $V_{DD}=6V, V_{SS}=0V$	-	50	nA
High Level Input Current 2 ( $R_{ext}/C_{ext}$ )	$I_{IH2}$	3010	$V_{IN}$ (Under Test)=6V $V_{IN}$ (Remaining Inputs)=0V $V_{DD}=6V, V_{SS}=0V$	-	500	nA
Low Level Output Voltage 1	$V_{OL1}$	3007	$V_{IL}=0.3V, V_{IH}=1.5V,$ $I_{OL}=20\mu A$ $V_{DD}=2V, V_{SS}=0V$	-	100	mV
Low Level Output Voltage 2	$V_{OL2}$	3007	$V_{IL}=0.9V, V_{IH}=3.15V,$ $I_{OL}=20\mu A$ $V_{DD}=4.5V, V_{SS}=0V$	-	100	mV



Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Low Level Output Voltage 3	$V_{OL3}$	3007	$V_{IL}=1.2V, V_{IH}=4.2V, I_{OL}=20\mu A, V_{DD}=6V, V_{SS}=0V$	-	100	mV
Low Level Output Voltage 4	$V_{OL4}$	3007	$V_{IL}=0.9V, V_{IH}=3.15V, I_{OL}=4mA, V_{DD}=4.5V, V_{SS}=0V$	-	260	mV
Low Level Output Voltage 5	$V_{OL5}$	3007	$V_{IL}=1.2V, V_{IH}=4.2V, I_{OL}=5.2mA, V_{DD}=6V, V_{SS}=0V$	-	260	mV
High Level Output Voltage 1	$V_{OH1}$	3006	$V_{IL}=0.3V, V_{IH}=1.5V, I_{OH}=-20\mu A, V_{DD}=2V, V_{SS}=0V$	1.9	-	V
High Level Output Voltage 2	$V_{OH2}$	3006	$V_{IL}=0.9V, V_{IH}=3.15V, I_{OH}=-20\mu A, V_{DD}=4.5V, V_{SS}=0V$	4.4	-	V
High Level Output Voltage 3	$V_{OH3}$	3006	$V_{IL}=1.2V, V_{IH}=4.2V, I_{OH}=-20\mu A, V_{DD}=6V, V_{SS}=0V$	5.9	-	V
High Level Output Voltage 4	$V_{OH4}$	3006	$V_{IL}=0.9V, V_{IH}=3.15V, I_{OH}=-4mA, V_{DD}=4.5V, V_{SS}=0V$	3.98	-	V
High Level Output Voltage 5	$V_{OH5}$	3006	$V_{IL}=1.2V, V_{IH}=4.2V, I_{OH}=-5.2mA, V_{DD}=6V, V_{SS}=0V$	5.48	-	V
Threshold Voltage N-Channel	$V_{THN}$	-	$\overline{1CLR}$ Input at Ground All Other Inputs: $V_{IN}=5V, V_{DD}=5V, I_{SS}=-10\mu A$	-0.45	-1.45	V
Threshold Voltage P-Channel	$V_{THP}$	-	$\overline{1CLR}$ Input at Ground All Other Inputs: $V_{IN}=-5V, V_{SS}=-5V, I_{DD}=10\mu A$	0.45	1.35	V
Input Clamp Voltage 1, to $V_{SS}$ (A, $\overline{B}$ , $\overline{CLR}$ )	$V_{IC1}$	-	$I_{IN}$ (Under Test) = $-100\mu A, V_{DD}=\text{Open}, V_{SS}=0V$ All Other Pins Open	-400	-900	mV
Input Clamp Voltage 2, to $V_{DD}$ (A, $\overline{B}$ , $\overline{CLR}$ )	$V_{IC2}$	-	$I_{IN}$ (Under Test) = $100\mu A, V_{DD}=0V, V_{SS}=\text{Open}$ All Other Pins Open	400	900	mV
Input Capacitance (A, $\overline{B}$ , $\overline{CLR}$ )	$C_{IN}$	3012	$V_{IN}$ (Not Under Test) = $0V, V_{DD}=V_{SS}=0V, f = 100\text{ kHz to }1\text{ MHz}$ Note 4	-	10	pF

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Propagation Delay Low to High 1, A to Q	$t_{PLH1}$	3003	$V_{IN}$ (Under Test) =Pulse Generator $V_{IN}$ (Remaining Inputs)=Truth Table $V_{IL}=0V, V_{IH}=4.5V$ $V_{DD}=4.5V, V_{SS}=0V$ Note 5	-	50	ns
Propagation Delay High to Low 1, A to $\bar{Q}$	$t_{PHL1}$	3003	$V_{IN}$ (Under Test) =Pulse Generator $V_{IN}$ (Remaining Inputs)=Truth Table $V_{IL}=0V, V_{IH}=4.5V$ $V_{DD}=4.5V, V_{SS}=0V$ Note 5	-	50	ns
Propagation Delay Low to High 2, $\overline{CLR}$ to $\bar{Q}$	$t_{PLH2}$	3003	$V_{IN}$ (Under Test) =Pulse Generator $V_{IN}$ (Remaining Inputs)=Truth Table $V_{IL}=0V, V_{IH}=4.5V$ $V_{DD}=4.5V, V_{SS}=0V$ Note 5	-	39	ns
Propagation Delay High to Low 2, $\overline{CLR}$ to Q	$t_{PHL2}$	3003	$V_{IN}$ (Under Test) =Pulse Generator $V_{IN}$ (Remaining Inputs)=Truth Table $V_{IL}=0V, V_{IH}=4.5V$ $V_{DD}=4.5V, V_{SS}=0V$ Note 5	-	39	ns
Transition Time Low to High, Q, $\bar{Q}$	$t_{TLH}$	3004	$V_{IN}$ (Under Test)=Pulse Generator $V_{IN}$ (Remaining Inputs)=Truth Table $V_{IL}=0V, V_{IH}=4.5V$ $V_{DD}=4.5V, V_{SS}=0V$ Note 5	-	15	ns
Transition Time High to Low, Q, $\bar{Q}$	$t_{THL}$	3004	$V_{IN}$ (Under Test)=Pulse Generator $V_{IN}$ (Remaining Inputs)=Truth Table $V_{IL}=0V, V_{IH}=4.5V$ $V_{DD}=4.5V, V_{SS}=0V$ Note 5	-	15	ns

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at  $T_{amb}=+125 (+0 -5) ^\circ C$  and  $T_{amb}=- 55(+5-0)^\circ C$ .

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table without Load $V_{IL}=0.3V, V_{IH}=1.5V$ $V_{DD}=2V, V_{SS}=0V$ $t_r=t_f < 1\mu s$ (CLR only) Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table without Load $V_{IL}=0.9V, V_{IH}=3.15V$ $V_{DD}=4.5V, V_{SS}=0V$ $t_r=t_f < 500ns$ (CLR only) Note 2	-	-	-
Functional Test 3	-	3014	Verify Truth Table without Load $V_{IL}=1.2V, V_{IH}=4.2V$ $V_{DD}=6V, V_{SS}=0V$ $t_r=t_f < 400ns$ (CLR only) Note 2	-	-	-
Quiescent Current	$I_{DD}$	3005	$V_{IL}=0V, V_{IH}=6V$ $V_{DD}=6V, V_{SS}=0V$ All Outputs Open Note 3	-	8	$\mu A$
Active Supply Current 1	$I_{DD(S1)}$	3005	$V_{IL}=0V, V_{IH}=2V,$ $V_{DD}=2V, V_{SS}=0V$ All Outputs Open Note 3	-	350	$\mu A$
Active Supply Current 2	$I_{DD(S2)}$	3005	$V_{IL}=0V, V_{IH}=4.5V,$ $V_{DD}=4.5V, V_{SS}=0V$ All Outputs Open Note 3	-	1	mA
Active Supply Current 3	$I_{DD(S3)}$	3005	$V_{IL}=0V, V_{IH}=6V,$ $V_{DD}=6V, V_{SS}=0V$ All Outputs Open Note 3	-	1.7	mA
Low Level Input Current 1 (A, $\bar{B}$ , $\overline{CLR}$ )	$I_{IL1}$	3009	$V_{IN}$ (Under Test)=0V $V_{IN}$ (Remaining Inputs)=6V $V_{DD}=6V, V_{SS}=0V$	-	-1	$\mu A$
Low Level Input Current 2 ( $R_{ext}/C_{ext}$ )	$I_{IL2}$	3009	$V_{IN}$ (Under Test)=0V $V_{IN}$ (Remaining Inputs)=6V $V_{DD}=6V, V_{SS}=0V$	-	-10	$\mu A$
High Level Input Current 1 (A, $\bar{B}$ , $\overline{CLR}$ )	$I_{IH1}$	3010	$V_{IN}$ (Under Test)=6V $V_{IN}$ (Remaining Inputs)=0V $V_{DD}=6V, V_{SS}=0V$	-	1	$\mu A$

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
High Level Input Current 2 (R <sub>ext</sub> /C <sub>ext</sub> )	I <sub>IH2</sub>	3010	V <sub>IN</sub> (Under Test)=6V V <sub>IN</sub> (Remaining Inputs)=0V V <sub>DD</sub> =6V, V <sub>SS</sub> =0V	-	10	μA
Low Level Output Voltage 1	V <sub>OL1</sub>	3007	V <sub>IL</sub> =0.3V, V <sub>IH</sub> =1.5V, I <sub>OL</sub> =20μA V <sub>DD</sub> =2V, V <sub>SS</sub> =0V	-	100	mV
Low Level Output Voltage 2	V <sub>OL2</sub>	3007	V <sub>IL</sub> =0.9V, V <sub>IH</sub> =3.15V, I <sub>OL</sub> =20μA V <sub>DD</sub> =4.5V, V <sub>SS</sub> =0V	-	100	mV
Low Level Output Voltage 3	V <sub>OL3</sub>	3007	V <sub>IL</sub> =1.2V, V <sub>IH</sub> =4.2V, I <sub>OL</sub> =20μA V <sub>DD</sub> =6V, V <sub>SS</sub> =0V	-	100	mV
Low Level Output Voltage 4	V <sub>OL4</sub>	3007	V <sub>IL</sub> =0.9V, V <sub>IH</sub> =3.15V, I <sub>OL</sub> =4mA V <sub>DD</sub> =4.5V, V <sub>SS</sub> =0V	-	260	mV
Low Level Output Voltage 5	V <sub>OL5</sub>	3007	V <sub>IL</sub> =1.2V, V <sub>IH</sub> =4.2V, I <sub>OL</sub> =5.2mA V <sub>DD</sub> =6V, V <sub>SS</sub> =0V	-	260	mV
High Level Output Voltage 1	V <sub>OH1</sub>	3006	V <sub>IL</sub> =0.3V, V <sub>IH</sub> =1.5V, I <sub>OH</sub> =-20μA V <sub>DD</sub> =2V, V <sub>SS</sub> =0V	1.9	-	V
High Level Output Voltage 2	V <sub>OH2</sub>	3006	V <sub>IL</sub> =0.9V, V <sub>IH</sub> =3.15V, I <sub>OH</sub> =-20μA V <sub>DD</sub> =4.5V, V <sub>SS</sub> =0V	4.4	-	V
High Level Output Voltage 3	V <sub>OH3</sub>	3006	V <sub>IL</sub> =1.2V, V <sub>IH</sub> =4.2V, I <sub>OH</sub> =-20μA V <sub>DD</sub> =6V, V <sub>SS</sub> =0V	5.9	-	V
High Level Output Voltage 4	V <sub>OH4</sub>	3006	V <sub>IL</sub> =0.9V, V <sub>IH</sub> =3.15V, I <sub>OH</sub> =-4mA V <sub>DD</sub> =4.5V, V <sub>SS</sub> =0V	3.7	-	V
High Level Output Voltage 5	V <sub>OH5</sub>	3006	V <sub>IL</sub> =1.2V, V <sub>IH</sub> =4.2V, I <sub>OH</sub> =-5.2mA V <sub>DD</sub> =6V, V <sub>SS</sub> =0V	5.2	-	V
Input Clamp Voltage 1, to V <sub>SS</sub> (A, $\bar{B}$ , $\overline{CLR}$ )	V <sub>IC1</sub>	-	I <sub>IN</sub> (Under Test)= -100μA V <sub>DD</sub> =Open, V <sub>SS</sub> =0V All Other Pins Open	-0.1	-1.2	mV
Input Clamp Voltage 2, to V <sub>DD</sub> (A, $\bar{B}$ , $\overline{CLR}$ )	V <sub>IC2</sub>	-	I <sub>IN</sub> (Under Test)= 100μA V <sub>DD</sub> =0V, V <sub>SS</sub> =Open All Other Pins Open	0.1	1.2	V

2.3.3

Notes to Electrical Measurement Tables

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic, inputs not

- under test shall be  $V_{IN} = V_{SS}$  or  $V_{DD}$  and outputs not under test shall be open.
2. Functional tests shall be performed with  $f = 10$  kHz (min). The maximum time to output comparator strobe =  $30\mu s$ .
  3. Quiescent and Active Supply Current shall be tested using the following input conditions:
    - Quiescent Current
    - (a) All Inputs =  $V_{IL}$
    - (b) Inputs  $1C_{ext} = 2C_{ext} = V_{IL}$  ; All other inputs =  $V_{IH}$
    - Active Supply Current
    - Each gate shall be tested separately. For gate not under test all inputs =  $V_{IL}$
    - (a)  $R_{ext}/C_{ext} = V_{DD}/2$  ; Inputs  $A = \bar{B} = \bar{CLR} = V_{IL}$
    - (b)  $R_{ext}/C_{ext} = V_{DD}/2$  ; Input  $\bar{CLR} = V_{IH}$  ; Inputs  $A = \bar{B} = V_{IL}$
    - (c)  $R_{ext}/C_{ext} = V_{DD}/2$  ; Inputs  $\bar{CLR} = \bar{B} = V_{IH}$  ; Input  $A = \uparrow$  (transition, Low to High)
  4. Guaranteed but not tested.
  5. Measurements shall be performed as a go-no-go test on a 100% basis. Read and record measurements shall be performed on a sample of 5 components.  
 The pulse generator shall have the following characteristics:  
 $V_{GEN} = 0$  to  $V_{DD}$ ;  $f_{GEN} = 1$  MHz minimum;  $t_r$  and  $t_f \leq 6$  ns (10% to 90%); duty cycle = 50%;  $Z_{out} = 50\Omega$ .  
 Output load capacitance  $C_L = 50pF \pm 5\%$  including scope probe, wiring and stray capacitance without component in the test fixture and output load resistance  $R_L = 1k\Omega \pm 5\%$ .  
 Propagation delay shall be measured referenced to the 50% input and output voltages.  
 Transition time shall be measured referenced to the 10% and 90% output voltage.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at  $T_{amb} = +22 \pm 3^\circ C$ .

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values ( $\Delta$ ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value $\Delta$	Absolute		
			Min	Max	
Quiescent Current	$I_{DD}$	$\pm 120$	-	400	nA
Active Supply Current 2	$I_{DD(S2)}$	$\pm 180$	-	600	$\mu A$

Characteristics	Symbols	Limits			Units
		Drift Value $\Delta$	Absolute		
			Min	Max	
Low Level Input Current 1	$I_{IL1}$	$\pm 20$	-	-50	nA
Low Level Input Current 2	$I_{IL2}$	$\pm 150$	-	-500	nA
High Level Input Current 1	$I_{IH1}$	$\pm 20$	-	50	nA
High Level Input Current 2	$I_{IH2}$	$\pm 150$	-	500	nA
Low Level Output Voltage 4	$V_{OL4}$	$\pm 26$	-	260	mV
High Level Output Voltage 4	$V_{OH4}$	$\pm 0.2$	3.98	-	V
Threshold Voltage N-Channel	$V_{THN}$	$\pm 0.3$	-0.45	-1.45	V
Threshold Voltage P-Channel	$V_{THP}$	$\pm 0.3$	0.45	1.35	V

**NOTES:**

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5

**INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS**

Unless otherwise specified, the measurements shall be performed at  $T_{amb} = +22 \pm 3^{\circ}C$ .

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values ( $\Delta$ ) shall not be exceeded for each characteristic where specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value $\Delta$	Absolute		
			Min	Max	
Functional Test 1	-	-	-	-	-
Functional Test 2	-	-	-	-	-
Functional Test 3	-	-	-	-	-
Quiescent Current	$I_{DD}$	$\pm 120$	-	400	nA
Active Supply Current 1	$I_{DD(S1)}$	$\pm 60$	-	200	$\mu A$
Active Supply Current 2	$I_{DD(S2)}$	$\pm 180$	-	600	$\mu A$
Active Supply Current 3	$I_{DD(S3)}$	$\pm 0.3$	-	1	mA

Characteristics	Symbols	Limits			Units
		Drift Value $\Delta$	Absolute		
			Min	Max	
Low Level Input Current 1	$I_{IL1}$	$\pm 20$	-	-50	nA
Low Level Input Current 2	$I_{IL2}$	$\pm 200$	-	-500	nA
High Level Input Current 1	$I_{IH1}$	$\pm 20$	-	50	nA
High Level Input Current 2	$I_{IH2}$	$\pm 200$	-	500	nA
Low Level Output Voltage 4	$V_{OL4}$	$\pm 26$	-	260	mV
Low Level Output Voltage 5	$V_{OL5}$	$\pm 26$	-	260	mV
High Level Output Voltage 4	$V_{OH4}$	$\pm 0.2$	3.98	-	V
High Level Output Voltage 5	$V_{OH5}$	$\pm 0.2$	5.48	-	V
Threshold Voltage N-Channel	$V_{THN}$	$\pm 0.3$	-0.45	-1.45	V
Threshold Voltage P-Channel	$V_{THP}$	$\pm 0.3$	0.45	1.35	V

**NOTES:**

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic.
2. The drift values ( $\Delta$ ) are applicable to the Operating Life test only.

2.6 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

2.6.1 N-Channel HTRB

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	$T_{amb}$	+125 (+0 -5)	$^{\circ}C$
Outputs 1Q, 1 $\bar{Q}$ , 2Q, 2 $\bar{Q}$	$V_{OUT}$	Open or $V_{SS}$	V
Inputs A, $\bar{B}$ , $\overline{CLR}$ , $R_{ext}/C_{ext}$ (all gates)	$V_{IN}$	$V_{SS}$	V
Inputs 1 $C_{ext}$ , 2 $C_{ext}$	$V_{IN}$	Open	V
Positive Supply Voltage	$V_{DD}$	6 (+0 -0.5)	V
Negative Supply Voltage	$V_{SS}$	0	V
Duration	t	72	Hours

**NOTES:**

1. Input Protection Resistor = 680 $\Omega$  min to 47k $\Omega$  max.
2. Output Load = 1k $\Omega$  min to 10k $\Omega$  max.

2.6.2 P-Channel HTRB

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	$T_{amb}$	+125 (+0 -5)	$^{\circ}C$

Characteristics	Symbols	Test Conditions	Units
Outputs 1Q, 1 $\bar{Q}$ , 2Q, 2 $\bar{Q}$	V <sub>OUT</sub>	Open or V <sub>DD</sub>	V
Inputs A, $\bar{B}$ , $\overline{\text{CLR}}$ , R <sub>ext</sub> /C <sub>ext</sub> (all gates)	V <sub>IN</sub>	V <sub>DD</sub>	V
Inputs 1C <sub>ext</sub> , 2C <sub>ext</sub>	V <sub>IN</sub>	Open	V
Positive Supply Voltage	V <sub>DD</sub>	6 (+0 -0.5)	V
Negative Supply Voltage	V <sub>SS</sub>	0	V
Duration	t	72	Hours

**NOTES:**

1. Input Protection Resistor = 680Ω min to 47kΩ max.
2. Output Load = 1kΩ min to 10kΩ max.

2.7 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T <sub>amb</sub>	+125 (+0 -5)	°C
Outputs 1Q, 1 $\bar{Q}$ , 2Q, 2 $\bar{Q}$	V <sub>OUT</sub>	V <sub>DD</sub>	V
Inputs 1R <sub>ext</sub> /C <sub>ext</sub> , 2R <sub>ext</sub> /C <sub>ext</sub>	V <sub>IN</sub>	V <sub>DD</sub>	V
Inputs 1A, 2 $\bar{B}$	V <sub>IN</sub>	V <sub>GEN1</sub>	V
Inputs 1 $\bar{B}$ , 2A	V <sub>IN</sub>	V <sub>GEN2</sub>	V
Input 1 $\overline{\text{CLR}}$	V <sub>IN</sub>	V <sub>GEN3</sub>	V
Input 2 $\overline{\text{CLR}}$	V <sub>IN</sub>	V <sub>GEN4</sub>	V
Inputs 1C <sub>ext</sub> , 2C <sub>ext</sub>	V <sub>IN</sub>	Open	V
Pulse Voltage	V <sub>GEN</sub>	0V to V <sub>DD</sub>	V
Pulse Frequency Square Wave	f <sub>GEN1</sub> f <sub>GEN2</sub>	100k ± 10% 20k ± 10% 50 ± 15% Duty Cycle t <sub>r</sub> =t <sub>f</sub> ≤400ns	Hz
Pulse Square Wave	GEN3 GEN4	One 5μs negative pulse each 35ms One 5μs negative pulse each 35ms t <sub>r</sub> = t <sub>f</sub> ≤ 400ns	-
Positive Supply Voltage	V <sub>DD</sub>	6 (+0 -0.5)	V
Negative Supply Voltage	V <sub>SS</sub>	0	V

**NOTES:**

1. Input Protection Resistor = 680Ω min to 47kΩ max.
2. Output Load = 1kΩ min to 10kΩ max.

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.



**APPENDIX 'A'**

**AGREED DEVIATIONS FOR STMICROELECTRONICS (F)**

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
<p>Deviations from Screening Tests - Chart F3</p>	<p>External Visual Inspection: The criteria applicable to chip-outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a).</p> <p>High Temperature Reverse Bias Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.</p> <p>Power Burn-in test is performed using STMicroelectronics Specification Ref: 0019255.</p> <p>Solderability is not applicable unless specifically stipulated in the Purchase Order.</p>
<p>Deviations from Qualification and Periodic Tests - Chart F4</p>	<p>External Visual Inspection: The criteria applicable to chip-outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a).</p> <p>Operating Life: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.</p>
<p>Deviations from High and Low Temperatures Electrical Measurements</p>	<p>High and Low Temperatures Electrical Measurements may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes High and Low Temperatures Electrical Measurements per the Detail Specification.</p> <p>A summary of the pilot lot testing shall be provided if required by the Purchase Order.</p>
<p>Deviations from Room Temperature Electrical Measurements</p>	<p>All AC characteristics (Capacitance and Timings) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the Detail Specification.</p> <p>A summary of the pilot lot testing shall be provided if required by the Purchase Order.</p>