INTEGRATED CIRCUITS, SILICON MONOLITHIC,

QUAD EIA-422/423 LINE RECEIVER WITH

3-STATE OUTPUTS,

BASED ON TYPE AM26LS32

ESCC Detail Specification No. 9403/003

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APPENDICES (Applicable to specific Manufacturers only)

None.

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, low power, Quad EIA-422/423 Line Receiver with 3-State Outputs, based on Type AM26LS32. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

As per Figure 1.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

As per Figure 3(b).

1.8 CIRCUIT SCHEMATIC

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

TABLE 1(a) - TYPE VARIANTS

VARIANT	BASED ON TYPE	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
01	AM26LS32	DIL	2(a)	G4
02	AM26LS32	FLAT	2(b)	G4
03	AM26LS32	DIL	2(c)	G4
04	AM26LS32	CHIP CARRIER	2(d)	7
05	AM26LS32	CHIP CARRIER	2(d)	4

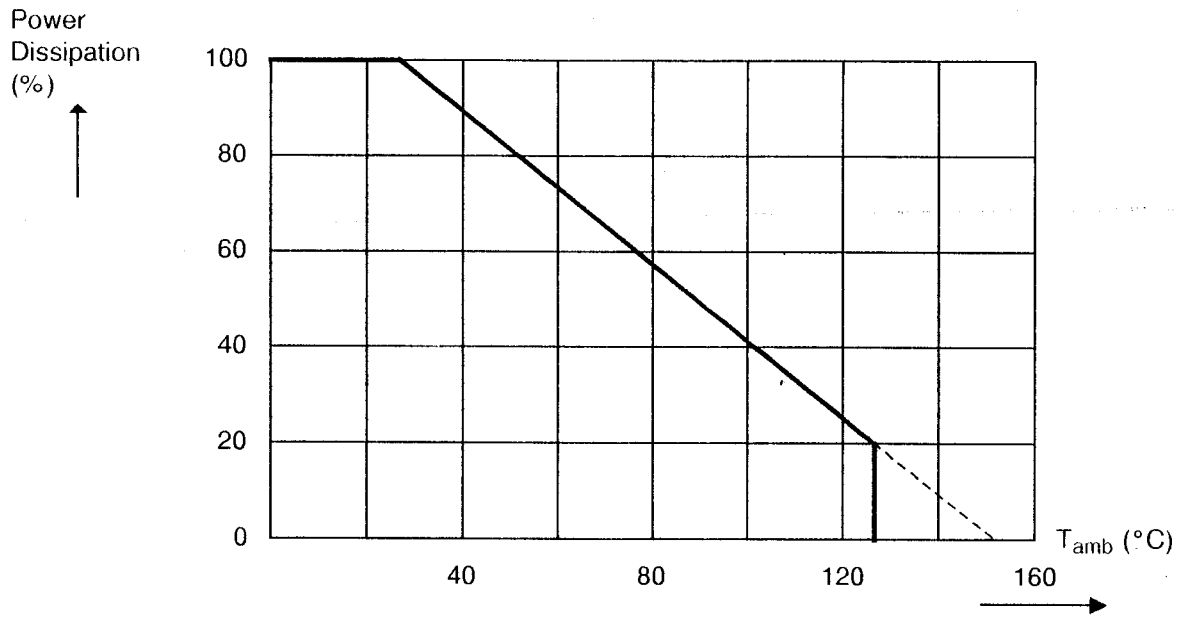
TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage	V_{CC}	7.0	V	-
2	Control Input Voltage	VCTRL	7.0	V	-
3	Input Common Mode Voltage	VICM	± 25	V	-
4	Input Differential Voltage	V_{ID}	± 25	V	-
5	Output Sink Current	I_{OUT}	50	mA	-
6	Power Dissipation Variant 01 Variant 02 Variants 03 to 05	P_{tot}	 1.2 1.0 1.4	W	Note 1
7	Operating Temperature Range	T_{op}	– 55 to + 125	°C	T_{amb}
8	Storage Temperature Range	T_{stg}	– 65 to + 150	°C	-
9	Soldering Temperature For DIL For FP and CCP	T_{sol}	+ 300	°C	 Note 2 Note 3
10	Junction Temperature	T_J	+ 150	°C	-
11	Thermal Resistance Variant 01 Variant 02 Variants 03 to 05	$R_{TH\ (J-A)}$	 100 125 91	°C/W	

NOTES

1. At T_{amb} = + 25°C. For derating at T_{amb} > + 25°C, see Figure 1.
2. Duration 10 seconds maximum at a distance of not less than 1.5mm from the package and the same lead shall not be resoldered until 3 minutes have elapsed.
3. Duration 5 seconds maximum at a distance of not less than 1.5mm from the package and the same lead shall not be resoldered until 3 minutes have elapsed.

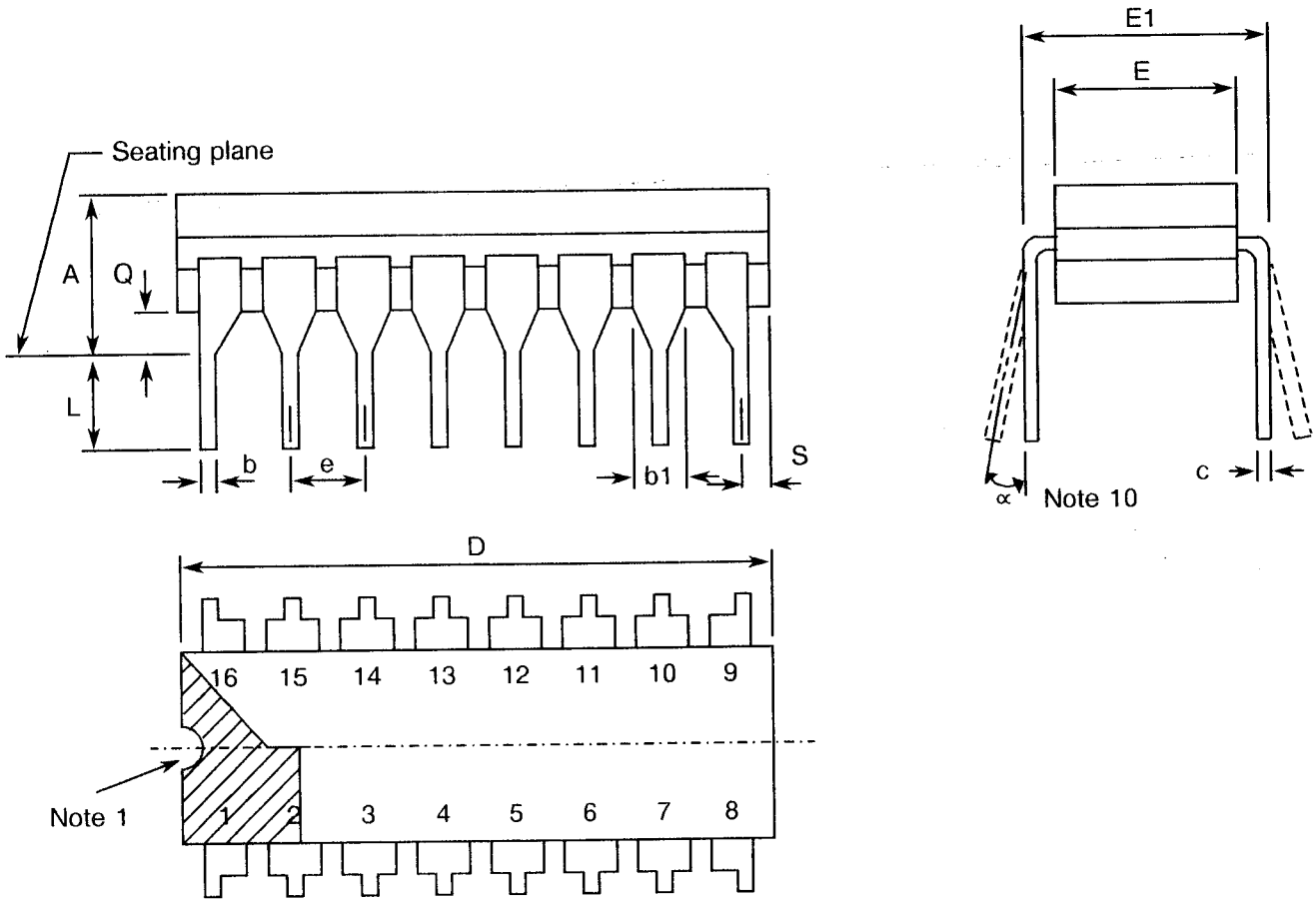
FIGURE 1 - PARAMETER DERATING INFORMATION



Total Device Dissipation versus Temperature

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - DUAL-IN-LINE PACKAGE, 16-PIN

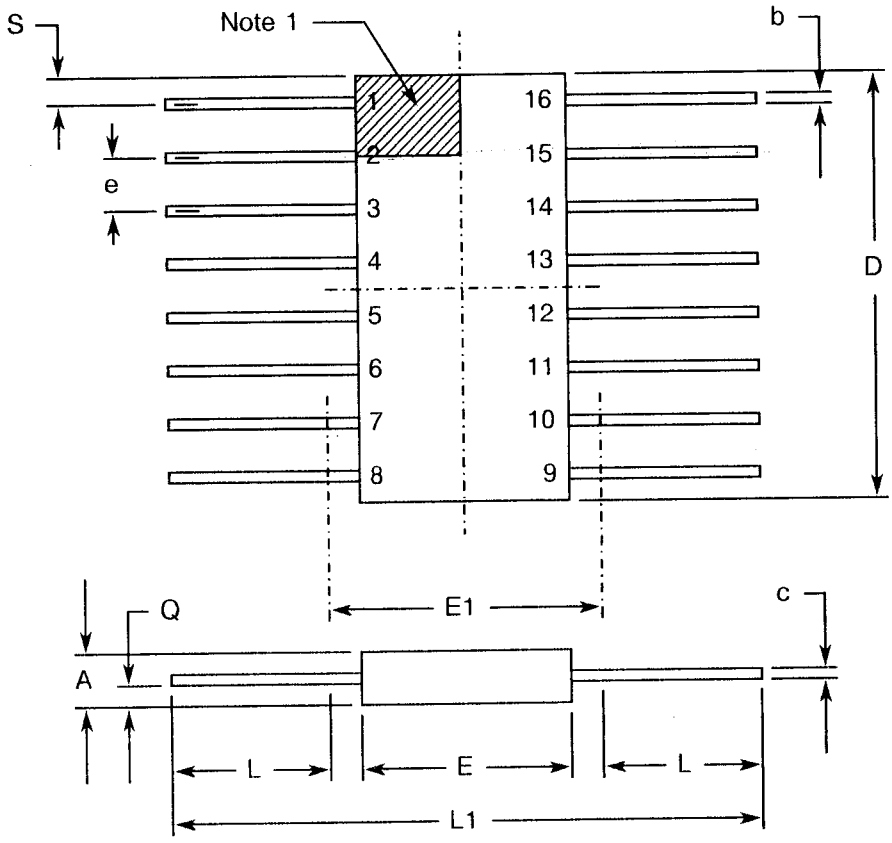


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	-	5.08	
b	0.39	0.50	8
b1	1.40	1.65	8
c	0.21	0.38	8
D	19.05	19.95	4
E	6.10	7.49	4
E1	7.62 TYPICAL		
e	2.54 TYPICAL		6, 9
L	3.18	4.31	8
Q	0.51	1.01	3
S	0.40	1.10	7
α	0°	15°	10

NOTES: See Page 12.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - FLAT PACKAGE, 16-PIN

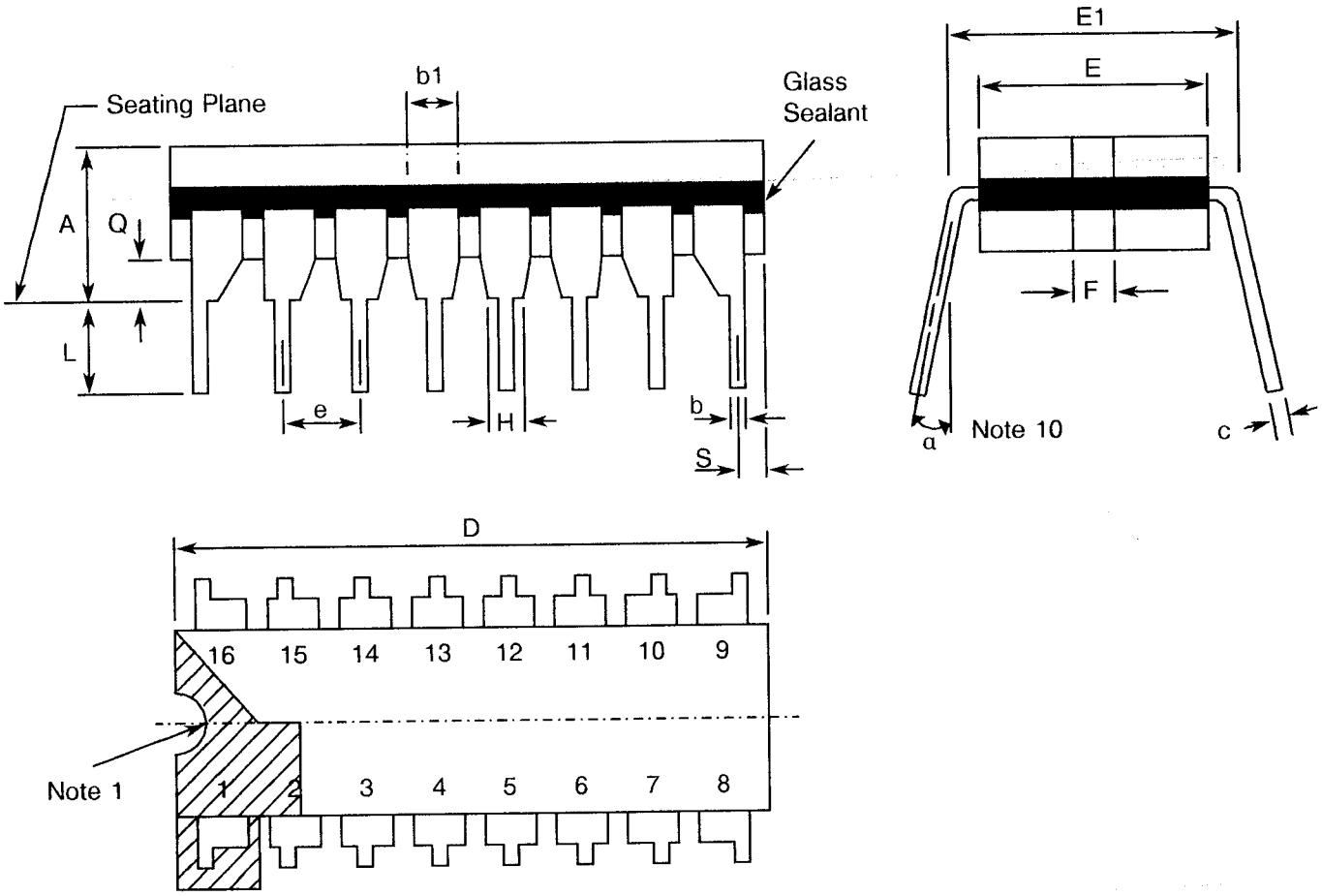


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	1.27	2.03	
b	0.38	0.56	8
c	0.08	0.23	8
D	9.42	10.16	4
E	6.27	7.24	
E1	7.00 TYPICAL		4
e	1.27 TYPICAL		5, 9
L	7.87	8.89	8
L1	23.88	24.38	
Q	0.51	1.02	2
S	0.25	0.64	7

NOTES: See Page 12.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(c) - DUAL-IN-LINE PACKAGE, 16-PIN

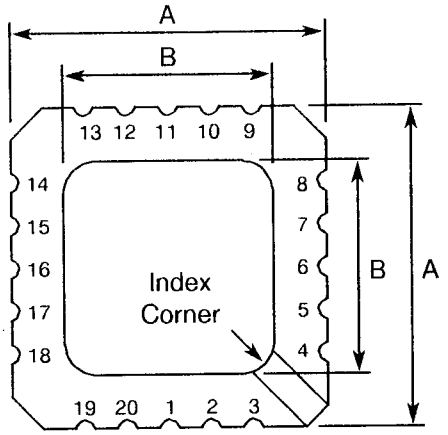


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	-	5.08	
b	0.38	0.66	8
b1	-	1.78	8
c	0.20	0.44	8
D	19.18	19.94	4
E	6.22	7.62	4
E1	7.37	8.13	
e	2.54 TYPICAL		6, 9
F	1.27 TYPICAL		
H	0.76	-	
L	3.30	5.08	8
Q	0.51	-	3
S	0.38	1.27	7
α	0°	15°	10

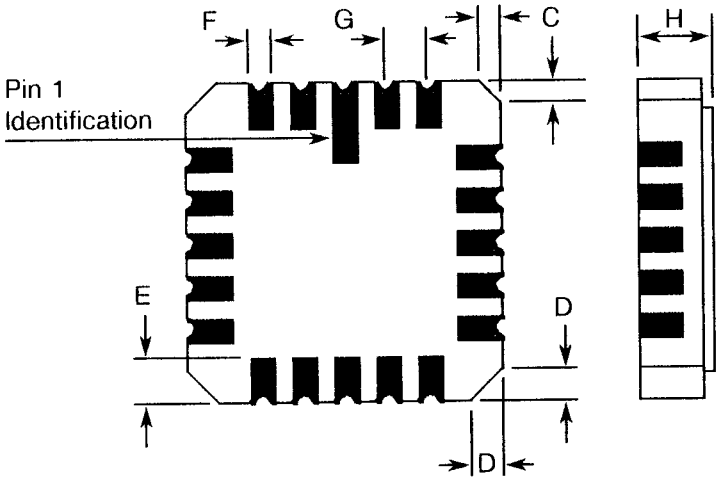
NOTES: See Page 12.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(d) - SQUARE CHIP CARRIER PACKAGE, 20-TERMINAL



20 TERMINAL



SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	8.69	9.09	
B	7.80	9.09	
C	0.25	0.51	11
D	0.89	1.14	12
E	1.14	1.40	8
F	0.56	0.71	8
G	1.27 TYPICAL		5, 9
H	1.63	2.54	

NOTES: See Page 12.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

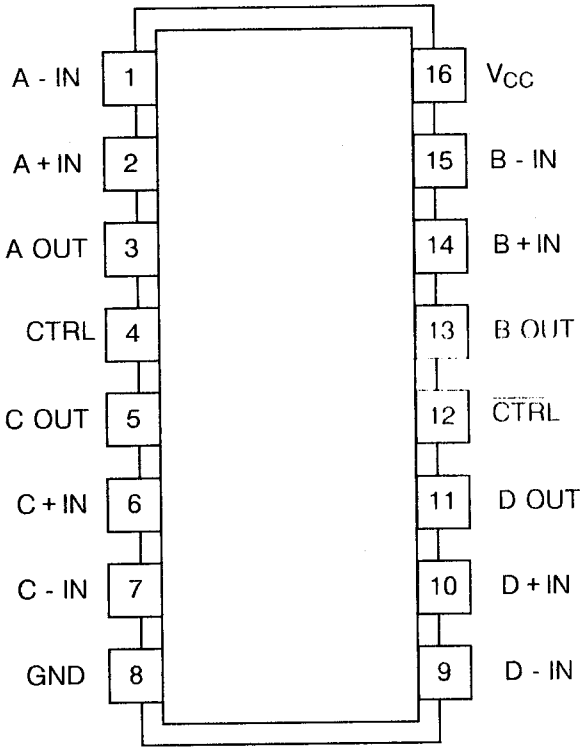
NOTES TO FIGURES 2(a) TO 2(d) INCLUSIVE

1. Index area; a notch or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages the index shall be as defined in Figure 2(d).
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. The dimension shall be measured from the seating plane to the base plane.
4. This dimension allows for off-centre lids, meniscus and glass overrun.
5. The true position pin or terminal spacing is 1.27mm between centrelines. Each pin or terminal centreline shall be located within ±0.13mm of its true longitudinal position relative to Pins 1 and the highest pin number.
6. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of its true longitudinal position relative to Pins 1 and the highest pin number.
7. Applies to all 4 corners.
8. All leads or terminals.
9. 14 spaces for flat and dual-in-line packages.

   16 spaces for chip carrier packages.
10. Lead centre when α is 0°.
11. Index corner only - 2 dimensions.
12. 3 non-index corners - 6 dimensions.

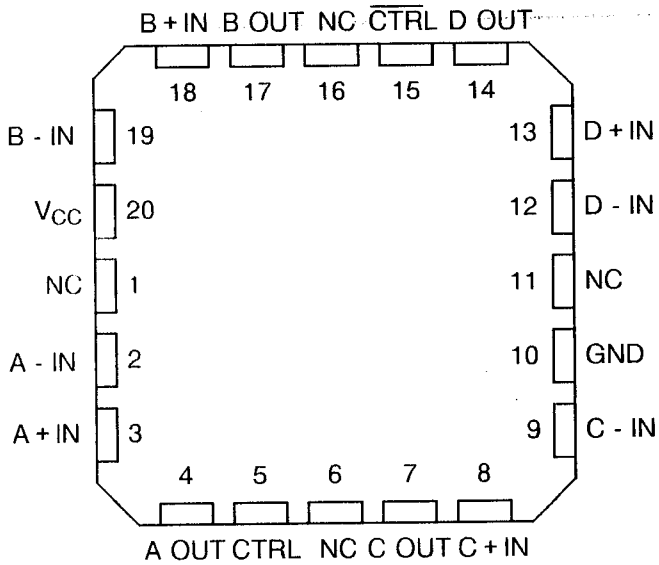
FIGURE 3(a) - PIN ASSIGNMENT

DUAL-IN-LINE AND FLAT PACKAGE



TOP VIEW

CHIP CARRIER PACKAGE



TOP VIEW

FLAT PACKAGE AND DUAL-IN-LINE TO CHIP CARRIER PIN ASSIGNMENT

FLAT PACKAGE AND DUAL-IN-LINE PIN OUTS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
CHIP CARRIER PIN OUTS	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20

FIGURE 3(b) - TRUTH TABLE (EACH RECEIVER)

DIFFERENTIAL INPUT	ENABLES		OUTPUT
	CTRL	$\overline{CTRL}$	
$V_{ID} \geq V_{TH}$	H	X	H
	X	L	H
$V_{TL} \leq V_{ID} \leq V_{TH}$	H	X	?
	X	L	?
$V_{ID} \leq V_{TL}$	H	X	L
	X	L	L
X	L	H	Z

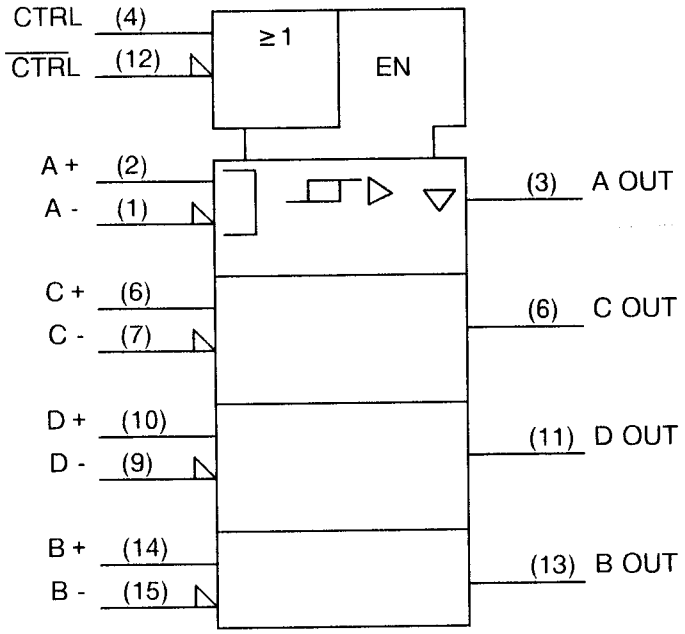
NOTES

1. Logic Level Definitions: L = Low Level, H = High Level , X = Irrelevant, Z = High Impedance, ? = Indeterminate.
2. V_{ID} = Differential Input Voltage, V_{TH} = Input Threshold Voltage High, V_{TL} = Input Threshold Voltage

FIGURE 3(c) - CIRCUIT SCHEMATIC

Not applicable.

FIGURE 3(d) - FUNCTIONAL DIAGRAM



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following symbols are used:-

I_{CC} = Supply Current.
I_{OZH} = Off-State Output Current, High Level Applied.
I_{OZL} = Off-State Output Current, Low Level Applied.
I_{OS} = Output Short Circuit Current.
V_{IC} = Enable Clamp Voltage.
V_{OLT} = Output Threshold Low Level Voltage.
V_{OHT} = Output Threshold High Level Voltage.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein shall be as stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

(a) Para. 7.1.1(a), High Temperature Reverse Bias test and subsequent electrical measurements related to this test shall be omitted.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 2.2 grammes for the dual-in-line package, 0.7 grammes for the flat package and 0.6 grammes for the chip carrier package.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body and the lids shall be welded, brazed, preform-soldered or glass frit-sealed.

4.4.2 Lead Material and Finish

For dual-in-line and flat packages, the material shall be Type 'G' with Type '4' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. For chip carrier packages, the finish shall be Type '4' or Type '7' in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

4.5.2 Lead Identification

For dual-in-line and flat packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side. For chip carrier packages, the index shall be as defined by Figure 2(d).

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:

940300301B

Detail Specification Number

Type Variant (see Table 1(a))

Testing Level (B or C, as applicable)

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ °C and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2. Conditions for H.T.R.B. Burn-in

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for power burn-in shall be as specified in Table 5 of this specification.

4.7.4 Electrical Circuit for H.T.R.B. Burn-in

Not applicable.

4.7.5 Electrical Circuit for Power Burn-in

A circuit for use in performing the power burn-in tests is shown in Figure 5 of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1 to 16	Functional Test	-	-	4(a)	V_{CC} = 5.0V Verify Truth Table with Load. Note 1	-	-	-
17	Supply Current	I_{CC}	3005	4(b)	V_{CC} = 5.5V $V_{IN(+)}$ = 0V, $V_{IN(-)}$ = 0V VCTRL = 0V, $\overline{VCTRL}$ = 2.7V (Pin D/F 16) (Pin C 20)	-	70	mA
18 to 19	Enable Current High Level 1	I_{ENH1}	3010	4(c)	V_{CC} = 5.5V VCTRL = $\overline{VCTRL}$ = 2.7V (Pins D/F 4-12) (Pins C 5-15)	-	20	µA
20 to 21	Enable Current High Level 2	I_{ENH2}	3010	4(c)	V_{CC} = 5.5V VCTRL = $\overline{VCTRL}$ = 5.5V (Pins D/F 4-12) (Pins C 5-15)	-	100	µA
22 to 23	Enable Current Low Level	I_{ENL}	3009	4(c)	V_{CC} = 5.5V VCTRL = $\overline{VCTRL}$ = 0.4V (Pins D/F 4-12) (Pins C 5-15)	-	−360	µA
24 to 27	Negative Input Current 1	$-I_{IN1}$	3010	4(d)	V_{CC} = 5.5V $V_{IN(+)}$ = −10V, $V_{IN(-)}$ = 15V (Pins D/F 1-7-9-15) (Pins C 2-9-12-19)	-	2.3	mA
28 to 31	Negative Input Current 2	$-I_{IN2}$	3010	4(d)	V_{CC} = 5.5V $V_{IN(+)}$ = 15V, $V_{IN(-)}$ = 15V (Pins D/F 1-7-9-15) (Pins C 2-9-12-19)	-	2.3	mA
32 to 35	Positive Input Current 1	$+I_{IN1}$	3010	4(d)	V_{CC} = 5.5V $V_{IN(+)}$ = 15V, $V_{IN(-)}$ = −10V (Pins D/F 2-6-10-14) (Pins C 3-8-13-18)	-	2.3	mA
36 to 39	Positive Input Current 2	$+I_{IN2}$	3010	4(d)	V_{CC} = 5.5V $V_{IN(+)}$ = 15V, $V_{IN(-)}$ = 15V (Pins D/F 2-6-10-14) (Pins C 3-8-13-18)	-	2.3	mA
40 to 43	Input Current 1	I_{IN1}	3010	4(d)	V_{CC} = 5.5V $V_{IN(+)}$ = 10V, $V_{IN(-)}$ = −15V All other $V_{IN(-)}$ pins = 0V (Pins D/F 1-7-9-15) (Pins C 2-9-12-19)	-	−2.8	mA

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
44 to 47	Input Current 2	I_{IN2}	3010	4(e)	V_{CC} = 5.5V $V_{IN(+)}$ = − 15V, $V_{IN(-)}$ = − 15V All other $V_{IN(-)}$ pins = 0V (Pins D/F 1-7-9-15) (Pins C 2-9-12-19)	-	− 2.8	mA
48 to 51	Input Current 3	I_{IN3}	3010	4(e)	V_{CC} = 5.5V $V_{IN(+)}$ = − 15V, $V_{IN(-)}$ = 10V All other $V_{IN(+)}$ pins = 0V (Pins D/F 2-6-10-14) (Pins C 3-8-13-18)	-	− 2.8	mA
52 to 55	Input Current 4	I_{IN4}	3010	4(e)	V_{CC} = 5.5V $V_{IN(+)}$ = − 15V, $V_{IN(-)}$ = − 15V All other $V_{IN(+)}$ pins = 0V (Pins D/F 2-6-10-14) (Pins C 3-8-13-18)	-	− 2.8	mA
56 to 59	Off-State Output Current (Low Level Applied)	I_{OZL}	3006	4(f)	V_{CC} = 5.5V, V_{OUT} = 0.4V $V_{IN(+)}$ = 1.0V, $V_{\overline{IN(-)}}$ = 0V VCTRL = 0.8V, $\overline{VCTRL}$ = 2.0V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	− 20	µA
60 to 63	Off-State Output Current (High Level Applied)	I_{OZH}	3006	4(f)	V_{CC} = 5.5V, V_{OUT} = 2.4V $V_{IN(+)}$ = 0V, $V_{\overline{IN(-)}}$ = 1.0V VCTRL = 0.8V, $\overline{VCTRL}$ = 2.0V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	20	µA
64 to 67	Output Voltage Low Level 1	V_{OL1}	3007	4(g)	V_{CC} = 4.5V, I_{OUT} = 4.0mA $V_{IN(+)}$ = − 8.0V, $V_{\overline{IN(-)}}$ = − 7.0V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	0.4	V
68 to 71	Output Voltage Low Level 2	V_{OL2}	3007	4(g)	V_{CC} = 4.5V, I_{OUT} = 4.0mA $V_{IN(+)}$ = 0V, $V_{\overline{IN(-)}}$ = 1.0V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	0.4	V
72 to 75	Output Voltage Low Level 3	V_{OL3}	3007	4(g)	V_{CC} = 4.5V, I_{OUT} = 4.0mA $V_{IN(+)}$ = 7.0V, $V_{\overline{IN(-)}}$ = 8.0V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	0.4	V

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
76 to 79	Output Voltage Low Level 4	V_{OL4}	3007	4(g)	V_{CC} = 4.5V, I_{OUT} = 8.0mA $V_{IN(+)}$ = − 8.0V, $V_{IN(-)}$ = − 7.0V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	0.45	V
80 to 83	Output Voltage Low Level 5	V_{OL5}	3007	4(g)	V_{CC} = 4.5V, I_{OUT} = 8.0mA $V_{IN(+)}$ = 0V, $V_{IN(-)}$ = 1.0V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	0.45	V
84 to 87	Output Voltage Low Level 6	V_{OL6}	3007	4(g)	V_{CC} = 4.5V, I_{OUT} = 8.0mA $V_{IN(+)}$ = 7.0V, $V_{IN(-)}$ = 8.0V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	0.45	V
88 to 91	Output Voltage High Level 1	V_{OH1}	3006	4(g)	V_{CC} = 4.5V, I_{OUT} = − 440µA $V_{IN(+)}$ = − 7.0V, $V_{IN(-)}$ = − 8.0V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	2.5	-	V
92 to 95	Output Voltage High Level 2	V_{OH2}	3006	4(g)	V_{CC} = 4.5V, I_{OUT} = − 440µA $V_{IN(+)}$ = 1.0V, $V_{IN(-)}$ = 0V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	2.5	-	V
96 to 99	Output Voltage High Level 3	V_{OH3}	3006	4(g)	V_{CC} = 4.5V, I_{OUT} = − 440µA $V_{IN(+)}$ = 8.0V, $V_{IN(-)}$ = 7.0V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	2.5	-	V
100 to 103	Output Threshold Voltage Low Level 1	V_{OLT1}	-	4(g)	V_{CC} = 4.5V, I_{OUT} = 8.0mA $V_{IN(+)}$ = − 6.9V, $V_{IN(-)}$ = − 6.7V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	0.45	V
104 to 107	Output Threshold Voltage Low Level 2	V_{OLT2}	-	4(g)	V_{CC} = 4.5V, I_{OUT} = 8.0mA $V_{IN(+)}$ = 6.7V, $V_{IN(-)}$ = 6.9V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	0.45	V

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
108 to 111	Output Threshold Voltage High Level 1	V_{OHT1}	-	4(g)	V_{CC} = 4.5V, I_{OUT} = − 440µA $V_{IN(+)}$ = − 6.7V, $V_{IN(-)}$ = − 6.9V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	2.5	-	V
112 to 115	Output Threshold Voltage High Level 2	V_{OHT2}	-	4(g)	V_{CC} = 4.5V, I_{OUT} = − 440µA $V_{IN(+)}$ = 6.9V, $V_{IN(-)}$ = 6.7V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	2.5	-	V
116 to 119	Output Short Circuit Current 1	I_{OS1}	3011	4(h)	V_{CC} = 5.5V, V_{OUT} = 0V $V_{IN(+)}$ = 1.0V, $V_{IN(-)}$ = 0V Note 2 VCTRL = $\overline{VCTRL}$ = 2.0V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	− 15	− 85	mA
120 to 123	Output Short Circuit Current 2	I_{OS2}	3011	4(h)	V_{CC} = 5.5V, V_{OUT} = 0V $V_{IN(+)}$ = 1.0V, $V_{IN(-)}$ = 0V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V Note 2 (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	− 15	− 85	mA
124	Enable Clamp Voltage 1	V_{IC1}	-	4(i)	ICTRL = − 18mA, V_{CC} = 4.5V (Pin D/F 4) (Pin C 5)	− 1.5	-	V
125	Enable Clamp Voltage 2	V_{IC2}	-	4(i)	$\overline{ICTRL}$ = − 18mA, V_{CC} = 4.5V (Pin D/F 12) (Pin C 15)	− 1.5	-	V

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP) (NOTE 3)	LIMITS		UNIT
						MIN	MAX	
126 to 129	Propagation Delay Low to High 1	t_{PLH1}	3004	4(j)	$V_{IN(+)}$ = 1.5V VCTRL = $\overline{VCTRL}$ = 2.0V Switches = 00 (Note 4) $V_{IN(-)}$ = PI2, V_{OUT} = PO2 (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	30	ns
130 to 133	Propagation Delay Low to High 2	t_{PLH2}	3004	4(j)	$V_{IN(-)}$ = 1.5V VCTRL = $\overline{VCTRL}$ = 2.0V Switches = 00 (Note 4) $V_{IN(+)}$ = PI1, V_{OUT} = PO1 (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	30	ns
134 to 137	Propagation Delay High to Low 1	t_{PHL1}	3004	4(j)	$V_{IN(-)}$ = 1.5V VCTRL = $\overline{VCTRL}$ = 2.0V Switches = 00 (Note 4) $V_{IN(+)}$ = PI1, V_{OUT} = PO1 (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	30	ns
138 to 141	Propagation Delay High to Low 2	t_{PHL2}	3004	4(j)	$V_{IN(+)}$ = 1.5V VCTRL = $\overline{VCTRL}$ = 2.0V Switches = 00 (Note 4) $V_{IN(-)}$ = PI2, V_{OUT} = PO2 (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	30	ns
142 to 145	Output Disable Time from Low Level 1	t_{PLZ1}	3003	4(j)	$V_{IN(+)}$ = − 1.5V, $V_{IN(-)}$ = 0V VCTRL = PI4, $\overline{VCTRL}$ = 2.0V Switches = 11 (Note 4) V_{OUT} = PO3 (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	35	ns
146 to 149	Output Enable Time to Low Level 1	t_{PZL1}	3003	4(j)	$V_{IN(+)}$ = − 1.5V, $V_{IN(-)}$ = 0V VCTRL = PI4, $\overline{VCTRL}$ = 2.0V Switches = 10 (Note 4) V_{OUT} = PO6 (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	22	ns
150 to 153	Output Disable Time from High Level 1	t_{PHZ1}	3003	4(j)	$V_{IN(+)}$ = 1.5V, $V_{IN(-)}$ = 0V VCTRL = PI4, $\overline{VCTRL}$ = 2.0V Switches = 11 (Note 4) V_{OUT} = PO4 (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	30	ns

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP) (NOTE 3)	LIMITS		UNIT
						MIN	MAX	
154 to 157	Output Enable Time to High Level 1	t_{PZH1}	3003	4(j)	$V_{IN(+)}$ = 1.5V, $V_{IN(-)}$ = 0V VCTRL = PI4, $\overline{VCTRL}$ = 2.0V Switches = 01 (Note 4) V_{OUT} = PO5 (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	22	ns
158 to 161	Output Disable Time from Low Level 2	t_{PLZ2}	3003	4(j)	$V_{IN(+)}$ = − 1.5V, $V_{IN(-)}$ = 0V VCTRL = 0V, $\overline{VCTRL}$ = PI3 Switches = 11 (Note 4) V_{OUT} = PO3 (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	35	ns
162 to 165	Output Enable Time to Low Level 2	t_{PZL2}	3003	4(j)	$V_{IN(+)}$ = − 1.5V, $V_{IN(-)}$ = 0V VCTRL = 0V, $\overline{VCTRL}$ = PI3 Switches = 10 (Note 4) V_{OUT} = PO6 (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	22	ns
166 to 169	Output Disable Time from High Level 2	t_{PHZ2}	3003	4(j)	$V_{IN(+)}$ = 1.5V, $V_{IN(-)}$ = 0V VCTRL = 0V, $\overline{VCTRL}$ = PI3 Switches = 11 (Note 4) V_{OUT} = PO4 (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	30	ns
170 to 173	Output Enable Time to High Level 2	t_{PZH2}	3003	4(j)	$V_{IN(+)}$ = 1.5V, $V_{IN(-)}$ = 0V VCTRL = 0V, $\overline{VCTRL}$ = PI3 Switches = 01 (Note 4) V_{OUT} = PO5 (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	22	ns

NOTES

1. Go-no-go test with $V_{IL} \leq 0.5V$, $2.5V \leq V_{IH} \leq 3.0V$.
   $1.3V < \text{Trip point} < 1.6V$.
   $50\mu A < I_L < 300\mu A$.
2. Only one output may be shorted at a time and only for 1 second maximum.
3. V_{CC} = 5.0V.
4. Switches SW1 and SW2 operating status, 0 = Open, 1 = Closed.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1 to 16	Functional Test	-	-	4(a)	V_{CC} = 5.0V Verify Truth Table with Load. Note 1	-	-	-
17	Supply Current	I_{CC}	3005	4(b)	V_{CC} = 5.5V $V_{IN(+)}$ = 0V, $V_{IN(-)}$ = 0V VCTRL = 0V, $\overline{VCTRL}$ = 2.7V (Pin D/F 16) (Pin C 20)	-	70	mA
18 to 19	Enable Current High Level 1	I_{ENH1}	3010	4(c)	V_{CC} = 5.5V VCTRL = $\overline{VCTRL}$ = 2.7V (Pins D/F 4-12) (Pins C 5-15)	-	20	µA
20 to 21	Enable Current High Level 2	I_{ENH2}	3010	4(c)	V_{CC} = 5.5V VCTRL = $\overline{VCTRL}$ = 5.5V (Pins D/F 4-12) (Pins C 5-15)	-	100	µA
22 to 23	Enable Current Low Level	I_{ENL}	3009	4(c)	V_{CC} = 5.5V VCTRL = $\overline{VCTRL}$ = 0.4V (Pins D/F 4-12) (Pins C 5-15)	-	− 360	µA
24 to 27	Negative Input Current 1	$-I_{IN1}$	3010	4(d)	V_{CC} = 5.5V $V_{IN(+)}$ = − 10V, $V_{IN(-)}$ = 15V (Pins D/F 1-7-9-15) (Pins C 2-9-12-19)	-	2.3	mA
28 to 31	Negative Input Current 2	$-I_{IN2}$	3010	4(d)	V_{CC} = 5.5V $V_{IN(+)}$ = 15V, $V_{IN(-)}$ = 15V (Pins D/F 1-7-9-15) (Pins C 2-9-12-19)	-	2.3	mA
32 to 35	Positive Input Current 1	$+I_{IN1}$	3010	4(d)	V_{CC} = 5.5V $V_{IN(+)}$ = 15V, $V_{IN(-)}$ = − 10V (Pins D/F 2-6-10-14) (Pins C 3-8-13-18)	-	2.3	mA
36 to 39	Positive Input Current 2	$+I_{IN2}$	3010	4(d)	V_{CC} = 5.5V $V_{IN(+)}$ = 15V, $V_{IN(-)}$ = 15V (Pins D/F 2-6-10-14) (Pins C 3-8-13-18)	-	2.3	mA
40 to 43	Input Current 1	I_{IN1}	3010	4(d)	V_{CC} = 5.5V $V_{IN(+)}$ = 10V, $V_{IN(-)}$ = − 15V All other $V_{IN(-)}$ pins = 0V (Pins D/F 1-7-9-15) (Pins C 2-9-12-19)	-	− 2.8	mA

NOTES: See Page 23.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
44 to 47	Input Current 2	I_{IN2}	3010	4(e)	V_{CC} = 5.5V $V_{IN(+)}$ = − 15V, $V_{IN(-)}$ = − 15V All other $V_{IN(-)}$ pins = 0V (Pins D/F 1-7-9-15) (Pins C 2-9-12-19)	-	− 2.8	mA
48 to 51	Input Current 3	I_{IN3}	3010	4(e)	V_{CC} = 5.5V $V_{IN(+)}$ = − 15V, $V_{IN(-)}$ = 10V All other $V_{IN(+)}$ pins = 0V (Pins D/F 2-6-10-14) (Pins C 3-8-13-18)	-	− 2.8	mA
52 to 55	Input Current 4	I_{IN4}	3010	4(e)	V_{CC} = 5.5V $V_{IN(+)}$ = − 15V, $V_{IN(-)}$ = − 15V All other $V_{IN(+)}$ pins = 0V (Pins D/F 2-6-10-14) (Pins C 3-8-13-18)	-	− 2.8	mA
56 to 59	Off-State Output Current (Low Level Applied)	I_{OZL}	3006	4(f)	V_{CC} = 5.5V, V_{OUT} = 0.4V $V_{IN(+)}$ = 1.0V, $V_{IN(-)}$ = 0V VCTRL = 0.8V, $\overline{VCTRL}$ = 2.0V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	− 20	µA
60 to 63	Off-State Output Current (High Level Applied)	I_{OZH}	3006	4(f)	V_{CC} = 5.5V, V_{OUT} = 2.4V $V_{IN(+)}$ = 0V, $V_{IN(-)}$ = 1.0V VCTRL = 0.8V, $\overline{VCTRL}$ = 2.0V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	20	µA
64 to 67	Output Voltage Low Level 1	V_{OL1}	3007	4(g)	V_{CC} = 4.5V, I_{OUT} = 4.0mA $V_{IN(+)}$ = − 8.0V, $V_{IN(-)}$ = − 7.0V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	0.4	V
68 to 71	Output Voltage Low Level 2	V_{OL2}	3007	4(g)	V_{CC} = 4.5V, I_{OUT} = 4.0mA $V_{IN(+)}$ = 0V, $V_{IN(-)}$ = 1.0V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	0.4	V
72 to 75	Output Voltage Low Level 3	V_{OL3}	3007	4(g)	V_{CC} = 4.5V, I_{OUT} = 4.0mA $V_{IN(+)}$ = 7.0V, $V_{IN(-)}$ = 8.0V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	0.4	V

NOTES: See Page 23.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
76 to 79	Output Voltage Low Level 4	V_{OL4}	3007	4(g)	V_{CC} = 4.5V, I_{OUT} = 8.0mA $V_{IN(+)}$ = − 8.0V, $V_{\overline{IN(-)}}$ = − 7.0V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	0.45	V
80 to 83	Output Voltage Low Level 5	V_{OL5}	3007	4(g)	V_{CC} = 4.5V, I_{OUT} = 8.0mA $V_{IN(+)}$ = 0V, $V_{IN(-)}$ = 1.0V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	0.45	V
84 to 87	Output Voltage Low Level 6	V_{OL6}	3007	4(g)	V_{CC} = 4.5V, I_{OUT} = 8.0mA $V_{IN(+)}$ = 7.0V, $V_{\overline{IN(-)}}$ = 8.0V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	0.45	V
88 to 91	Output Voltage High Level 1	V_{OH1}	3006	4(g)	V_{CC} = 4.5V, I_{OUT} = − 440µA $V_{IN(+)}$ = − 7.0V, $V_{\overline{IN(-)}}$ = − 8.0V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	2.5	-	V
92 to 95	Output Voltage High Level 2	V_{OH2}	3006	4(g)	V_{CC} = 4.5V, I_{OUT} = − 440µA $V_{IN(+)}$ = 1.0V, $V_{\overline{IN(-)}}$ = 0V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	2.5	-	V
96 to 99	Output Voltage High Level 3	V_{OH3}	3006	4(g)	V_{CC} = 4.5V, I_{OUT} = − 440µA $V_{IN(+)}$ = 8.0V, $V_{\overline{IN(-)}}$ = 7.0V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	2.5	-	V
100 to 103	Output Threshold Voltage Low Level 1	V_{OLT1}	-	4(g)	V_{CC} = 4.5V, I_{OUT} = 8.0mA $V_{IN(+)}$ = − 6.9V, $V_{\overline{IN(-)}}$ = − 6.7V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	0.45	V
104 to 107	Output Threshold Voltage Low Level 2	V_{OLT2}	-	4(g)	V_{CC} = 4.5V, I_{OUT} = 8.0mA $V_{IN(+)}$ = 6.7V, $V_{\overline{IN(-)}}$ = 6.9V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	-	0.45	V

NOTES: See Page 23.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
108 to 111	Output Threshold Voltage High Level 1	V_{OHT1}	-	4(g)	V_{CC} = 4.5V, I_{OUT} = −440µA $V_{IN(+)}$ = −6.7V, $V_{\overline{IN(-)}}$ = −6.9V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	2.5	-	V
112 to 115	Output Threshold Voltage High Level 2	V_{OHT2}	-	4(g)	V_{CC} = 4.5V, I_{OUT} = −440µA $V_{IN(+)}$ = 6.9V, $V_{\overline{IN(-)}}$ = 6.7V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	2.5	-	V
116 to 119	Output Short Circuit Current 1	I_{OS1}	3011	4(h)	V_{CC} = 5.5V, V_{OUT} = 0V $V_{IN(+)}$ = 1.0V, $V_{\overline{IN(-)}}$ = 0V VCTRL = $\overline{VCTRL}$ = 2.0V Note 2 (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	−15	−85	mA
120 to 123	Output Short Circuit Current 2	I_{OS2}	3011	4(h)	V_{CC} = 5.5V, V_{OUT} = 0V $V_{IN(+)}$ = 1.0V, $V_{\overline{IN(-)}}$ = 0V VCTRL = 2.0V, $\overline{VCTRL}$ = 0.8V Note 2 (Pins D/F 3-5-11-13) (Pins C 4-7-14-17)	−15	−85	mA
124	Enable Clamp Voltage 1	V_{IC1}	-	4(i)	ICTRL = −18mA, V_{CC} = 4.5V (Pin D/F 4) (Pin C 5)	−1.5	-	V
125	Enable Clamp Voltage 2	V_{IC2}	-	4(i)	$\overline{ICTRL}$ = −18mA, V_{CC} = 4.5V (Pin D/F 12) (Pin C 15)	−1.5	-	V

NOTES: See Page 23.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - FUNCTIONAL TEST

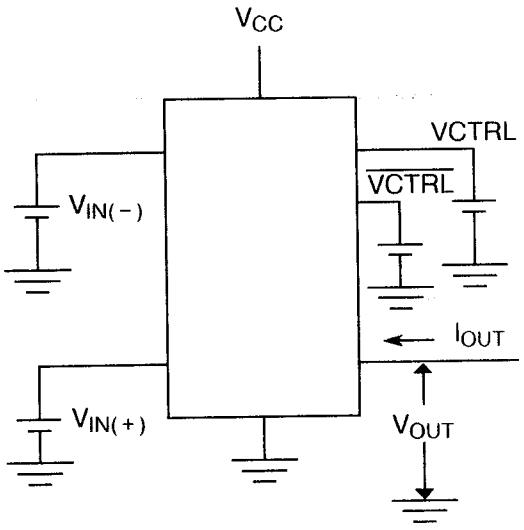


FIGURE 4(b) - SUPPLY CURRENT

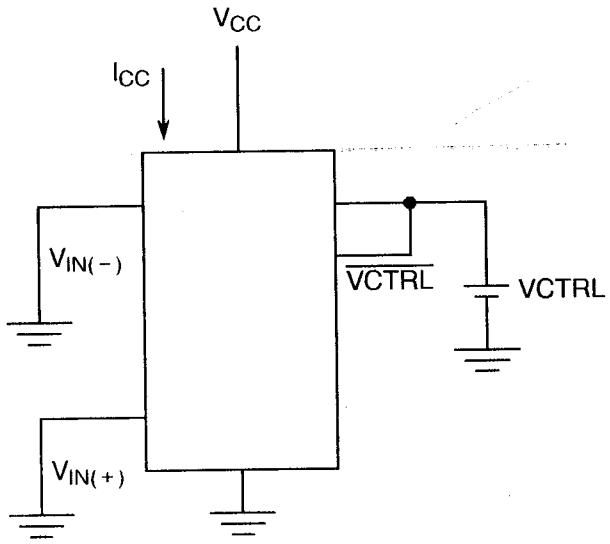


FIGURE 4(c) - ENABLE CURRENT

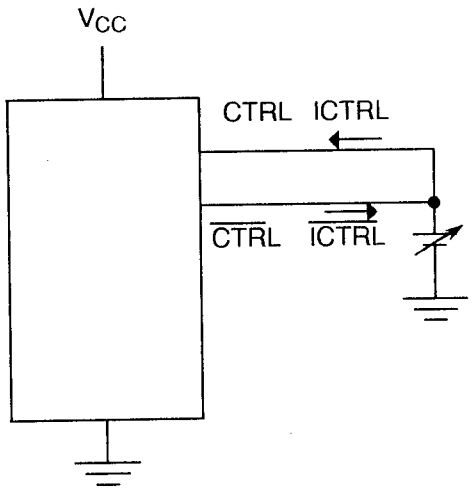
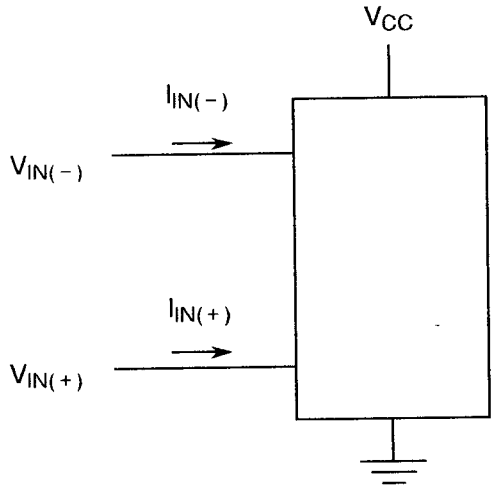


FIGURE 4(d) - INPUT CURRENT



NOTES

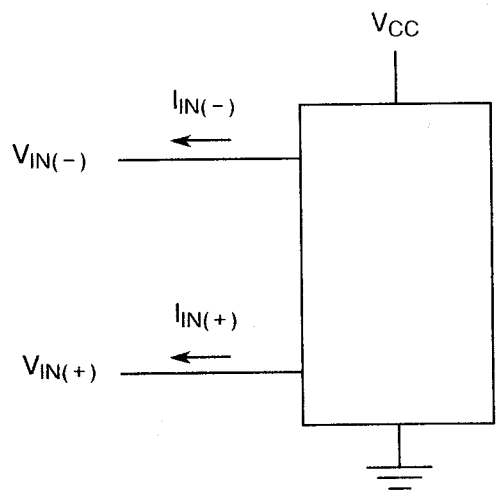
1. Each input to be tested separately.

NOTES

1. Each input to be tested separately.

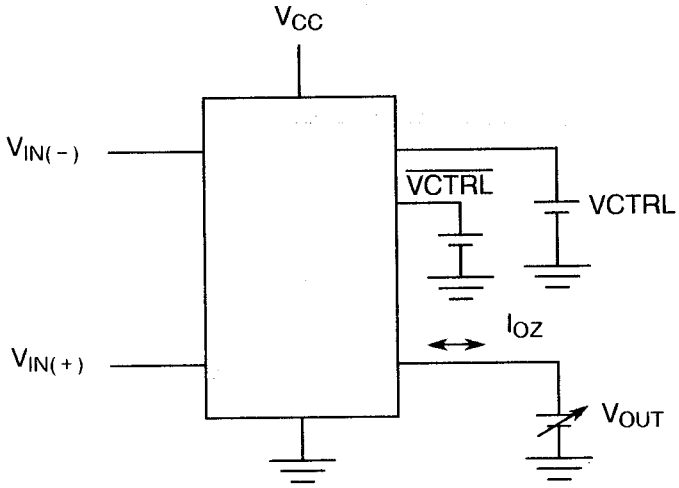
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(e) - INPUT CURRENT



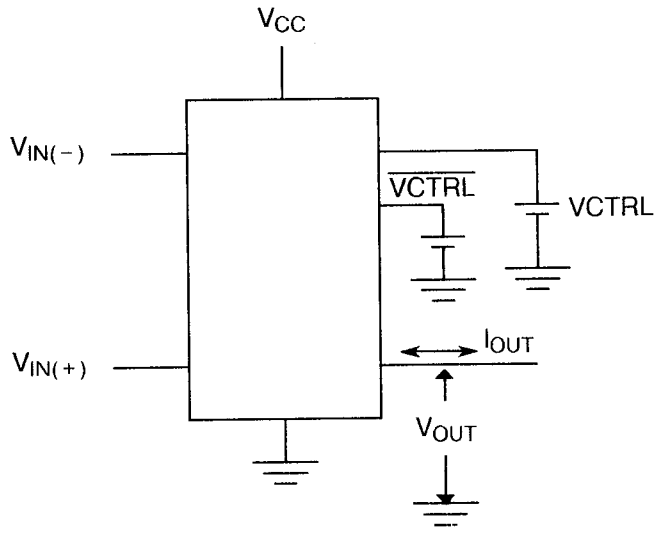
NOTES
1. Each input to be tested separately.

FIGURE 4(f) - OFF-STATE OUTPUT CURRENT



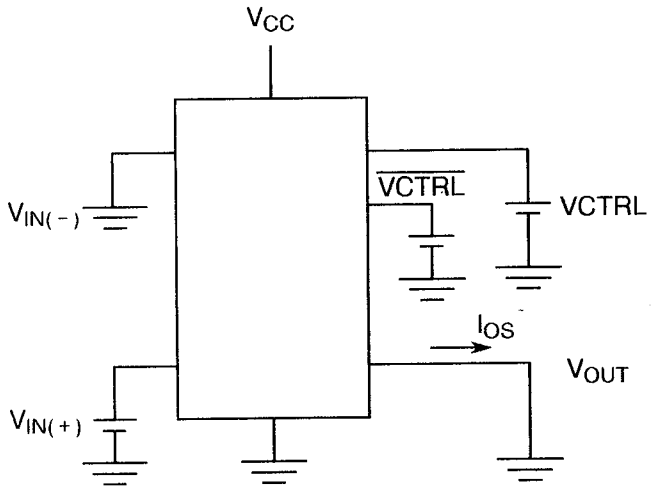
NOTES
1. Each output to be tested separately.

FIGURE 4(g) - OUTPUT LOW LEVEL/ HIGH LEVEL/THRESHOLD VOLTAGE



NOTES
1. Each output to be tested separately.

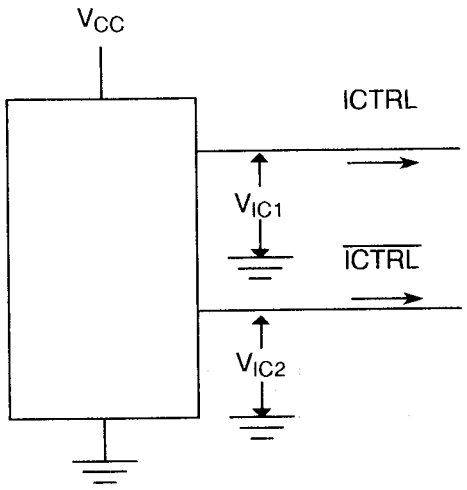
FIGURE 4(h) - OUTPUT SHORT CIRCUIT CURRENT



NOTES
1. Each output to be tested separately.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - ENABLE CLAMP VOLTAGE



NOTES

1. Each input to be tested separately.

FIGURE 4(j) - PROPAGATION DELAY

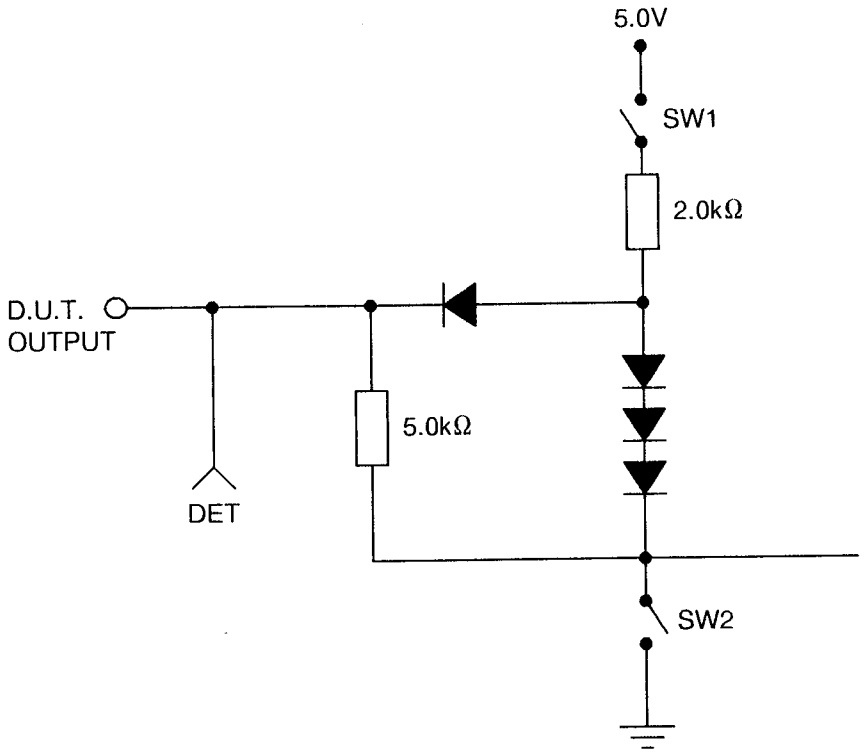
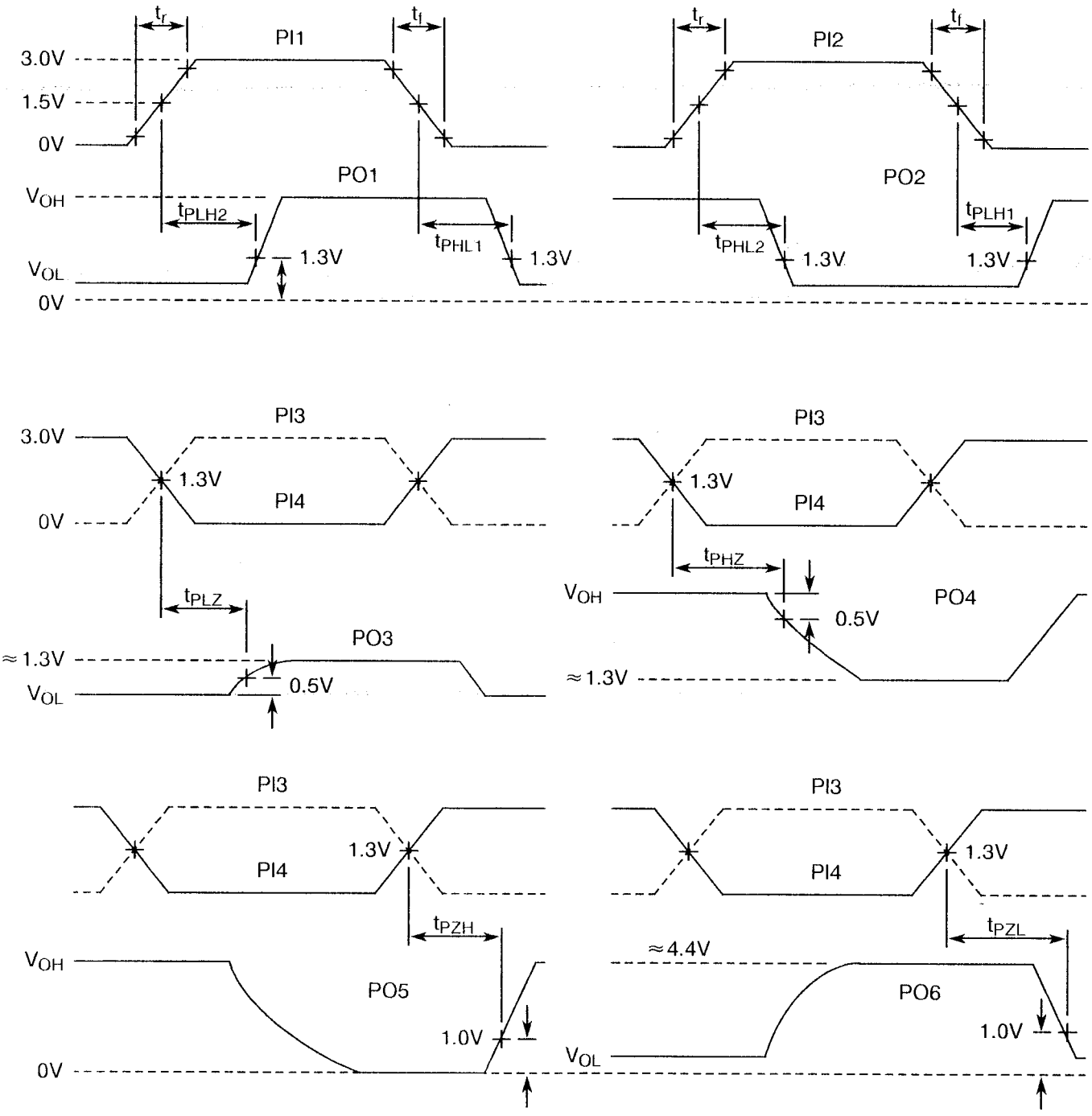


FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(j) - PROPAGATION DELAY (CONT'D)

VOLTAGE WAVEFORMS



NOTES

1. Input Waveform (all inputs): f = 1.0MHz, Duty Cycle = 50%, $t_r = t_f = 5.0$ns between10% to 90%.
2. For Input/Output Conditions, see Table 2.

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
17	Supply Current	I_{CC}	As per Table 2	As per Table 2	±5.0	mA
20 to 21	Enable Current High Level 2	I_{ENH2}	As per Table 2	As per Table 2	±10	µA
22 to 23	Enable Current Low Level	I_{ENL}	As per Table 2	As per Table 2	±36	µA
24 to 27	Negative Input Current 1	$-I_{IN1}$	As per Table 2	As per Table 2	±200	µA
32 to 35	Positive Input Current 1	$+I_{IN1}$	As per Table 2	As per Table 2	±200	µA
40 to 43	Input Current 1	I_{IN1}	As per Table 2	As per Table 2	±200	µA
44 to 47	Input Current 2	I_{IN2}	As per Table 2	As per Table 2	±200	µA
76 to 79	Output Voltage Low Level 4	V_{OL4}	As per Table 2	As per Table 2	±45	mV
84 to 87	Output Voltage Low Level 6	V_{OL6}	As per Table 2	As per Table 2	±45	mV
88 to 91	Output Voltage High Level 1	V_{OH1}	As per Table 2	As per Table 2	±250	mV
96 to 99	Output Voltage High Level 3	V_{OH3}	As per Table 2	As per Table 2	±250	mV

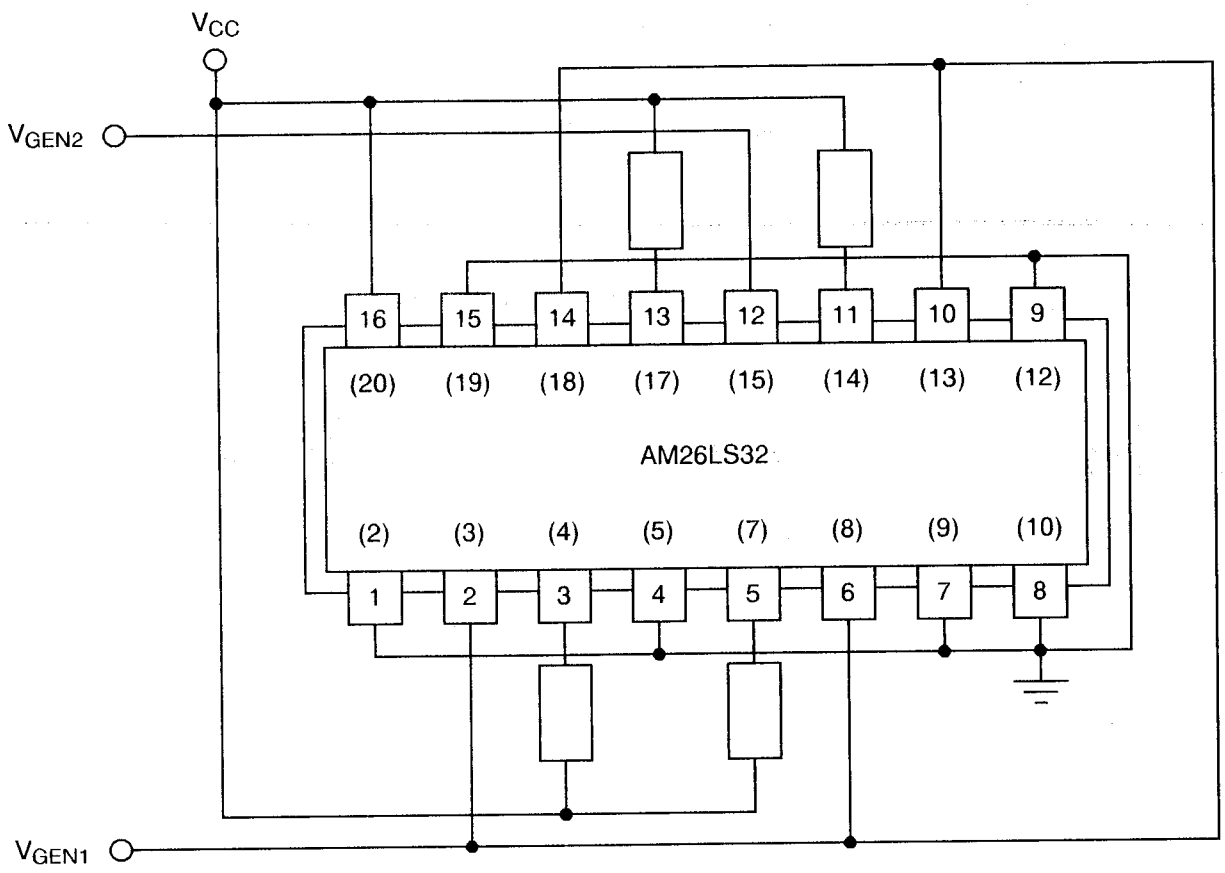
TABLE 5 - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0−5)	°C
2	Outputs - (Pins D/F 3-5-11-13) - (Pins C 4-7-14-17)	V_{OUT}	V_{CC}	V
3	Inputs - (Pins D/F 2-6-10-14) - (Pins C 3-8-13-18)	V_{IN}	V_{GEN1}	Vac
4	Input - (Pin D/F 12) - (Pin C 15)	V_{IN}	V_{GEN2} (Note 1)	Vac
5	Inputs - (Pins D/F 1-4-7-9-15) - (Pins C 2-5-9-12-19)	V_{IN}	GND	V
6	Pulse Voltage	V_{GEN1}	(-2.5 to -1.0) to (+1.0 to +2.5)	Vac
7	Pulse Voltage	V_{GEN2}	0 to 3.0	Vac
8	Pulse Frequency Square Wave	f_{GEN1} f_{GEN2}	100k 50k 50% Duty Cycle $t_r = t_f \leq 10$ns	Hz
9	Positive Supply Voltage (Pin D/F 16) (Pin C 20)	V_{CC}	5.5(+0−0.5)	V
10	Negative Supply Voltage (Pin D/F 8) (Pin C 10)	GND	0	V

NOTES

1. Triggered by V_{GEN1}.
2. Output Load = 1.0kΩ

FIGURE 5 - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



NOTES

1. Pin numbers in parenthesis are for the chip carrier package.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5 of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5 of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	ABSOLUTE		UNIT
						MIN.	MAX.	
1 to 16	Functional Test	-	As per Table 2	As per Table 2	-	-	-	-
17	Supply Current	I_{CC}	As per Table 2	As per Table 2	±5.0	-	70	mA
20 to 21	Enable Current High Level 2	I_{ENH2}	As per Table 2	As per Table 2	±10	-	100	µA
22 to 23	Enable Current Low Level	I_{ENL}	As per Table 2	As per Table 2	±36	-	−360	µA
24 to 27	Negative Input Current 1	$-I_{IN1}$	As per Table 2	As per Table 2	±0.2	-	2.3	mA
32 to 35	Positive Input Current 1	$+I_{IN1}$	As per Table 2	As per Table 2	±0.2	-	2.3	mA
40 to 43	Input Current 1	I_{IN1}	As per Table 2	As per Table 2	±0.2	-	−2.8	mA
44 to 47	Input Current 2	I_{IN2}	As per Table 2	As per Table 2	±0.2	-	−2.8	mA
56 to 59	Off-State Output Current (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	-	-	−20	µA
60 to 63	Off-State Output Current (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	-	-	20	µA
76 to 79	Output Voltage Low Level 4	V_{OL4}	As per Table 2	As per Table 2	±45	-	450	mV
84 to 87	Output Voltage Low Level 6	V_{OL6}	As per Table 2	As per Table 2	±45	-	450	mV
88 to 91	Output Voltage High Level 1	V_{OH1}	As per Table 2	As per Table 2	±0.25	2.5	-	V
96 to 99	Output Voltage High Level 3	V_{OH3}	As per Table 2	As per Table 2	±0.25	2.5	-	V