INTEGRATED CIRCUITS, MONOLITHIC,

SILICON ON SAPPHIRE,

CMOS PROGRAMMABLE DMA CONTROLLER,

BASED ON TYPE MAS28137

ESCC Detail Specification No. 9543/003

ISSUE 1

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Pages 1 to 58

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space components
coordination group

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TABLE OF CONTENTS

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a Monolithic, Silicon on Sapphire CMOS Programmable DMA Controller, based on Type MAS28137. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE/INSTRUCTION SET

As per Figure 3(b).

1.8 CIRCUIT DESCRIPTION

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 with a Minimum Critical Path Failure Voltage of 300Volts.

1.11 INPUT PROTECTION NETWORKS

Protection Networks shall be incorporated into each input as shown in Figure 3(e).

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND FINISH
01	DIL	2(a)	D2
02	DIL	2(b)	D2
03	FLAT	2(c)	D2

TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage	V_{DD}	−0.3 to +7.0	V	-
2	Input Voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V	-
3	Supply Current	$I_{DD(op)}$	50	mA	-
4	Device Dissipation	P_D	500	mWdc	Note 1
5	Operating Temperature Range	T_{op}	−55 to +125	°C	T_{amb}
6	Storage Temperature Range	T_{stg}	−65 to +150	°C	-
7	Soldering Temperature	T_{sol}	+250	°C	Note 2

NOTES

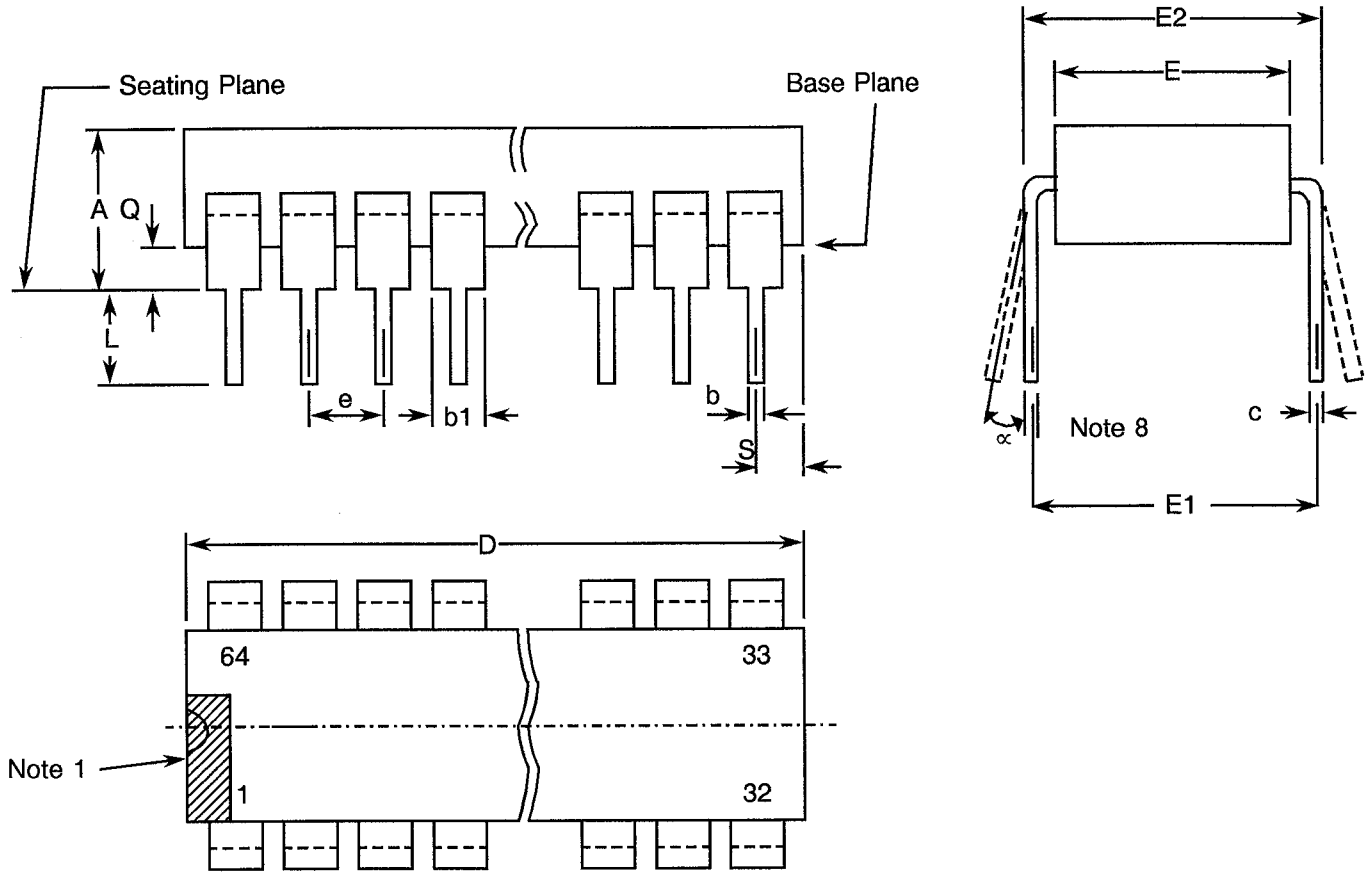
1. Current through any 1 pin limited to ±20mA.
2. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION

Not applicable.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - DUAL-IN-LINE PACKAGE, 64 PIN

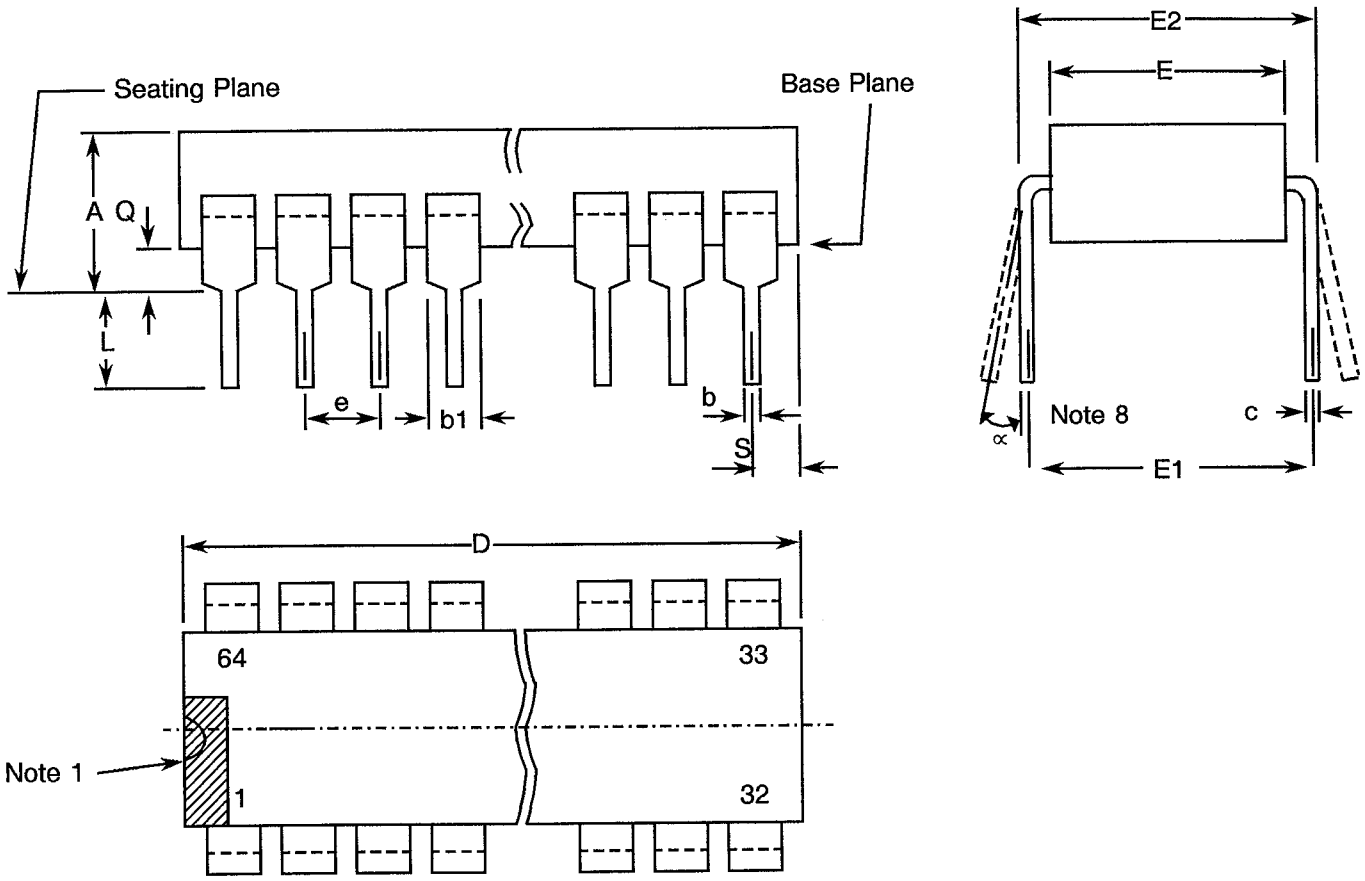


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	-	4.24	2
b	0.40	0.51	4
b1	-	1.53	4
c	0.20	0.31	4
D	-	82.17	
E	22.70 TYPICAL		
E1	22.86 TYPICAL		
E2	-	23.50	
e	2.54 TYPICAL		5,6
L	3.18	4.36	4
Q	1.02	1.53	3
S	-	1.27	7
∝	0°	15°	8

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - DUAL-IN-LINE PACKAGE, 64 PIN

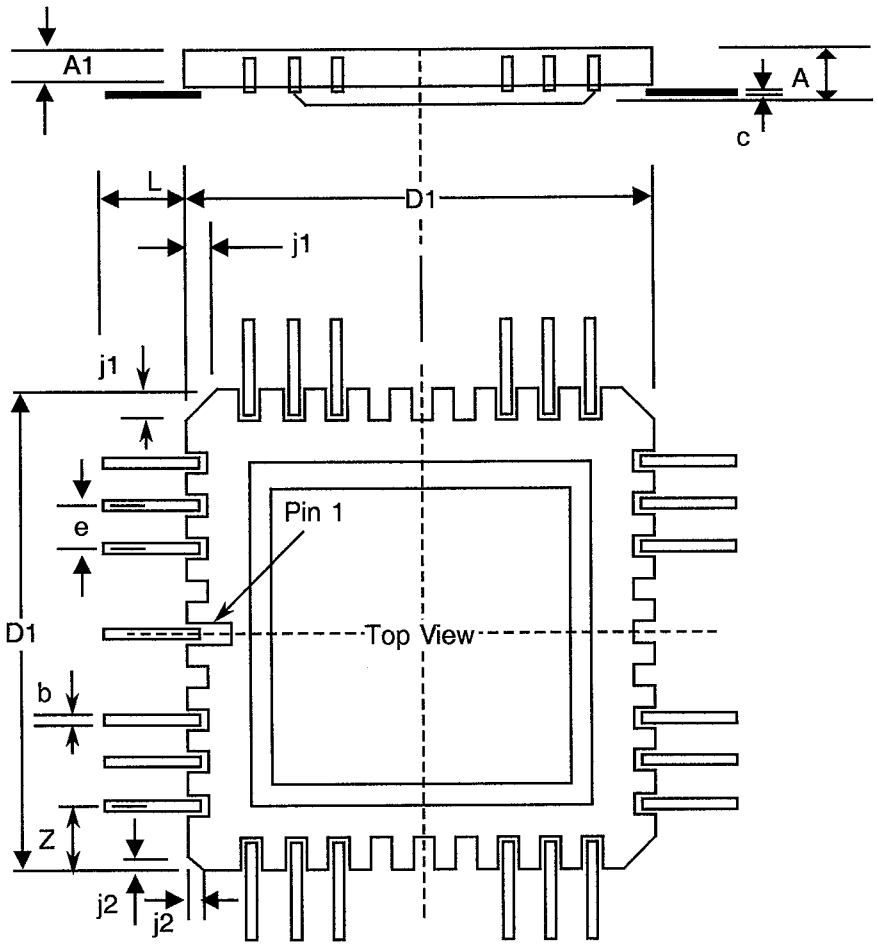


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	-	4.24	2
b	0.40	0.51	4
b1	-	1.53	4
c	0.20	0.31	4
D	-	82.17	
E	22.70 TYPICAL		
E1	22.86 TYPICAL		
E2	-	23.50	
e	2.54 TYPICAL		5,6
L	3.18	4.36	4
Q	1.02	1.53	3
S	-	1.27	7
∝	0°	15°	8

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(c) - FLAT PACKAGE, 68 TERMINAL



SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	-	2.59	3
A1	1.83	2.24	
b	0.25	0.51	
c	0.10	0.20	4
D1	23.88	24.51	
e	2.54 TYPICAL		2
j1	1.02 TYPICAL		
j2	0.51 TYPICAL		
L	8.89	9.27	
Z	1.65	2.16	

NOTES: See Page 10.

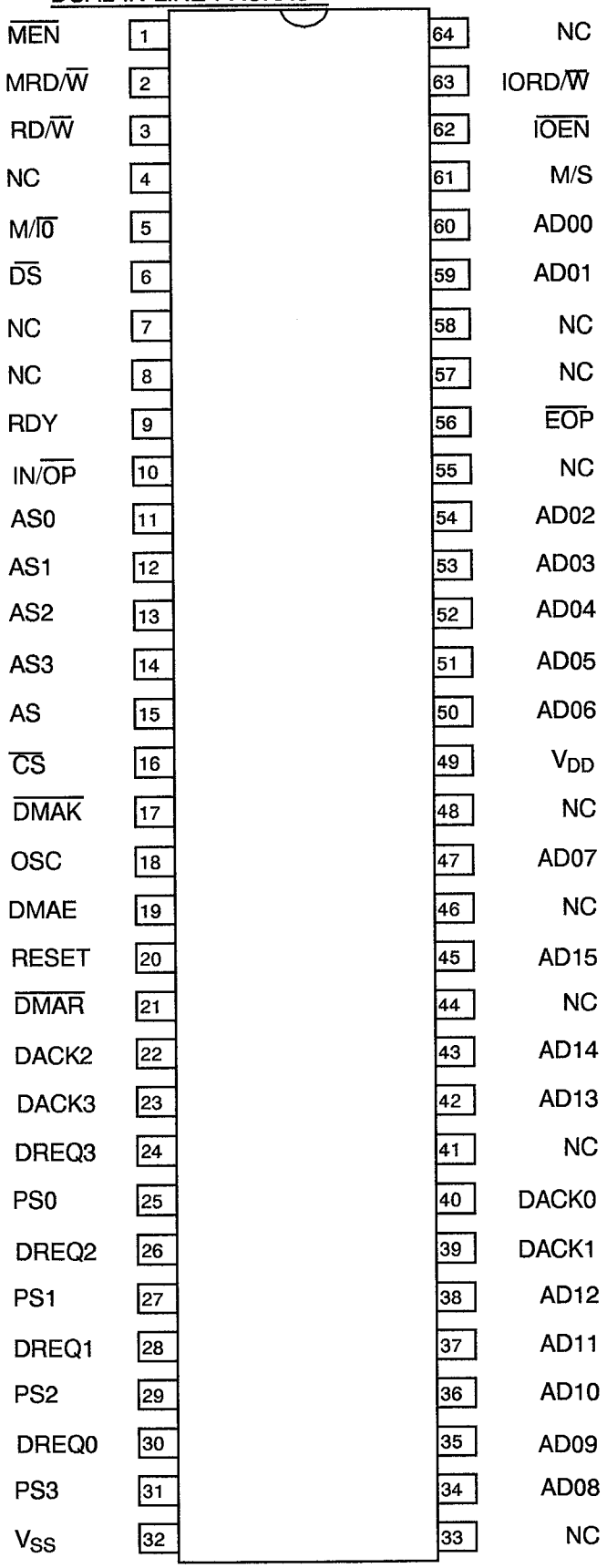
FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURES 2(a) TO 2(c) INCLUSIVE

1. Index area; a notch, letter or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown.
2. This dimension includes any lid.
3. The dimension shall be measured from the seating plane to the base plane.
4. All leads.
5. 62 spaces for dual-in-line packages.
   64 spaces for flat packages.
6. The true position pins spacing is 2.54mm between centre lines. Each pin centreline shall be located within 0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.
7. All 4 corners.
8. Lead centre when $\propto$ is 0°.
9. The dimension shall be measured at the point of exit of the lead from the body.

FIGURE 3(a) - PIN ASSIGNMENT

DUAL-IN-LINE PACKAGE



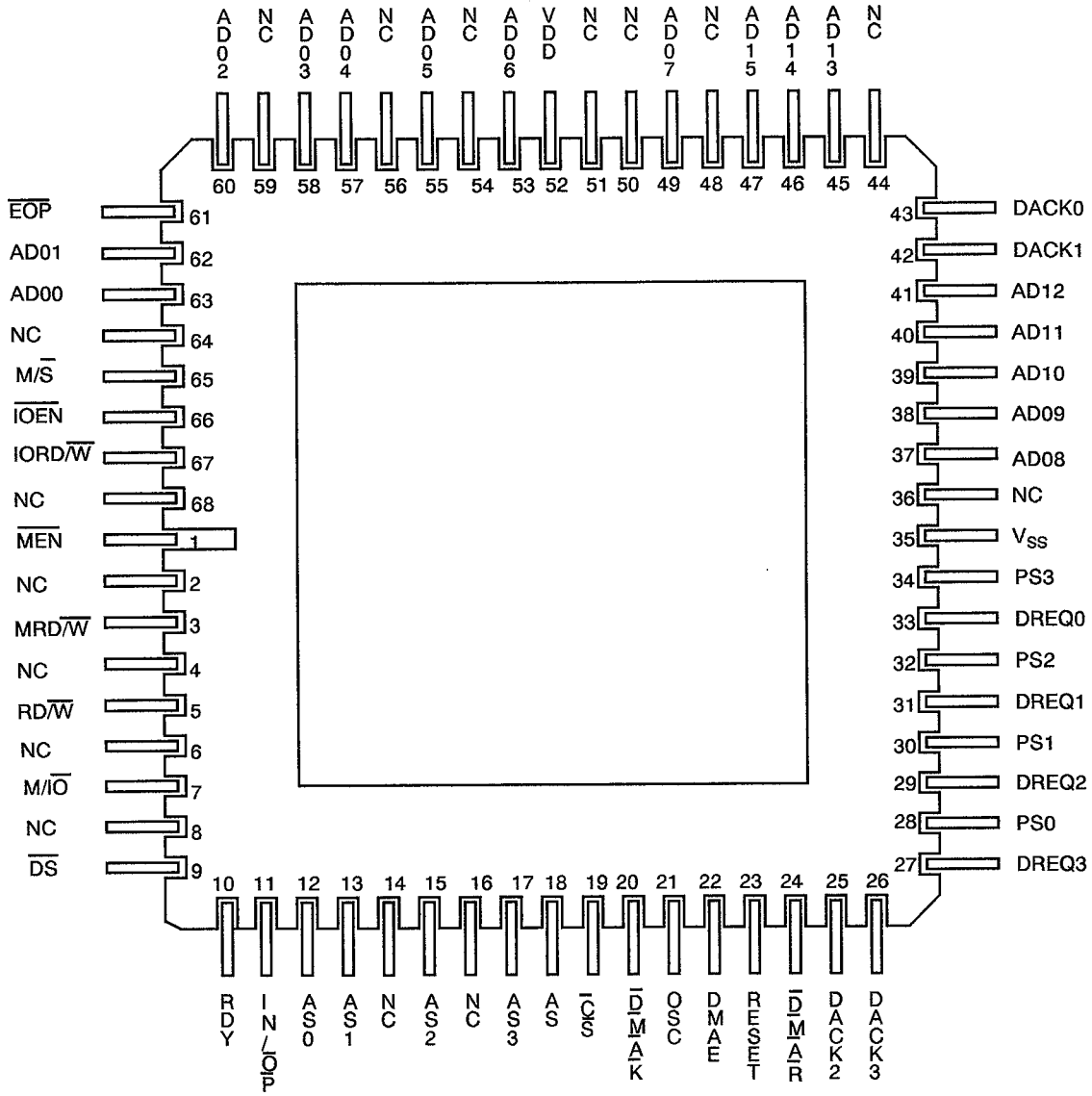
TOP VIEW

NOTES

1. For pin descriptions, see Page 13.

FIGURE 3(a) - PIN ASSIGNMENT (CONTINUED)

FLAT PACKAGE



TOP VIEW

NOTES

1. For pin descriptions, see Page 13.

FIGURE 3(a) - PIN ASSIGNMENT (CONTINUED)

PIN DESCRIPTION

SYMBOL	DESCRIPTION	FUNCTION	PIN NUMBER	
			DIL	F/P
$\overline{MEN}$	Memory Enable	Output	1	1
MRD/$\overline{W}$	Memory Read/Write	Output	2	3
RD/$\overline{W}$	Read/Write	Input	3	5
M/$\overline{IO}$	Memory or I/O	Input	5	7
$\overline{DS}$	Data Strobe	Input/Output	6	9
RDY	Ready	Input	9	10
IN/$\overline{OP}$	Instruction/Operation	Output	10	11
AS0	Address Status	Output	11	12
AS1	Address Status	Output	12	13
AS2	Address Status	Output	13	15
AS3	Address Status	Output	14	17
AS	Address Strobe	Input/Output	15	18
$\overline{CS}$	Chip Select	Input	16	19
$\overline{DMAK}$	DMA Acknowledge	Input	17	20
OSC	Clock Input	Input	18	21
DMAE	DMA Enable	Input	19	22
RESET	Reset	Input	20	23
$\overline{DMAR}$	DMA Request	Output	21	24
DACK2	DMA Acknowledge	Output	22	25
DACK3	DMA Acknowledge	Output	23	26
DREQ3	DMA Request	Input	24	27
PS0	Process Status	Output	25	28
DREQ2	DMA Request	Input	26	29
PS1	Process Status	Output	27	30
DREQ1	DMA Request	Input	28	31
PS2	Process Status	Output	29	32

SYMBOL	DESCRIPTION	FUNCTION	PIN NUMBER	
			DIL	F/P
DREQ0	DMA Request	Input	30	33
PS3	Process Status	Output	31	34
V_{SS}	Negative Supply	Input	32	35
AD08	Address/Data Bus	Input/Output	34	37
AD09	Address/Data Bus	Input/Output	35	38
AD10	Address/Data Bus	Input/Output	36	39
AD11	Address/Data Bus	Input/Output	37	40
AD12	Address/Data Bus	Input/Output	38	41
DACK1	DMA Acknowledge	Output	39	42
DACK0	DMA Acknowledge	Output	40	43
AD13	Address/Data Bus	Input/Output	42	45
AD14	Address/Data Bus	Input/Output	43	46
AD15	Address/Data Bus	Input/Output	45	47
AD07	Address/Data Bus	Input/Output	47	49
V_{DD}	Positive Supply	Input	49	52
AD06	Address/Data Bus	Input/Output	50	53
AD05	Address/Data Bus	Input/Output	51	55
AD04	Address/Data Bus	Input/Output	52	57
AD03	Address/Data Bus	Input/Output	53	58
AD02	Address/Data Bus	Input/Output	54	60
$\overline{EOP}$	End of Process	Input/Output	56	61
AD01	Address/Data Bus	Input/Output	59	62
AD00	Address/Data Bus	Input/Output	60	63
M/$\overline{S}$	Master/Slave Mode	Input	61	65
$\overline{IOEN}$	Input/Output Enable	Output	62	66
IORD/$\overline{W}$	Input/Output-Read/Write	Output	63	67

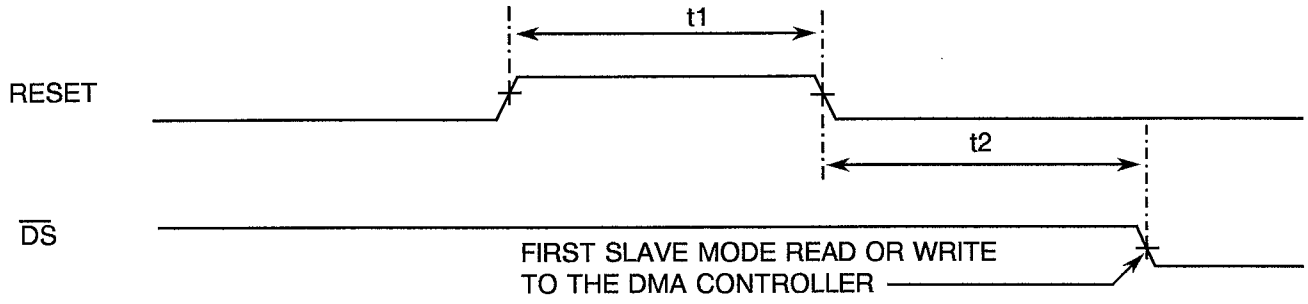
NOTES

1. The following pins have pull-down structures: AD00 to AD15, RD/$\overline{W}$, M/$\overline{IO}$, DMAE and AS.
   The following pins have pull-up structures: M/$\overline{S}$, $\overline{DS}$ and $\overline{DMAK}$.

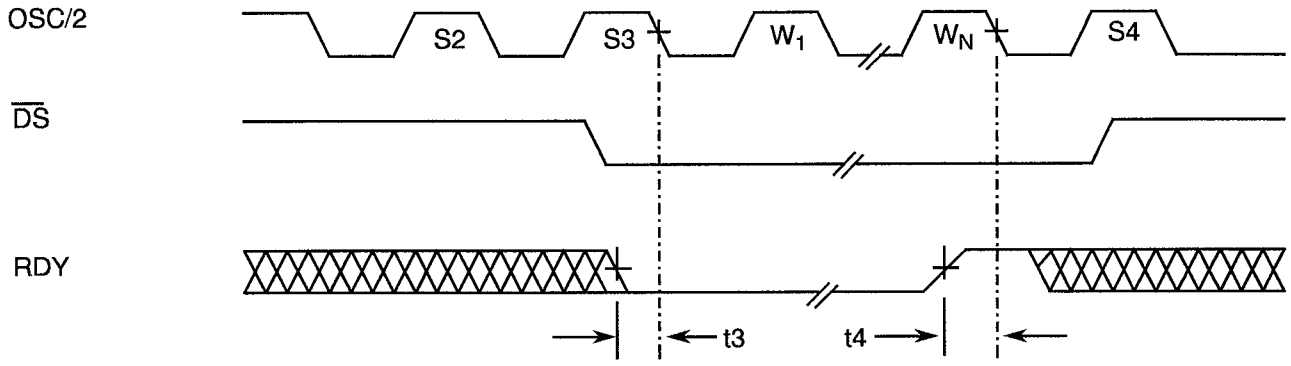
FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET

TIMING DIAGRAMS

REST TIMING DIAGRAM



READY TIMING DIAGRAM



PROGRAMME MODE CPU WRITE TIMING DIAGRAM

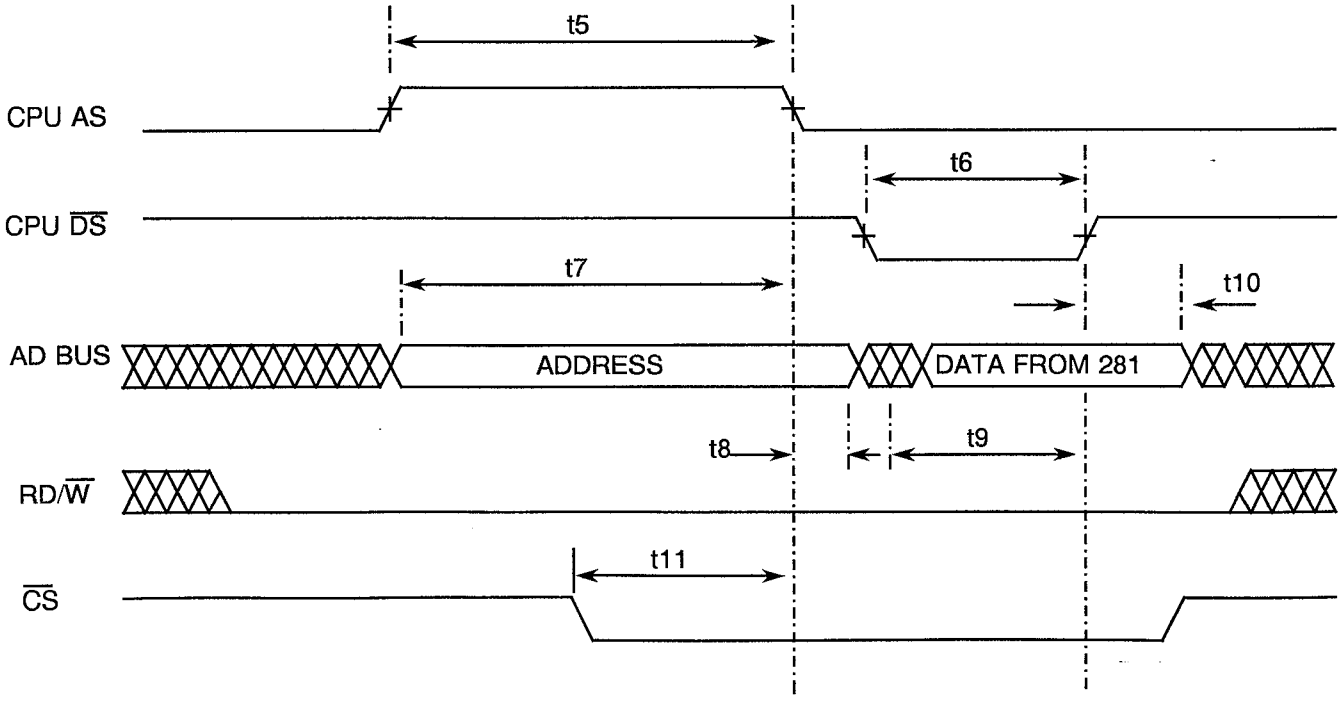
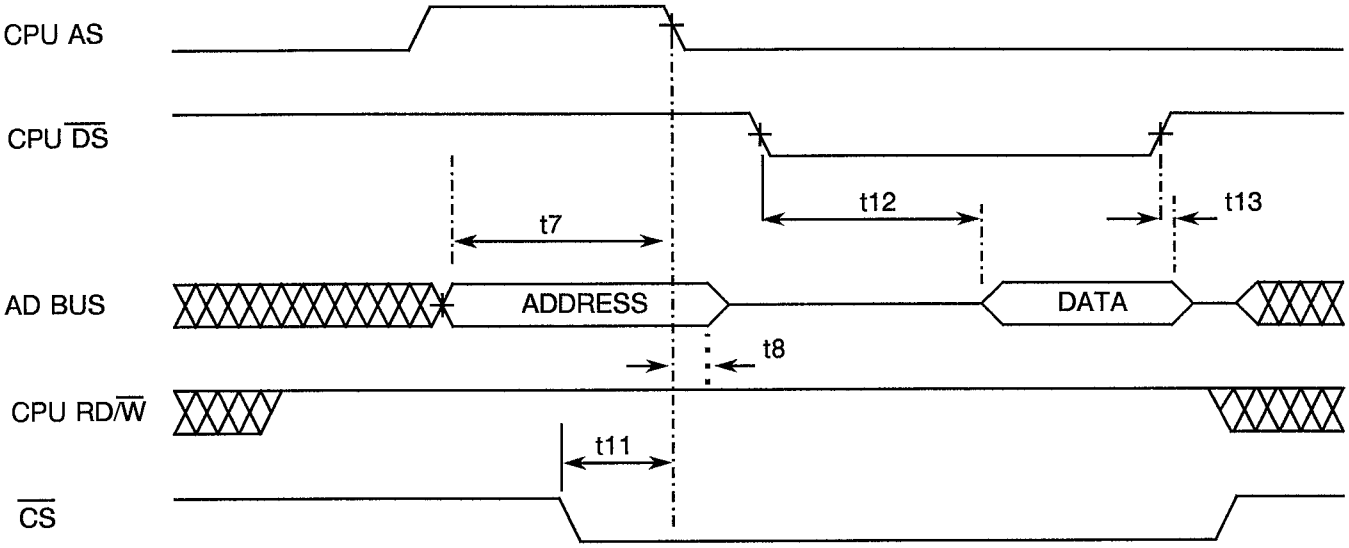


FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

TIMING DIAGRAMS (CONTINUED)

PROGRAME MODE CPU READ TIMING DIAGRAM



MEMORY AND I/O CONTROL SIGNAL (NON DMA) TIMING DIAGRAM

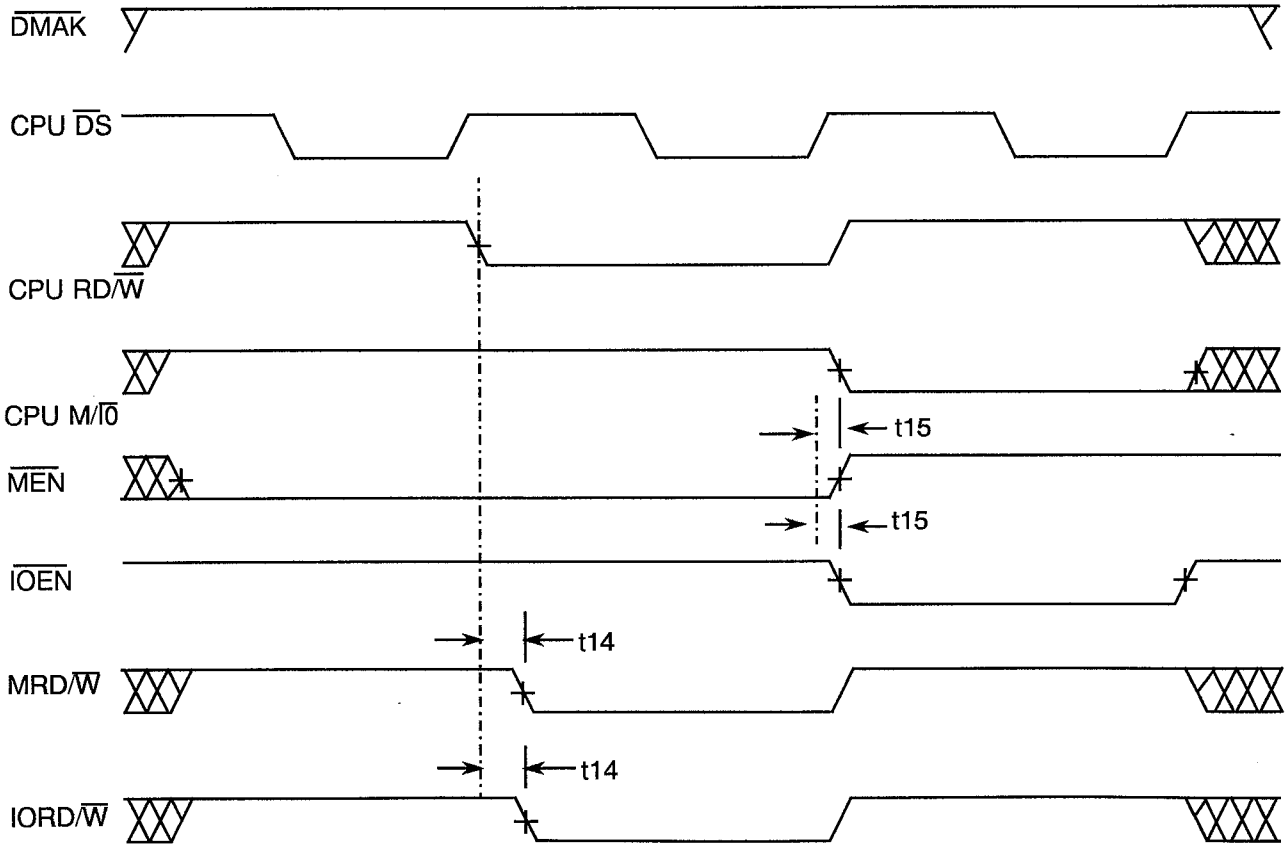
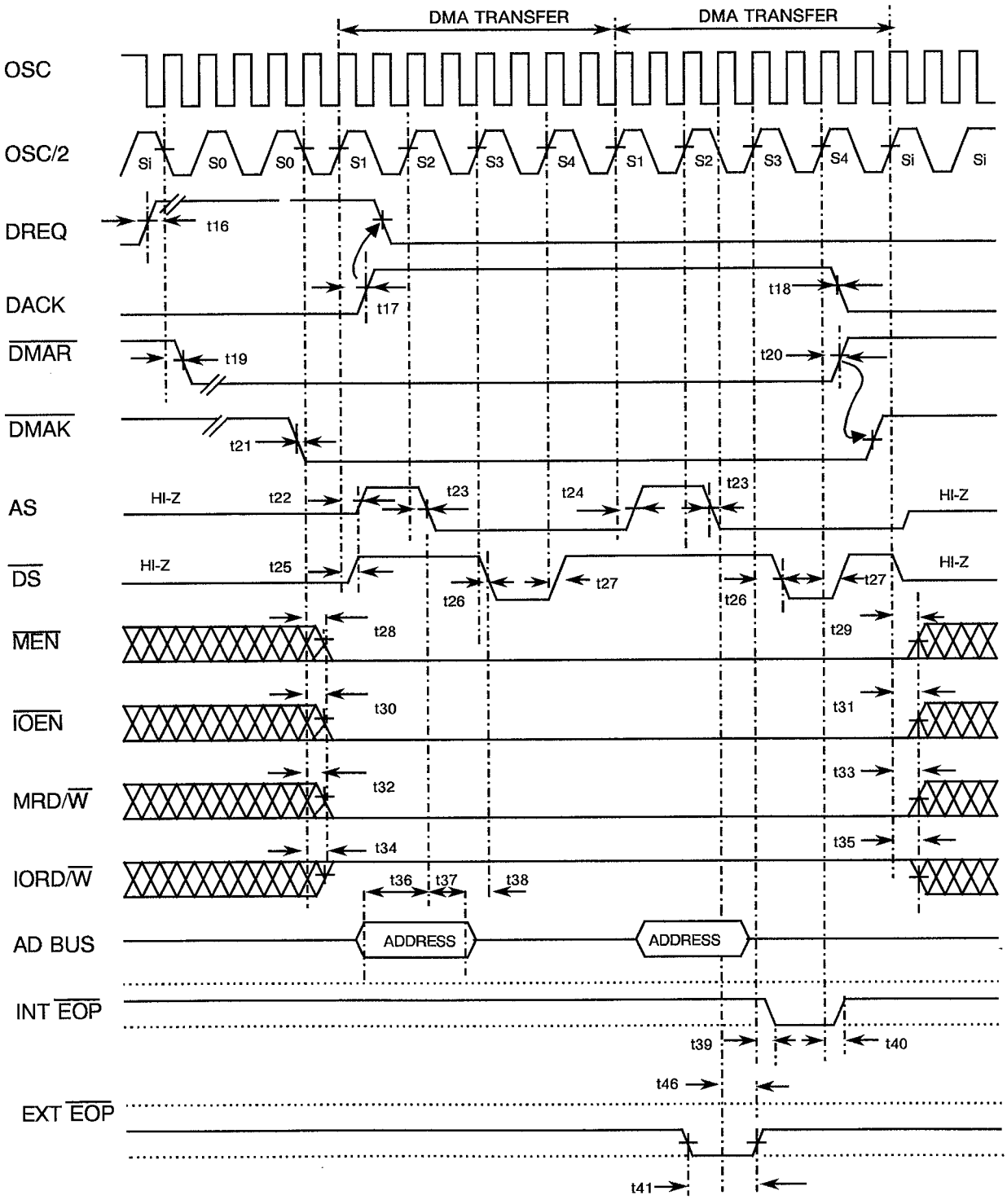


FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

TIMING DIAGRAMS (CONTINUED)

DMA TRANSFER, I/O TO MEMORY TIMING DIAGRAM



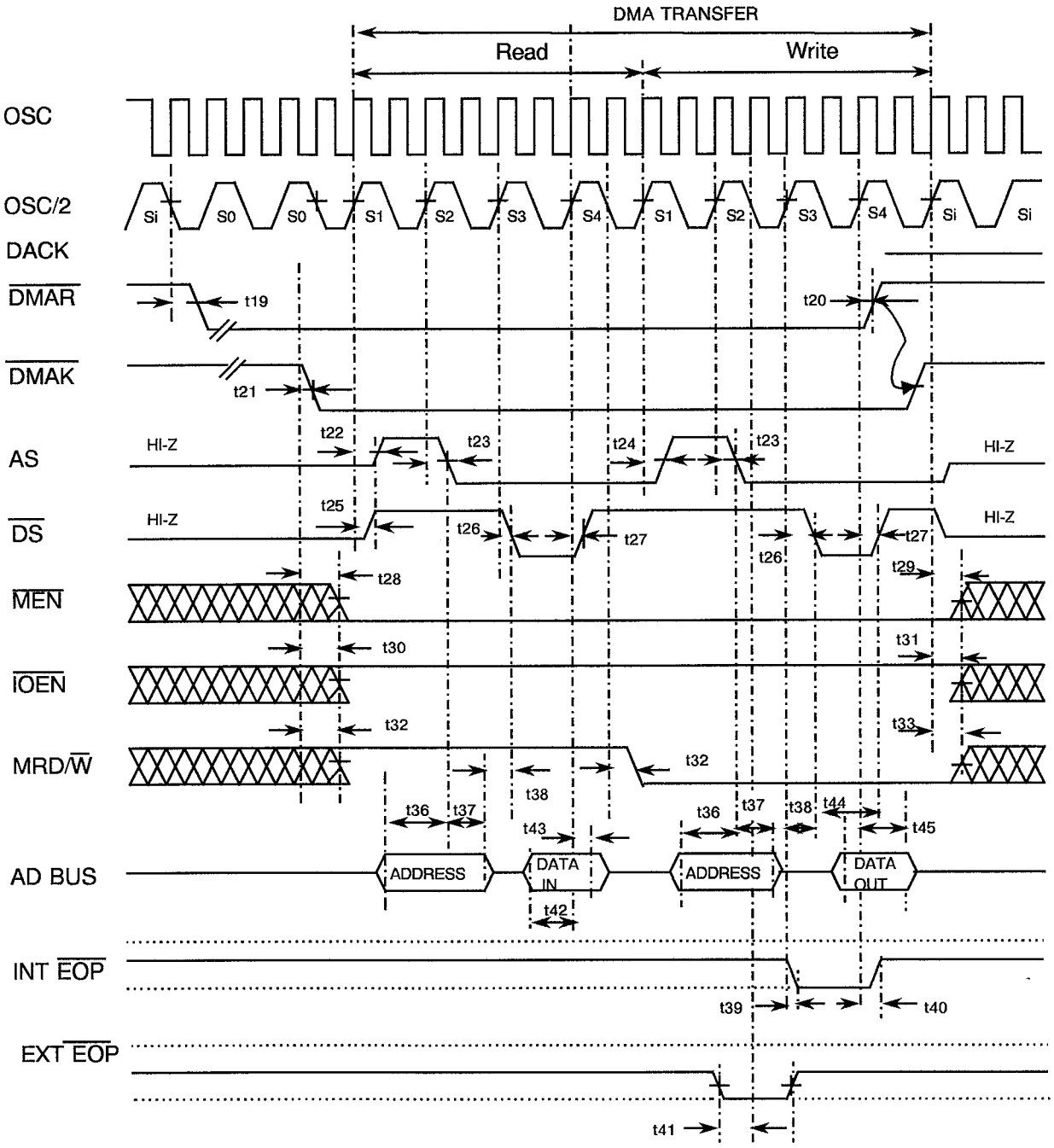
NOTES

1. OSC/2 is internally generated from the input signal OSC.
2. This diagram shows a peripheral to memory transfer. The control signals MRD/$\overline{W}$ and IORD/$\overline{W}$ are in the opposite state for a memory to peripheral transfer.

FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

TIMING DIAGRAM (CONTINUED)

DMA TRANSFER, MEMORY TO MEMORY TIMING DIAGRAM



NOTES

1. OSC/2 is internally generated from the input signal OSC.
2. A memory to memory transfer is initiated by setting a software DREQ for channel 0.

FIGURE 3(c) - CIRCUIT DESCRIPTION

OSC - This is the clock input and is used to generate the timing for internal operations and rate of data transfer. The maximum clock input is 20MHz.

OSC/2 - This is the internal clock and is derived from OSC.

RDY - A logic 1 on this input signal allows the MAS28137 to complete the machine cycle. A logic 0 is used to extend the data strobe signal from the MAS28137 to accommodate slow memories or I/O peripheral devices.

DMAE - The active logic 1 input signal DMA enable from the Central processing unit (C.P.U.) indicates that DMA requests from the controller will be acknowledged.

$\overline{\text{DMAK}}$ - The C.P.U. sets $\overline{\text{DMAK}}$ to logic 0 to indicate it has relinquished control of the system busses.

$\overline{\text{DMAR}}$ - The DMA controller requests control of the system bus from the C.P.U. by setting $\overline{\text{DMAR}}$ to logic 0. If the corresponding mask bit is clear, presence of a valid request causes the MAS28317 to issue the $\overline{\text{DMAR}}$ to the processor. After the $\overline{\text{DMAR}}$ goes active at least one clock cycle must occur before $\overline{\text{DMAK}}$ goes active.

AD00 to AD15 - These connections carry multiplexed addresses and data when the MAS28137 has bus control.

$\overline{\text{DS}}$ - This is a 3-state active logic 0 signal. When $\overline{\text{DMAK}}$ is high, $\overline{\text{DS}}$ signal is generated by the system processor. When the $\overline{\text{DMAK}}$ line is low, DMA controller produces this signal. In both cases the rising edge of $\overline{\text{DS}}$ indicates that valid data is present on the AD bus.

AS - This 3-state active logic 1 signal functions in a similar way to $\overline{\text{DS}}$, except that its falling edge indicates the presence of a valid address on the AD bus.

$\overline{\text{CS}}$ - Chip select is an active logic 0 input used to select the MAS28137 as an I/O device during the idle cycle. This allows the C.P.U. to communicate with the DMA Controller across the data bus.

RESET - Reset is an active logic 1 input which clears the command status, request and temporary registers, and sets the mask register. Following a reset the device is in the idle cycle.

DREQ0-3 - The DMA request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. The polarity of DREQ lines is programmable. Reset initialises them to active logic 1 in fixed priority. DREQ has the highest priority and DREQ3 the lowest. A request is generated by activating the DREQ line of a channel and DACK will acknowledge the recognition of the DREQ signal. Polarity of DREQ must be maintained until the corresponding DACK goes active.

DACKO-3 - These outputs are acknowledgements of DREQ prioritisation.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

$\overline{EOP}$ - End of process is an active logic 0 bidirectional signal. The MAS28137 allows an external $\overline{EOP}$ signal to terminate an active DMA service. This is accomplished by pulling the $\overline{EOP}$ line low. The MAS28137 also generates a pulse when the terminal count (TC) for a channel is reached. This generates an $\overline{EOP}$ signal which is output through the $\overline{EOP}$ line.

The reception of $\overline{EOP}$, either internal or external, will cause the MAS28137 to terminate the service, reset the request, and, if autoinitialise is enabled, to write the base registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by $\overline{EOP}$, unless the channel is programmed for autoinitialise. In this case, the mask bit remains clear. During memory to memory transfers, $\overline{EOP}$ will be output when the TC for Channel 1 occurs. $\overline{EOP}$ should be tied high with a pull-up resistor if it is not used so as to prevent erroneous end of process inputs.

RD/$\overline{W}$ - This input signal indicates the direction of data flow to and from the C.P.U. A logic 1 indicates a read by the processor.

M/$\overline{IO}$ - This is an input from the C.P.U. and indicates the type of instruction currently being executed by the processor.

$\overline{MEN}$ - When low, this output signal enables access to the system memory.

$\overline{IOEN}$ - When low, this output signal enables access to system I/O.

MRD/$\overline{W}$ - This output signal defines the direction of data transfer to and from the system. A logic 1 indicates a read from memory and a logic 0 a write to memory.

IORD/$\overline{W}$ - This output signal defines the direction of data transfer to and from system I/O. A logic 1 indicates a read from I/O, and a logic 0 a write to I/O.

M/$\overline{S}$ - When this output is set to a logic 1 and no DMAK has been issued, the controller is in master mode and will generate the system control signals MEN, IOEN, MRD/W and IORD/$\overline{W}$ from the incoming signals M/$\overline{IO}$ and RD/$\overline{W}$. A logic 0 places these outputs in a high impedance state, allowing another controller to drive these lines.

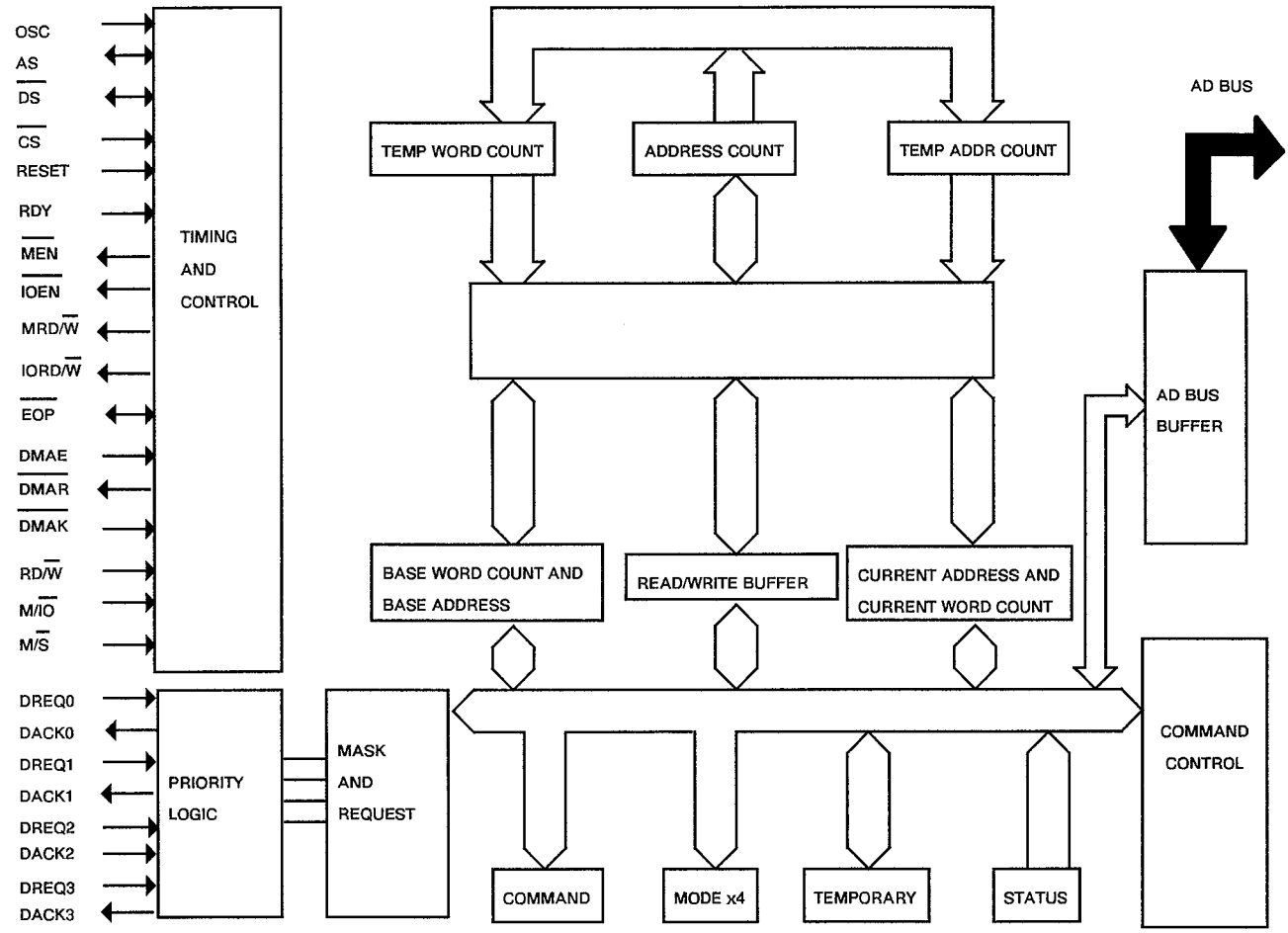
AS0 to AS3 - These 3-state outputs are used by an M.M.U. during expanded memory access to define the page register set used during DMA transfers.

PS0 to PS3 - These 3-state outputs are used by an M.M.U. during expanded memory access to provide page access protection during DMA transfers.

IN/$\overline{OP}$ - This I/O is produced to select the instruction or operand page register set in conjunction with the M.M.U.

FIGURE 3(d) - FUNCTIONAL DIAGRAM

DMA CONTROLLER PRINCIPAL FUNCTIONAL BLOCKS



DMA CONTROLLER CONNECTIONS

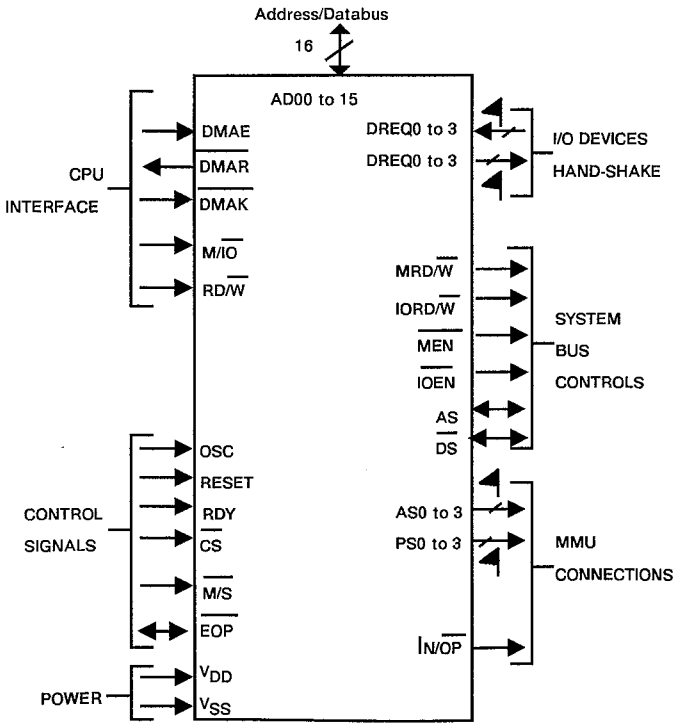
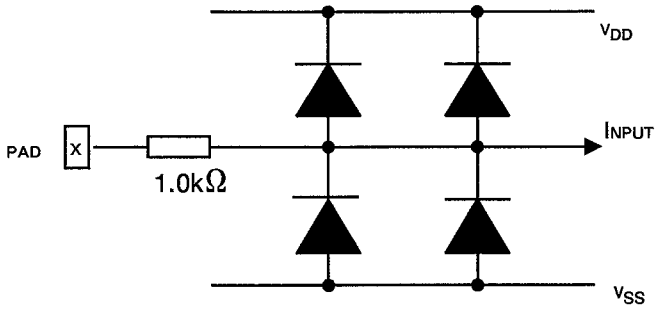


FIGURE 3(e) - INPUT PROTECTION NETWORK



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviation is used:-

V_{IC} - Input Clamp Voltage.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

(a) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during qualification and maintenance of qualification.

(b) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during procurement on lot acceptance basis at the total dose irradiation level specified in the Purchase Order.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

(a) Para. 7.1.1(a), H.T.R.B.: Shall not be performed.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 7.0 grammes.

4.3.3 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESA/SCC Basic Specification No. 9000. The test conditions shall be as follows:-

Applied Force: 1.0 ± 0.1 Newtons, 3 bends at 45°.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body and the lids shall be pre-form soldered.

4.4.2 Lead Material and Finish

The material shall be Type 'D' with Type '2' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

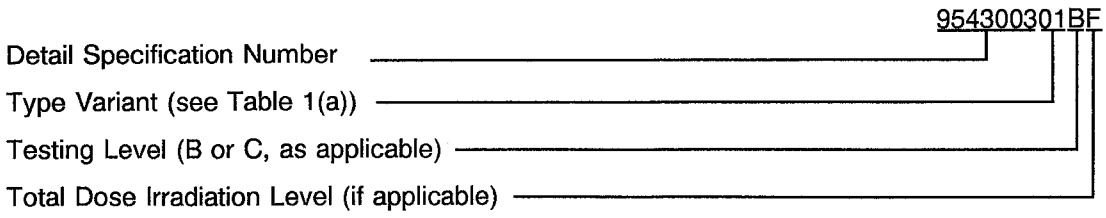
(c) Traceability Information.

4.5.2 Lead Identification

An index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



The Total Dose Irradiation Level designation shall be added for those devices for which a sample has been successfully tested to the level in question. For these devices, a code shall be added in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ °C and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +25 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for H.T.R.B. Burn-in

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for Power Burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for Power Burn-in shall be as specified in Table 5 of this specification.

4.7.4 Electrical Circuits for H.T.R.B. Burn-in

Not applicable.

4.7.5 Electrical Circuits for Power Burn-in

A circuit for use in performing the Power Burn-in test is shown in Figure 5 of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
1 to 2	Functional Test 1	-	3014	-	Verify Device Operation without Load V_{IL} = 0V, V_{IH} = 5.0V V_{OL} = V_{OH} = 1.5V V_{DD} = 5.0V, V_{SS} = 0V f_{OSC} = 1.0MHz, Pattern fma 001 f_{OSC} = 2.0MHz, Pattern fma 002	-	-	-
3	Functional Test 2	-	3014	-	Verify Device Operation without Load V_{IL} = 0.4V, V_{IH} = 3.0V V_{OL} = V_{OH} = 1.5V V_{DD} = 5.5V, V_{SS} = 0V f_{OSC} = 1.0MHz, Pattern fma 001	-	-	-
4	Functional Test 3	-	3014	-	Verify Device Operation without Load V_{IL} = 0.4V, V_{IH} = 3.0V V_{OL} = V_{OH} = 1.5V V_{DD} = 4.5V, V_{SS} = 0V f_{OSC} = 1.0MHz, Pattern fma 001	-	-	-
5	Quiescent Current	I_{DD}	3005	4(a)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V All Outputs Open Note 1 (Pin D 49) (Pin F 52)	-	2.0	mA
6 to 13	Input Current Low Level 1	I_{IL1}	3009	4(b)	V_{IN} (Under Test) = 0V V_{IN}(Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 9-16-18-20-24-26-28-30) (Pins F 10-19-21-23-27-29-31-33)	-	-1.0	µA
14 to 16	Input Current Low Level 2 (Pull-down)	I_{IL2}	3009	4(b)	V_{IN}(Under Test) = 0V R_P = 68kΩ V_{IN}(Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 3-5-19) (Pins F 5-7-22)	-	10	µA

NOTES: See Page 35.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
17 to 33	Input Current Low Level 3 (Pull-down)	I_{IL3}	3009	4(b)	V_{IN}(Under Test) = 0V R_p = 68kΩ V_{IN}(3-State Controls) = Note 2 V_{IN}(Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V Note 3 (Pins D 15-34-35-36-37-38-42-43-45-47-50-51-52-53-54-59-60) (Pins F 18-37-38-39-40-41-45-46-47-49-53-55-57-58-60-62-63)	-	-50	µA
34 to 35	Input Current Low Level 4 (Pull-up)	I_{IL4}	3009	4(b)	V_{IN}(Under Test) = 0V R_p = 68kΩ V_{IN}(Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 17-61) (Pins F 20-65)	-30	-300	µA
36	Input Current Low Level 5 (Pull-up)	I_{IL5}	3009	4(b)	V_{IN}(Under Test) = 0V R_p = 68kΩ V_{IN}(3-State Controls) = Note 2 V_{IN}(Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V Note 3 (Pin D 6) (Pin F 9)	-30	-300	µA
37 to 44	Input Current High Level 1	I_{IH1}	3010	4(c)	V_{IN}(Under Test) = 5.5V V_{IN}(Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 9-16-18-20-24-26-28-30) (Pins F 10-19-21-23-27-29-31-33)	-	1.0	µA
45 to 47	Input Current High Level 2 (Pull-down)	I_{IH2}	3010	4(c)	V_{IN}(Under Test) = 5.5V R_p = 68kΩ V_{IN}(Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 3-5-19) (Pins F 5-7-22)	30	300	µA

NOTES: See Page 35.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
48 to 64	Input Current High Level 3 (Pull-down)	I_{IH3}	3010	4(c)	V_{IN}(Under Test) = 5.5V R_p = 68kΩ V_{IN}(3-State Controls) = Note 2 V_{IN}(Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V Note 3 (Pins D 15-34-35-36-37-38-42-43-45-47-50-51-52-53-54-59-60) (Pins F 18-37-38-39-40-41-45-46-47-49-53-55-57-58-60-62-63)	30	300	µA
65 to 66	Input Current High Level 4 (Pull-up)	I_{IH4}	3010	4(c)	V_{IN}(Under Test) = 5.5V R_p = 68kΩ V_{IN}(Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 17-61) (Pins F 20-65)	-	10	µA
67	Input Current High Level 5 (Pull-up)	I_{IH5}	3010	4(c)	V_{IN}(Under Test) = 5.5V R_p = 68kΩ V_{IN}(3-State Controls) = Note 2 V_{IN}(Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V Note 3 (Pin D 6) (Pin F 9)	-	50	µA
68 to 104	Output Voltage Low Level	V_{OL}	3007	4(d)	V_{IL} = 0.4V, V_{IH} = 3.0V I_{OL} = 2.0MA V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins D 1-2-6-10-11-12-13-14-15-21-22-23-25-27-29-31-34-35-36-37-38-39-40-42-43-45-47-50-51-52-53-54-56-59-60-62-63) (Pins F 1-3-9-11-12-13-15-17-18-24-25-26-28-30-32-34-37-38-39-40-41-42-43-45-46-47-49-53-55-57-58-60-61-62-63-66-67)	-	0.4	V

NOTES: See Page 35.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
105 to 140	Output Voltage High Level	V_{OH}	3006	4(e)	V_{IL} = 0.4V, V_{IH} = 3.0V I_{OH} = -0.8mA V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins D 1-2-6-10-11-12-13-14-15-21-22-23-25-27-29-31-34-35-36-37-38-39-40-42-43-45-47-50-51-52-53-54-59-60-62-63) (Pins F 1-3-9-11-12-13-15-17-18-24-25-26-28-30-32-34-37-38-39-40-41-42-43-45-46-47-49-53-55-57-58-60-62-63-66-67)	2.4	-	V
141 to 172	Threshold Voltage N-Channel	V_{THN}	-	4(f)	V_{IN} = Note 5 V_{DD} = 5.5V, V_{SS} = 0V (Pins D 3-5-6-9-15-16-17-18-19-20-24-26-28-30-34-35-36-37-38-42-43-45-47-50-51-52-53-54-56-59-60-61) (Pins F 5-7-9-10-18-19-20-21-22-23-27-29-31-33-37-38-39-40-41-45-46-47-49-53-55-57-58-60-61-62-63-65)	0.8	-	V
173 to 204	Threshold Voltage P-Channel	V_{THP}	-	4(f)	V_{IN} = Note 5 V_{DD} = 5.5V, V_{SS} = 0V (Pins D 3-5-6-9-15-16-17-18-19-20-24-26-28-30-34-35-36-37-38-42-43-45-47-50-51-52-53-54-56-59-60-61) (Pins F 5-7-9-10-18-19-20-21-22-23-27-29-31-33-37-38-39-40-41-45-46-47-49-53-55-57-58-60-61-62-63-65)	-	2.0	V

NOTES: See Page 35.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
205 to 254	Input Clamp Voltage (to V_{SS})	V_{IC1}	-	4(g)	I_{IN}(Under Test) = -100µA V_{DD} = Open, V_{SS} = 0V All Other Pins Open (Pins D 1-2-3-5-6-9-10-11-12-13-14-15-16-17-18-19-20-21-22-23-24-25-26-27-28-29-30-31-34-35-36-37-38-39-40-42-43-45-47-50-51-52-53-54-56-59-60-61-62-63) (Pins F 1-3-5-7-9-10-11-12-13-15-17-18-19-20-21-22-23-24-25-26-27-28-29-30-31-32-33-34-37-38-39-40-41-42-43-45-46-47-49-53-55-57-58-60-61-62-63-65-66-67)	-0.1	-6.0	V
255 to 304	Input Clamp Voltage (to V_{DD})	V_{IC2}	-	4(g)	I_{IN}(Under Test) = 100µA V_{DD} = 0V, V_{SS} = Open All Other Pins Open (Pins D 1-2-3-5-6-9-10-11-12-13-14-15-16-17-18-19-20-21-22-23-24-25-26-27-28-29-30-31-34-35-36-37-38-39-40-42-43-45-47-50-51-52-53-54-56-59-60-61-62-63) (Pins F 1-3-5-7-9-10-11-12-13-15-17-18-19-20-21-22-23-24-25-26-27-28-29-30-31-32-33-34-37-38-39-40-41-42-43-45-46-47-49-53-55-57-58-60-61-62-63-65-66-67)	0.1	6.0	V
305 to 318	Output Leakage Current Third-State (Low Level Applied)	I_{OZL}	-	4(h)	V_{IN}(3-State Controls) = Note 2 V_{OUT} = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 1-2-10-11-12-13-14-25-27-29-31-56-62-63) (Pins F 1-3-11-12-13-15-17-28-30-32-34-61-66-67)	-	-10	µA

NOTES: See Page 35.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
319 to 332	Output Leakage Current Third-State (High Level Applied)	I_{OZH}	-	4(h)	V_{IN}(3-State Controls) = Note 2 V_{OUT} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 1-2-10-11-12-13-14-25-27-29-31-56-62-63) (Pins F1-3-11-12-13-15-17-28-30-32-34-61-66-67)	-	10	µA

NOTES: See Page 35.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D= DIP, F= FP)	LIMITS		UNIT
						MIN	MAX	
333 to 345	Input Capacitance	C_{IN}	3012	4(i)	V_{IN}(Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 6 (Pins D 3-5-9-16-17-18-19-20-24-26-28-30-61) (Pins F 5-7-10-19-20-21-22-23-27-29-31-33-65)	-	10	pF
346 to 364	Input/Output Capacitance	C_{IN}/O_{UT}	3012	4(i)	V_{IN}(Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 6 (Pins D 6-15-34-35-36-37-38-42-43-45-47-50-51-52-53-54-56-59-60) (Pins F 9-18-37-38-39-40-41-45-46-47-49-53-55-57-58-60-61-62-63)	-	10	pF
365 to 368	Functional Test 4	-	-	-	Verify Device Operation without Load $V_{IL} = 0V, V_{ih} = 4.0V$ $V_{OL} = V_{OH} = 1.5V$ $V_{DD} = 4.5V$ and 5.5V, $V_{SS} = 0V$ $f_{OSC} = 1.0MHz$, Pattern fma 001 $f_{OSC} = 2.0MHz$, Pattern fma 002	-	-	-
369 to 370	OSC Rise and Fall Time	tr/tf	3004	-	Note 6	-	10	ns
371 to 372	Minimum Reset Pulse Width	t1	3003	4(j)	$V_{DD} = 4.5V$ and 5.5V, $V_{SS} = 0V$ Notes 7 and 8	100	-	ns
373 to 374	Ready Low Setup to OSC	t3	3003	4(j)	$V_{DD} = 4.5V$ and 5.5V, $V_{SS} = 0V$ Notes 7 and 8	10	-	ns
375 to 376	Ready Low Setup to OSC	t4	3003	4(j)	$V_{DD} = 4.5V$ and 5.5V, $V_{SS} = 0V$ Notes 7 and 8	10	-	ns
377 to 378	Minimum AS Pulse Width	t5	3003	4(j)	$V_{DD} = 4.5V$ and 5.5V, $V_{SS} = 0V$ Notes 7 and 8	50	-	ns

NOTES: See Page 35.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
379 to 380	Minimum $\overline{DS}$ Pulse Width	t6	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	70	-	ns
381 to 382	Address Setup to AS Low (CPU Read/Write)	t7	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	25	-	ns
383 to 384	Address Hold to AS Low (CPU Read/Write)	t8	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	0	-	ns
385 to 386	Data Setup $\overline{DS}$ High (CPU Write)	t9	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	20	-	ns
387 to 388	Data Hold after $\overline{DS}$ High (CPU Write)	t10	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	0	-	ns
389 to 390	CS Setup to AS Low (CPU Read/Write)	t11	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	40	-	ns
391 to 392	$\overline{DS}$ Low to Data Valid (CPU Read)	t12	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	25	85	ns
393 to 394	Data Valid after $\overline{DS}$ High (CPU Read)	t13	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	15	50	ns
395 to 396	RD/$\overline{W}$ Low to MRD/$\overline{W}$ IORD/$\overline{W}$ (Non-DMA)	t14	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	-	45	ns
397 to 398	M/$\overline{IO}$ Low to $\overline{MEN}$ $\overline{IOEN}$ (Non-DMA)	t15	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	-	45	ns
399 to 400	DREQ Setup to OSC	t16	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	45	-	ns
401 to 402	OSC to DACK (Active)	t17	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	-	75	ns
403 to 404	OSC to DACK (Inactive)	t18	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	-	75	ns
405 to 406	OSC to $\overline{DMAR}$ Low	t19	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	-	60	ns

NOTES: See Page 35.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
407 to 408	OSC to $\overline{DMAR}$ High	t20	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	-	60	ns
409 to 410	$\overline{DMAK}$ Low Setup to OSC	t21	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7and 8	20	-	ns
411 to 412	OSC to AS High Impedance to High	t22	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7, 8 and 9		55	ns
413 to 414	OSC to AS High to Low	t23	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	-	55	ns
415 to 416	OSC to AS Low to High	t24	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	-	55	ns
417 to 418	OSC to $\overline{DS}$ High Impedance to High	t25	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7, 8 and 9	-	50	ns
419 to 420	OSC to $\overline{DS}$ High to Low	t26	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	-	50	ns
421 to 422	OSC to $\overline{DS}$ Low to High	t27	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	-	50	ns
423 to 424	OSC to $\overline{MEN}$ (Active)	t28	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	-	70	ns
425 to 426	OSC to $\overline{MEN}$ (Inactive)	t29	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	-	70	ns
427 to 428	OSC to $\overline{IOEN}$ (Active)	t30	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	-	70	ns
429 to 430	OSC to $\overline{IOEN}$ (Inactive)	t31	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	-	70	ns
431 to 432	OSC to MRD/$\overline{W}$ (Active)	t32	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	10	70	ns
433 to 434	OSC to MRD/$\overline{W}$ (Inactive)	t33	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	-	70	ns

NOTES: See Page 35.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
435 to 436	OSC to IORD/$\overline{W}$ Low	t34	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	-	70	ns
437 to 438	OSC to IORD/$\overline{W}$ (Inactive)	t35	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	-	70	ns
439 to 440	AS Low after Address Valid	t36	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	30	-	ns
441 to 442	Address High Impedance after AS Low	t37	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7, 8 and 9	10	-	ns
443 to 444	$\overline{DS}$ Low after Address High Impedance	t38	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7, 8 and 9	15	-	ns
445 to 446	OSC to Internal $\overline{EOP}$ High Impedance to Low	t39	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7, 8 and 9	-	55	ns
447 to 448	OSC to Internal $\overline{EOP}$ Low to High Impedance	t40	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7, 8 and 9	-	65	ns
449 to 450	External $\overline{EOP}$ Setup to OSC	t41	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	10	-	ns
451 to 452	Data Setup to OSC	t42	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	35	-	ns
453 to 454	Data Hold after OSC	t43	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	35	-	ns
455 to 456	$\overline{DS}$ High after Data Valid	t44	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	55	-	ns
457 to 458	Data High Impedance after $\overline{DS}$ High	t45	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7, 8 and 9	10	-	ns
459 to 460	Exernal $\overline{EOP}$ Hold from OSC	t46	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 8	-	10	ns
461 to 462	OSC to AS Low to High Impedance	t47	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7, 8 and 9	-	55	ns

NOTES: See Page 35.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
463 to 464	OSC to $\overline{DS}$ High to High Impedance	t48	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7, 8 and 9	-	55	ns
465 to 466	$\overline{DS}$ High to $\overline{DMAR}$ Low	t49	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 10	5.0	-	ns
467 to 468	$\overline{DS}$ High to Data In Invalid	t50	3003	-	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 7 and 10	5.0	-	ns
469 to 470	Reset to First Programme	t2	3003	-	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 11 and 12	100	-	ns

NOTES

1. Measurement is performed with the device having been initialised using functional test pattern fma 001.
2. The device is configured using a functional test pattern so that the pin under test is in the third-state condition for the measurement.
3. For I/O Ports, the measurements include the third-state output leakage currents (I_{OZL} and I_{OZH}).
4. The output pin under test is configured into the correct state for the measurement by using a functional test pattern on the inputs which produces a low or high level at the pin, as appropriate.
5. V_{IN} is applied to the pin under test and is varied until a change in output state occurs. The measured value is V_{TH}.
6. Guaranteed but not tested. Characterised at initial design and after major process changes.
7. V_{IL} = 0V, V_{IH} = 4.0V, f_{OSC} = 2.0MHz, Pattern fma 002.
8. Parameter measured during Functional Test 4.
9. 3-State timings measured by a 1.0V change in output voltage with an additional 1.0kΩ load to V_{SS} or V_{DD}.
10. Parameter is calculated using results of earlier measurement.
11. V_{IL} = 0V, V_{IH} = 4.0V, f_{OSC} = 1.0MHx, Pattern fma 001.
12. Parameter tested go-no-go during Functional Test 4.
13. Guaranteed but not tested at -55° C.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
1 to 2	Functional Test 1	-	3014	-	Verify Device Operation without Load V_{IL} = 0V, V_{IH} = 5.0V V_{OL} = V_{OH} = 1.5V V_{DD} = 5.0V, V_{SS} = 0V f_{OSC} = 1.0MHz, Pattern fma 001 f_{OSC} = 2.0MHz, Pattern fma 002	-	-	-
3	Functional Test 2	-	3014	-	Verify Device Operation without Load V_{IL} = 0.4V, V_{IH} = 3.0V V_{OL} = V_{OH} = 1.5V V_{DD} = 5.5V, V_{SS} = 0V f_{OSC} = 1.0MHz, Pattern fma 001	-	-	-
4	Functional Test 3	-	3014	-	Verify Device Operation without Load V_{IL} = 0.4V, V_{IH} = 3.0V V_{OL} = V_{OH} = 1.5V V_{DD} = 4.5V, V_{SS} = 0V f_{OSC} = 1.0MHz, Pattern fma 001	-	-	-
5	Quiescent Current	I_{DD}	3005	4(a)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V All Outputs Open Note 1 (Pin D 49) (Pin F 52)	-	10	mA
6 to 13	Input Current Low Level 1	I_{IL1}	3009	4(b)	V_{IN} (Under Test) = 0V V_{IN}(Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V Note 13 (Pins D 9-16-18-20-24-26-28-30) (Pins F 10-19-21-23-27-29-31-33)	-	-10	µA
14 to 16	Input Current Low Level 2 (Pull-down)	I_{IL2}	3009	4(b)	V_{IN}(Under Test) = 0V R_P = 68kΩ V_{IN}(Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 3-5-19) (Pins F 5-7-22)	-	-10	µA

NOTES: See Page 35.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
17 to 33	Input Current Low Level 3 (Pull-down)	I_{IL3}	3009	4(b)	V_{IN}(Under Test) = 0V R_p = 68kΩ V_{IN}(3-State Controls) = Note 2 V_{IN}(Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V Note 3 (Pins D 15-34-35-36-37-38-42-43-45-47-50-51-52-53-54-59-60) (Pins F 18-37-38-39-40-41-45-46-47-49-53-55-57-58-60-62-63)	-	-50	µA
34 to 35	Input Current Low Level 4 (Pull-up)	I_{IL4}	3009	4(b)	V_{IN}(Under Test) = 0V R_p = 68kΩ V_{IN}(Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 17-61) (Pins F 20-65)	-30	-300	µA
36	Input Current Low Level 5 (Pull-up)	I_{IL5}	3009	4(b)	V_{IN}(Under Test) = 0V R_p = 68kΩ V_{IN}(3-State Controls) = Note 2 V_{IN}(Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V Note 3 (Pin D 6) (Pin F 9)	-30	-300	µA
37 to 44	Input Current High Level 1	I_{IH1}	3010	4(c)	V_{IN}(Under Test) = 5.5V V_{IN}(Remaining Inputs) = 0V Note 13 V_{DD} = 5.5V, V_{SS} = 0V (Pins D 9-16-18-20-24-26-28-30) (Pins F 10-19-21-23-27-29-31-33)	-	10	µA
45 to 47	Input Current High Level 2 (Pull-down)	I_{IH2}	3010	4(c)	V_{IN}(Under Test) = 5.5V R_p = 68kΩ V_{IN}(Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 3-5-19) (Pins F 5-7-22)	30	300	µA

NOTES: See Page 35.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
48 to 64	Input Current High Level 3 (Pull-down)	I_{IH3}	3010	4(c)	V_{IN}(Under Test) = 5.5V R_p = 68kΩ V_{IN}(3-State Controls) = Note 2 V_{IN}(Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V Note 3 (Pins D 15-34-35-36-37-38-42-43-45-47-50-51-52-53-54-59-60) (Pins F 18-37-38-39-40-41-45-46-47-49-53-55-57-58-60-62-63)	30	300	µA
65 to 66	Input Current High Level 4 (Pull-up)	I_{IH4}	3010	4(c)	V_{IN}(Under Test) = 5.5V R_p = 68kΩ V_{IN}(Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 17-61) (Pins F 20-65)	-	10	µA
67	Input Current High Level 5 (Pull-up)	I_{IH5}	3010	4(c)	V_{IN}(Under Test) = 5.5V R_p = 68kΩ V_{IN}(3-State Controls) = Note 2 V_{IN}(Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V Note 3 (Pin D 6) (Pin F 9)	-	50	µA
68 to 104	Output Voltage Low Level	V_{OL}	3007	4(d)	V_{IL} = 0.4V, V_{IH} = 3.0V I_{OL} = 2.0MA V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins D 1-2-6-10-11-12-13-14-15-21-22-23-25-27-29-31-34-35-36-37-38-39-40-42-43-45-47-50-51-52-53-54-56-59-60-62-63) (Pins F 1-3-9-11-12-13-15-17-18-24-25-26-28-30-32-34-37-38-39-40-41-42-43-45-46-47-49-53-55-57-58-60-61-62-63-66-67)	-	0.4	V

NOTES: See Page 35.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
105 to 140	Output Voltage High Level	V_{OH}	3006	4(e)	V_{IL} = 0.4V, V_{IH} = 3.0V I_{OH} = -0.8mA V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins D 1-2-6-10-11-12-13-14-15-21-22-23-25-27-29-31-34-35-36-37-38-39-40-42-43-45-47-50-51-52-53-54-59-60-62-63) (Pins F 1-3-9-11-12-13-15-17-18-24-25-26-28-30-32-34-37-38-39-40-41-42-43-45-46-47-49-53-55-57-58-60-62-63-66-67)	2.4	-	V
141 to 172	Threshold Voltage N-Channel	V_{THN}	-	4(f)	V_{IN} = Note 5 V_{DD} = 5.5V, V_{SS} = 0V (Pins D 3-5-6-9-15-16-17-18-19-20-24-26-28-30-34-35-36-37-38-42-43-45-47-50-51-52-53-54-56-59-60-61) (Pins F 5-7-9-10-18-19-20-21-22-23-27-29-31-33-37-38-39-40-41-45-46-47-49-53-55-57-58-60-61-62-63-65)	0.8	-	V
173 to 204	Threshold Voltage P-Channel	V_{THP}	-	4(f)	V_{IN} = Note 5 V_{DD} = 5.5V, V_{SS} = 0V (Pins D 3-5-6-9-15-16-17-18-19-20-24-26-28-30-34-35-36-37-38-42-43-45-47-50-51-52-53-54-56-59-60-61) (Pins F 5-7-9-10-18-19-20-21-22-23-27-29-31-33-37-38-39-40-41-45-46-47-49-53-55-57-58-60-61-62-63-65)	-	2.0	V

NOTES: See Page 35.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
205 to 254	Input Clamp Voltage (to V_{SS})	V_{IC1}	-	4(g)	I_{IN}(Under Test) = -100µA V_{DD} = Open, V_{SS} = 0V All Other Pins Open (Pins D 1-2-3-5-6-9-10-11-12-13-14-15-16-17-18-19-20-21-22-23-24-25-26-27-28-29-30-31-34-35-36-37-38-39-40-42-43-45-47-50-51-52-53-54-56-59-60-61-62-63) (Pins F 1-3-5-7-9-10-11-12-13-15-17-18-19-20-21-22-23-24-25-26-27-28-29-30-31-32-33-34-37-38-39-40-41-42-43-45-46-47-49-53-55-57-58-60-61-62-63-65-66-67)	-0.1	-6.0	V
255 to 304	Input Clamp Voltage (to V_{DD})	V_{IC2}	-	4(g)	I_{IN}(Under Test) = 100µA V_{DD} = 0V, V_{SS} = Open All Other Pins Open (Pins D 1-2-3-5-6-9-10-11-12-13-14-15-16-17-18-19-20-21-22-23-24-25-26-27-28-29-30-31-34-35-36-37-38-39-40-42-43-45-47-50-51-52-53-54-56-59-60-61-62-63) (Pins F 1-3-5-7-9-10-11-12-13-15-17-18-19-20-21-22-23-24-25-26-27-28-29-30-31-32-33-34-37-38-39-40-41-42-43-45-46-47-49-53-55-57-58-60-61-62-63-65-66-67)	0.1	6.0	V
305 to 318	Output Leakage Current Third-State (Low Level Applied)	I_{OZL}	-	4(h)	V_{IN}(3-State Controls) = Notes 2 and 13 V_{OUT} = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 1-2-10-11-12-13-14-25-27-29-31-56-62-63) (Pins F 1-3-11-12-13-15-17-28-30-32-34-61-66-67)	-	-50	µA

NOTES: See Page 35.

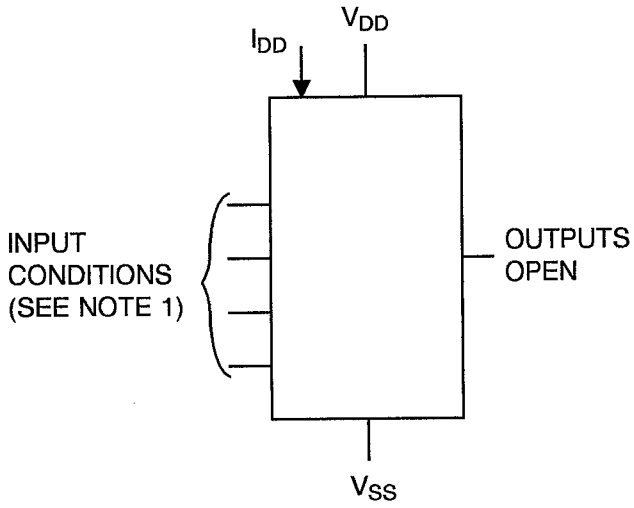
TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
319 to 332	Output Leakage Current Third-State (High Level Applied)	I_{OZH}	-	4(h)	V_{IN}(3-State Controls) = Notes 2 and 13 V_{OUT} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 1-2-10-11-12-13-14-25-27-29-31-56-62-63) (Pins F1-3-11-12-13-15-17-28-30-32-34-61-66-67)	-	50	µA

NOTES: See Page 35.

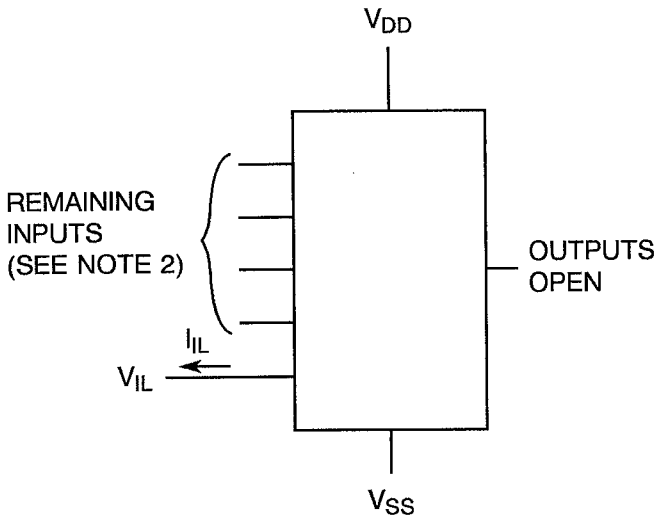
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - QUIESCENT CURRENT



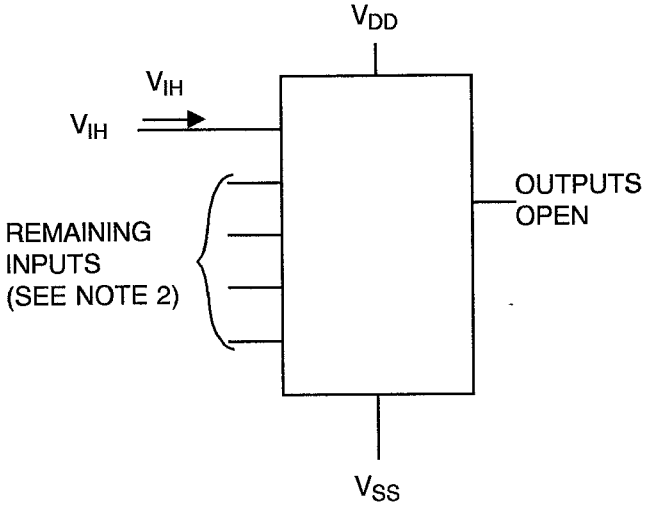
NOTES
1. Input conditions as per Table 2.

FIGURE 4(b) - INPUT CURRENT LOW LEVEL



NOTES
1. Each input to be tested separately.
2. Input conditions as per Table 2.

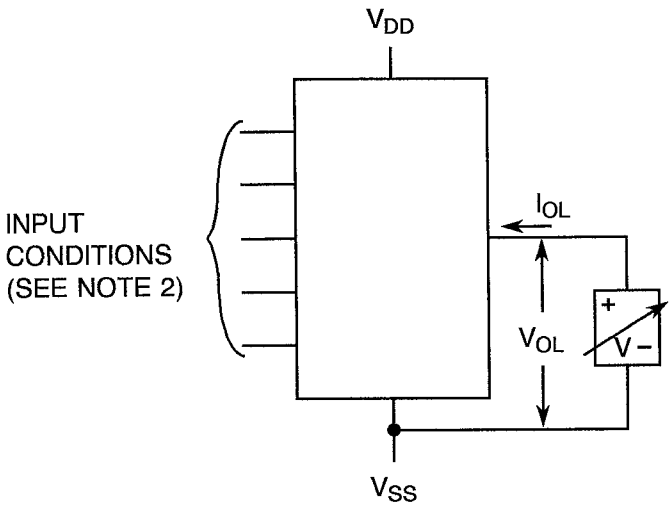
FIGURE 4(c) - INPUT CURRENT HIGH LEVEL



NOTES
1. Each input to be tested separately.
2. Input conditions as per Table 2.

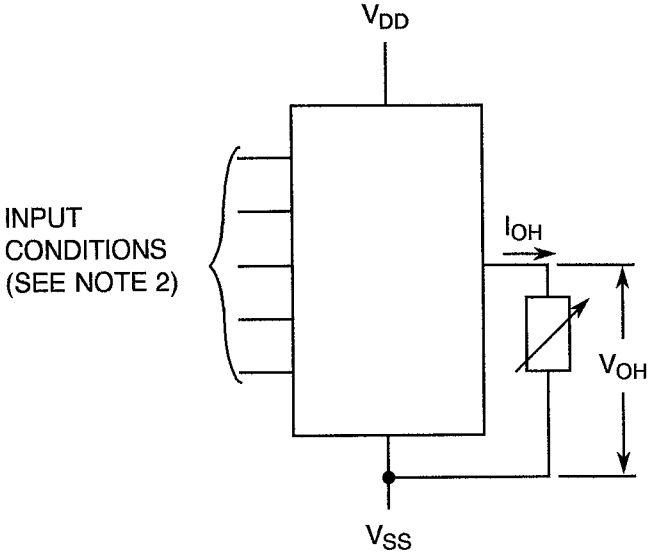
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(d) - OUTPUT VOLTAGE LOW LEVEL



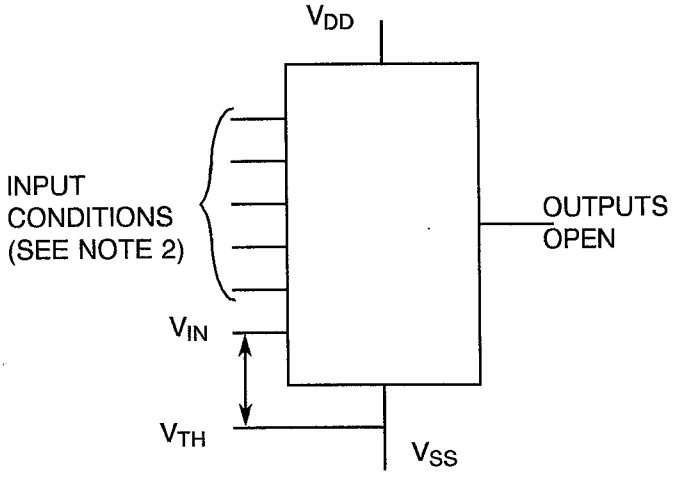
NOTES
1. Each output to be tested separately.
2. Input conditions as per Table 2.

FIGURE 4(e) - OUTPUT VOLTAGE HIGH LEVEL



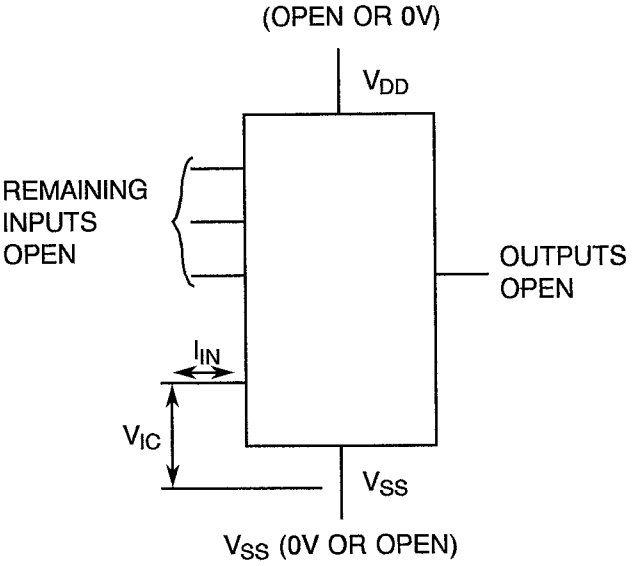
NOTES
1. Each output to be tested separately.
2. Input conditions as per Table 2.

FIGURE 4(f) - THRESHOLD VOLTAGE



NOTES
1. Each input to be tested separately.
2. Input conditions as per Table 2.

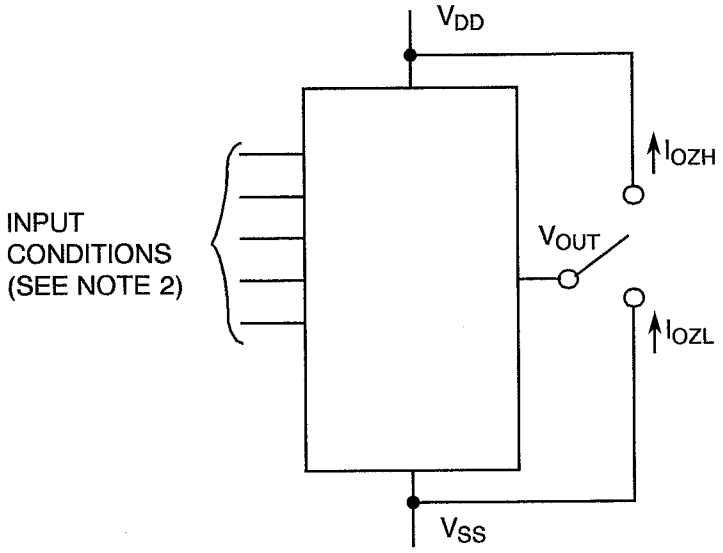
FIGURE 4(g) - INPUT CLAMP VOLTAGE



NOTES
1. Each input to be tested separately.

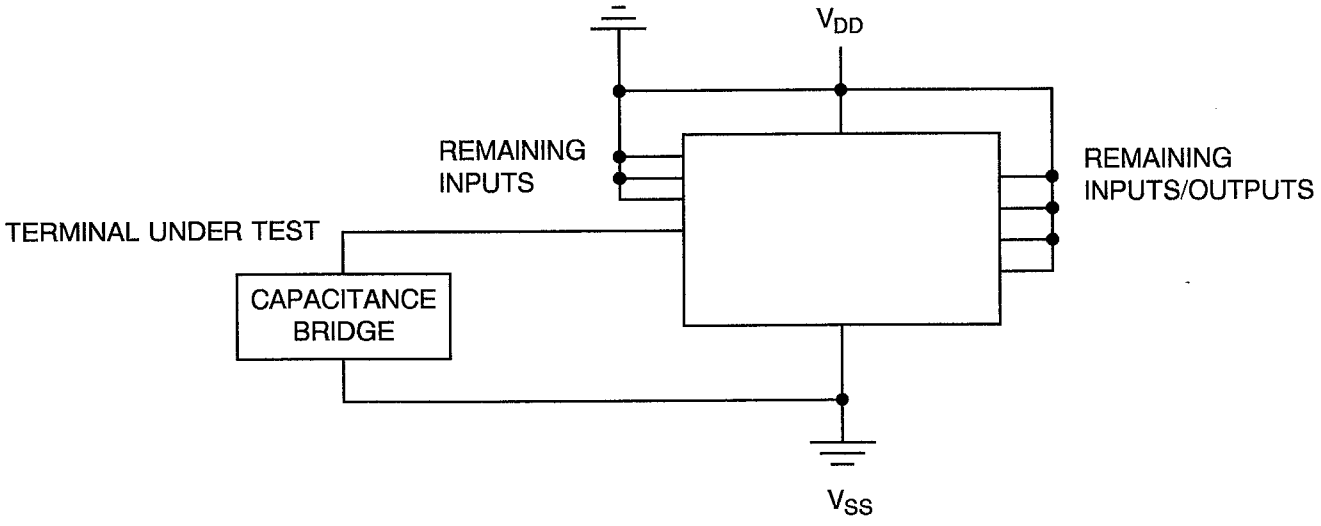
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(h) - OUTPUT LEAKAGE CURRENT THIRD STATE



NOTES
1. Each output to be tested separately.
2. Input conditions as per Table 2.

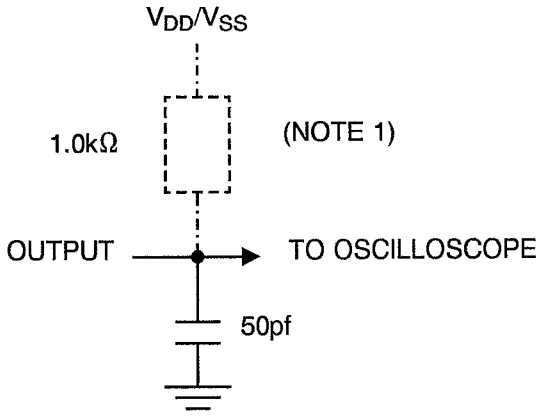
FIGURE 4(i) - INPUT AND INPUT/OUTPUT CAPACITANCE



NOTES
1. Test frequency = 1.0MHz.
2. Each input and input/output is to be tested separately.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(j) - PROPAGATION DELAY



NOTES

1. For high impedance timing measurements only.
2. Voltage waveforms as per Figure 3(b).

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
5	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	±500	µA
6 to 13	Input Current Low Level 1	I_{IL1}	As per Table 2	As per Table 2	±250	nA
37 to 44	Input Current High Level 1	I_{IH1}	As per Table 2	As per Table 2	±250	nA
68 to 104	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	±100	mV
105 to 140	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	±240	mV
305 to 318	Output Leakage Current (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	±4.0	µA
319 to 332	Output Leakage Current (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	±4.0	µA

TABLE 5 - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0−5)	°C
2	Outputs - (Pins D 1-2-10-11-12-13-14-21-22-23-25-27-29-31-39-40-62-63) - (Pins F 1-3-11-12-13-15-17-24-25-26-28-30-32-34-42-43-66-67)	V_{OUT}	$V_{DD/2}$	V
3	Inputs - (Pins D 5-9-17-56-61) - (Pins F 7-10-20-61-65)	V_{IN}	V_{DD}	V
4	Inputs - (Pins D 3-16-19-24-26-28-30) - (Pins F 5-19-22-27-29-31-33)	V_{IN}	V_{SS}	V
5	Input - (Pin D 18) - (Pin F 21)	V_{IN}	V_{GEN1}	Vac
6	Input/Output - (Pin D 15) - (Pin F 18)	V_{IN}	V_{GEN2}	Vac
7	Input/Output - (Pin D 6) - (Pin F 9)	V_{IN}	V_{GEN3}	Vac
8	Input/Outputs - (Pins D 34-35-36-37-38-42-43-45-47-50-51-52-53-54-59-60) - (Pins F 37-38-39-40-41-45-46-47-49-53-55-57-58-60-62-63)	V_{IN}	V_{GEN4}	Vac
9	Input - (Pin D 20) - (Pin F 23)	V_{IN}	V_{GEN5}	Vac
10	Pulse Voltage	V_{GEN}	0V to V_{DD}	Vac
11	Pulse Frequency Square Wave	f_{GEN1} f_{GEN2} f_{GEN3} f_{GEN4} f_{GEN5}	1.0M 125k 125k 125k 125k	Hz
12	Positive Supply Voltage (Pin D 49) (Pin F 52)	V_{DD}	5.5(+0−0.5)	V
13	Negative Supply Voltage (Pin D 32) (Pin F 35)	V_{SS}	0	V

TABLE 5 - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS - (CONT'D)

NOTES

1.

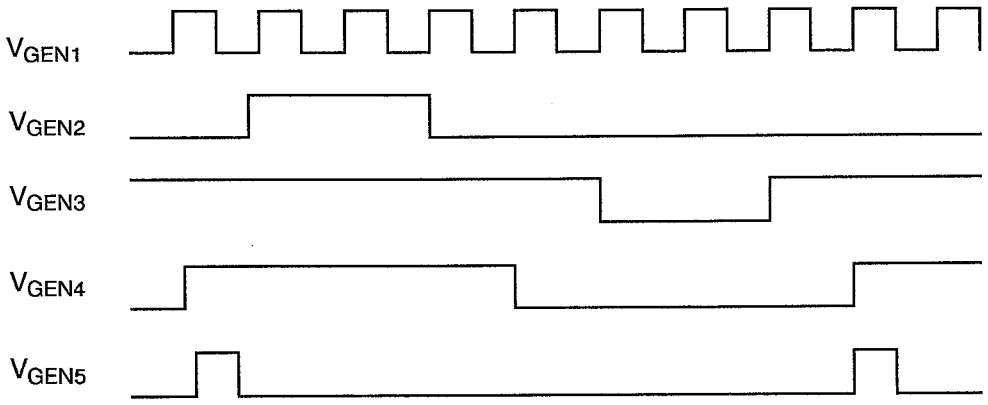
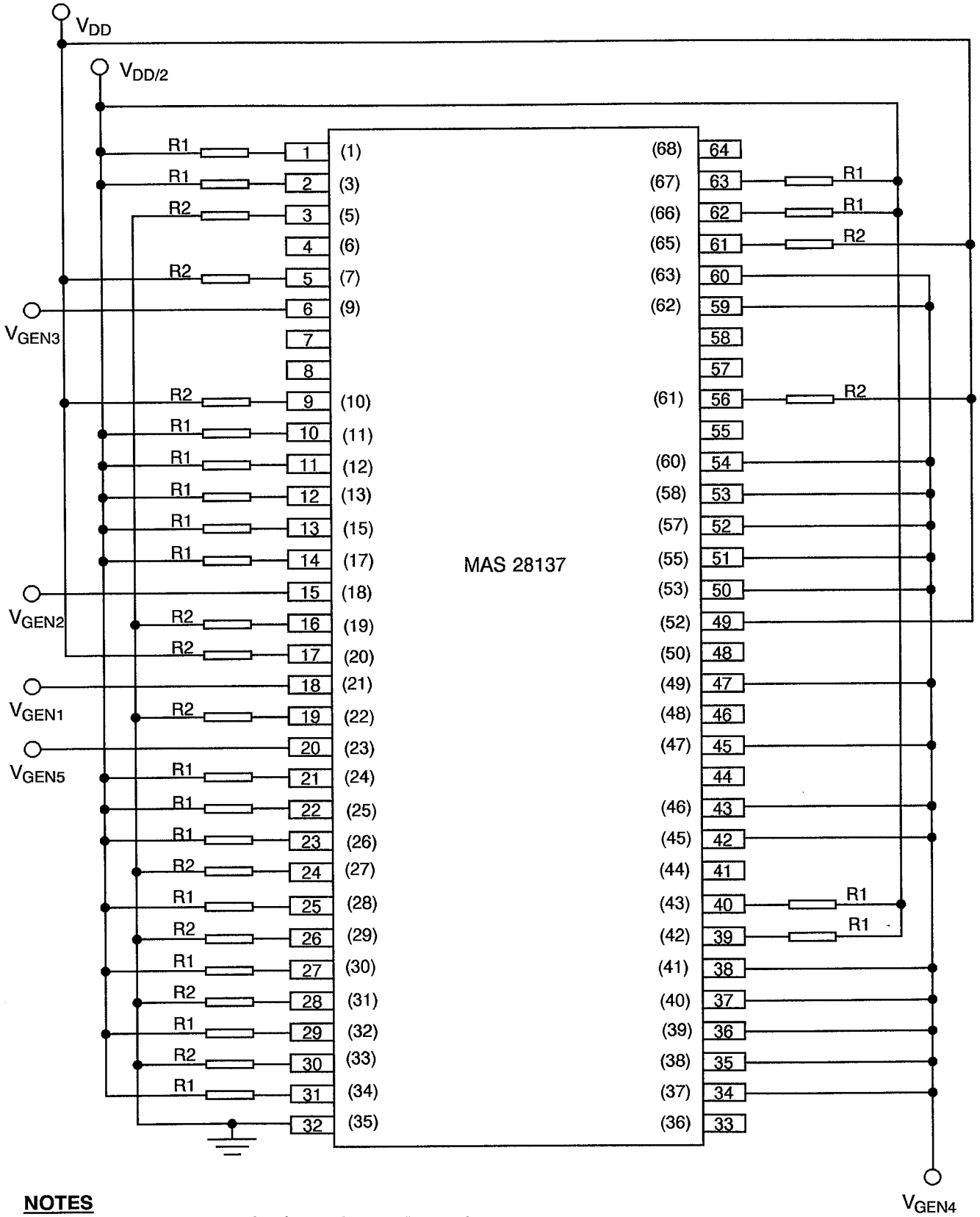


FIGURE 5 - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



NOTES

1. Pin numbers in parenthesis are for the flat package.
2. R1 = 2.7kΩ, R2 = 47kΩ.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5 of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5 of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

4.9 TOTAL DOSE IRRADIATION TESTING

4.9.1 Application

If specified in Para. 4.2.1 of this specification, total dose irradiation testing shall be performed in accordance with the requirements of ESA/SCC basic Specification No. 22900.

4.9.2 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6.

4.9.3 Electrical Measurements

The parameters to be measured prior to irradiation exposure are scheduled in Table 2 of the specification. Only devices which meet the requirements of Table 2 shall be scheduled in the test sample.

The parameters to be measured during and on completion of irradiation testing are scheduled in Table 7 of this specification.

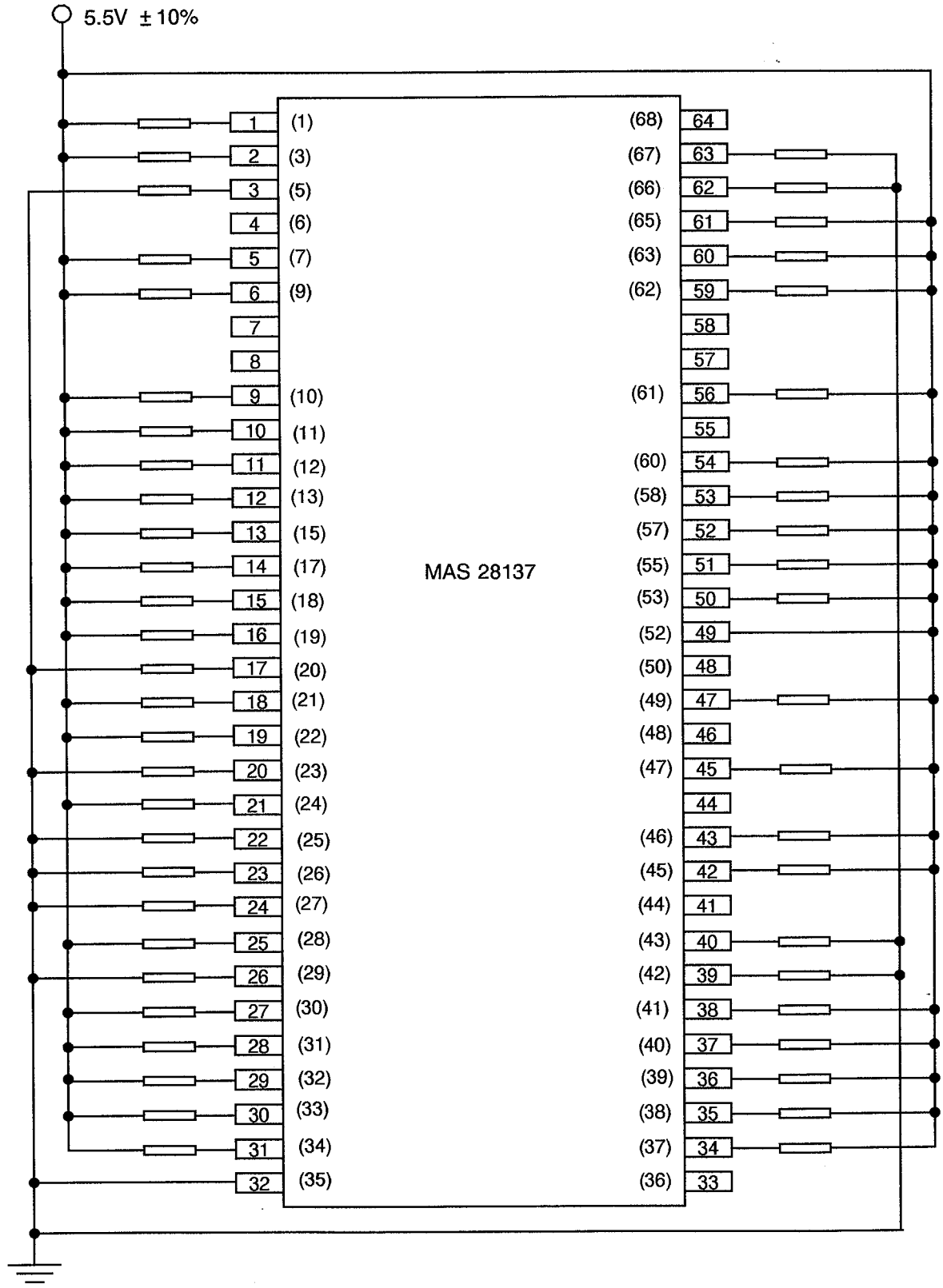
TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1 to 2	Functional Test 1	-	As per Table 2	As per Table 2	-	-	-
3	Functional Test 2	-	As per Table 2	As per Table 2	-	-	-
4	Functional Test 3	-	As per Table 2	As per Table 2	-	-	-
5	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	-	2.0	mA
6 to 13	Input Current Low Level 1	I_{IL1}	As per Table 2	As per Table 2	-	-1.0	µA
14 to 16	Input Current Low Level 2 (Pull-down)	I_{IL2}	As per Table 2	As per Table 2	-	-10	µA
17 to 33	Input Current Low Level 3 (Pull-down)	I_{IL3}	As per Table 2	As per Table 2	-	-50	µA
34 to 35	Input Current Low Level 4 (Pull-up)	I_{IL4}	As per Table 2	As per Table 2	-30	-300	µA
36	Input Current Low Level 5 (Pull-up)	I_{IL5}	As per Table 2	As per Table 2	-30	-300	µA
37 to 44	Input Curent High Level 1	I_{IH1}	As per Table 2	As per Table 2	-	1.0	µA
45 to 47	Input Current High Level 2 (Pull-down)	I_{IH2}	As per Table 2	As per Table 2	30	300	µA
48 to 64	Input Current High Level 3 (Pull-down)	I_{IH3}	As per Table 2	As per Table 2	30	300	µA
65 to 66	Input Current High Level 4 (Pull-up)	I_{IH4}	As per Table 2	As per Table 2	–	10	µA
67	Input Current High Level 5 (Pull-up)	I_{IH5}	As per Table 2	As per Table 2	–	50	µA
68 to 104	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	–	0.4	V
105 to 140	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	2.4	-	V

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
141 to 172	Threshold Voltage N-Channel	V_{THN}	As per Table 2	As per Table 2	0.8	-	V
173 to 204	Threshold Voltage P-Channel	V_{THP}	As per Table 2	As per Table 2	–	2.0	V
205 to 254	Input Clamp Voltage (to V_{SS})	V_{IC1}	As per Table 2	As per Table 2	-0.1	-6.0	V
255 to 304	Input Clamp Voltage to (V_{DD})	V_{IC2}	As per Table 2	As per Table 2	0.1	6.0	V
305 to 318	Output Leakage Current Third-State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	-	-10	µA
319 to 332	Output Leakage Current Third-State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	-	10	µA

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING



NOTES

1. Pin numbers in parenthesis are for the flat package.
2. Protection resistor = 10kΩ.

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1 to 2	Functional Test 1	-	As per Table 2	As per Table 2	-	-	-
5	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	-	10	mA
6 to 13	Input Current Low Level 1	I_{IL1}	As per Table 2	As per Table 2	-	-10	µA
14 to 16	Input Current Low Level 2 (Pull-down)	I_{IL2}	As per Table 2	As per Table 2	-	-10	µA
17 to 33	Input Current Low Level 3 (Pull-down)	I_{IL3}	As per Table 2	As per Table 2	-	-50	µA
34 to 35	Input Current Low Level 4 (Pull-up)	I_{IL4}	As per Table 2	As per Table 2	-30	-300	µA
36	Input Current Low Level 5 (Pull-up)	I_{IL5}	As per Table 2	As per Table 2	-30	-300	µA
37 to 44	Input Curent High Level 1	I_{IH1}	As per Table 2	As per Table 2	-	10	µA
45 to 47	Input Current High Level 2 (Pull-down)	I_{IH2}	As per Table 2	As per Table 2	30	300	µA
48 to 64	Input Current High Level 3 (Pull-down)	I_{IH3}	As per Table 2	As per Table 2	30	300	µA
65 to 66	Input Current High Level 4 (Pull-up)	I_{IH4}	As per Table 2	As per Table 2	–	10	µA
67	Input Current High Level 5 (Pull-up)	I_{IH5}	As per Table 2	As per Table 2	–	50	µA
68 to 104	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	–	0.4	V
105 to 140	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	2.4	-	V

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
141 to 172	Threshold Voltage N-Channel	V_{THN}	As per Table 2	As per Table 2	0.8	-	V
173 to 204	Threshold Voltage P-Channel	V_{THP}	As per Table 2	As per Table 2	–	2.0	V
305 to 318	Output Leakage Current Third-State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	-	-50	µA
319 to 332	Output Leakage Current Third-State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	-	50	µA

APPENDIX 'A'

AGREED DEVIATIONS FOR GPS (G.B.)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.3	Two additional optional tests may be performed: Static Burn-ins 1 and 2, as specified below. Each burn-in shall be 24 hours and Table 4 Parameter Drift Values shall be applied at 0 and 24 hours and 24 and 48 hours. If these tests are perfomed, they shall be recorded and counted for PDA.

CONDITIONS FOR STATIC BURN-IN 1

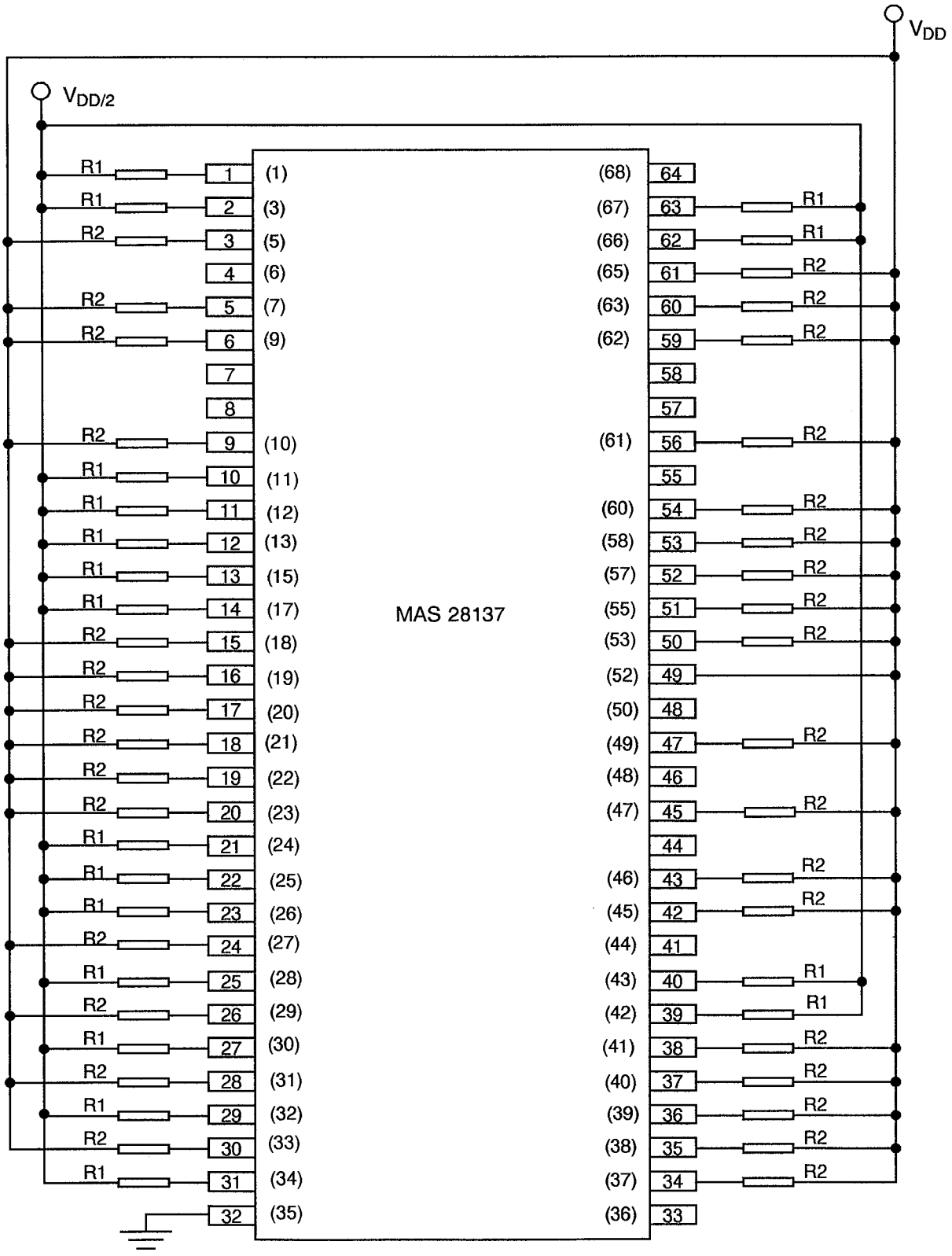
NO.	CHARACTERISTIC	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	Tamb	+125(+0−5)	°C
2	Outputs - (Pins D 1-2-10-11-12-13-14-21-22-23-25-27-29-31-39-40-62-63) - (Pins F 1-3-11-12-13-15-17-24-25-26-28-30-32-34-42-43-66-67)	V_{OUT}	$V_{DD/2}$	V
3	Inputs - (Pins D 3-5-9-16-17-18-19-20-24-26-28-30-61) - (Pins F 5-7-10-19-20-21-22-23-27-29-31-33-65)	V_{IN}	V_{DD}	V
4	Inputs/Outputs - (Pins D 6-15-34-35-36-37-38-42-43-45-47-50-51-52-53-54-56-59-60) - (Pins F 9-18-37-38-39-40-41-45-46-47-49-53-55-57-58-60-61-62-63)	$V_{IN/OUT}$	V_{DD}	V
5	Postive Supply Voltage - (Pin D 49) (Pin F 52)	V_{DD}	5.5(+0−0.5)	V
6	Negative Supply Voltage - (Pin D 32) (Pin F 35)	V_{SS}	0	V

CONDITIONS FOR STATIC BURN-IN 2

NO.	CHARACTERISTIC	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	Tamb	+125(+0−5)	°C
2	Outputs - (Pins D 1-2-10-11-12-13-14-21-22-23-25-27-29-31-39-40-62-63) - (Pins F 1-3-11-12-13-15-17-24-25-26-28-30-32-34-42-43-66-67)	V_{OUT}	$V_{DD/2}$	V
3	Inputs - (Pins D 3-5-9-16-17-18-19-20-24-26-28-30-61) - (Pins F 5-7-10-19-20-21-22-23-27-29-31-33-65)	V_{IN}	V_{SS}	V
4	Inputs/Outputs - (Pins D 6-15-34-35-36-37-38-42-43-45-47-50-51-52-53-54-56-59-60) - (Pins F 9-18-37-38-39-40-41-45-46-47-49-53-55-57-58-60-61-62-63)	$V_{IN/OUT}$	V_{SS}	V
5	Postive Supply Voltage - (Pin D 49) (Pin F 52)	V_{DD}	5.5(+0−0.5)	V
6	Negative Supply Voltage - (Pin D 32) (Pin F 35)	V_{SS}	0	V

APPENDIX 'A'

ELECTRICAL CIRCUIT FOR STATIC BURN-IN 1

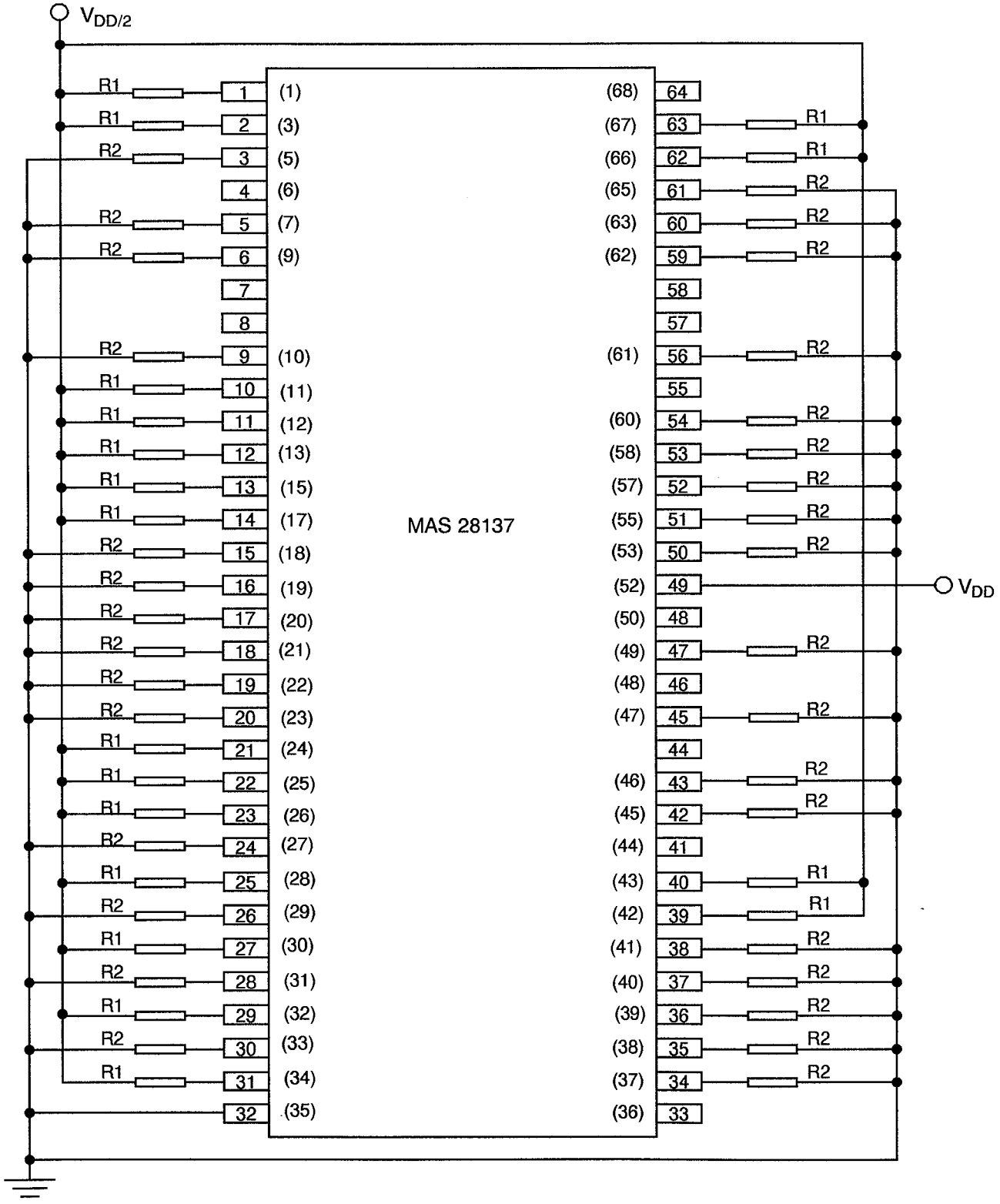


NOTES

1. Pin numbers in parenthesis are for the flat package.
2. R1 = 2.7kΩ, R2 = 47kΩ.

APPENDIX 'A'

ELECTRICAL CIRCUIT FOR STATIC BURN-IN 2



NOTES

1. Pin numbers in parenthesis are for the flat package.
2. R1 = 2.7kΩ, R2 = 47kΩ.