INTEGRATED CIRCUITS, SILICON MONOLITHIC,

HIGH PERFORMANCE PROGRAMMABLE

ARRAY LOGIC CIRCUIT,

BASED ON TYPE PAL20R8

ESCC Detail Specification No. 9304/006

ISSUE 1

October 2002

Document Custodian: European Space Agency - see https://escies.org

LEGAL DISCLAIMER AND COPYRIGHT

european space agency
agence spatiale européenne

Pages 1 to 52

INTEGRATED CIRCUITS, SILICON MONOLITHIC, HIGH PERFORMANCE PROGRAMMABLE ARRAY LOGIC CIRCUIT, BASED ON TYPE PAL20R8

ESA/SCC Detail Specification No. 9304/006

space components
coordination group

Issue/Rev.	Date	Approved by	
		SCCG Chairman	ESA Director General or his Deputy
Issue 1	May 1993		
Revision 'A'	January 1994		

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.
'A'	Jan. '94	P1. Cover Page		None
		P2. DCN		None
		P41. Table 4	: Limits for items 54 to 61, 62 to 69 and 70 to 77 amended	221093

TABLE OF CONTENTS

Page

TABLES

FIGURES

APPENDICES (Applicable to specific Manufacturers only)

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, High Performance Programmable Array Logic Circuit, based on Type PAL20R8. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 PROGRAMMING PROCEDURE

As per Figure 3(b).

1.8 PROGRAMMING MATRIX

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are catagorised as Class 1 with a Minimum Critical Path Failure Voltage of 500Volts.

TABLE 1(a) - TYPE VARIANTS

VARIANT	BASED ON TYPE	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
01	20R8-20	FLAT	2(a)	G4
02	20R8-20	D.I.L.	2(b)	G4
03	20R8-20	CHIP CARRIER	2(c)	7
04	20R8-20	CHIP CARRIER	2(c)	4
05	20R8-10	FLAT	2(a)	G4
06	20R8-10	D.I.L.	2(b)	G4
07	20R8-10	CHIP CARRIER	2(c)	7
08	20R8-10	CHIP CARRIER	2(c)	4

TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	NOTES
1	Supply Voltage	V_{CC}	7.0	V	Note 1
2	Input Voltage (Operating Condition)	V_{IN}	5.5	V	Note 1
3	Input Voltage (Programming and Test)	V_{IN}	10.75	V	-
4	Voltage applied to a disabled output	V_{OUT}	5.5	V	Note 1
5	Power Dissipation (Programmed) Variants 01 to 04 Variants 05 to 08	P_D	 0.99 1.21	W	-
6	Operating Temperature Range	T_{op}	−55 to +125	°C	T_{amb}
7	Storage Temperature Range	T_{stg}	−65 to +150	°C	-
8	Soldering Temperature For FP and DIP For CCP	T_{sol}	 +265 +245	°C	 Note 2 Note 3

NOTES

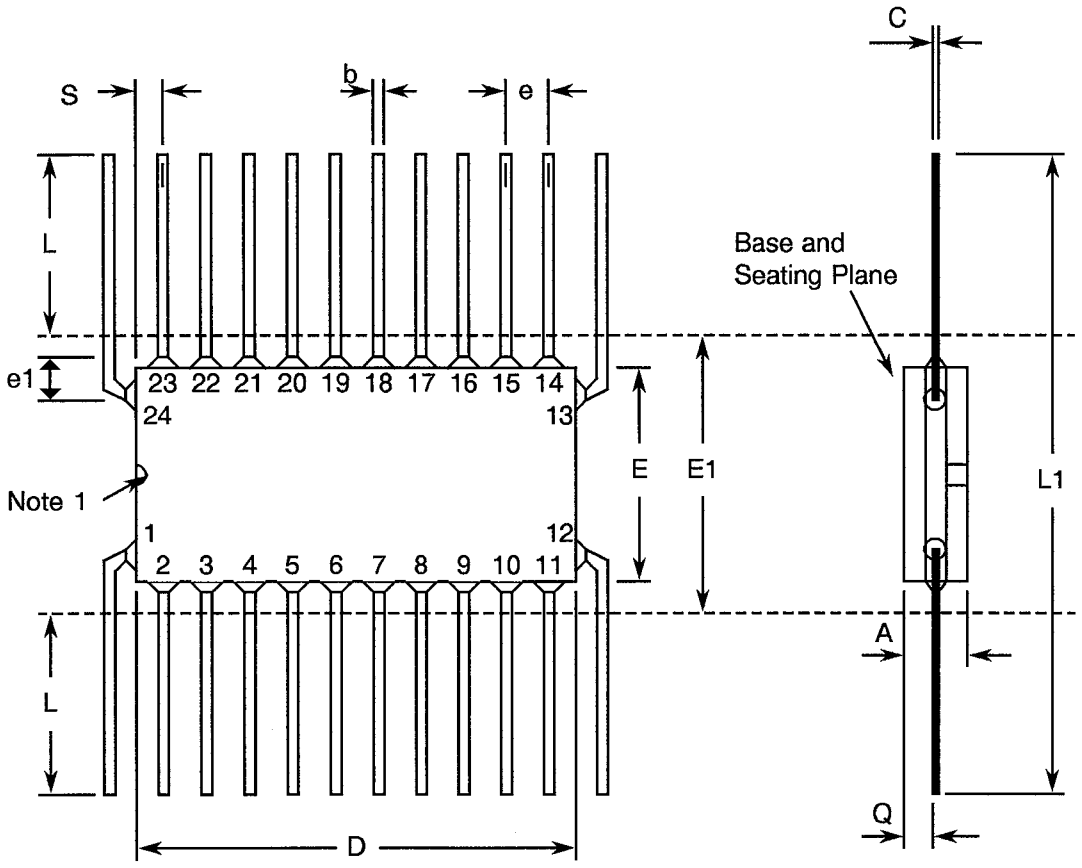
1. These ratings apply except for programming pins during a programming cycle.
2. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
3. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION

Not applicable.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - FLAT PACKAGE, 24-PIN

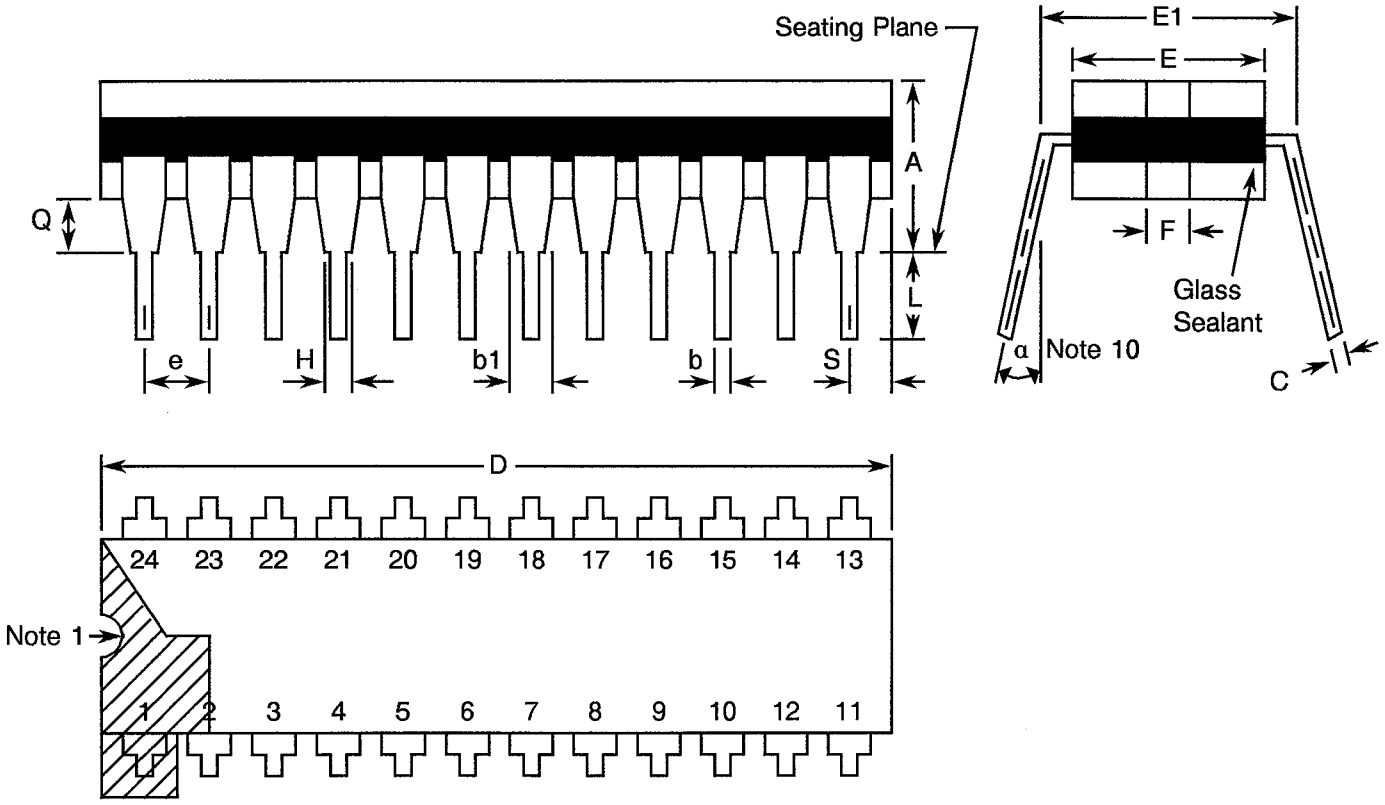


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	1.39	2.16	
b	0.38	0.56	8
C	0.08	0.23	8
D	12.30	-	4
E	8.50	10.10	
E1	10.16	TYPICAL	4
e	1.27	TYPICAL	5, 9
e1	1.10	TYPICAL	5, 9
L	6.98	10.16	
L1	24.13	30.48	
Q	0.25	1.02	2
S	0.71	1.27	7

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - DUAL-IN-LINE PACKAGE, 24-PIN

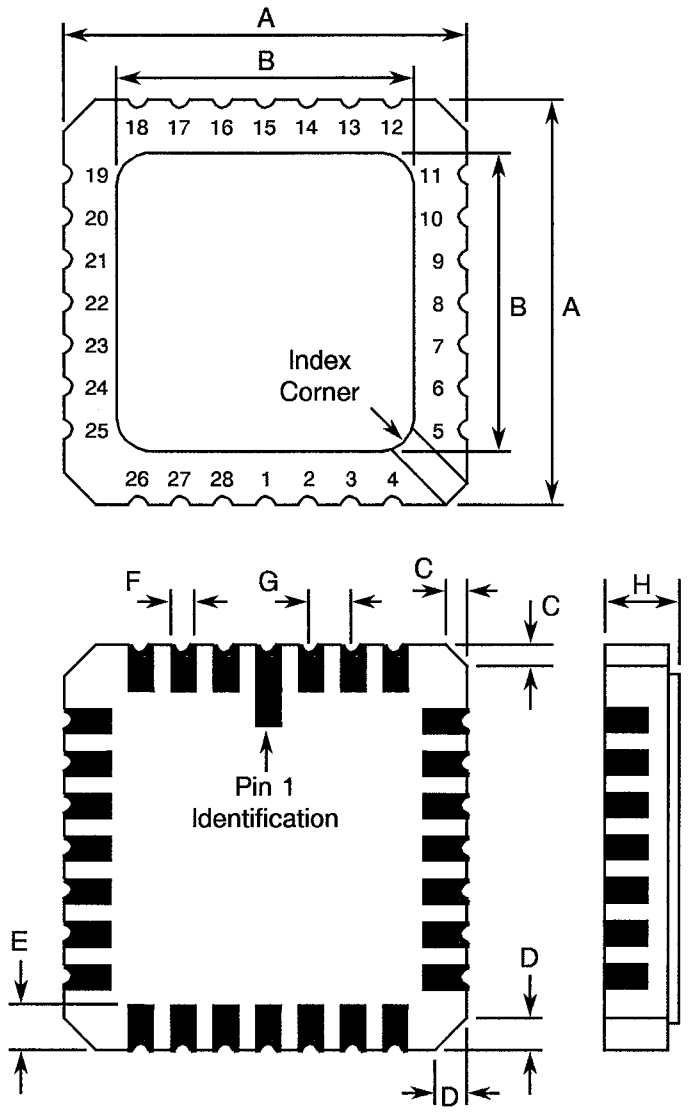


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	-	5.08	
b	0.38	0.66	8
b1	-	1.78	8
C	0.20	0.44	8
D	31.50	32.51	4
E	6.22	7.62	4
E1	7.37	8.13	
e	2.54 TYPICAL		6, 9
F	1.27 TYPICAL		
H	0.69	-	8
L	3.30	5.08	8
Q	0.51	-	3
S	-	2.54	7
α	0°	15°	10

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(c) - SQUARE CHIP CARRIER PACKAGE, 28 TERMINAL



SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	11.23	11.63	
B	10.31	11.63	
C	0.25	0.51	11
D	0.89	1.14	12
E	1.14	1.40	8
F	0.56	0.71	8
G	1.27 TYPICAL		5, 9
H	1.63	2.54	

NOTES: See Page 10.

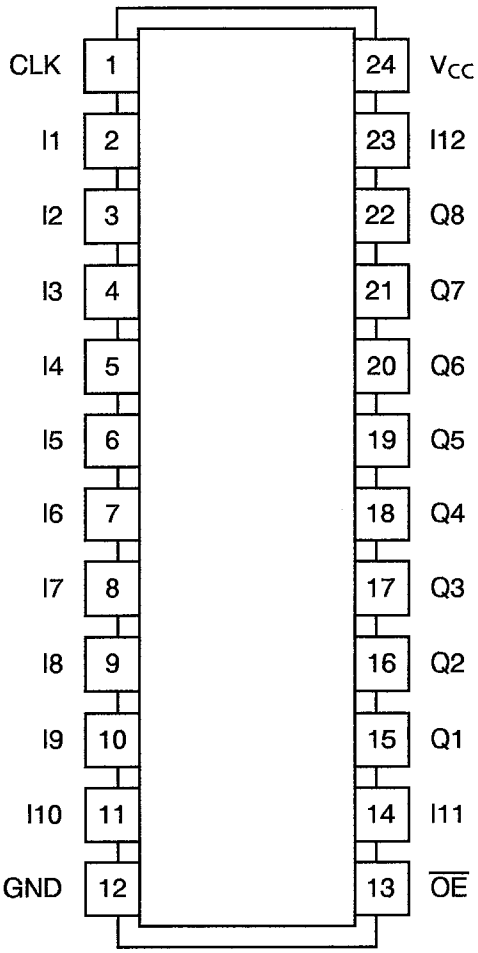
FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURES 2(a) TO 2(c) INCLUSIVE

1. Index area: a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown in Figure 2(c).
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-centre lids, meniscus and glass overrun.
5. The true position pin or terminal spacing is 1.27mm between centrelines. Each pin or terminal centreline shall be located within ±0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
6. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.
7. Applies to all 4 corners.
8. All leads or terminals.
9. 22 spaces for flat and dual-in-line packages.
   24 spaces for chip carrier packages.
10. Lead centre when α is 0°.
11. Index corner only - 2 dimensions.
12. 3 non-index corners - 6 dimensions.

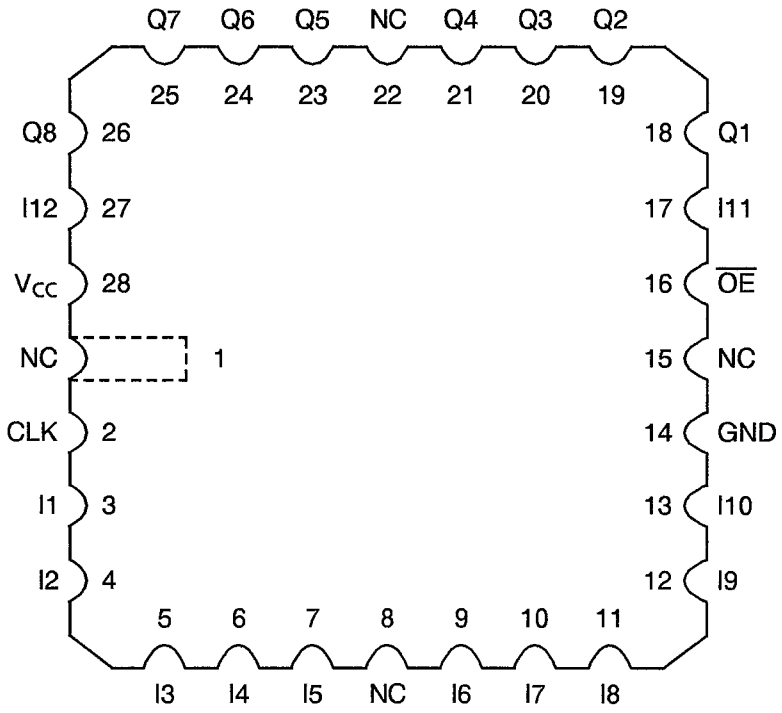
FIGURE 3(a) - PIN ASSIGNMENT

DUAL-IN-LINE AND FLAT PACKAGE



(TOP VIEW)

CHIP CARRIER PACKAGE



(TOP VIEW)

FLAT PACKAGES AND DUAL-IN-LINE TO CHIP CARRIER PIN ASSIGNMENT

FLAT PACKAGE AND DUAL-IN-LINE PIN OUTS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
CHIP CARRIER PIN OUTS	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28

FIGURE 3(b) - PROGRAMMING PROCEDURE

1. GENERAL

Devices shall be programmed in accordance with the following sequence:-

(a) The appropriate programme shall be selected, either:-

(i) The programme specified in Appendix 'A' to this specification for use during Qualification Testing, Extension of Qualification and during Endurance Testing during LAT2, or

(ii) A programme as supplied by the Orderer for use during Endurance Testing during Lot Acceptance Testing.

(b) Marking as per Para. 4.5.4 of this specification.

(c) The appropriate programming procedure as specified hereafter.

(d) Pre burn-in electrical measurements at $T_{amb} = -55$, $+22$ and $+125°C$ in accordance with Table 6 of this specification.

(e) Check programming and electrical measurements yield >90% of the components submitted for programming.

(f) Power burn-in of 168 hours in accordance with Table 5(b) of this specification.

(g) Post burn-in electrical measurements at $T_{amb} = +22°C$ in accordance with Table 6 of this specification, PDA = 5% or 1 device whichever is the greater.

(h) Preparation of a Certificate of Conformance which should contain information correlating a unique identifier with the Programme, Programmer and date of Programming.

2. PROCEDURES

Programming procedures shall be as given in the following paragraphs.

2.1 VARIANTS 01 TO 04

Array fuses are programmed executing the following programming sequence. Each fuse can be opened by selecting the appropriate Input Line (1 of 40) and then pulsing the correct Product Line (1 of 8). The levels for selecting Input Lines and Product Lines are shown in Tables II/1 and III/1 .

Step 1: Raise PGM ENABLE to V_{IHH}.

Step 2: Select an Input Line by applying appropriate levels to PI pins in accordance with Table II/1.

Step 3: Select a Product Line group by applying appropriate levels to PA pins in accordance with Table III/1. The actual product line selected will be determined by the PO pin (described in step 5).

Step 4: Raise $\overline{OE}$ to V_{IH}.

Step 5: Raise the selected PO pin to V_{IHH}.

Step 6: Programme the fuse by pulsing V_{CC} to V_{IHH}.

Step 7: Remove the output voltage.

Step 8: Lower $\overline{OE}$ to V_{IL} to enable device.

Step 9: Pulse PGM VERIFY pin to V_{IH}.

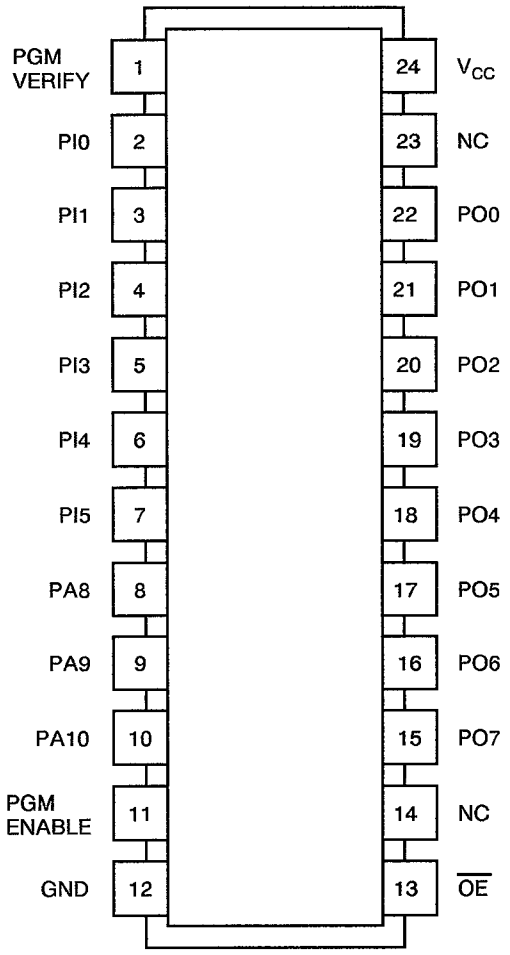
Step 10: Verify the blowing of the fuse by checking for a V_{OL} at the selected PO pin.

NOTES

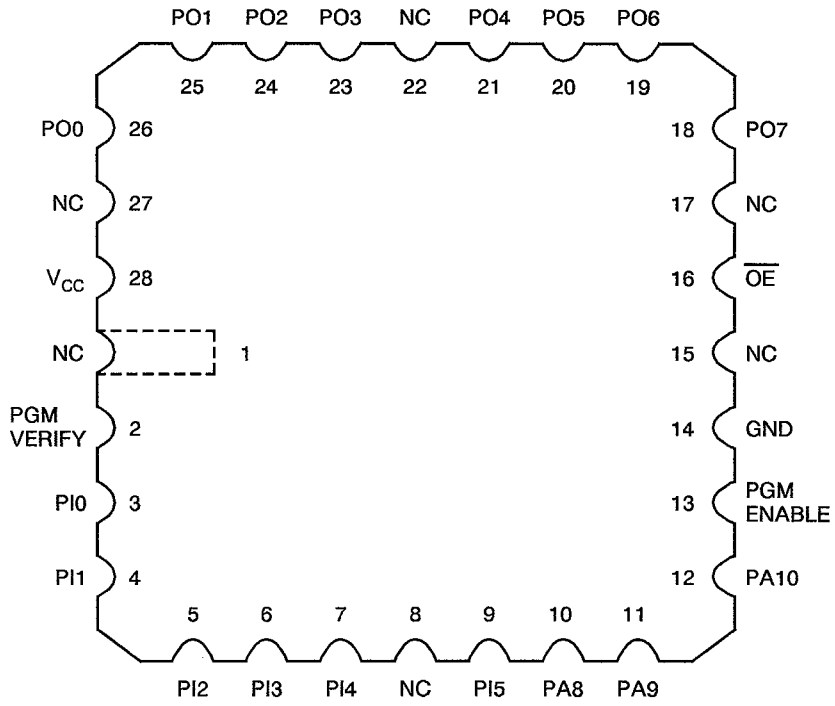
1. If the fuse is still intact, steps 1 to 10 may be repeated until the fuse is successfully blown, but this shall not exceed 4 times. Do not apply additional pulses to a fuse once it is correctly programmed. Verification is possible only with the security fuse intact.
2. A single security fuse is provided on each device to discourage the unauthorised copying of fuse patterns. To programme the security fuse, follow the steps above omitting steps 2, 5 and 9. Verification is achieved by verifying the entire fuse array. If the security fuse is blown, all other fuses will appear to be unblown.

FIGURE I/1 - PIN ASSIGNMENT IN PROGRAMMING MODE

PRODUCT TERM



(TOP VIEW)



(TOP VIEW)

NOTES

1. NC = Not Connected

TABLE I/1 - PROGRAMMING PARAMETERS, T_{amb} = +25°C

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT
1	Programme-pulse Voltage	V_{IHH}	10.25 to 10.75	V
2	Programme-pulse Current PO	I_{IHH}	50 Max.	mA
3	Programme-pulse Current PGM ENABLE, $\overline{OE}$, PI, PA	I_{IHH}	25 Max.	mA
4	Programme-pulse Current I_{CC}	I_{IHH}	500 Max.	mA
5	Programme-pulse duration at PO	t_{w1}	10 to 50	µs
6	Pulse duration at PGM VERIFY	t_{w2}	100 Min.	ns
7	Set-up time	t_{su}	100 Min.	ns
8	Hold time	t_h	100 Min.	ns
9	Delay time from $\overline{OE}$ LOW to PGM VERIFY	t_{d1}	100 Min.	ns
10	Delay time from PGM VERIFY pulse to valid output.	t_{d2}	200 Min.	ns

TABLE II/1 - INPUT LINE SELECT

INPUT LINE No.	INPUT LINE NUMBER - ADDRESS PIN STATES						HEX
	PI0	PI1	PI2	PI3	PI4	PI5	
0	L	L	L	L	L	L	00
1	L	L	L	L	L	H	01
2	L	L	L	L	H	L	02
3	L	L	L	L	H	H	03
4	L	L	L	H	L	L	04
5	L	L	L	H	L	H	05
6	L	L	L	H	H	L	06
7	L	L	L	H	H	H	07
8	L	L	H	L	L	L	08
9	L	L	H	L	L	H	09
10	L	L	H	L	H	L	0A
11	L	L	H	L	H	H	0B
12	L	L	H	H	L	L	0C
13	L	L	H	H	L	H	0D
14	L	L	H	H	H	L	0E
15	L	L	H	H	H	H	0F
16	L	H	L	L	L	L	10
17	L	H	L	L	L	H	11
18	L	H	L	L	H	L	12
19	L	H	L	L	H	H	13
20	L	H	L	H	L	L	14
21	L	H	L	H	L	H	15
22	L	H	L	H	H	L	16
23	L	H	L	H	H	H	17
24	L	H	H	L	L	L	18
25	L	H	H	L	L	H	19
26	L	H	H	L	H	L	1A
27	L	H	H	L	H	H	1B
28	L	H	H	H	L	L	1C
29	L	H	H	H	L	H	1D
30	L	H	H	H	H	L	1E
31	L	H	H	H	H	H	1F
32	H	L	L	L	L	L	20
33	H	L	L	L	L	H	21
34	H	L	L	L	H	L	22
35	H	L	L	L	H	H	23
36	H	L	L	H	L	L	24
37	H	L	L	H	L	H	25
38	H	L	L	H	H	L	26
39	H	L	L	H	H	H	27
SF	H	H	H	H	H	H	3F

NOTES: See Page 16.

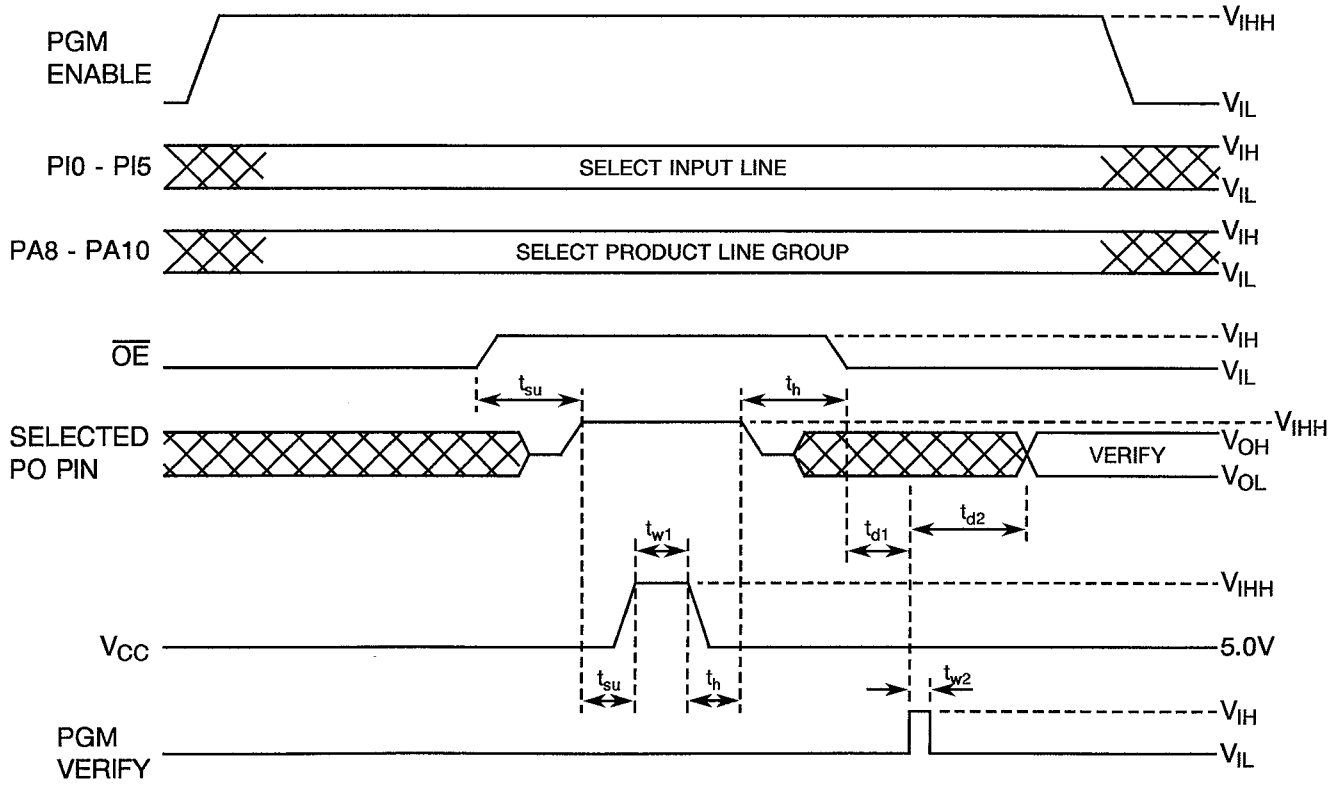
TABLE III/1 - PRODUCT TERM ADDRESSING

PRODUCT TERM								PRODUCT TERM SELECT ADDRESS PIN STATES		
								PA8	PA9	PA10
0	8	16	24	32	40	48	56	L	L	L
1	9	17	25	33	41	49	57	L	L	H
2	10	18	26	34	42	50	58	L	H	L
3	11	19	27	35	43	51	59	L	H	H
4	12	20	28	36	44	52	60	H	L	L
5	13	21	29	37	45	53	61	H	L	H
6	14	22	30	38	46	54	62	H	H	L
7	15	23	31	39	47	55	63	H	H	H
SF → -	-	-	-	-	-	-	-	X	X	HH ← SF
PO0	PO1	PO2	PO3	PO4	PO5	PO6	PO7			
PROGRAMMING ACCESS AND VERIFY PIN										

NOTES

1. Logic Level Definitions: $L = V_{IL} = 0.5V$(max.), $H = V_{IH} = 2.4V$(min.), $HH = V_{IHH}$.
2. SF = Security Fuse (does not require voltage to the PO pin).

FIGURE II/1 - PROGRAMMING WAVEFORMS



NOTES

1. A high level during the verify interval indicates that the programming has not been successful.
2. A low level during the verify interval indicates that the programming has been successful.

2.2 VARIANTS 05 TO 08

Array fuses are programmed by executing the following programming sequence. Each fuse can be opened by selecting the appropriate Input Line (1 of 40) and then pulsing the correct Product Line (1 of 8). The levels for selecting Input Lines and Product Lines are shown in Tables II/2 and III/2.

Step 1: Raise PGM ENABLE to V_{IHH}.

Step 2: Select an Input Line by applying appropriate levels to PI pins in accordance with Table II/2.

Step 3: Select a Product Line group by applying appropriate logic levels to PA pins in accordance with Table III/2. The actual product line selected will be determined by the PO pin (described in step 5).

Step 4: Raise $\overline{OE}$ to V_{IH}.

Step 5: Raise the selected PO pin to V_{IHH}.

Step 6: Programme the fuse by pulsing V_{CC} to V_{IHH}.

Step 7: Remove the output voltage.

Step 8: Lower $\overline{OE}$ to V_{IL} to enable device.

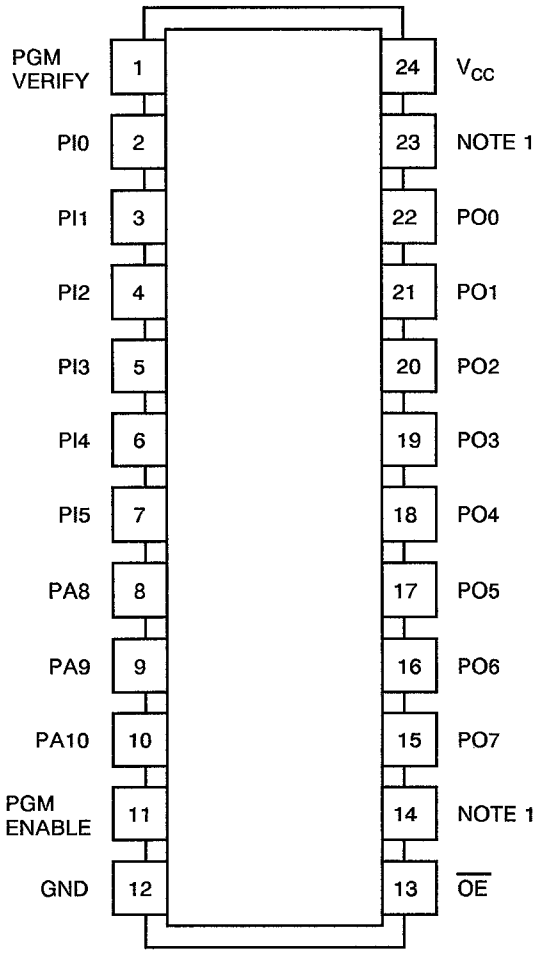
Step 9: Pulse PGM VERIFY pin to V_{IH}.

Step 10: Verify the blowing of the fuse by checking for a V_{OL} at the selected PO pin.

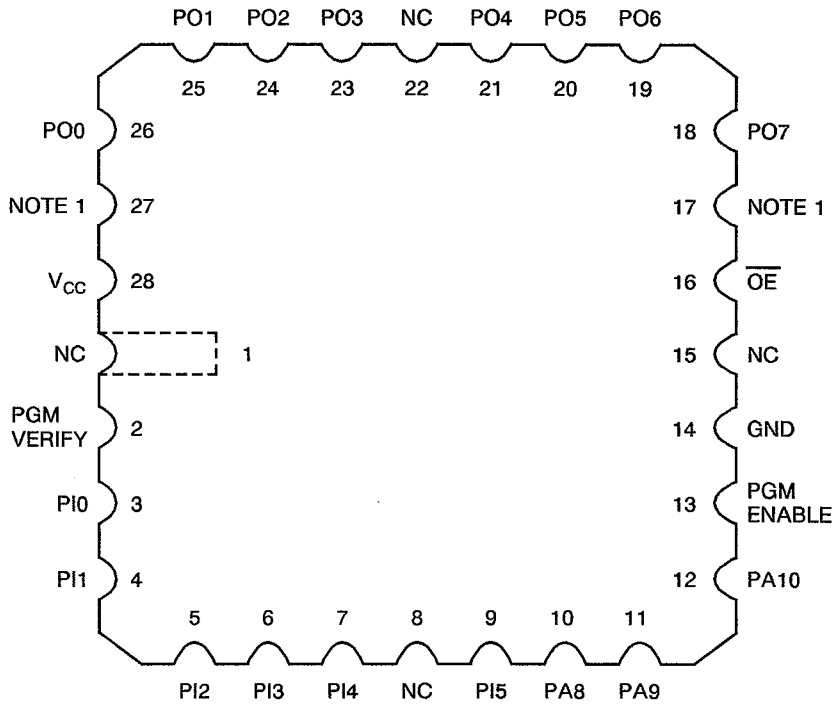
NOTES

1. If the fuse is still intact, steps 1 to 10 may be repeated until the fuse is successfully blown, but this shall not exceed 4 times. Do not apply additional pulses to a fuse once it is correctly programmed. Verification is possible only with the security fuse intact.
2. A single security fuse is provided on each device to discourage the unauthorised copying of fuse patterns. To programme the security fuse, follow the steps above omitting steps 5 and 10. Verification is achieved by verifying the entire fuse array. If the security fuse is blown, all other fuses will appear to be unblown.

FIGURE I/2 - PIN ASSIGNMENT IN PROGRAMMING MODE



(TOP VIEW)



(TOP VIEW)

NOTES

1. Set to H = V_{IH}.
2. NC = Not Connected.

TABLE I/2 - PROGRAMMING PARAMETERS, T_{amb} = +25°C

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT
1	Programme-pulse Voltage PO, PGM ENABLE, PI, PA, V_{CC}	V_{IHH}	10.25 to 10.75	V
2	Programme-pulse Current PO	I_{IHH}	50 Max.	mA
3	Programme-pulse Current PGM ENABLE, $\overline{OE}$, PI, PA	I_{IHH}	25 Max.	mA
4	Programme-pulse Current I_{CC}	I_{IHH}	500 Max.	mA
5	Programme-pulse duration at V_{CC}	t_{w1}	10 to 50	µs
6	Pulse duration at PGM VERIFY	t_{w2}	100 Min.	ns
7	Set-up time	t_{su}	100 Min.	ns
8	Hold time	t_h	100 Min.	ns
9	Delay time from $\overline{OE}$ low to PGM VERIFY high	t_{d1}	100 Min.	ns
10	Delay time from PGM VERIFY high to valid output	t_{d2}	200 Min.	ns

TABLE II/2 - INPUT LINE SELECT

INPUT LINE No.	INPUT LINE NUMBER - ADDRESS PIN STATES						HEX
	PI0	PI1	PI2	PI3	PI4	PI5	
0	L	L	L	L	L	L	00
1	L	L	L	L	L	H	01
2	L	L	L	L	H	L	02
3	L	L	L	L	H	H	03
4	L	L	L	H	L	L	04
5	L	L	L	H	L	H	05
6	L	L	L	H	H	L	06
7	L	L	L	H	H	H	07
8	L	L	H	L	L	L	08
9	L	L	H	L	L	H	09
10	L	L	H	L	H	L	0A
11	L	L	H	L	H	H	0B
12	L	L	H	H	L	L	0C
13	L	L	H	H	L	H	0D
14	L	L	H	H	H	L	0E
15	L	L	H	H	H	H	0F
16	L	H	L	L	L	L	10
17	L	H	L	L	L	H	11
18	L	H	L	L	H	L	12
19	L	H	L	L	H	H	13
20	L	H	L	H	L	L	14
21	L	H	L	H	L	H	15
22	L	H	L	H	H	L	16
23	L	H	L	H	H	H	17
24	L	H	H	L	L	L	18
25	L	H	H	L	L	H	19
26	L	H	H	L	H	L	1A
27	L	H	H	L	H	H	1B
28	L	H	H	H	L	L	1C
29	L	H	H	H	L	H	1D
30	L	H	H	H	H	L	1E
31	L	H	H	H	H	H	1F
32	H	L	L	L	L	L	20
33	H	L	L	L	L	H	21
34	H	L	L	L	H	L	22
35	H	L	L	L	H	H	23
36	H	L	L	H	L	L	24
37	H	L	L	H	L	H	25
38	H	L	L	H	H	L	26
39	H	L	L	H	H	H	27
SF	H	H	H	H	H	H	3F

NOTES: See Page 21.

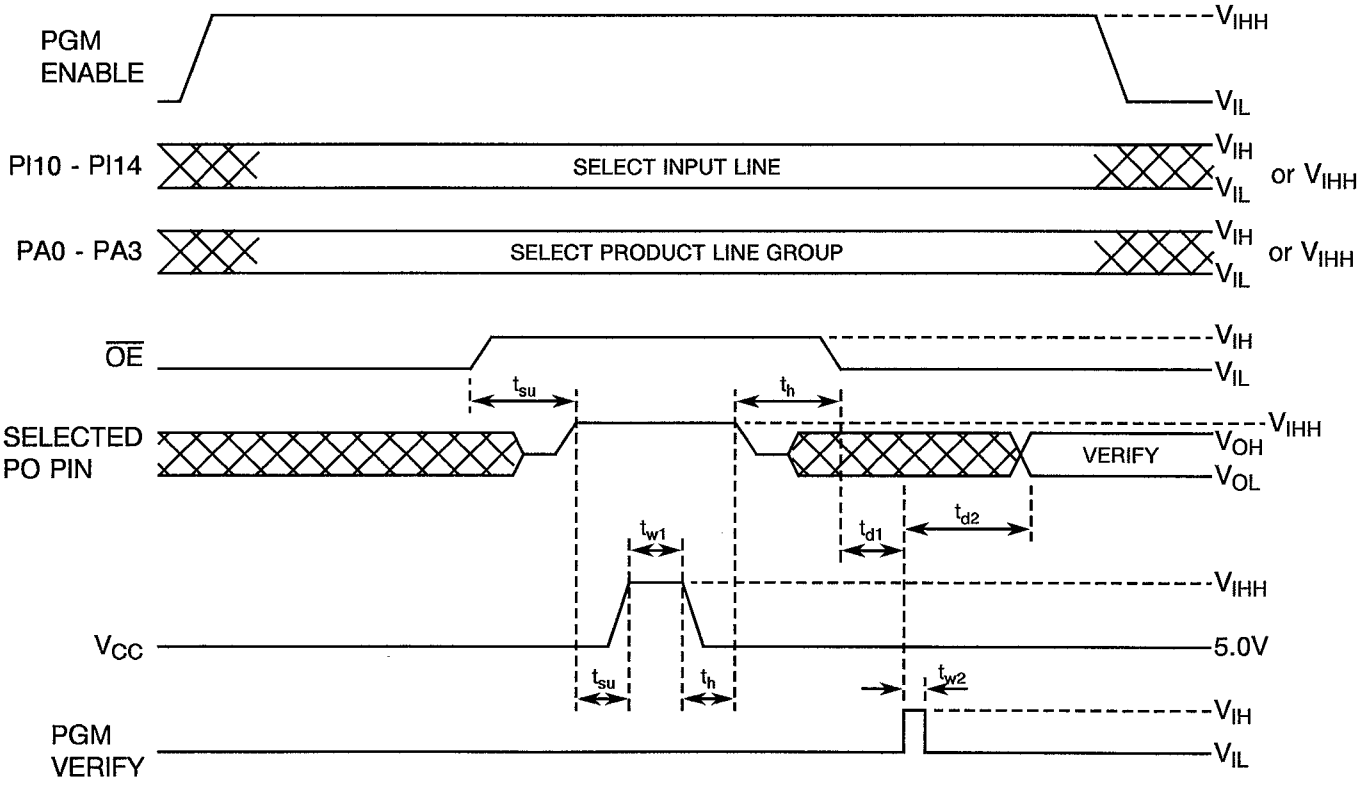
TABLE III/2 - PRODUCT TERM ADDRESSING

PRODUCT TERM								PRODUCT TERM SELECT ADDRESS PIN STATES		
								PA8	PA9	PA10
0	8	16	24	32	40	48	56	L	L	L
1	9	17	25	33	41	49	57	H	L	H
2	10	18	26	34	42	50	58	L	H	L
3	11	19	27	35	43	51	59	L	H	H
4	12	20	28	36	44	52	60	H	H	L
5	13	21	29	37	45	53	61	H	L	H
6	14	22	30	38	46	54	62	H	L	L
7	15	23	31	39	47	55	63	H	H	H
SF → -	-	-	-	-	-	-	-	X	X	HH ← SF
PO0	PO1	PO2	PO3	PO4	PO5	PO6	PO7			
PROGRAMMING ACCESS AND VERIFY PIN										

NOTES

1. Logic Level Definitions: L = V_{IL} = 0.5V(max.), H = V_{IH} = 2.4V(min.), HH = V_{IHH}, X = Don't Care.
2. SF = Security Fuse (does not require voltage to the P0 pin).

FIGURE II/2 - PROGRAMMING WAVEFORMS

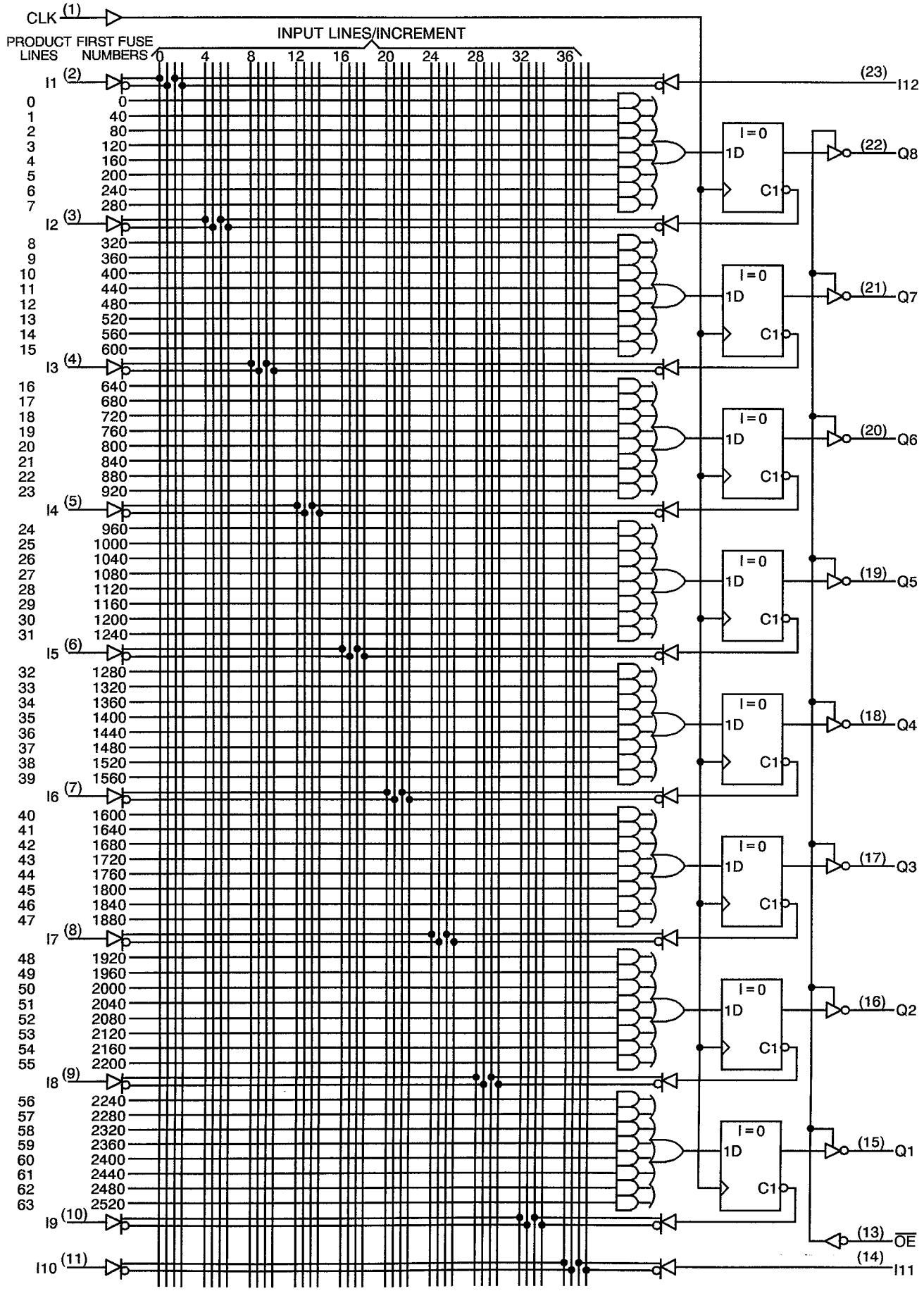


NOTES

1. A high level during the verify interval indicates that the programming has not been successful.
2. A low level during the verify interval indicates that the programming has been successful.

FIGURE 3(c) - PROGRAMMING MATRIX

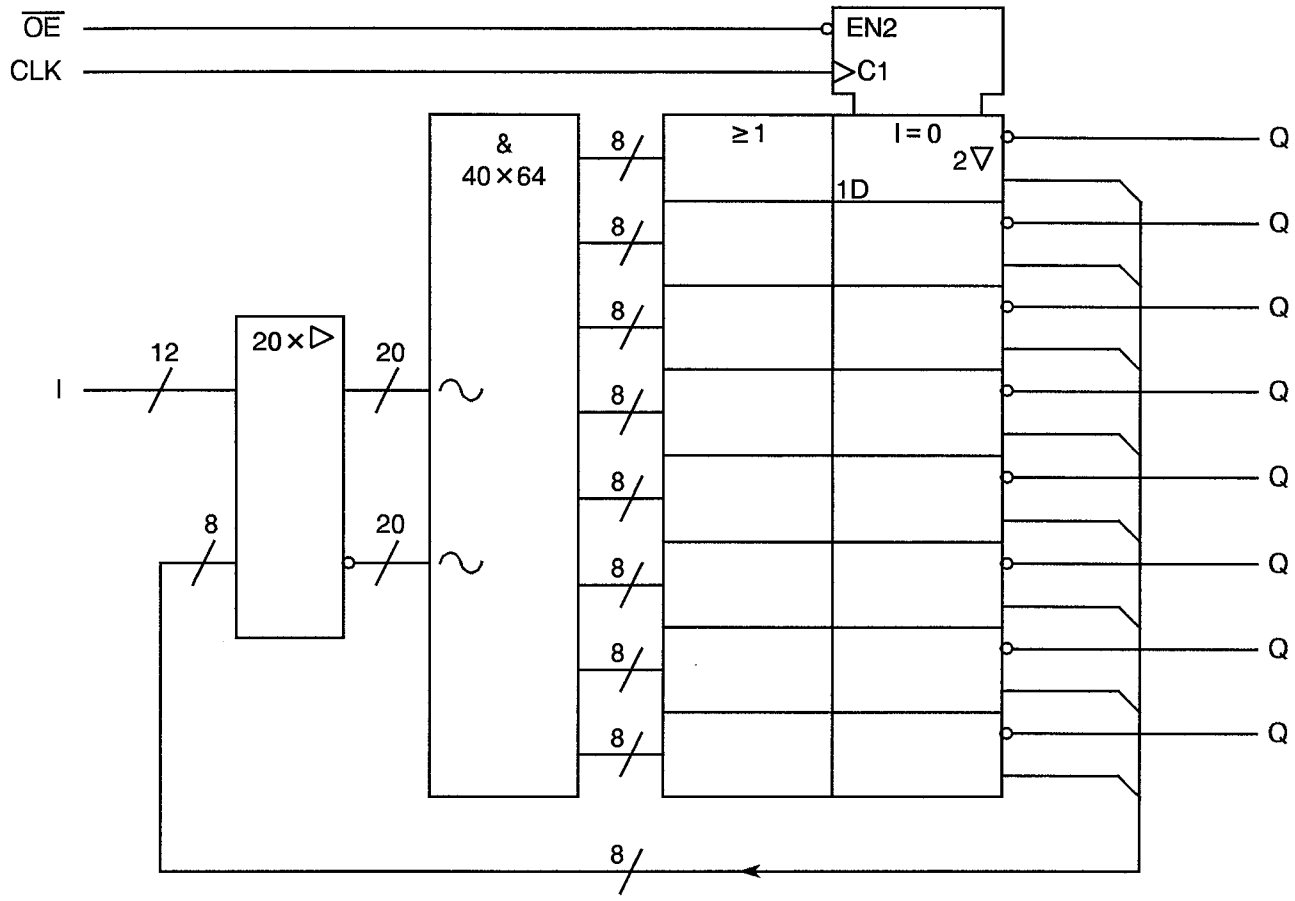
NOTES: See Page 23.



NOTES TO FIGURE 3(c)

1. Fuse Number = First Fuse Number plus Increment.
2. Pin numbers shown are for DIL and FP.

FIGURE 3(d) - FUNCTIONAL DIAGRAM



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:

V_{IC} = Input Clamp Voltage.
I_{IC} = Input Clamp Diode Current.
PGM = Programme.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein shall be as stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirement and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

(a) Para. 4.4 - Additional marking, as specified in Para. 4.5.4 of this specification, shall be added immediately prior to programming.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

(a) Para. 7.1.1(a), "High Temperature Reverse Bias" tests and subsequent electrical measurements related to this test shall be omitted.

(b) Para. 7.1.1(b), "Power Burn-in" shall be performed for 168 hours. After programming, a further Power Burn-in of 168 hours shall be performed as part of the sequence specified in Figure 3(b) of this specification.

(c) Para. 9.9.2, "Electrical Measurements at High and Low Temperatures": Only a test result summary, based on go-no-go tests and presented in histogram form, is required.

4.2.4 Deviations from Qualification Tests (Chart IV)

(a) Prior to Qualification testing, all devices to be subjected to qualification testing shall be programmed to the Qualification Pattern specified in Appendix 'A' of this specification.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

(a) Prior to LAT1 testing, all devices to be subjected to LAT1 testing shall be programmed to the Qualification Pattern specified in Appendix 'A' of this specification, but see (c) below.

(b) Prior to LAT2 testing, all devices to be subjected to LAT2 testing shall be programmed to either:-

(i) The Qualification Pattern specified in Appendix 'A' of this specification or,

(ii) A programme specified by the Orderer,

but see (c) below.

(c) LAT3 testing shall be performed on unprogrammed devices.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 1.1 grammes for the flat package, 5.0 grammes for the dual-in-line package and 0.7 grammes for the chip carrier package.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body and the lids shall be welded, brazed, preform-soldered or glass frit sealed.

4.4.2 Lead Material and Finish

For dual-in-line and flat packages, the material shall be Type 'G' with Type '4' finish in accordance with ESA/SCC Basic Specification No. 23500. For chip carrier packages the finish shall be Type '4' or Type '7' in accordance with ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

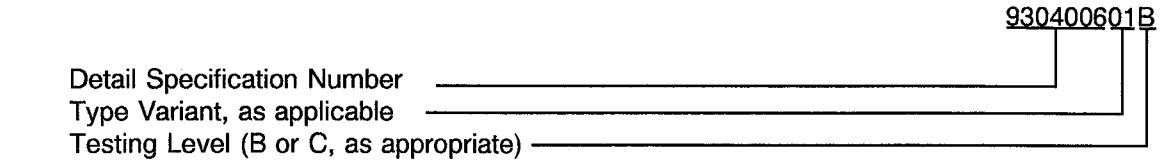
(c) Traceability Information.

4.5.2 Lead Identification

For dual-in-line and flat packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side. For chip carrier packages, the index shall be as defined by Figure 2(c).

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

For programmed devices, a unique programme identifier shall be added. This identifier shall identify Programme, Programmer and date of programming.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ °C and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits and functional test sequence for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-in

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for power burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuit for High Temperature Reverse Bias Burn-in

Not applicable.

4.7.5 Electrical Circuit for Power Burn-in

A circuit for use in performing the power burn-in tests is shown in Figure 5(b) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP and FP C = CCP) (NOTE 1)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test 1	-	-	-	Verify Fuse Integrity V_{IL} = 0V, V_{IH} = 4.5V, V_{IHH} = 10.75V V_{CC} = 4.5V, GND = 0V	-	-	-
2	Functional Test 2	-	-		Verify Fuse Integrity V_{IL} = 0V, V_{IH} = 5.5V, V_{IHH} = 10.75V V_{CC} = 5.5V, GND = 0V	-	-	-
3	Supply Current	I_{CC}	3005	4(a)	V_{IN} (All Inputs) = 0V All Outputs Open V_{CC} = 5.5V, GND = 0V Variants 01 to 04 Variants 05 to 08 (Pin D/F 24) (Pin C 28)	 - -	 180 220	mA
4 to 17	Input Current Low Level	I_{IL}	3009	4(b)	V_{IN} (Under Test) = 0.4V V_{IN} (Remaining Inputs) = 5.5V V_{CC} = 5.5V, GND = 0V (Pins D/F 1-2-3-4-5-6-7-8-9-10-11-13-14-23) (Pins C 2-3-4-5-6-7-9-10-11-12-13-16-17-27)	-	−250	µA
18 to 31	Input Current High Level 1	I_{IH1}	3010	4(c)	V_{IN} (Under Test) = 2.7V V_{IN} (Remaining Inputs) = 0V V_{CC} = 5.5V, GND = 0V (Pins D/F 1-2-3-4-5-6-7-8-9-10-11-13-14-23) (Pins C 2-3-4-5-6-7-9-10-11-12-13-16-17-27)	-	25	µA
32 to 45	Input Current High Level 2	I_{IH2}	3010	4(c)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{CC} = 5.5V, GND = 0V (Pins D/F 1-2-3-4-5-6-7-8-9-10-11-13-14-23) (Pins C 2-3-4-5-6-7-9-10-11-12-13-16-17-27)	-	1.0	mA

NOTES: See Page 29.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP and FP C = CCP) (NOTE 1)	LIMITS		UNIT
						MIN	MAX	
46 to 53	Output Voltage Low Level	V_{OL}	3007	4(d)	V_{IL} = 0.8V, V_{IH} = 2.0V I_{OL} = 12mA V_{CC} = 4.5V, GND = 0V Note 2 (Pins D/F 15-16-17-18-19-20-21-22) (Pins C 18-19-20-21-23-24-25-26)	-	0.5	V
54 to 61	Output Voltage High Level	V_{OH}	3006	4(e)	V_{IL} = 0.8V, V_{IH} = 2.0V I_{OH} = 2.0mA V_{CC} = 4.5V, GND = 0V Note 2 (Pins D/F 15-16-17-18-19-20-21-22) (Pins C 18-19-20-21-23-24-25-26)	2.4	-	V
62 to 69	Output Leakage Current Third State (High Level Applied)	I_{OZH}	3006	4(f)	V_{IL} = 0.8V, V_{IH} = 2.0V V_{OUT} = 2.7V V_{CC} = 5.5V, GND = 0V Note 2 Variants 01 to 04 Variants 05 to 08 (Pins D/F 15-16-17-18-19-20-21-22) (Pins C 18-19-20-21-23-24-25-26)	 - -	 100 20	µA
70 to 77	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	3006	4(g)	V_{IL} = 0.8V, V_{IH} = 2.0V V_{OUT} = 0.4V V_{CC} = 5.5V, GND = 0V Note 2 Variants 01 to 04 Variants 05 to 08 (Pins D/F 15-16-17-18-19-20-21-22) (Pins C 18-19-20-21-23-24-25-26)	 - -	 −20 −100	µA
78 to 91	Input Clamp Voltage	V_{IC}	-	4(h)	I_{IN} (Under Test) = − 18mA Remaining Inputs Open V_{CC} = 4.5V, GND = 0V (Pins D/F 1-2-3-4-5-6-7-8-9-10-11-13-14-23) (Pins C 2-3-4-5-6-7-9-10-11-12-13-16-17-27)	-	−1.5	V

NOTES: See Page 29.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP and FP C = CCP) (NOTE 1)	LIMITS		UNIT
						MIN	MAX	
92 to 99	Short Circuit Output Current	I_{OS}	3011	4(i)	V_{IL} = 0.8V, V_{IH} = 2.0V V_{OUT} (Under Test) = 0.5V Remaining Outputs Open V_{CC} = 5.5V, GND = 0V Notes 2 and 3 Variants 01 to 04 Variants 05 to 08 (Pins D/F 15-16-17-18-19-20-21-22) (Pins C 18-19-20-21-23-24-25-26)	 −30 −30	 −250 −130	mA

NOTES

1. To be performed on unprogrammed devices only.
2. The Manufacturer's input sequence is to be used to activate output conditions via internal circuitry.
3. No more than one output should be shorted at a time and the duration shall not exceed 1 second.
4. Guaranteed but not tested, with LTPD10.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST) (NOTE 1)	LIMITS		UNIT
						MIN	MAX	
100	Propagation Delay Low to High (CLK to Q)	t_{PLH}	3004	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Note 2 V_{CC} = 4.5V, GND = 0V Note 4 Variants 01 to 04 Variants 05 to 08	 - -	 15 10	ns
101	Propagation Delay High to Low (CLK to Q)	t_{PHL}	3004	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Note 2 V_{CC} = 4.5V, GND = 0V Note 4 Variants 01 to 04 Variants 05 to 08	 - -	 15 10	ns
102	Output Enable Time High Impedance to Low Output ($\overline{OE}$ to Q)	t_{PZL}	3004	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Note 2 V_{CC} = 4.5V, GND = 0V Note 4 Variants 01 to 04 Variants 05 to 08	 - -	 20 10	ns
103	Output Enable Time High Impedance to High Output ($\overline{OE}$ to Q)	t_{PZH}	3004	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Note 2 V_{CC} = 4.5V, GND = 0V Note 4 Variants 01 to 04 Variants 05 to 08	 - -	 20 10	ns

NOTES: See Page 29.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST) (NOTE 1)	LIMITS		UNIT
						MIN	MAX	
104	Output Disable Time Low Output to High Impedance ($\overline{OE}$ to Q)	t_{PLZ}	3004	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Note 2 V_{CC} = 4.5V, GND = 0V Note 4 Variants 01 to 04 Variants 05 to 08	 - -	 20 10	ns
105	Output Disable Time High Output to High Impedance ($\overline{OE}$ to Q)	t_{PHZ}	3004	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Note 2 V_{CC} = 4.5V, GND = 0V Note 4 Variants 01 to 04 Variants 05 to 08	 - -	 20 10	ns

NOTES: See Page 29.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP and FP C = CCP) (NOTE 1)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test 1	-	-	-	Verify Fuse Integrity V_{IL} = 0V, V_{IH} = 4.5V, V_{IHH} = 10.75V V_{CC} = 4.5V, GND = 0V	-	-	-
2	Functional Test 2	-	-		Verify Fuse Integrity V_{IL} = 0V, V_{IH} = 5.5V, V_{IHH} = 10.75V V_{CC} = 5.5V, GND = 0V	-	-	-
3	Supply Current	I_{CC}	3005	4(a)	V_{IN} (All Inputs) = 0V All Outputs Open V_{CC} = 5.5V, GND = 0V Variants 01 to 04 Variants 05 to 08 (Pin D/F 24) (Pin C 28)	 - -	 180 220	mA
4 to 17	Input Current Low Level	I_{IL}	3009	4(b)	V_{IN} (Under Test) = 0.4V V_{IN} (Remaining Inputs) = 5.5V V_{CC} = 5.5V, GND = 0V (Pins D/F 1-2-3-4-5-6-7-8-9-10-11-13-14-23) (Pins C 2-3-4-5-6-7-9-10-11-12-13-16-17-27)	-	−250	µA
18 to 31	Input Current High Level 1	I_{IH1}	3010	4(c)	V_{IN} (Under Test) = 2.7V V_{IN} (Remaining Inputs) = 0V V_{CC} = 5.5V, GND = 0V (Pins D/F 1-2-3-4-5-6-7-8-9-10-11-13-14-23) (Pins C 2-3-4-5-6-7-9-10-11-12-13-16-17-27)	-	25	µA
32 to 45	Input Current High Level 2	I_{IH2}	3010	4(c)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{CC} = 5.5V, GND = 0V (Pins D/F 1-2-3-4-5-6-7-8-9-10-11-13-14-23) (Pins C 2-3-4-5-6-7-9-10-11-12-13-16-17-27)	-	1.0	mA

NOTES: See Page 29.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP and FP C = CCP) (NOTE 1)	LIMITS		UNIT
						MIN	MAX	
46 to 53	Output Voltage Low Level	V_{OL}	3007	4(d)	V_{IL} = 0.8V, V_{IH} = 2.0V I_{OL} = 12mA V_{CC} = 4.5V, GND = 0V Note 2 (Pins D/F 15-16-17-18-19-20-21-22) (Pins C 18-19-20-21-23-24-25-26)	-	0.5	V
54 to 61	Output Voltage High Level	V_{OH}	3006	4(e)	V_{IL} = 0.8V, V_{IH} = 2.0V I_{OH} = 2.0mA V_{CC} = 4.5V, GND = 0V Note 2 (Pins D/F 15-16-17-18-19-20-21-22) (Pins C 18-19-20-21-23-24-25-26)	2.4	-	V
62 to 69	Output Leakage Current Third State (High Level Applied)	I_{OZH}	3006	4(f)	V_{IL} = 0.8V, V_{IH} = 2.0V V_{OUT} = 2.7V V_{CC} = 5.5V, GND = 0V Note 2 Variants 01 to 04 Variants 05 to 08 (Pins D/F 15-16-17-18-19-20-21-22) (Pins C 18-19-20-21-23-24-25-26)	 - -	 100 20	µA
70 to 77	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	3006	4(g)	V_{IL} = 0.8V, V_{IH} = 2.0V V_{OUT} = 0.4V V_{CC} = 5.5V, GND = 0V Note 2 Variants 01 to 04 Variants 05 to 08 (Pins D/F 15-16-17-18-19-20-21-22) (Pins C 18-19-20-21-23-24-25-26)	 - -	 −20 −100	µA
78 to 91	Input Clamp Voltage	V_{IC}	-	4(h)	I_{IN} (Under Test) = − 18mA Remaining Inputs Open V_{CC} = 4.5V, GND = 0V (Pins D/F 1-2-3-4-5-6-7-8-9-10-11-13-14-23) (Pins C 2-3-4-5-6-7-9-10-11-12-13-16-17-27)	-	−1.5	V

NOTES: See Page 29.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP and FP C = CCP) (NOTE 1)	LIMITS		UNIT
						MIN	MAX	
92 to 99	Short Circuit Output Current	I_{OS}	3011	4(i)	V_{IL} = 0.8V, V_{IH} = 2.0V V_{OUT} (Under Test) = 0.5V Remaining Outputs Open V_{CC} = 5.5V, GND = 0V Notes 2 and 3 Variants 01 to 04 Variants 05 to 08 (Pins D/F 15-16-17-18-19-20-21-22) (Pins C 18-19-20-21-23-24-25-26)	 −30 −30	 −250 −130	mA

NOTES: See Page 29.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST) (NOTE 1)	LIMITS		UNIT
						MIN	MAX	
100	Propagation Delay Low to High (CLK to Q)	t_{PLH}	3004	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Note 2 V_{CC} = 4.5V, GND = 0V Note 4 Variants 01 to 04 Variants 05 to 08	 - -	 15 10	ns
101	Propagation Delay High to Low (CLK to Q)	t_{PHL}	3004	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Note 2 V_{CC} = 4.5V, GND = 0V Note 4 Variants 01 to 04 Variants 05 to 08	 - -	 15 10	ns
102	Output Enable Time High Impedance to Low Output ($\overline{OE}$ to Q)	t_{PZL}	3004	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Note 2 V_{CC} = 4.5V, GND = 0V Note 4 Variants 01 to 04 Variants 05 to 08	 - -	 20 10	ns
103	Output Enable Time High Impedance to High Output ($\overline{OE}$ to Q)	t_{PZH}	3004	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Note 2 V_{CC} = 4.5V, GND = 0V Note 4 Variants 01 to 04 Variants 05 to 08	 - -	 20 10	ns

NOTES: See Page 29.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST) (NOTE 1)	LIMITS		UNIT
						MIN	MAX	
104	Output Disable Time Low Output to High Impedance ($\overline{OE}$ to Q)	t_{PLZ}	3004	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Note 2 V_{CC} = 4.5V, GND = 0V Note 4 Variants 01 to 04 Variants 05 to 08	 - -	 20 10	ns
105	Output Disable Time High Output to High Impedance ($\overline{OE}$ to Q)	t_{PHZ}	3004	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Note 2 V_{CC} = 4.5V, GND = 0V Note 4 Variants 01 to 04 Variants 05 to 08	 - -	 20 10	ns

NOTES: See Page 29.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - SUPPLY CURRENT

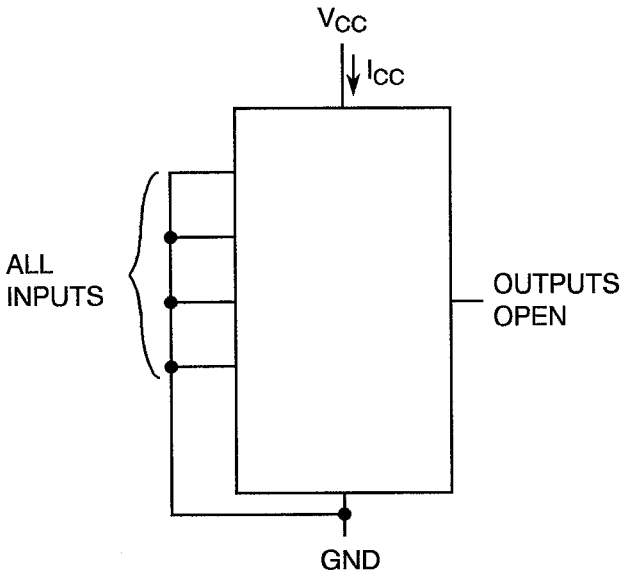
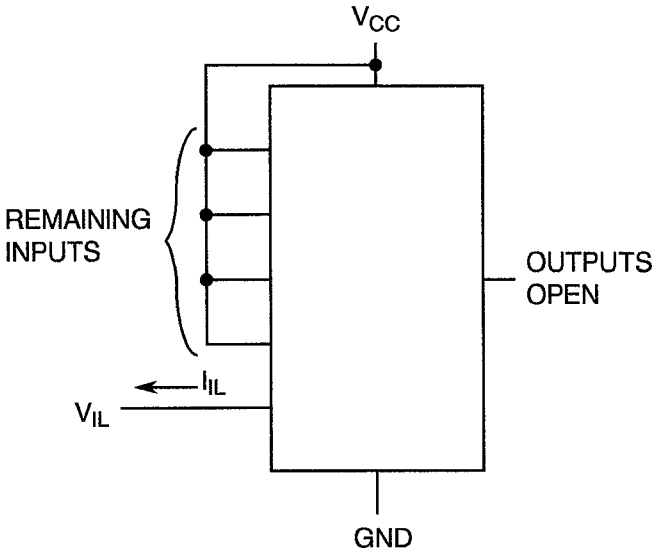
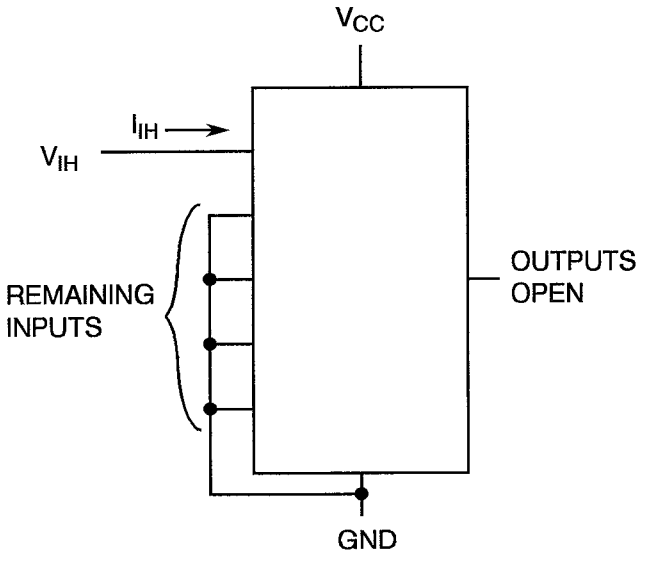


FIGURE 4(b) - INPUT CURRENT LOW LEVEL



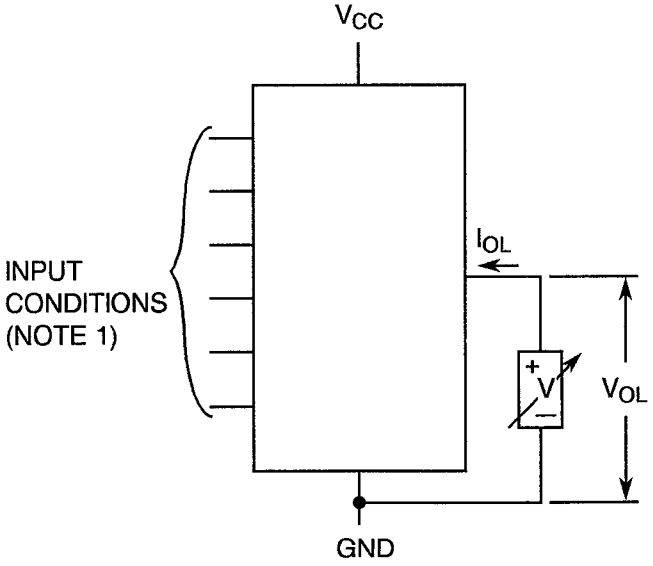
NOTES
1. Each input to be tested separately.

FIGURE 4(c) - INPUT CURRENT HIGH LEVEL



NOTES
1. Each input to be tested separately.

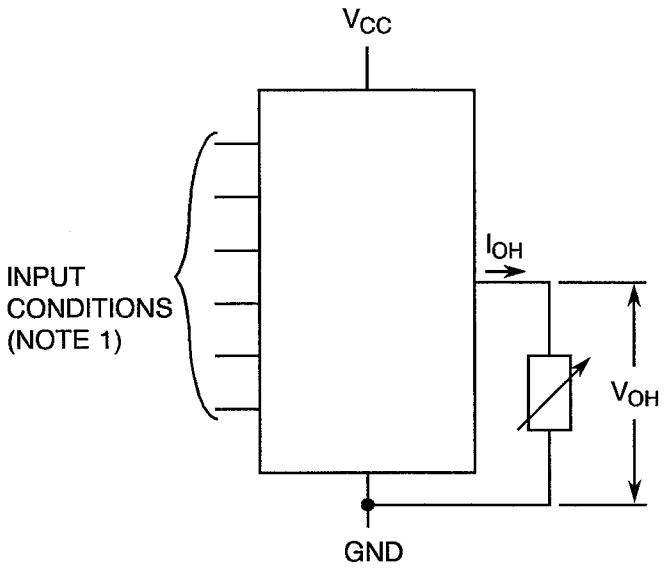
FIGURE 4(d) - OUTPUT VOLTAGE LOW LEVEL



NOTES
1. Manufacturer's Input sequence or Programmed Test sequence.
2. Each output to be tested separately.

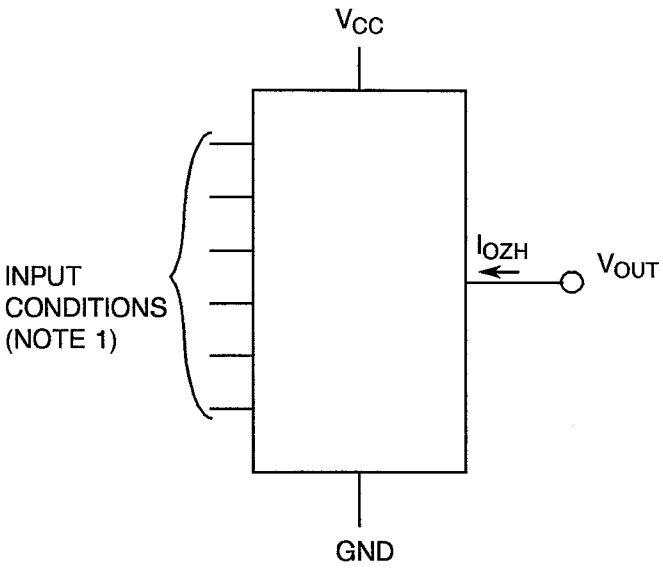
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(e) - OUTPUT VOLTAGE HIGH LEVEL



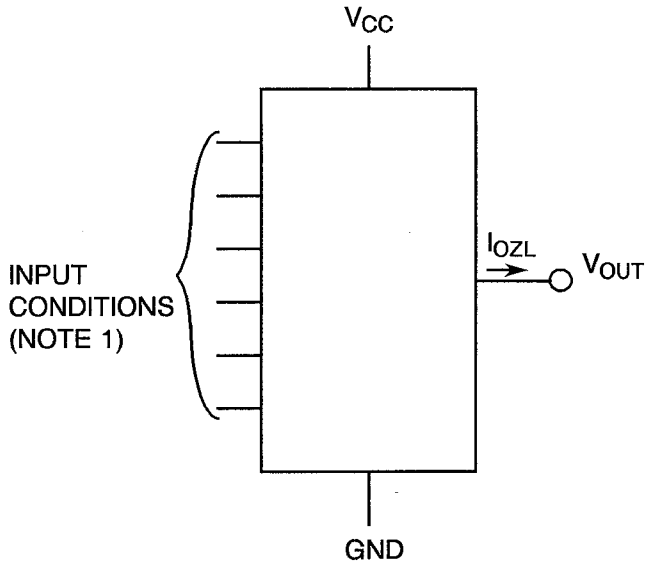
NOTES
1. Manufacturer's Input sequence or Programmed Test sequence.
2. Each output to be tested separately.

FIGURE 4(f) - OUTPUT LEAKAGE CURRENT HIGH LEVEL APPLIED



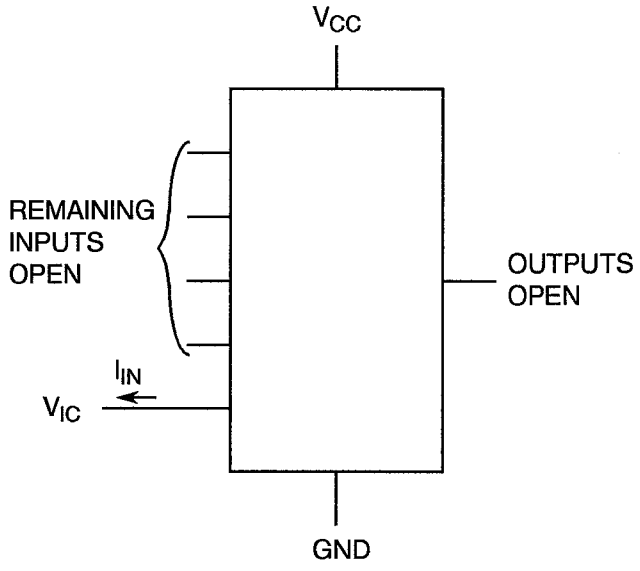
NOTES
1. Manufacturer's Input sequence or Programmed Test sequence.
2. Each output to be tested separately.

FIGURE 4(g) - OUTPUT LEAKAGE CURRENT LOW LEVEL APPLIED



NOTES
1. Manufacturer's Input sequence or Programmed Test sequence.
2. Each output to be tested separately.

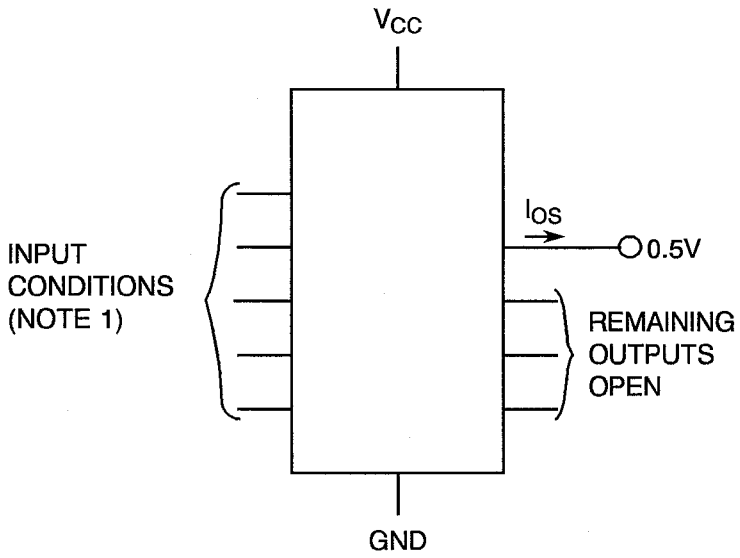
FIGURE 4(h) - INPUT CLAMP VOLTAGE



NOTES
1. Each input to be tested separately.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - SHORT CIRCUIT OUTPUT CURRENT



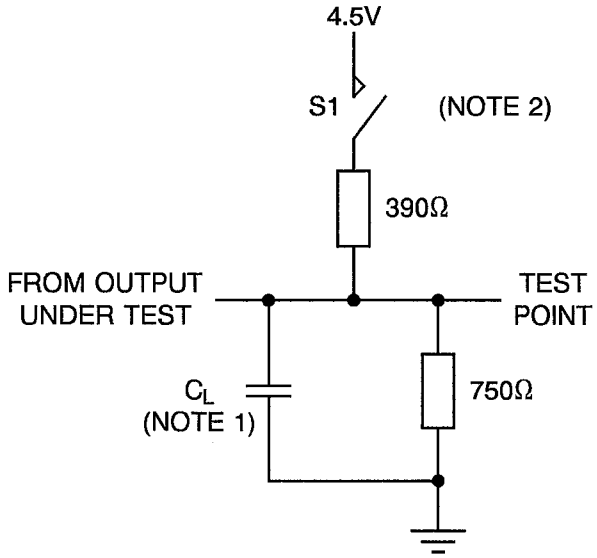
NOTES

1. Manufacturer's Input sequence or Programmed Test sequence.
2. Each output to be tested separately.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

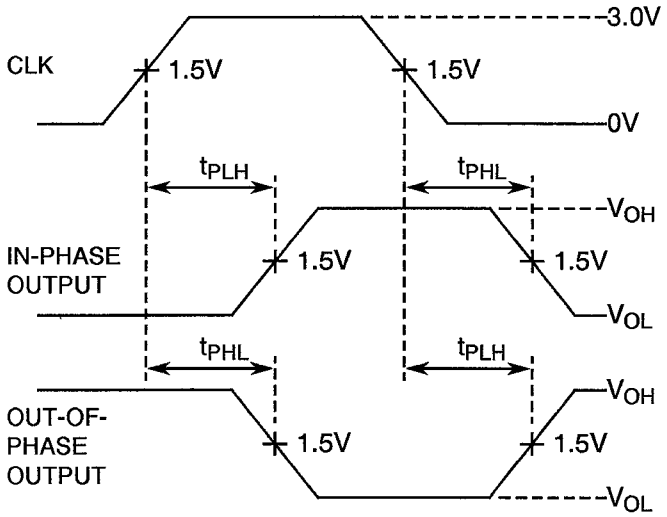
FIGURE 4(j) - PROPAGATION DELAY

a.c. MEASUREMENT LOAD CIRCUIT

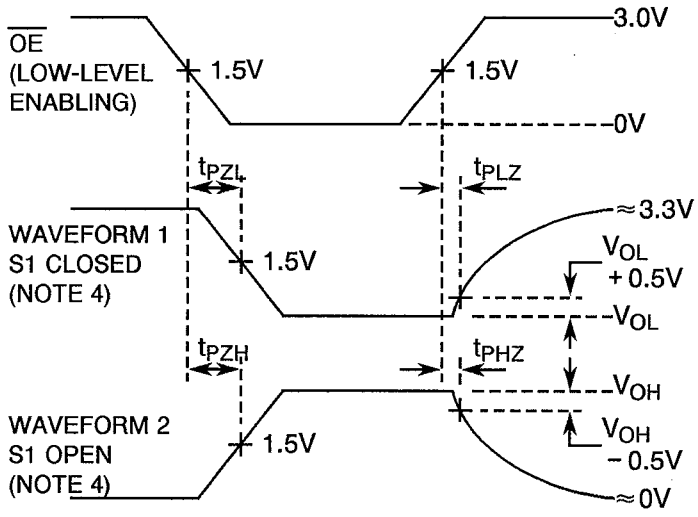


VOLTAGE WAVEFORMS

PROPAGATION DELAY



ENABLE/DISABLE



NOTES

1. C_L includes probe and jig capacitance and is 50pF for t_{pd} and t_{en}, 5.0pF for t_{dis}.
2. When measuring propagation delay times, switch S1 is closed.
3. All input pulses have the following characteristics: PRR ≤ 10MHz, t_r and t_f = 2.0ns, Duty Cycle = 50%.
4. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
3	Supply Current	I_{CC}	As per Table 2	As per Table 2	±10	%
4 to 17	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	±25	µA
18 to 31	Input Current High Level 1	I_{IH1}	As per Table 2	As per Table 2	±1.25 or (1) ±5.0	µA %
46 to 53	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	±50 or (1) ±10	mV %
54 to 61	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	±240 or (1) ±10	mV %
62 to 69	Output Leakage Current Third State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2 Variants 01 to 04 Variants 05 to 08	±10 ±2.0	µA
70 to 77	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2 Variants 01 to 04 Variants 05 to 08	±2.0 ±10	µA

NOTES

1. Whichever is greater, referred to the initial value.

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125 (+0−5)	°C
2	Outputs - (Pins D/F 15-16-17-18-19-20-21-22) (Pins C 18-19-20-21-23-24-25-26)	V_{OUT}	V_{CC}	V
3	Input - (Pin D/F 1) (Pin C 2)	V_{IN}	V_{GEN1}	Vac
4	Inputs - (Pins D/F 2-3-4-5-6-7-8-9-10-11-13-14-23) (Pins C 3-4-5-6-7-9-10-11-12-13-16-17-27)	V_{IN}	V_{GEN2}	Vac
5	Pulse Voltage	V_{GEN}	0.5 to 3.0	Vac
6	Pulse Frequency Square Wave	f_{GEN1} f_{GEN2}	100k 50k 50% Duty Cycle $t_r = t_f \leq 10$ ns	Hz
7	Positive Supply Voltage (Pin D/F 24) (Pin C 28)	V_{CC}	5.5 (+0−0.5)	V
8	Negative Supply Voltage (Pin D/F 12) (Pin C 14)	GND	0	V

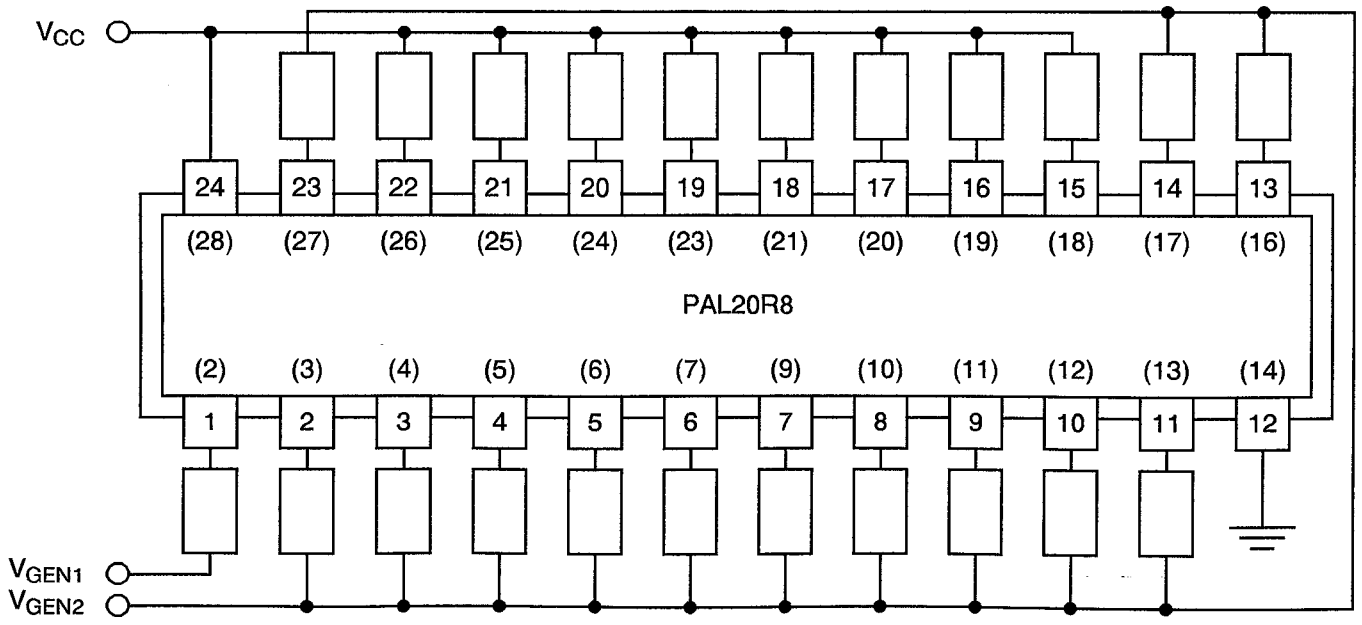
NOTES

1. Input Protection Resistor = Output Load = 470Ω ± 5%.

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Test

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.5 Electrical Circuit for Operating Life Tests

A circuit for use in performing the operating life test is shown in Figure 5(b) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

4.9 TOTAL DOSE IRRADIATION TESTING

Not applicable.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP and FP C = CCP) (NOTE 1)	CHANGE LIMITS (Δ)	LIMITS		UNIT
							MIN	MAX	
1	Functional Test 1	-	-	-	Verify Fuse Integrity V_{IL} = 0V, V_{IH} = 4.5V, V_{IHH} = 10.75V V_{CC} = 4.5V, GND = 0V	-	-	-	-
2	Functional Test 2	-	-		Verify Fuse Integrity V_{IL} = 0V, V_{IH} = 5.5V, V_{IHH} = 10.75V V_{CC} = 5.5V, GND = 0V	-	-	-	-
3	Supply Current	I_{CC}	3005	4(a)	V_{IN} (All Inputs) = 0V All Outputs Open V_{CC} = 5.5V, GND = 0V Variants 01 to 04 Variants 05 to 08 (Pin D/F 24) (Pin C 28)	 ±18 ±22	 - -	 180 220	mA
4 to 17	Input Current Low Level	I_{IL}	3009	4(b)	V_{IN} (Under Test) = 0.4V V_{IN} (Remaining Inputs) = 5.5V V_{CC} = 5.5V, GND = 0V (Pins D/F 1-2-3-4-5-6-7-8-9-10-11-13-14-23) (Pins C 2-3-4-5-6-7-9-10-11-12-13-16-17-27)	±25	-	−250	µA
18 to 31	Input Current High Level 1	I_{IH1}	3010	4(c)	V_{IN} (Under Test) = 2.7V V_{IN} (Remaining Inputs) = 0V V_{CC} = 5.5V, GND = 0V (Pins D/F 1-2-3-4-5-6-7-8-9-10-11-13-14-23) (Pins C 2-3-4-5-6-7-9-10-11-12-13-16-17-27)	±2.5	-	25	µA
32 to 45	Input Current High Level 2	I_{IH2}	3010	4(c)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{CC} = 5.5V, GND = 0V (Pins D/F 1-2-3-4-5-6-7-8-9-10-11-13-14-23) (Pins C 2-3-4-5-6-7-9-10-11-12-13-16-17-27)	-	-	1.0	mA

NOTES: See Page 46.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP and FP C = CCP) (NOTE 1)	CHANGE LIMITS (Δ)	LIMITS		UNIT
							MIN	MAX	
46 to 53	Output Voltage Low Level	V_{OL}	3007	4(d)	V_{IL} = 0.8V, V_{IH} = 2.0V I_{OL} = 12mA V_{CC} = 4.5V, GND = 0V Note 2 (Pins D/F 15-16-17-18-19-20-21-22) (Pins C 18-19-20-21-23-24-25-26)	±0.05	-	0.5	V
54 to 61	Output Voltage High Level	V_{OH}	3006	4(e)	V_{IL} = 0.8V, V_{IH} = 2.0V I_{OH} = 2.0mA V_{CC} = 4.5V, GND = 0V Note 2 (Pins D/F 15-16-17-18-19-20-21-22) (Pins C 18-19-20-21-23-24-25-26)	±0.24	2.4	-	V
62 to 69	Output Leakage Current Third State (High Level Applied)	I_{OZH}	3006	4(f)	V_{IL} = 0.8V, V_{IH} = 2.0V V_{OUT} = 2.7V V_{CC} = 5.5V, GND = 0V Note 2 Variants 01 to 04 Variants 05 to 08 (Pins D/F 15-16-17-18-19-20-21-22) (Pins C 18-19-20-21-23-24-25-26)	 ±10 ±2.0	 - -	 100 20	µA
70 to 77	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	3006	4(g)	V_{IL} = 0.8V, V_{IH} = 2.0V V_{OUT} = 0.4V V_{CC} = 5.5V, GND = 0V Note 2 Variants 01 to 04 Variants 05 to 08 (Pins D/F 15-16-17-18-19-20-21-22) (Pins C 18-19-20-21-23-24-25-26)	 ±2.0 ±10	 - -	 −20 −100	µA

NOTES: See Page 46.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP and FP C = CCP) (NOTE 1)	CHANGE LIMITS (Δ)	LIMITS		UNIT
							MIN	MAX	
78 to 91	Input Clamp Voltage	V_{IC}	-	4(h)	I_{IN} (Under Test) = −18mA Remaining Inputs Open V_{CC} = 4.5V, GND = 0V (Pins D/F 1-2-3-4-5-6-7-8-9-10-11-13-14-23) (Pins C 2-3-4-5-6-7-9-10-11-12-13-16-17-27)	-	-	−1.5	V
92 to 99	Short Circuit Output Current	I_{OS}	3011	4(i)	V_{IL} = 0.8V, V_{IH} = 2.0V V_{OUT} (Under Test) = 0.5V Remaining Outputs Open V_{CC} = 5.5V, GND = 0V Notes 2 and 3 Variants 01 to 04 Variants 05 to 08 (Pins D/F 15-16-17-18-19-20-21-22) (Pins C 18-19-20-21-23-24-25-26)	 - -	 −30 −30	 −250 −130	mA

NOTES

1. To be performed on programmed devices only.
2. The appropriate Truth Table for the programmed device shall be used.
3. No more than one output should be shorted at a time and the duration shall not exceed 1 second.
4. Measurements shall be performed on 100% basis go-no-go. The test pins given relate only to the Manufacturer's Qualification programme and shall be amended accordingly for other programmes.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING
- a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST) (NOTE 1)	LIMITS		UNIT
						MIN	MAX	
100	Propagation Delay Low to High (CLK to Q8)	t_{PLH}	3004	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Note 2 V_{CC} = 4.5V, GND = 0V Note 4 Variants 01 to 04 Variants 05 to 08 Pins D/F 1 to 22 Pins C 2 to 26	 - -	 15 10	ns
101	Propagation Delay High to Low (CLK to Q8)	t_{PHL}	3004	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Note 2 V_{CC} = 4.5V, GND = 0V Note 4 Variants 01 to 04 Variants 05 to 08 Pins D/F 1 to 22 Pins C 2 to 26	 - -	 15 10	ns
102	Output Enable Time High Impedance to Low Output ($\overline{OE}$ to Q8)	t_{PZL}	3004	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Note 2 V_{CC} = 4.5V, GND = 0V Note 4 Variants 01 to 04 Variants 05 to 08 Pins D/F 13 to 22 Pins C 16 to 26	 - -	 20 10	ns

NOTES: See Page 46.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST) (NOTE 1)	LIMITS		UNIT
						MIN	MAX	
103	Output Enable Time High Impedance to High Output ($\overline{OE}$ to Q8)	t_{PZH}	3004	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Note 2 V_{CC} = 4.5V, GND = 0V Note 4 Variants 01 to 04 Variants 05 to 08 Pins D/F 13 to 22 Pins C 16 to 26	 - -	 20 10	ns
104	Output Disable Time Low Output to High Impedance ($\overline{OE}$ to Q8)	t_{PLZ}	3004	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Note 2 V_{CC} = 4.5V, GND = 0V Note 4 Variants 01 to 04 Variants 05 to 08 Pins D/F 13 to 22 Pins C 16 to 26	 - -	 20 10	ns
105	Output Disable Time High Output to High Impedance ($\overline{OE}$ to Q8)	t_{PHZ}	3004	4(j)	V_{IN} (Under Test) = Pulse Generator V_{IN} (Remaining Inputs) = Note 2 V_{CC} = 4.5V, GND = 0V Note 4 Variants 01 to 04 Variants 05 to 08 Pins D/F 13 to 22 Pins C 16 to 26	 - -	 20 10	ns

NOTES: See Page 46.

APPENDIX 'A'

AGREED DEVIATIONS FOR TEXAS INSTRUMENTS (F)

QUALIFICATION PROGRAMMING PATTERN

Variants 01 to 04 — Family Code = A127 — Checksum = 1AA0
Variants 05 to 08 — Family Code = 0B27 — Checksum = 17D8

Variants 01 to 04

QP24
QF2560

L0000

Prod. Lines	Input Lines 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
0	0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
1	0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
2	1 1 1 1 1 1 0 1 0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
3	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
4	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
5	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 0 1 0 1 0 1 1 1 1 1 1 1
6	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 0 1 0 1 0
7	1 0 1 0 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 0
8	0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
9	0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

L0400 (2)

10	1 1 1 1 1 1 0 1 0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
11	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
12	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
13	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 0 1 0 1 0 1 1 1 1 1 1 1
14	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 0 1 0 1 0
15	1 0 1 0 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 0
16	0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
17	0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
18	1 1 1 1 1 1 0 1 0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
19	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

L0800 (2)

20	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
21	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 0 1 0 1 0 1 1 1 1 1 1 1
22	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 0 1 0 1 0
23	1 0 1 0 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 0
24	0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
25	0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
26	1 1 1 1 1 1 0 1 0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
27	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
28	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
29	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 0 1 0 1 0 1 1 1 1 1 1 1

L1200 (2)

NOTES: See Page 52.

APPENDIX 'A'

AGREED DEVIATIONS FOR TEXAS INSTRUMENTS (F)

QUALIFICATION PROGRAMMING PATTERN (CONT'D)

Variants 01 to 04 (Cont'd)

Prod. Lines	Input Lines 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39
30	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
31	1	0	1	0	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0
32	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
33	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
34	1	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
35	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
36	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
37	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1
38	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
39	1	0	1	0	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0
L1600 (2)																																								
40	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
41	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
42	1	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
43	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
44	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
45	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1
46	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
47	1	0	1	0	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0
48	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
49	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
L2000 (2)																																								
50	1	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
51	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
52	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
53	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1
54	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
55	1	0	1	0	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0
56	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
57	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
58	1	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
59	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
L2400 (2)																																								
60	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
61	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1
62	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
63	1	0	1	0	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0

C1AA0

NOTES: See Page 52.

APPENDIX 'A'

AGREED DEVIATIONS FOR TEXAS INSTRUMENTS (F)

QUALIFICATION PROGRAMMING PATTERN (CONT'D)

Variants 05 to 08

QP24
QP24
QF2560

L0000

Prod. Lines	Input Lines																																							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39
0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
3	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
5	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1
6	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
7	1	1	1	0	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0
8	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
9	1	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
L0400 (2)																																								
10	0	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
11	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
13	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1
14	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
15	1	1	1	0	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0
16	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
17	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
18	0	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
19	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
L0800 (2)																																								
20	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
21	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1
22	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
23	1	1	1	0	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0
24	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
25	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
26	0	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
27	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
28	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
29	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1

L1200 (2)

NOTES: See Page 52.

APPENDIX 'A'

AGREED DEVIATIONS FOR TEXAS INSTRUMENTS (F)

QUALIFICATION PROGRAMMING PATTERN (CONT'D)

Variants 05 to 08 (Cont'd)

Prod. Lines	Input Lines																																							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39
30	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
31	1	1	1	0	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0
32	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
33	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
34	1	0	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
35	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
36	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
37	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1
38	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
39	1	1	1	0	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0
L1600 (2)																																								
40	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
41	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
42	1	0	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
43	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
44	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
45	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1
46	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
47	1	1	1	0	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0
48	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
49	1	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
L2000 (2)																																								
50	1	0	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
51	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
52	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
53	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1
54	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
55	1	1	1	0	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0
56	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
57	1	0	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
58	1	0	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
59	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
L2400 (2)																																								
60	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
61	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1
62	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
63	1	1	1	0	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0
C17D8																																								

NOTES

1. 1 = Retained fuse, 0 = Blown fuse.
2. Intermediate sum.