INTEGRATED CIRCUITS, MONOLITHIC,

SILICON ON SAPPHIRE, CMOS PROGRAMMABLE

COMMUNICATION INTERFACE,

BASED ON TYPE MAS28151

ESCC Detail Specification No. 9544/003

ISSUE 1

October 2002

Document Custodian: European Space Agency - see https://escies.org

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Pages 1 to 53

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space components
coordination group

Issue/Rev.	Date	Approved by	
		SCCG Chairman	ESA Director General or his Deputy
Issue 1	August 1993		

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE Reference	CHANGE Item	Approved DCR No.

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1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a monolithic, Silicon on Sapphire CMOS Programmable Communication Interface, based on Type MAS28151. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE/INSTRUCTION SET

As per Figure 3(b).

1.8 CIRCUIT DESCRIPTION

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 with a Minimum Critical Path Failure Voltage of 500Volts.

1.11 INPUT PROTECTION NETWORKS

Protection networks shall be incorporated into each input as shown in Figure 3(e).

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND FINISH
01	DIL	2(a)	D2
02	DIL	2(b)	D2
03	FLAT	2(c)	D2

TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage	V_{DD}	− 0.3 to + 7.0	V	-
2	Input Voltage	V_{IN}	− 0.3 to V_{DD} + 0.3	V	-
3	Supply Current	$I_{DD(op)}$	50	mA	-
4	Device Dissipation	P_D	500	mWdc	Note 1
5	Operating Temperature Range	T_{op}	− 55 to + 125	°C	T_{amb}
6	Storage Temperature Range	T_{stg}	− 65 to + 150	°C	-
7	Soldering Temperature	T_{sol}	+ 250	°C	Note 2

NOTES

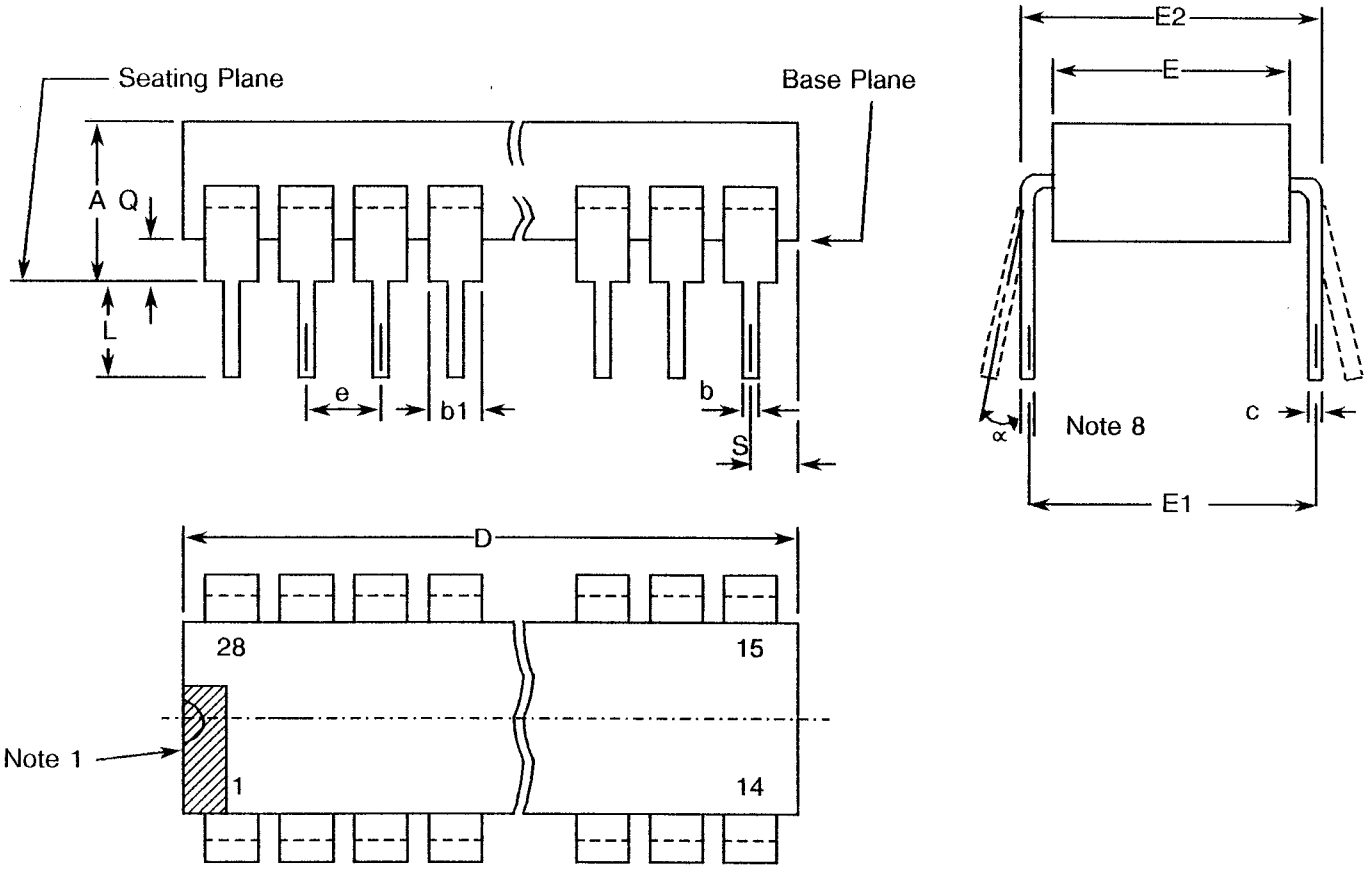
1. Current through any 1 pin limited to ± 20mA.
2. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION

Not applicable.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - DUAL-IN-LINE PACKAGE, 28 PIN

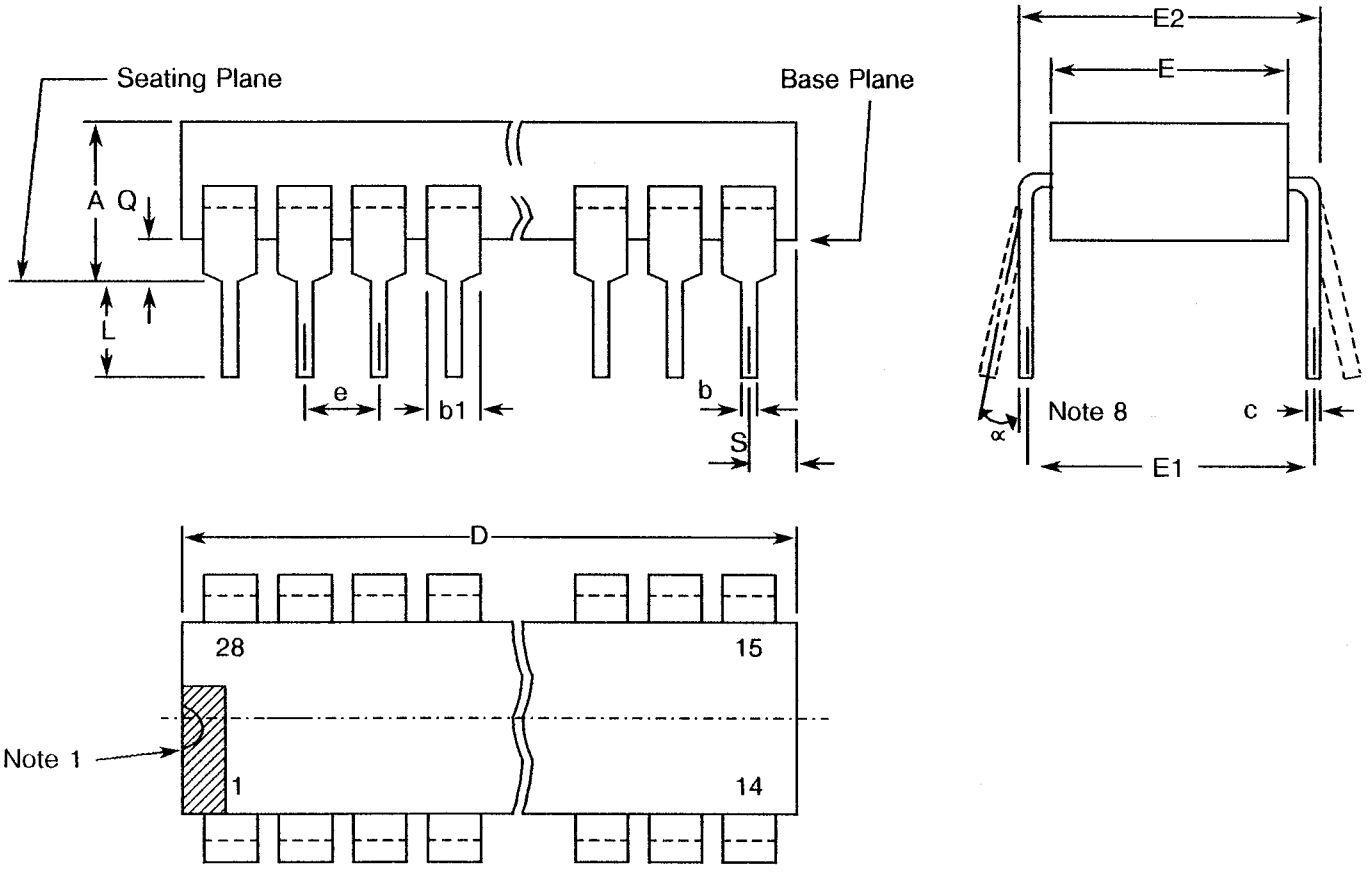


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	-	4.24	2
b	0.40	0.51	4
b1	-	1.53	4
c	0.20	0.31	4
D	-	36.02	
E	14.94 TYPICAL		
E1	15.24 TYPICAL		
E2	-	15.90	
e	2.54 TYPICAL		5,6
L	3.18	4.36	4
Q	1.02	1.53	3
S	-	1.27	7
α	0°	15°	8

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - DUAL-IN-LINE PACKAGE, 28 PIN

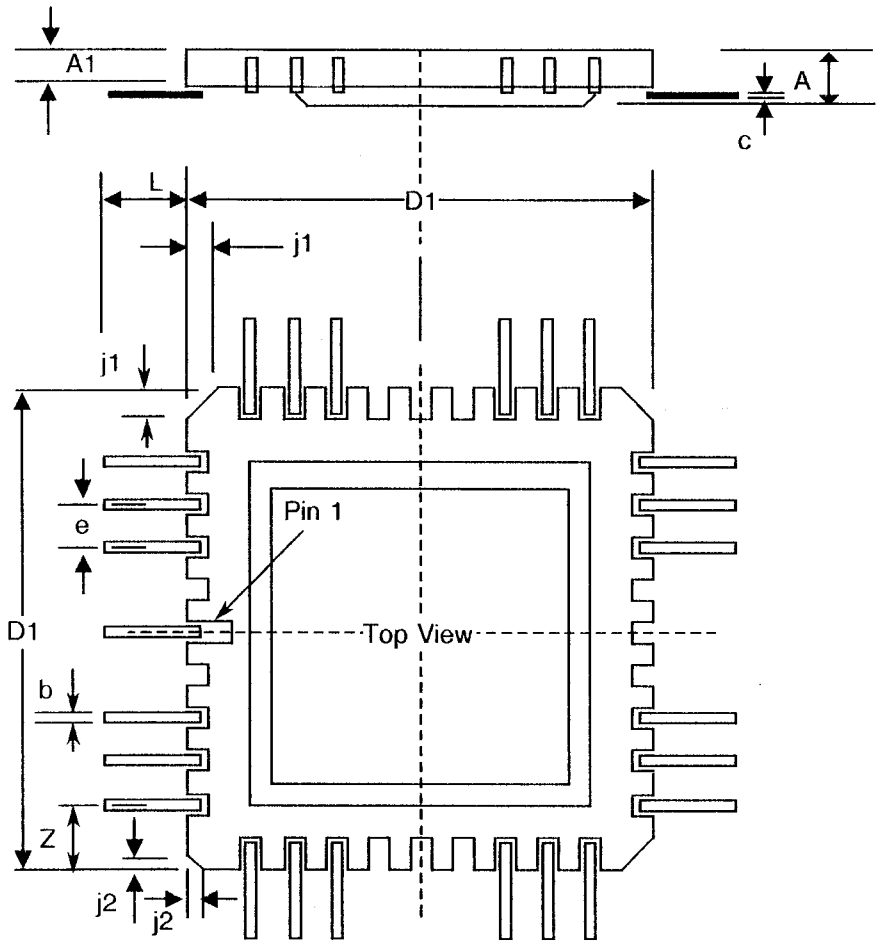


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	-	4.24	2
b	0.40	0.51	4
b1	-	1.53	4
c	0.20	0.31	4
D	-	36.02	
E	14.94 TYPICAL		
E1	15.24 TYPICAL		
E2	-	15.90	
e	2.54 TYPICAL		5,6
L	3.18	4.36	4
Q	1.02	1.53	3
S	-	1.27	7
∝	0°	15°	8

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(c) - FLAT PACKAGE, 68 TERMINAL



SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	-	2.59	3
A1	1.83	2.24	
b	0.25	0.51	
c	0.10	0.20	4
D1	23.88	24.51	
e	2.54 TYPICAL		2
j1	1.02 TYPICAL		
j2	0.51 TYPICAL		
L	8.89	9.27	
Z	1.65	2.16	

NOTES: See Page 10.

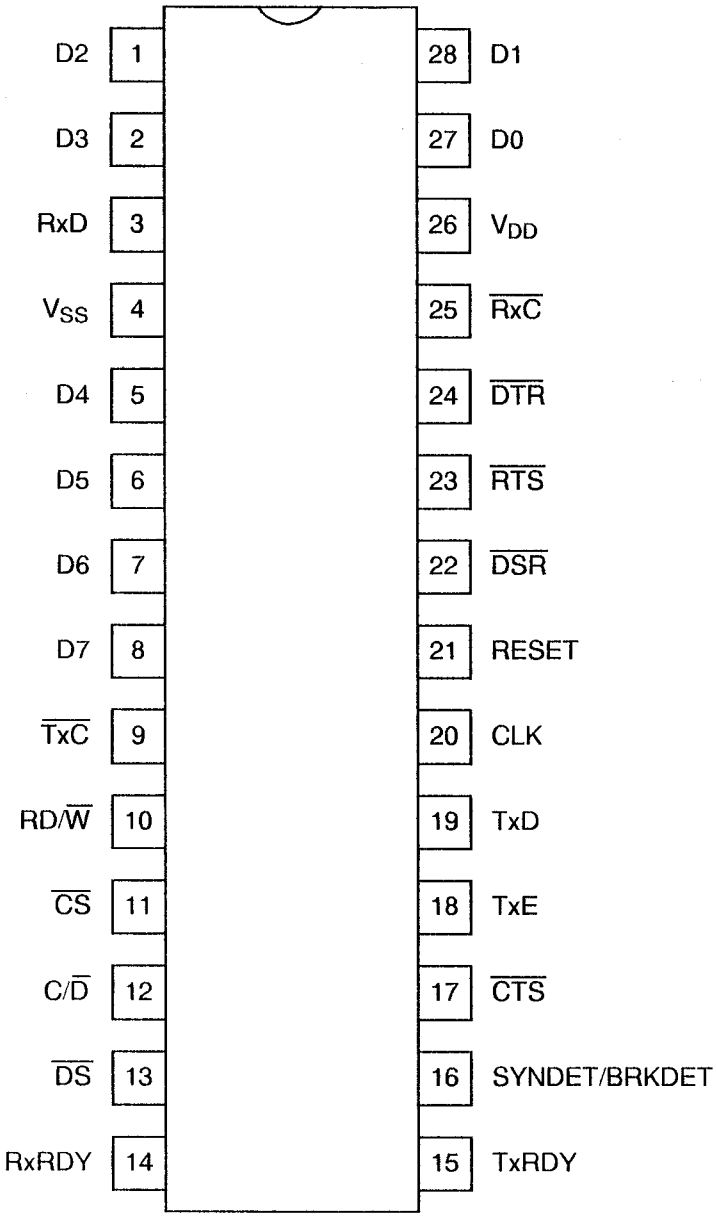
FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURES 2(a) TO 2(c)

1. Index area; a notch, letter or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown.
2. This dimension includes any lid.
3. The dimension shall be measured from the seating plane to the base plane.
4. All leads.
5. 26 spaces for dual-in-line packages.
   64 spaces for flat packages.
6. The true position pins spacing is 2.54mm between centre lines. Each pin centreline shall be located within 0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.
7. All 4 corners.
8. Lead centre when α is 0°.
9. The dimension shall be measured at the point of exit of the lead from the body.

FIGURE 3(a) - PIN ASSIGNMENT

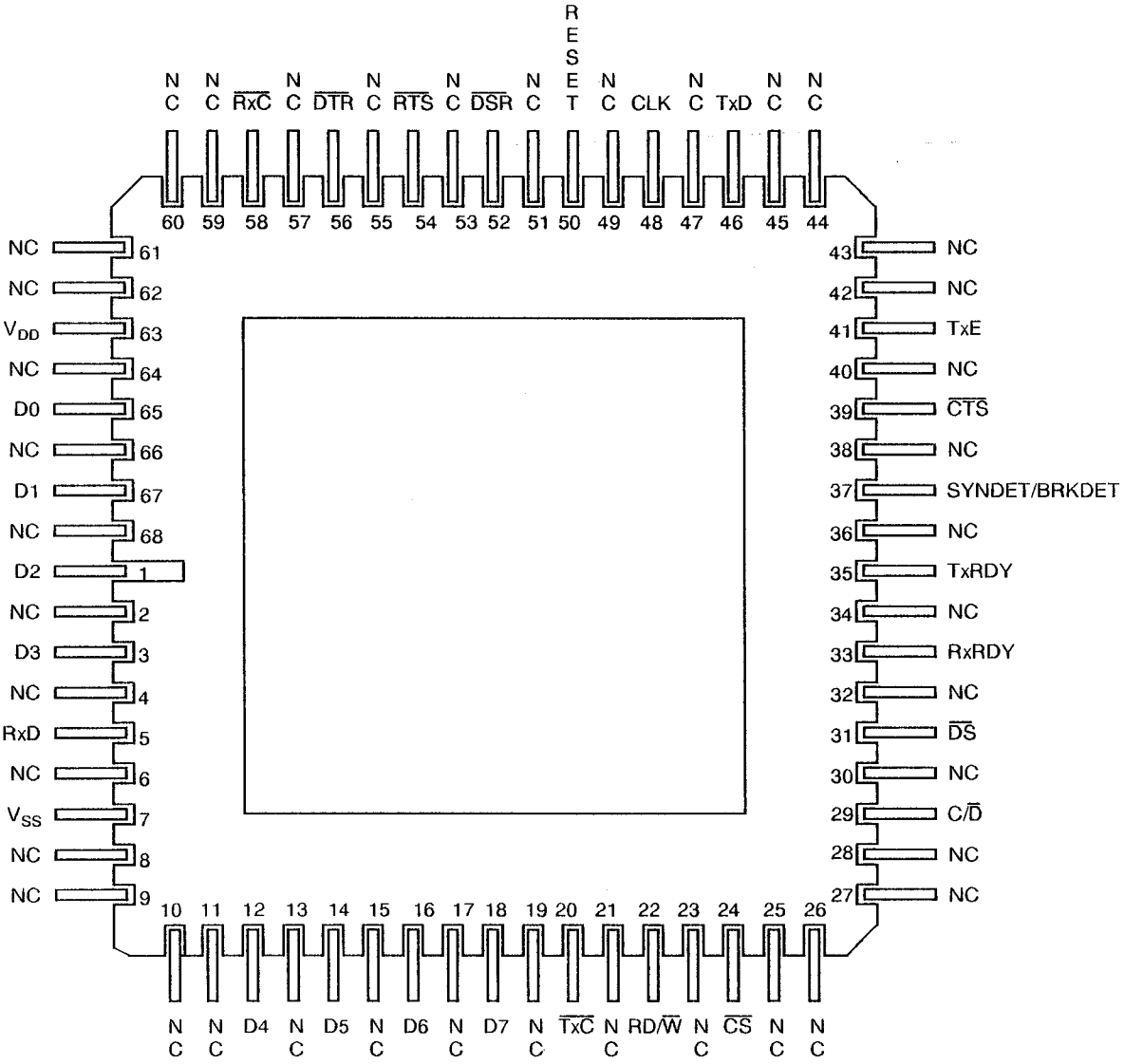
DUAL-IN-LINE PACKAGE



(TOP VIEW)

FIGURE 3(a) - PIN ASSIGNMENT (CONTINUED)

FLAT PACKAGE



TOP VIEW

NOTES

1. For pin descriptions, see Page 13.

FIGURE 3(a) - PIN ASSIGNMENT (CONTINUED)

PIN DESCRIPTION

SYMBOL	FUNCTION	DESCRIPTION	PIN NUMBER	
			DIL	FP
D2	Data Bus	Input/Output	1	1
D3	Data Bus	Input/Output	2	3
RxD	Receive Buffer	Input	3	5
V_{SS}	Input	Negative Supply	4	7
D4	Data Bus	Input/Output	5	12
D5	Data Bus	Input/Output	6	14
D6	Data Bus	Input/Output	7	16
D7	Data Bus	Input/Output	8	18
$\overline{TxC}$	Transmitter Clock	Input	9	20
RD/$\overline{W}$	Read/Write	Input	10	22
$\overline{CS}$	Chip Select	Input	11	24
C/$\overline{D}$	Control/Data	Input	12	29
$\overline{DS}$	Data Strobe	Input	13	31
RxRDY	Receiver Ready	Output	14	33
TxRDY	Transmitter Ready	Output	15	35
SYNDET/BRKDET	Sync/Break Detect	Input/Output	16	37
$\overline{CTS}$	Clear to Send	Input	17	39
TxE	Transmitter Empty	Output	18	41
TxD	Transmit Buffer	Output	19	46
CLK	Clock Input	Input	20	48
RESET	Reset	Input	21	50
$\overline{DSR}$	Data Set Ready	Input	22	52
$\overline{RTS}$	Request to Send	Output	23	54
$\overline{DTR}$	Data Terminal Ready	Output	24	56
$\overline{RxC}$	Receiver Clock	Input	25	58
V_{DD}	Input	Positive Supply	26	63
D0	Data Bus	Input/Output	27	65
D1	Data Bus	Input/Output	28	67

FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET

COMMAND INSTRUCTION FORMAT

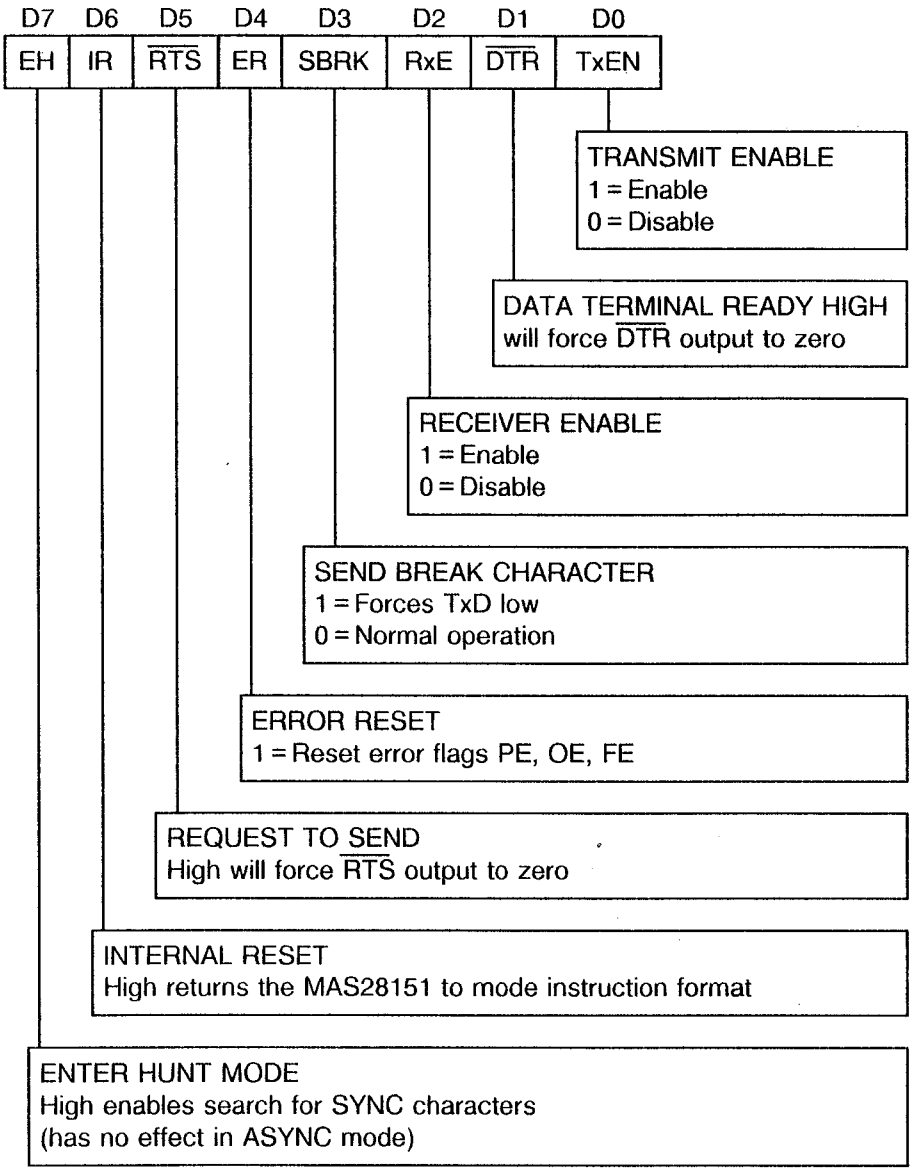
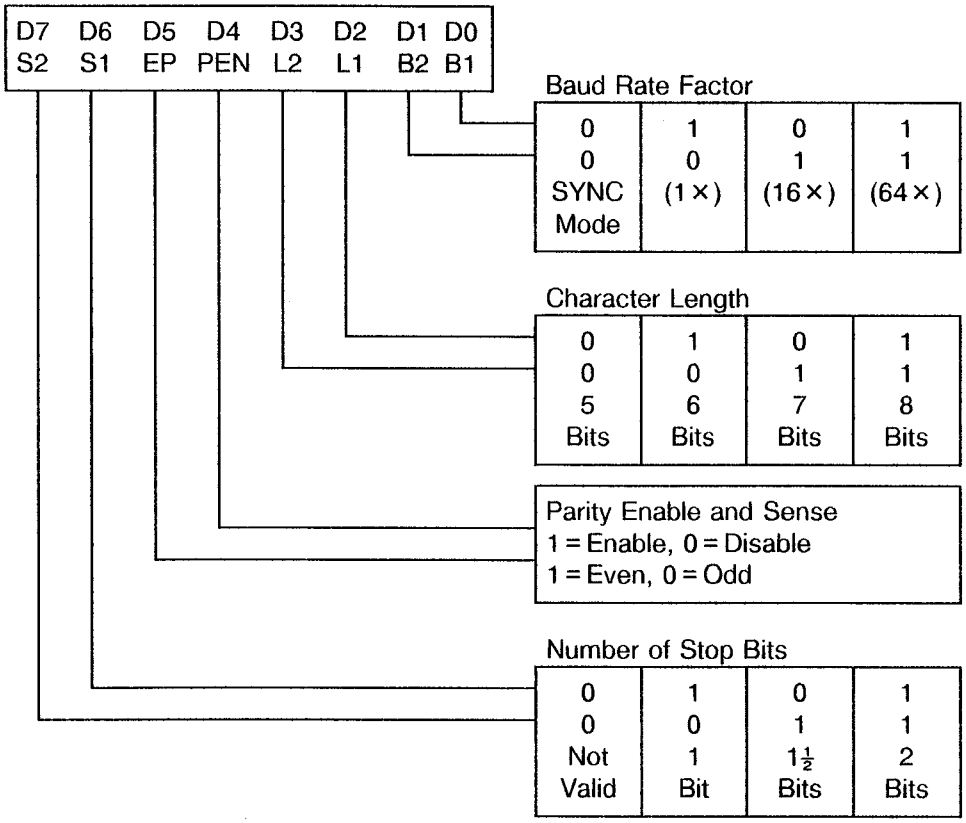


FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

MODE INSTRUCTION FORMAT - ASYNCHRONOUS MODE



MODE INSTRUCTION FORMAT - SYNCHRONOUS MODE

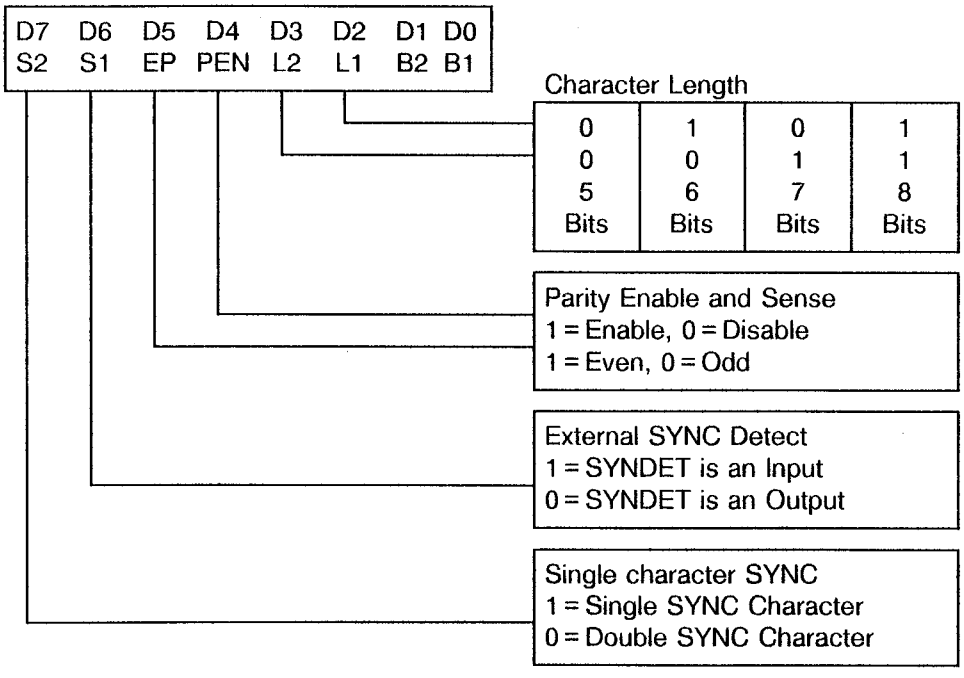
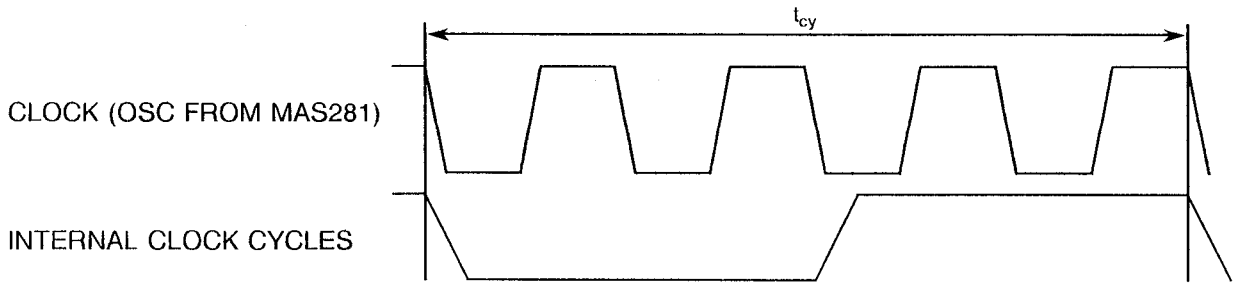


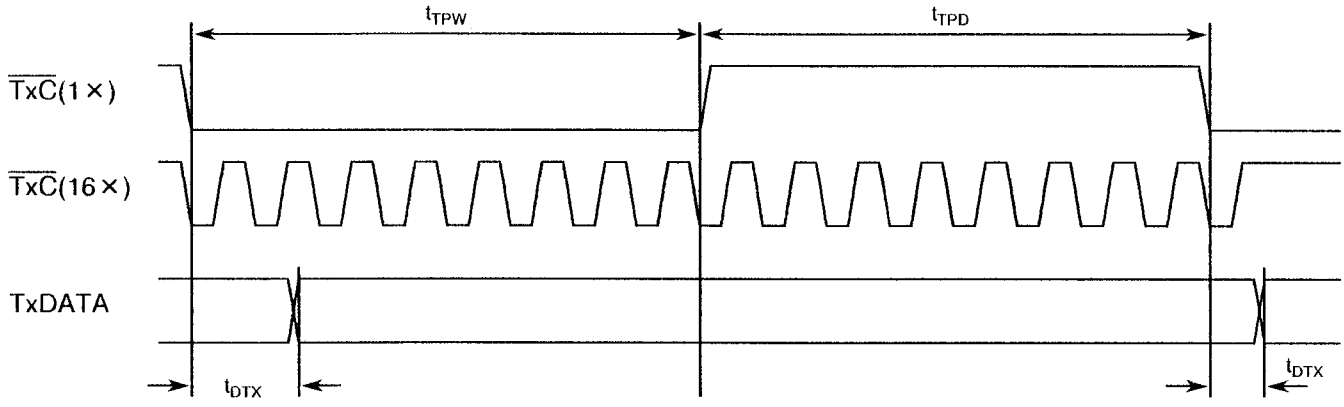
FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

TIMING DIAGRAMS

SYSTEM CLOCK INPUT TIMING DIAGRAM



TRANSMITTER CLOCK AND DATA TIMING DIAGRAM



RECEIVE CLOCK AND DATA TIMING DIAGRAM

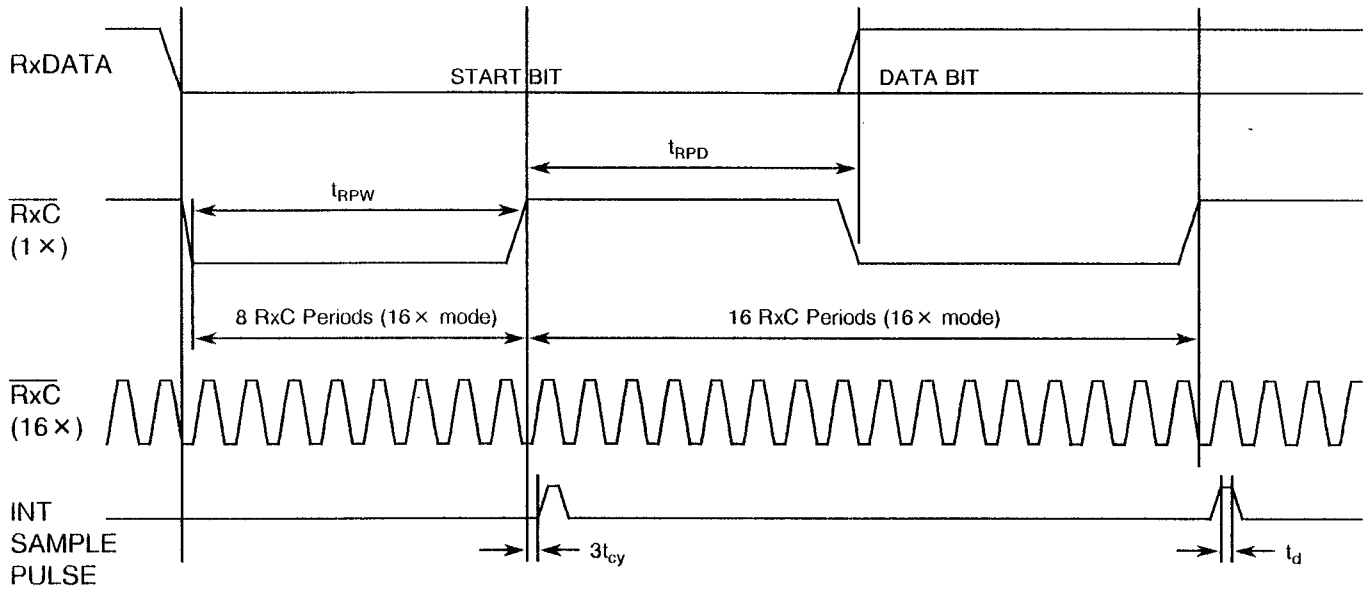
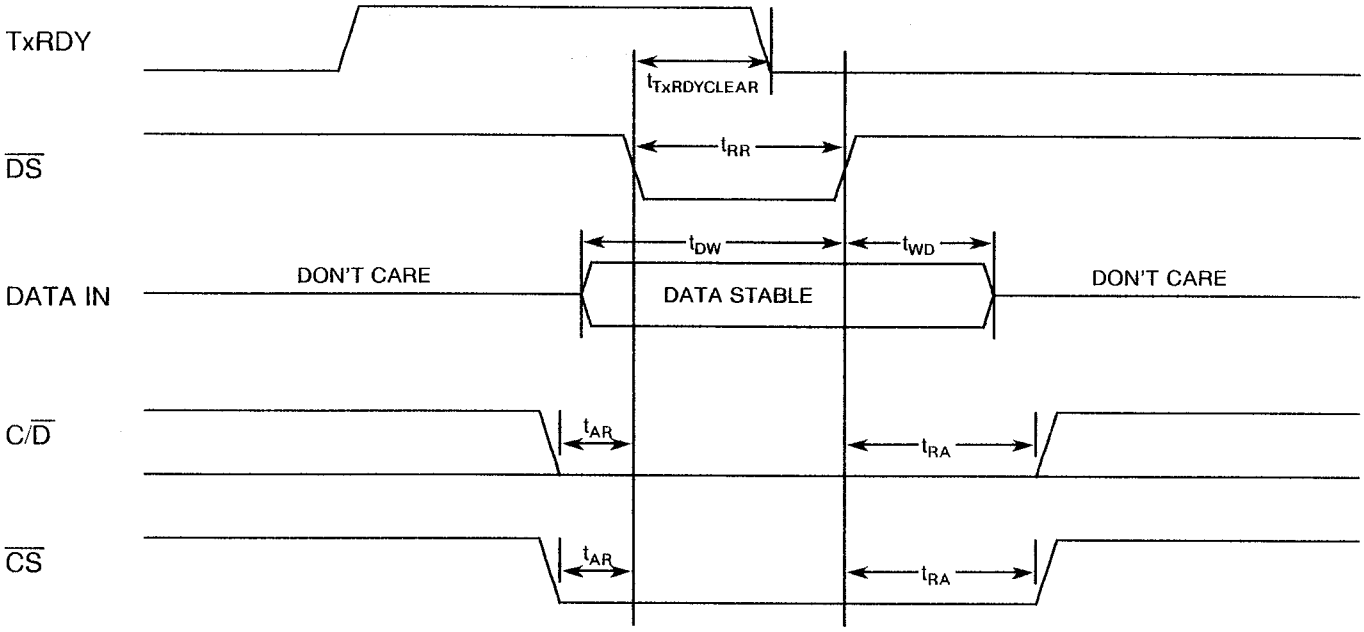


FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

TIMING DIAGRAMS (CONTINUED)

WRITE DATA CYCLE (CPU TO USART) TIMING DIAGRAM



READ DATA CYCLE (USART TO CPU) TIMING DIAGRAM

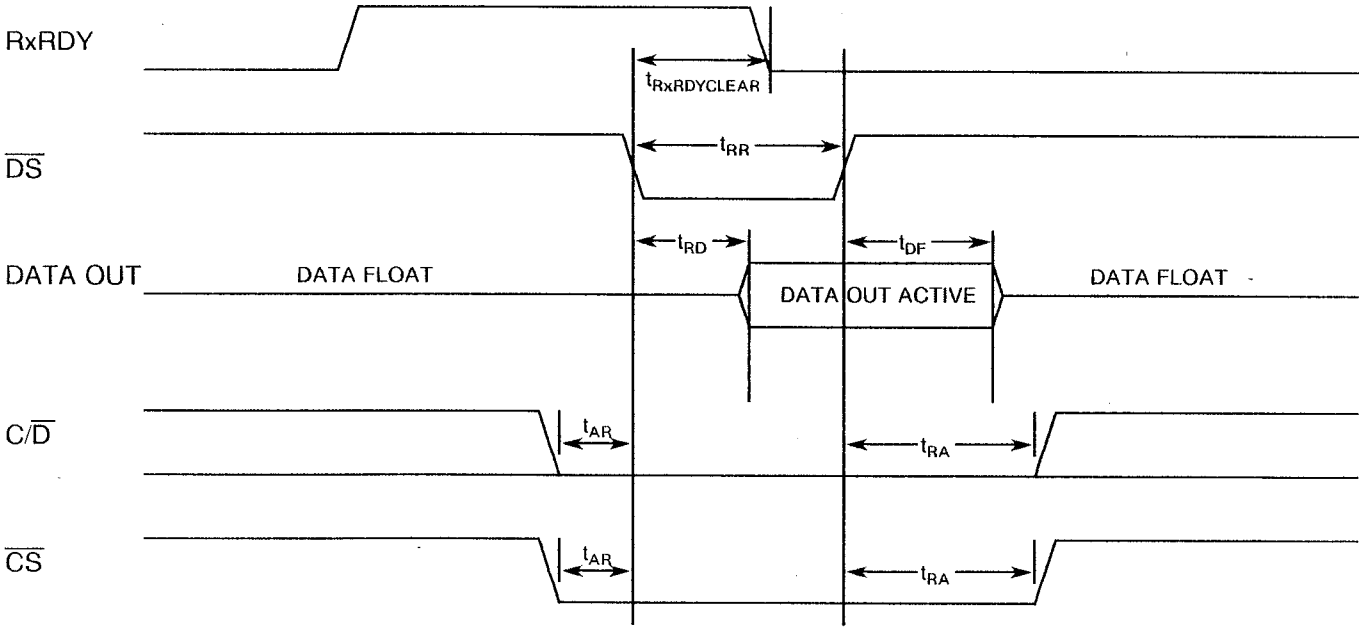
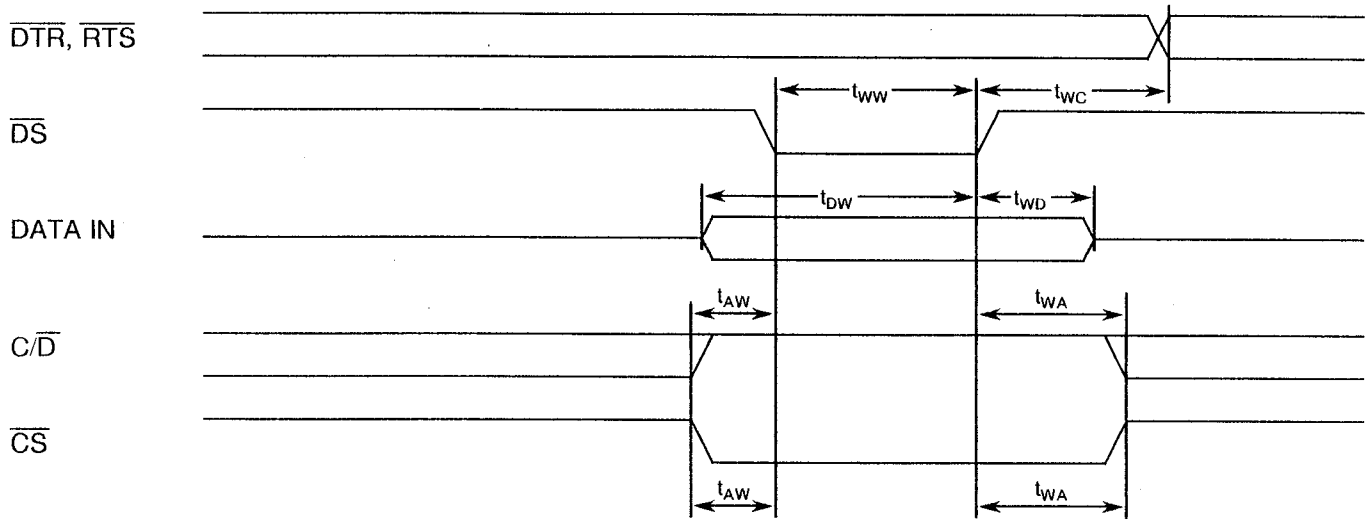


FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

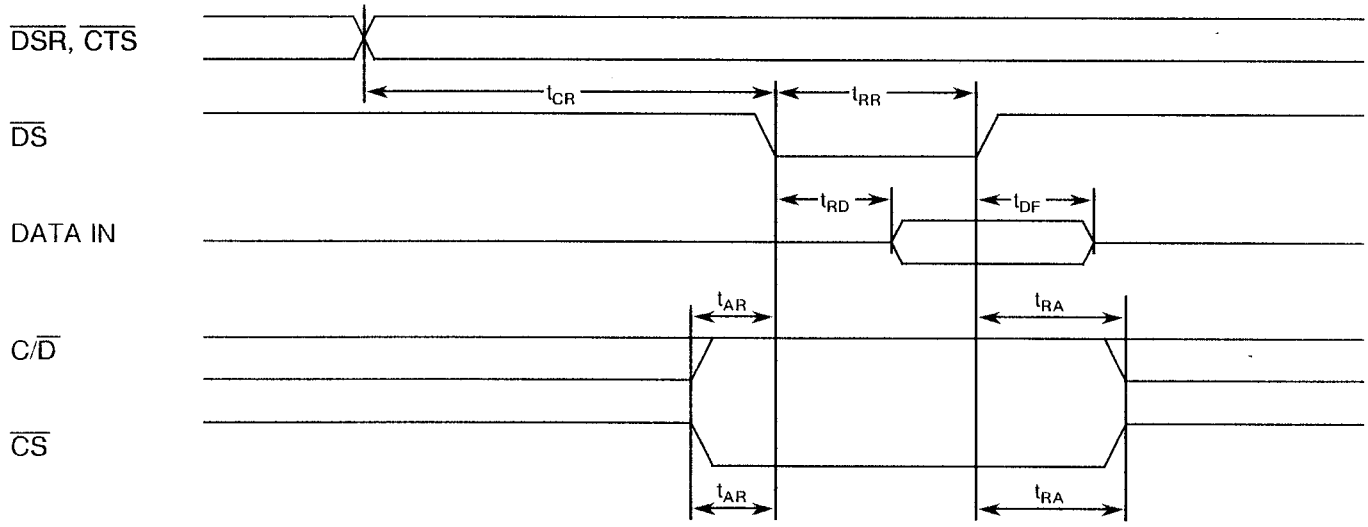
TIMING DIAGRAMS (CONTINUED)

WRITE CONTROL OR OUTPUT PORT CYCLE (CPU TO USART) TIMING DIAGRAM



NOTES
1. t_{WC} includes the response timing of a control byte.

READ CONTROL OR OUTPUT PORT CYCLE (USAR TO CPU) TIMING DIAGRAM

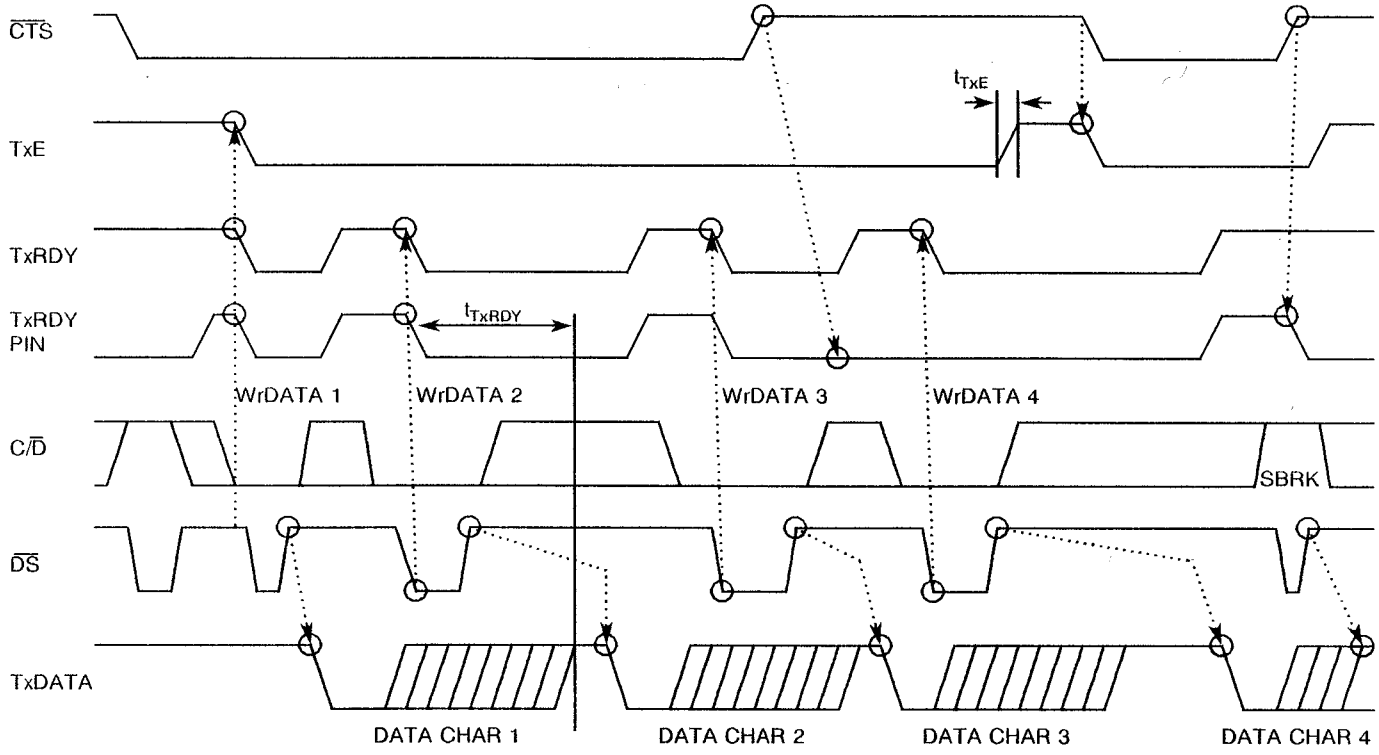


NOTES
1. t_{CR} includes the effect of $\overline{CTS}$ on the TxENABLE circuitry.

FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

TIMING DIAGRAMS (CONTINUED)

TRANSMITTER CONTROL AND FLAG TIMING (ASYNC MODE) TIMING DIAGRAM



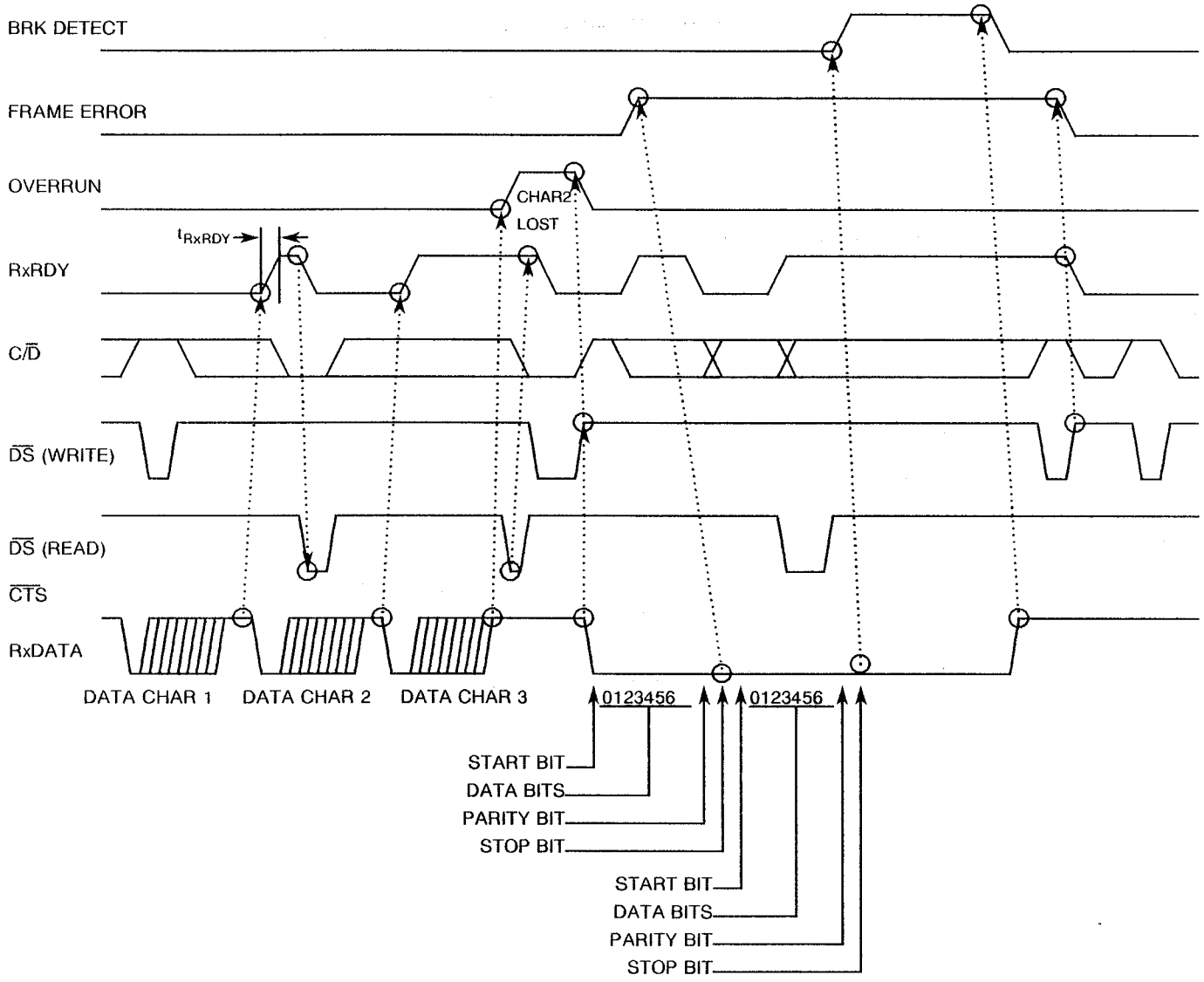
NOTES

1. Example format = 7 bit character with parity and 2 stop bits.

FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

TIMING DIAGRAMS (CONTINUED)

RECEIVER CONTROL AND FLAG TIMING (ASYNC MODE) TIMING DIAGRAM



NOTES

1. Example format = 7 bit character with parity and 2 stop bits.

FIGURE 3(c) - CIRCUIT DESCRIPTION

D0-7 - The Data Bus Buffer is a 3-State, bidirectional, 8 bit buffer used to interface the MAS28151 to the system data bus. Data is transmitted or received by the buffer on execution of output or input instructions from the CPU. Control word, command words and status information are also transferred through the Data Bus Buffer. The Command Status, Data-in and Data-out registers are separate 8-bit registers, communicating with the system bus through the Data Bus buffer.

This functional block accepts inputs from the system Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for the device functional definition.

RESET - A "high" on this input forces the MAS28151 into "idle" mode. The device will remain at "idle" until a new set of control words is written into the MAS28151 to programme its functional definition.

CLK - The Clock input is used to generate internal device timing and is normally connected to the clock generator of the CPU.

$\overline{DS}$ - The Data Strobe input indicates that a data transfer is taking place. During a CPU write operation the MAS28151 reads data from the bus on the rising edge of $\overline{DS}$. During a CPU read operation the MAS28151 can output data while $\overline{DS}$ is low.

RD/$\overline{W}$ - A high on the RD/$\overline{W}$ input indicates a read of data or status information from the MAS28151. A low indicates a transfer of data or control words into the MAS28151. The RD/$\overline{W}$ line is valid only when $\overline{DS}$ is low.

C/$\overline{D}$ - This input, in conjunction with the $\overline{DS}$ and RD/$\overline{W}$ inputs, informs the MAS28151 that the word on the Data Bus is either a data character, control word or status information. Logic 1 = Control/Status, Logic 0 = Data.

$\overline{CS}$ - A low on this input selects the MAS28151. No reading or writing will occur unless the device is selected. When $\overline{CS}$ is high, the Data Bus is in the float state and the $\overline{DS}$ and RD/$\overline{W}$ lines have no effect on the chip.

Modem Control - The MAS28151 has a set of control signals which can be used to simplify the interface to almost any modem. The modem control signals are general purpose in nature and can be used for functions other than modem control, if required.

$\overline{DSR}$ - The Data Set Ready input signal is a general purpose, 1-bit inverting input port. Its condition can be tested by the CPU using a status Read Operation. $\overline{DSR}$ input is normally used to test modem conditions such as Data Set Ready.

$\overline{DTR}$ - The Data Terminal Ready output signal is a general purpose, 1-bit inverting output port. It can be set low by programming the appropriate bit in the Command instruction word. The $\overline{DTR}$ output signal is normally used for modem control such as Data Terminal Ready.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

RxRDY - The Receiver Ready output indicates that the MAS28151 contains a character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU or, for polled operation, the CPU can check the condition of RxRDY using a status read operation. RxEnable, when off, holds RxRDY in the reset condition.

For asynchronous mode, to set RxRDY, the receiver must be enabled to sense a start bit and a complete character must be assembled and transferred to the data output register.

For synchronous mode, to set RxRDY, the receiver must be enabled and a character must be enabled and a character must finish assembly and be transferred to the data output register.

Failure to read the received character from the Rx data output register prior to the assembly of the next Rx data character will set overrun condition error and the previous character will be written over and lost. If the Rx data is being read by the CPU when the internal transfer is occurring, the overrun will be set and the old character will be lost.

$\overline{RxC}$ - The Receiver Clock controls the rate at which the character is to be received. In synchronous mode the Baud Rate (1×) is equal to the actual frequency of $\overline{RxC}$. In asynchronous mode, the Baud Rate is a fraction of the actual $\overline{RxC}$ frequency. A portion of the mode instruction selects this factor :1/16 or 1/64 of the receiver clock.

For example: Baud Rate = 300 Baud, if
$\overline{RxC}$ = 300Hz in the 1× mode
$\overline{RxC}$ = 4.80kHz in the 16× mode
$\overline{RxC}$ = 19.2kHz in the 64× mode

Baud Rate = 2400 Baud, if
$\overline{RxC}$ = 240kHz in the 1× mode
$\overline{RxC}$ = 38.4kHz in the 16× mode
$\overline{RxC}$ = 153.6kHz in the 64× mode

Data is sampled into the MAS28151 on the rising edge of $\overline{RxC}$.

N.B.
In most communications systems, the MAS28151 will be handling both the transmission and reception of a single link. Consequently the receive and transmit Baud Rates will be the same. Both $\overline{TxC}$ and $\overline{RxC}$ will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

SYNDET/BRKDET - This pin is used in synchronous mode for SYNC Detect and may be used as either input or output, programmable through the control word. It is reset to output mode low on RESET. When used as an output (internal Sync mode), the SYNDET pin will go "high" to indicate that the MAS28151 has located a Sync character in the receive mode.

If the MAS28151 is programmed to use double Sync characters (bi-sync), then SYNDET will go "high" in the middle of the last bit of the second Sync character. SYNDET is automatically reset on a status Read operation.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

When used as an input (external Sync detect mode), positive going signal will cause the MAS28151 to start assembling data characters on the rising edge of the next $\overline{RxC}$. Once in Sync, the "high" input signal can be removed. When external Sync Detect is programmed, internal Sync Detect is disabled.

$\overline{RTS}$ - The Request to Send signal is a general purpose, 1-bit inverting output port. It can be set low by programming the appropriate bit in the Command instruction word. The $\overline{RTS}$ output signal is normally used for modem control such as Request to Send.

$\overline{CTS}$ - A low on the Clear to Send input enables the MAS28151 to transmit serial data if the TxEnable bit in the Command byte is set to high. If either a TxEnable off or $\overline{CTS}$ off condition occurs while Tx is in operation, the Tx will transmit all of the data in the USART, written prior to the Tx disable command, before shutting down.

Transmitter Buffer - The Transmitter Buffer accepts parallel data from the data bus buffer, converts it to serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin on the falling edge of TxC. The transmitter will begin transmission on being enabled if $\overline{CTS} = 0$. The TxD line will be held in the marking state immediately on a master Reset, or when TxEnable or $\overline{CTS} = 1$, or the transmitter is empty.

TxRDY - The Transmitter Ready output signals the CPU that the transmitter is ready to accept a data character. The TxRDY output pin can be used as an interrupt to the system since it is masked by TxEnable, or, for polled operation, the CPU can check TxRDY using a status Read operation. TxRDY is automatically reset by the falling edge of $\overline{DS}$ (with RD/$\overline{W}$ low) when a data character is loaded from the CPU. Note that when using the polled operation the TxRDY status bit is not masked by TxEnable, but will only indicate the Empty/Full Status of the Tx Data input register.

TxE - This is the Transmitter Empty output. When MAS28151 has no characters to send, the TxE output will go high. It resets on receiving a character from the CPU if the transmitter is enabled. TxE remains high when the transmitter is disabled. TxE can be used to indicate the end of transmission mode so that the CPU can turn the line around in half-duplex operational mode.

In the synchronous mode, a high on the TxE output indicates that a character has not been loaded and the SYNC character or characters are about to be or are being automatically transmitted as fillers. TxE does not go low when SYNC characters are being shifted out.

TxC - The transmitter clock controls the rate at which the character is to be transmitted. In the synchronous mode, the baud rate (1 x) is equal to the $\overline{TxC}$ frequency. In asynchronous transmission mode, the baud rate is a fraction of the actual $\overline{TxC}$ frequency. A portion of the mode instruction selects this factor. It can be 1, 1/16 or 1/64 the $\overline{TxC}$.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

For Example: If Baud Rate = 110 Baud,
$\overline{TxC}$ = 110Hz in 1 × mode
$\overline{TxC}$ = 1.72kHz in 16 × mode
$\overline{TxC}$ = 7.04kHz in 64 × mode

The falling edge of $\overline{TxC}$ shifts the serial data out of the MAS28151.

RxD - The receiver buffer accepts serial data, converts the data to parallel format, checks for bits or characters that are unique to the communications techniques and sends an assembled character to the CPU. Serial data is input to the RxD pin and is clocked in on the rising edge of $\overline{RxC}$.

FIGURE 3(d) - FUNCTIONAL DIAGRAM

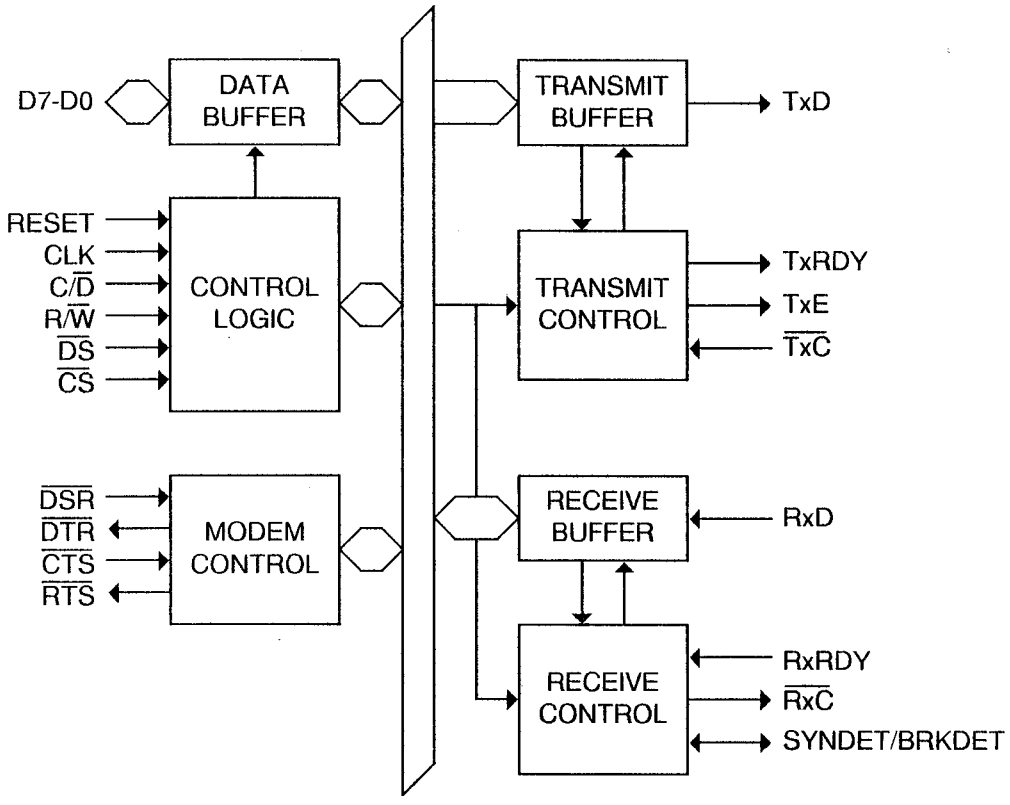
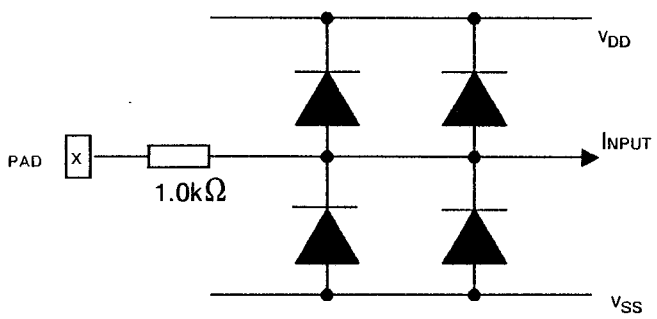


FIGURE 3(e) - INPUT PROTECTION NETWORK



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviation is used:-

V_{IC} - Input Clamp Voltage.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

(a) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during qualification and maintenance of qualification.

(b) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during procurement on a lot acceptance basis at the total dose irradiation level specified in the Purchase Order.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

(a) Para. 7.1.1(a), H.T.R.B.: Shall not be performed.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 4.61 grammes for the dual-in-line packages and 7.0 grammes for the flat package.

4.3.3 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESA/SCC Basic Specification No. 9000. The test conditions shall be as follows:-

Applied Force: 1.0 ± 0.1 Newtons, 3 bends at 45°.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body and the lids shall be pre-form soldered.

4.4.2 Lead Material and Finish

The material shall be Type 'D' with Type '2' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

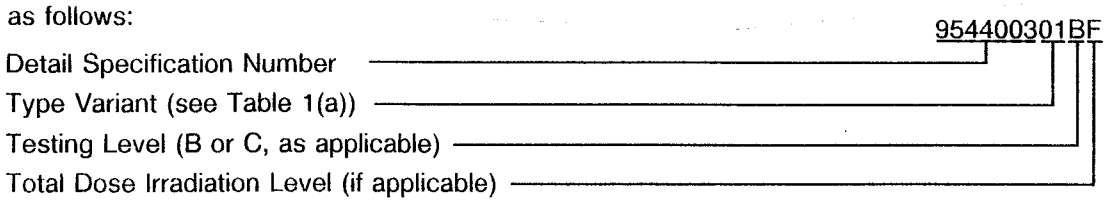
(c) Traceability Information.

4.5.2 Lead Identification

An index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



The Total Dose Irradiation Level designation shall be added for those devices for which a sample has been successfully tested to the level in question. For these devices, a code shall be added in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ °C and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +25 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for H.T.R.B. Burn-in

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for Power Burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for Power Burn-in shall be as specified in Table 5 of this specification.

4.7.4 Electrical Circuits for H.T.R.B. Burn-in

Not applicable.

4.7.5 Electrical Circuits for Power Burn-in

A circuit for use in performing the Power Burn-in test is shown in Figure 5 of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
1 to 6	Functional Test 1	-	3014	-	Verify Device Operation without Load V_{IL} = 0V, V_{IH} = 5.0V V_{OL} = V_{OH} = 1.5V V_{DD} = 5.0V, V_{SS} = 0V f_{CLK} = 600kHz, Patterns fp5101, fp5102, fp5103, fp5104, fp5105, fp5106	-	-	-
7 to 12	Functional Test 2	-	3014	-	Verify Device Operation without Load V_{IL} = 0.4V, V_{IH} = 3.0V V_{OL} = V_{OH} = 1.5V V_{DD} = 5.5V, V_{SS} = 0V f_{CLK} = 600kHz, Patterns fp5101, fp5102, fp5103, fp5104, fp5105, fp5106	-	-	-
13 to 18	Functional Test 3	-	3014	-	Verify Device Operation without Load V_{IL} = 0.4V, V_{IH} = 3.0V V_{OL} = V_{OH} = 1.5V V_{DD} = 4.5V, V_{SS} = 0V f_{CLK} = 600kHz, Patterns fp5101, fp5102, fp5103, fp5104, fp5105, fp5106	-	-	-
19 to 24	Functional Test 4	-	3014	-	Verify Device Operation without Load V_{IL} = 0.4V, V_{IH} = 5.0V V_{OL} = V_{OH} = 1.5V V_{DD} = 5.5V, V_{SS} = 0V f_{CLK} = 1.9MHz Patterns fp5102, fp5103 f_{CLK} = 6.25MHz Patterns fp5102, fp5106 f_{CLK} = 16.6MHz Patterns fp5102, fp5103	-	-	-
25	Quiescent Current	I_{DD}	3005	4(a)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V All Outputs Open Note 1 (Pin D 26) (Pin F 63)	-	2.0	mA

NOTES: See Page 34.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
26 to 36	Input Current Low Level	I_{IL}	3009	4(b)	V_{IN} (Under Test) = 0V V_{IN}(Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 3-9-10-11-12-13-17-20-21-22-25) (Pins F 5-20-22-24-29-31-39-48-50-52-58)	-	-1.0	µA
37 to 47	Input Current High Level	I_{IH}	3010	4(c)	V_{IN}(Under Test) = 5.5V V_{IN}(Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 3-9-10-11-12-13-17-20-21-22-25) (Pins F 5-20-22-24-29-31-39-48-50-52-58)	-	1.0	µA
48 to 62	Output Voltage Low Level	V_{OL}	3007	4(d)	V_{IL} = 0.4V, V_{IH} = 3.0V I_{OL} = 5.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 2 (Pins D 1-2-6-7-8-14-15-16-18-19-23-24-27-28) (Pins F 1-3-12-14-16-18-33-35-37-41-46-54-56-65-67)	-	0.4	V
63 to 77	Output Voltage High Level	V_{OH}	3006	4(e)	V_{IL} = 0.4V, V_{IH} = 3.0V I_{OH} = -2.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 2 (Pins D 1-2-6-7-8-14-15-16-18-19-23-24-27-28) (Pins F 1-3-12-14-16-18-33-35-37-41-46-54-56-65-67)	2.4	-	V
78 to 97	Threshold Voltage N-Channel	V_{THN}	-	4(f)	V_{IN} = Note 3 V_{DD} = 5.5V, V_{SS} = 0V (Pins D 1-2-3-5-6-7-8-9-10-11-12-13-16-17-21-22-25-27-28) (Pins F 1-3-5-12-14-16-18-20-22-24-29-31-37-39-48-50-52-58-65-67)	0.8	-	V

NOTES: See Page 34.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
98 to 117	Threshold Voltage P-Channel	V_{THP}	-	4(f)	V_{IN} = Note 3 V_{DD} = 5.5V, V_{SS} = 0V (Pins D 1-2-3-5-6-7-8-9-10-11-12-13-16-17-21-22-25-27-28) (Pins F 1-3-5-12-14-16-18-20-22-24-29-31-37-39-48-50-52-58-65-67)	-	2.0	V
118 to 135	Input Clamp Voltage (to V_{SS})	V_{IC1}	-	4(g)	I_{IN}(Under Test) = -100µA V_{DD} = Open, V_{SS} = 0V All Other Pins Open (Pins D 1-2-3-5-6-7-8-9-10-11-12-13-16-17-20-21-22-25-27-28) (Pins F 1-3-5-12-14-16-18-20-22-24-29-31-37-39-48-50-52-58-65-67)	-0.1	-6.0	V
136 to 153	Input Clamp Voltage (to V_{DD})	V_{IC2}	-	4(g)	I_{IN}(Under Test) = 100µA V_{DD} = 0V, V_{SS} = Open All Other Pins Open (Pins D 1-2-3-5-6-7-8-9-10-11-12-13-16-17-20-21-22-25-27-28) (Pins F 1-3-5-12-14-16-18-20-22-24-29-31-37-39-48-50-52-58-65-67)	0.1	6.0	V
154 to 162	Output Leakage Current Third-State (Low Level Applied)	I_{OZL}	-	4(h)	V_{IN}(3-State Controls) = Note 4 V_{OUT} = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 1-2-5-6-7-8-16-27-28) (Pins F 1-3-12-14-16-18-37-65-67)	-	-10	µA
163 to 171	Output Leakage Current Third-State (High Level Applied)	I_{OZH}	-	4(h)	V_{IN}(3-State Controls) = Note 4 V_{OUT} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 1-2-5-6-7-8-16-27-28) (Pins F 1-3-12-14-16-18-37-65-67)	-	10	µA

NOTES: See Page 34.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
172 to 182	Input Capacitance	C_{IN}	3012	4(i)	V_{IN}(Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 5 (Pins D 3-9-10-11-12-13-17-20-21-22-25) (Pins F 5-20-22-24-29-31-39-48-50-52-58)	-	10	pF
183 to 191	Input/Output Capacitance	C_{IN}/O_{UT}	3012	4(i)	V_{IN}(Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 5 (Pins D 1-2-5-6-7-8-16-27-28) (Pins F 1-3-12-14-16-18-37-65-67)	-	10	pF
193 to 204	Functional Test 5	-	-	-	Verify Device Operation without Load $V_{IL} = 0V, V_{ih} = 4.0V$ $V_{OL} = V_{OH} = 1.5V$ $V_{DD} = 4.5V$ and 5.5V, $V_{SS} = 0V$ $f_{CLK} = 600kHz$, Patterns fp5101, fp5102, fp5103, fp5104, fp5105, fp5106	-	-	-
205 to 207	CLK Rise and Fall Time	tr/tf	3004	-	$f_{CLK} = 1.9MHz$ $f_{CLK} = 6.25MHz$ $f_{CLK} = 16.6MHz$ Note 5	-	10	ns
208 to 209	TxRDY Fall from Leading-Edge of $\overline{W}$	$t_{TxRDY\ CLEAR}$	3003	4(j)	$V_{DD} = 4.5V$ and 5.5V, $V_{SS} = 0V$ Notes 6 and 7	-	400	ns
210 to 211	RxRDY Fall from Leading-Edge of RD	$t_{RxRDY\ CLEAR}$	3003	4(j)	$V_{DD} = 4.5V$ and 5.5V, $V_{SS} = 0V$ Notes 6 and 7	-	400	ns
212 to 213	$\overline{DS}$ Pulse Width	t_{RR}	3003	4(j)	$V_{DD} = 4.5V$ and 5.5V, $V_{SS} = 0V$ Notes 6 and 7	50	-	ns
214 to 215	Data Delay from $\overline{DS}$ (Read)	t_{RD}	3003	4(j)	$V_{DD} = 4.5V$ and 5.5V, $V_{SS} = 0V$ Notes 6, 7 and 8	-	200	ns

NOTES: See Page 34.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
216 to 217	$\overline{DS}$ Data Floating (Read)	t_{DF}	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 6, 7 and 8	10	100	ns
218 to 219	Clock Period	t_{cy}	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 6, 9, 10 and 11	200	1000	ns
220 to 221	Clock High Pulse Width	t_o	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 6 and 9	120	t_{cy}-90	ns
222 to 223	Clock Low Pulse Width	t_1	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 6 and 9	120	-	ns
224 to 225	TxD Delay from Falling-Edge of TxD	t_{DTY}	3003	4(j)	V_{DD} = 4.5V and 5.5V, V_{SS} = 0V Notes 6 and 9	-	1.0	µs
226 to 231	Transmitter Input Clock Frequency	f_{TX}	3003	4(i)	1× Baud Rate 16× Baud Rate 64× Baud Rate V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 6 and 9	- - -	64 310 615	kHz
232 to 237	Transmitter Input Clock Pulse Width	f_{PW}	3003	4(i)	1× Baud Rate 16× and 64× Baud Rate V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 6 and 9	$12 \times t_{cy}$ $1 \times t_{cy}$	- -	ns
238 to 243	Transmitter Input Clock Pulse Delay	f_{PD}	3003	4(i)	1× Baud Rate 16× and 64× Baud Rate V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 6 and 9	$15 \times t_{cy}$ $3 \times t_{cy}$	- -	ns
244 to 249	Receiver Input Clock Frequency	f_{RX}	3003	4(i)	1× Baud Rate 16× Baud Rate 64× Baud Rate V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 6 and 9	- - -	64 310 615	kHz

NOTES: See Page 34.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
250 to 255	Receiver Input Clock Pulse	t_{RPW}	3003	4(i)	1× Baud Rate 16× and 64× Baud Rate V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 6 and 9	$12 \times t_{cy}$ $1 \times t_{cy}$	- -	ns
256 to 261	Receiver Input Clock Pulse	t_{RPD}	3003	4(i)	1× Baud Rate 16× and 64× Baud Rate V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 6 and 9	$15 \times t_{cy}$ $3 \times t_{cy}$	- -	ns
262 to 263	TxRDY Pin Delay from Centre of Last Bit	t_{TxRDY}	3003	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 6 and 9	-	$8 \times t_{cy}$	ns
264 to 265	RxRDY Pin Delay from Centre of Last Bit	t_{RxRDY}	3003	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 6 and 9	-	$26 \times t_{cy}$	ns
266 to 267	TxEMPTY from Centre of Last Bit	$t_{TxEMPTY}$	3003	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 6 and 9	$20 \times t_{cy}$	-	ns
268 to 269	Control Delay from Rising-Edge of Write	t_{WC}	3003	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 6 and 9	$8 \times t_{cy}$	-	ns
270 to 271	Control READ Setup Time ($\overline{RTS}$, $\overline{CTS}$)	t_{CR}	3003	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 6 and 9	$20 \times t_{cy}$	-	ns
272 to 273	Address Stable before $\overline{DS}$ ($\overline{CS}$, C/$\overline{D}$)	t_{AR}	3003	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 6, 9 and 12	0	-	ns
274 to 275	Address Hold Time before $\overline{DS}$ ($\overline{CS}$, C/$\overline{D}$)	t_{RA}	3003	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 6, 9 and 12	0	-	ns
276 to 277	Data Setup Time $\overline{DS}$ (WRITE)	t_{DW}	3003	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 6 and 9	150	-	ns
278 to 279	Data Hold Time $\overline{DS}$ (WRITE)	t_{WD}	3003	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 6, 7 and 9	20	-	ns
280 to 281	Recovery Time between Writes	trv	3003	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 6, 7 and 9	$5 \times t_{cy}$	-	ns

NOTES: See Page 34.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE (CONT'D)

NOTES

1. Measurement is performed with the device having been initialised using functional test pattern fp5102.
2. The output pin under test is configured into the correct state for the measurement by using a functional test pattern on the inputs which produces a low or high level at the pin, as appropriate.
3. V_{IN} is applied to the pin under test and is varied until a change in output state occurs. The measured value is V_{TH}.
4. The device is configured using a functional test pattern so that the pin under test is in the third-state condition for the measurement. The measurements include the input currents (I_{IL} and I_{IH}).
5. Guaranteed but not tested. Characterised at initial design and after major process changes.
6. $V_{IL} = 0V$, $V_{IH} = 4.0V$.

   $f_{CLK} = 600kHz$, Patterns fp5101, fp5102, fp5103, fp5104, fp5105, fp5106.
7. Parameter measured during Functional Test 5.
8. 3-State timings measured by a 1.0V change in output voltage with an additional 680Ω load to V_{SS} or V_{DD}.
9. Parameter tested go-no-go during Functional Test 5.
10. The TxC and RxC frequencies have the following limitations with respect to clock:
    - For 1× Baud Rate, f_{TX} or $f_{RX} \leq 1/(30t_{cy})$.
    - For 16× and 64× Baud Rate, f_{TX} or $f_{RX} \leq 1/(4.5t_{cy})$.
11. Reset Pulse Width = $6xt_{cy}$ minimum. The system clock must be running during Reset.
12. $\overline{CS}$ and Command/Data are considered as addresses.
13. Guaranteed but not tested at −55°C.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
1 to 6	Functional Test 1	-	3014	-	Verify Device Operation without Load V_{IL} = 0V, V_{IH} = 5.0V V_{OL} = V_{OH} = 1.5V V_{DD} = 5.0V, V_{SS} = 0V f_{CLK} = 600kHz, Patterns fp5101, fp5102, fp5103, fp5104, fp5105, fp5106	-	-	-
7 to 12	Functional Test 2	-	3014	-	Verify Device Operation without Load V_{IL} = 0.4V, V_{IH} = 3.0V V_{OL} = V_{OH} = 1.5V V_{DD} = 5.5V, V_{SS} = 0V f_{CLK} = 600kHz, Patterns fp5101, fp5102, fp5103, fp5104, fp5105, fp5106	-	-	-
13 to 18	Functional Test 3	-	3014	-	Verify Device Operation without Load V_{IL} = 0.4V, V_{IH} = 3.0V V_{OL} = V_{OH} = 1.5V V_{DD} = 4.5V, V_{SS} = 0V f_{CLK} = 600kHz, Patterns fp5101, fp5102, fp5103, fp5104, fp5105, fp5106	-	-	-
19 to 24	Functional Test 4	-	3014	-	Verify Device Operation without Load V_{IL} = 0.4V, V_{IH} = 5.0V V_{OL} = V_{OH} = 1.5V V_{DD} = 5.5V, V_{SS} = 0V f_{CLK} = 1.9MHz Patterns fp5102, fp5103 f_{CLK} = 6.25MHz Patterns fp5102, fp5106 f_{CLK} = 16.6MHz Patterns fp5102, fp5103	-	-	-
25	Quiescent Current	I_{DD}	3005	4(a)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V All Outputs Open Note 1 (Pin D 26) (Pin F 63)	-	10	mA

NOTES: See Page 34.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
26 to 36	Input Current Low Level	I_{IL}	3009	4(b)	V_{IN} (Under Test) = 0V V_{IN}(Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V Note 13 (Pins D 3-9-10-11-12-13-17-20-21-22-25) (Pins F 5-20-22-24-29-31-39-48-50-52-58)	-	-10	µA
37 to 47	Input Current High Level	I_{IH}	3010	4(c)	V_{IN}(Under Test) = 5.5V V_{IN}(Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V Note 13 (Pins D 3-9-10-11-12-13-17-20-21-22-25) (Pins F 5-20-22-24-29-31-39-48-50-52-58)	-	10	µA
48 to 62	Output Voltage Low Level	V_{OL}	3007	4(d)	V_{IL} = 0.4V, V_{IH} = 3.0V I_{OL} = 5.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 2 (Pins D 1-2-6-7-8-14-15-16-18-19-23-24-27-28) (Pins F 1-3-12-14-16-18-33-35-37-41-46-54-56-65-67)	-	0.4	V
63 to 77	Output Voltage High Level	V_{OH}	3006	4(e)	V_{IL} = 0.4V, V_{IH} = 3.0V I_{OH} = -2.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 2 (Pins D 1-2-6-7-8-14-15-16-18-19-23-24-27-28) (Pins F 1-3-12-14-16-18-33-35-37-41-46-54-56-65-67)	2.4	-	V
78 to 97	Threshold Voltage N-Channel	V_{THN}	-	4(f)	V_{IN} = Note 3 V_{DD} = 5.5V, V_{SS} = 0V (Pins D 1-2-3-5-6-7-8-9-10-11-12-13-16-17-21-22-25-27-28) (Pins F 1-3-5-12-14-16-18-20-22-24-29-31-37-39-48-50-52-58-65-67)	0.8	-	V

NOTES: See Page 34.

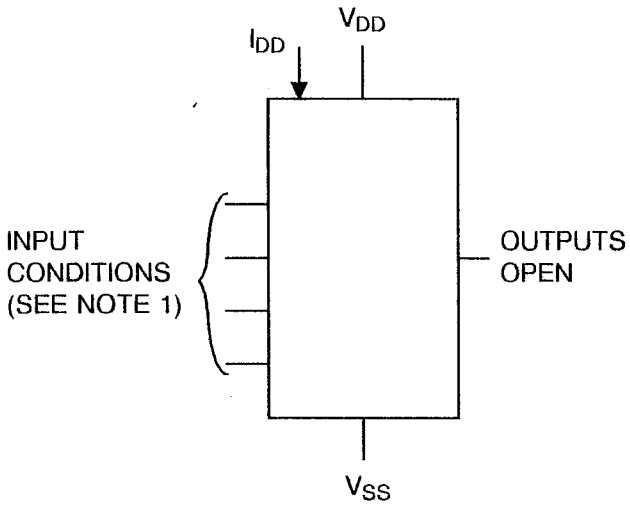
TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP, F = FP)	LIMITS		UNIT
						MIN	MAX	
98 to 117	Threshold Voltage P-Channel	V_{THP}	-	4(f)	V_{IN} = Note 3 V_{DD} = 5.5V, V_{SS} = 0V (Pins D 1-2-3-5-6-7-8-9-10-11-12-13-16-17-21-22-25-27-28) (Pins F 1-3-5-12-14-16-18-20-22-24-29-31-37-39-48-50-52-58-65-67)	-	2.0	V
118 to 135	Input Clamp Voltage (to V_{SS})	V_{IC1}	-	4(g)	I_{IN}(Under Test) = -100µA V_{DD} = Open, V_{SS} = 0V All Other Pins Open (Pins D 1-2-3-5-6-7-8-9-10-11-12-13-16-17-20-21-22-25-27-28) (Pins F 1-3-5-12-14-16-18-20-22-24-29-31-37-39-48-50-52-58-65-67)	-0.1	-6.0	V
136 to 153	Input Clamp Voltage (to V_{DD})	V_{IC2}	-	4(g)	I_{IN}(Under Test) = 100µA V_{DD} = 0V, V_{SS} = Open All Other Pins Open (Pins D 1-2-3-5-6-7-8-9-10-11-12-13-16-17-20-21-22-25-27-28) (Pins F 1-3-5-12-14-16-18-20-22-24-29-31-37-39-48-50-52-58-65-67)	0.1	6.0	V
154 to 162	Output Leakage Current Third-State (Low Level Applied)	I_{OZL}	-	4(h)	V_{IN}(3-State Controls) = Notes 4 and 13 V_{OUT} = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 1-2-5-6-7-8-16-27-28) (Pins F 1-3-12-14-16-18-37-65-67)	-	-50	µA
163 to 171	Output Leakage Current Third-State (High Level Applied)	I_{OZH}	-	4(h)	V_{IN}(3-State Controls) = Notes 4 and 13 V_{OUT} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 1-2-5-6-7-8-16-27-28) (Pins F 1-3-12-14-16-18-37-65-67)	-	50	µA

NOTES: See Page 34.

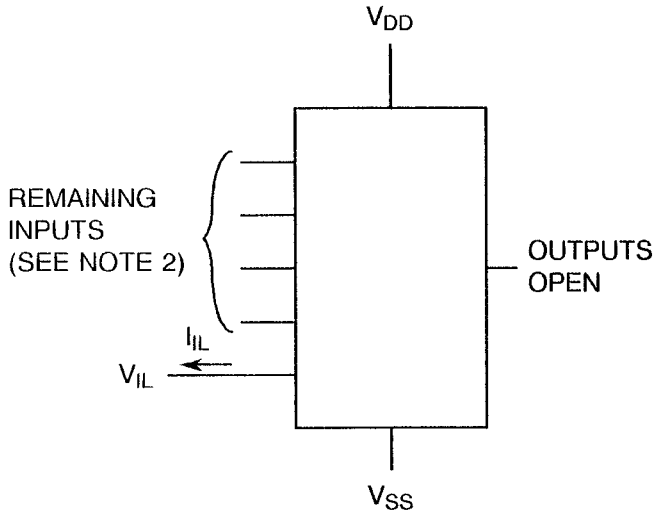
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - QUIESCENT CURRENT



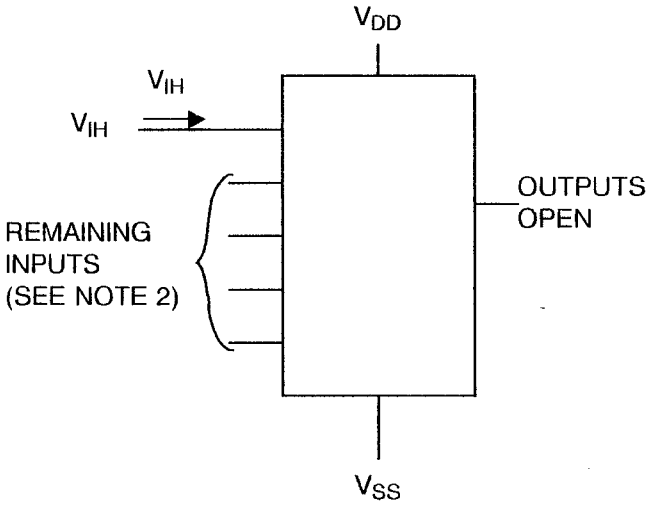
NOTES
1. Input conditions as per Table 2.

FIGURE 4(b) - INPUT CURRENT LOW LEVEL



NOTES
1. Each input to be tested separately.
2. Input conditions as per Table 2.

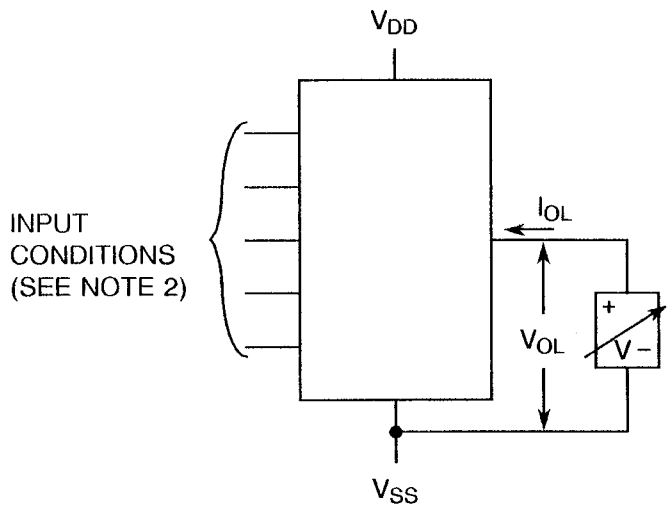
FIGURE 4(c) - INPUT CURRENT HIGH LEVEL



NOTES
1. Each input to be tested separately.
2. Input conditions as per Table 2.

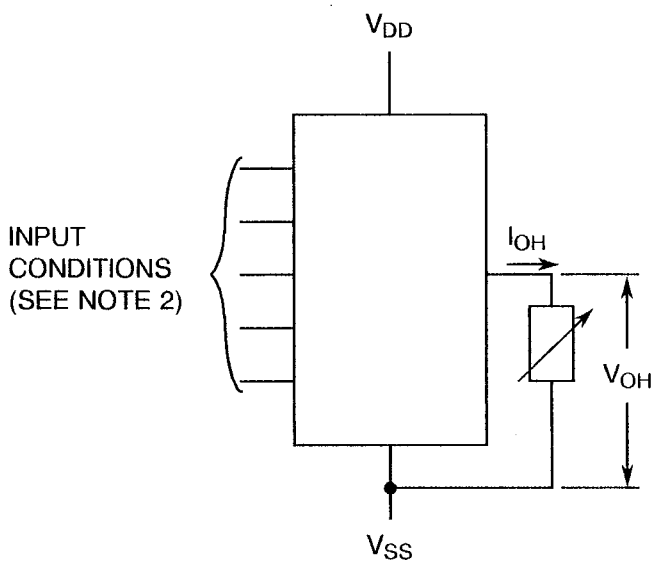
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(d) - OUTPUT VOLTAGE LOW LEVEL



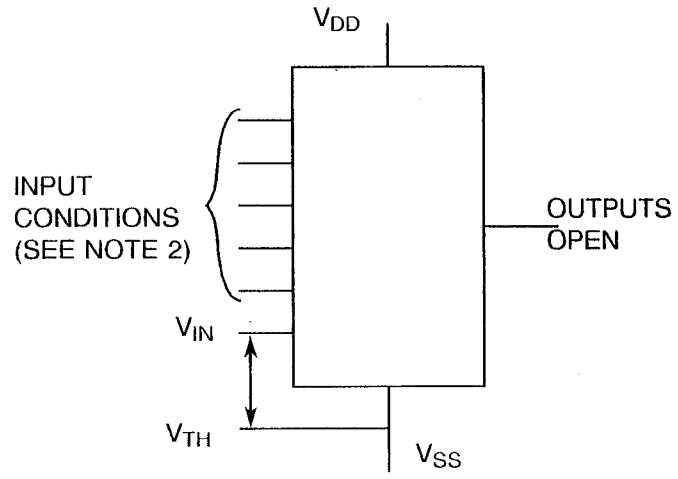
NOTES
1. Each output to be tested separately.
2. Input conditions as per Table 2.

FIGURE 4(e) - OUTPUT VOLTAGE HIGH LEVEL



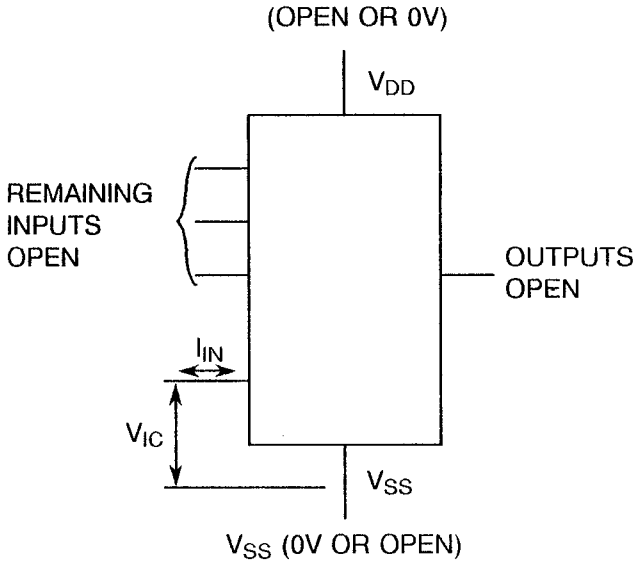
NOTES
1. Each output to be tested separately.
2. Input conditions as per Table 2.

FIGURE 4(f) - THRESHOLD VOLTAGE



NOTES
1. Each input to be tested separately.
2. Input conditions as per Table 2.

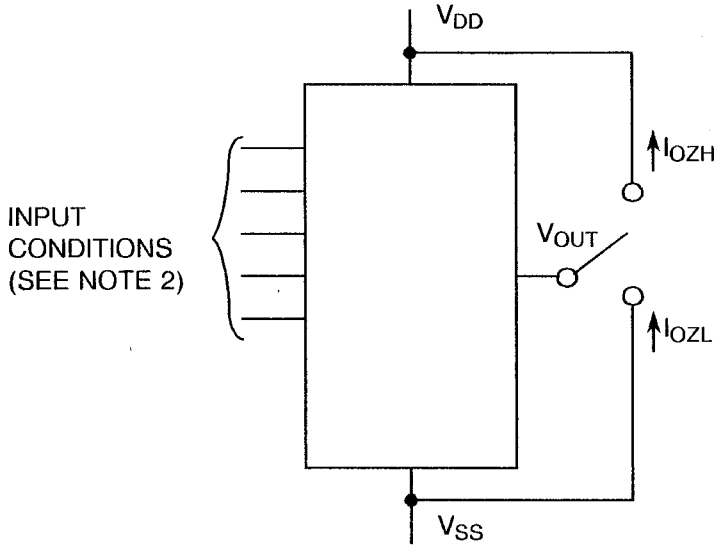
FIGURE 4(g) - INPUT CLAMP VOLTAGE



NOTES
1. Each input to be tested separately.

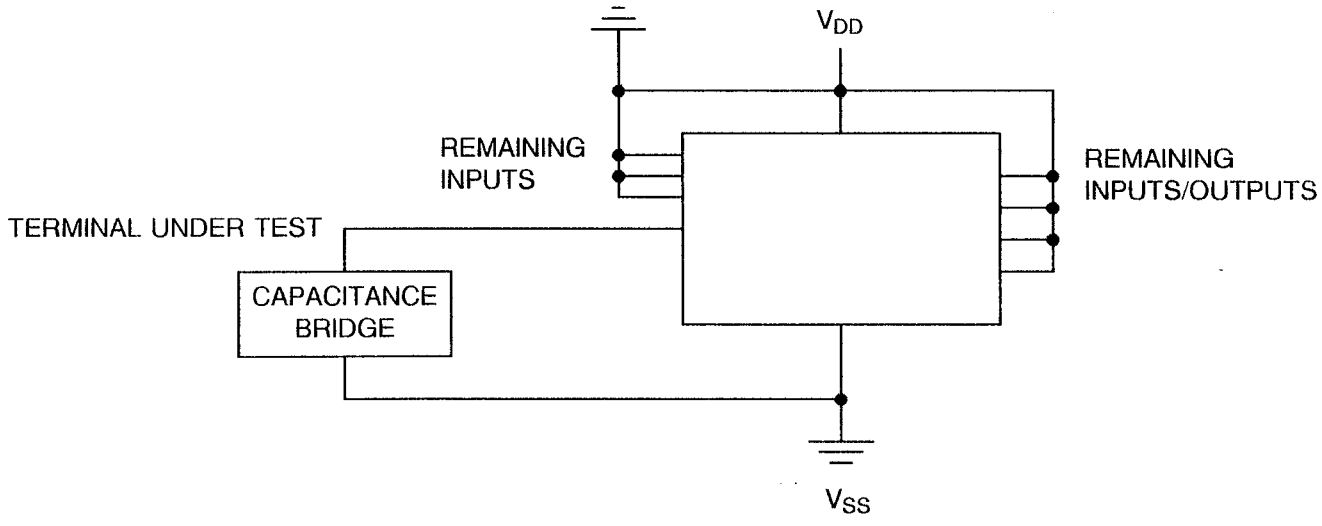
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(h) - OUTPUT LEAKAGE CURRENT THIRD STATE



NOTES
1. Each output to be tested separately.
2. Input conditions as per Table 2.

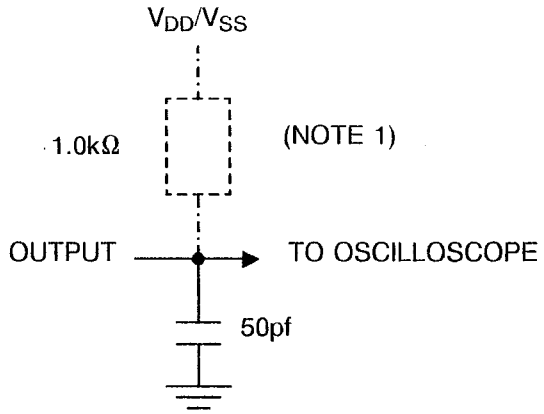
FIGURE 4(i) - INPUT AND INPUT/OUTPUT CAPACITANCE



NOTES
1. Test frequency = 1.0MHz.
2. Each input and input/output is to be tested separately.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(j) - PROPAGATION DELAY



NOTES

1. For high impedance timing measurements only.
2. Voltage waveforms as per Figure 3(b).

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
25	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	±500	µA
26 to 36	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	±250	nA
37 to 47	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	±250	nA
48 to 62	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	±100	mV
63 to 77	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	±240	mV
154 to 162	Output Leakage Current (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	±4.0	µA
163 to 174	Output Leakage Current (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	±4.0	µA

TABLE 5 - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0−5)	°C
2	Outputs - (Pins D 14-18-19) - (Pins F 33-41-46)	V_{OUT}	V_{DD}	V
3	Outputs - (Pins D 15-23-24) - (Pins F 35-54-56)	V_{OUT}	V_{SS}	V
4	Inputs - (Pins D 3-22-25) - (Pins F 5-52-58)	V_{IN}	V_{DD}	V
5	Inputs - (Pins D 10-11-17) - (Pins F 22-24-39)	V_{IN}	V_{SS}	V
6	Inputs/Outputs - (Pins D 1-2-8-16-27) - (Pins F 1-3-18-37-65)	$V_{IN/OUT}$	V_{DD}	V
7	Inputs/Outputs - (Pins D 5-6-7-28) - (Pins F 12-14-16-67)	$V_{IN/OUT}$	V_{SS}	V
8	Input - (Pin D 9) - (Pin F 20)	V_{IN}	V_{GEN1}	Vac
9	Input - (Pin D 20) - (Pin F 48)	V_{IN}	V_{GEN2}	Vac
10	Input - (Pin D 13) - (Pin F 31)	V_{IN}	V_{GEN3}	Vac
11	Input - (Pin D 21) - (Pin F 50)	V_{IN}	V_{GEN4}	Vac
12	Input - (Pin D 12) - (Pin F 29)	V_{IN}	V_{GEN5}	Vac
13	Pulse Voltage	V_{GEN}	0V to V_{DD}	Vac
14	Pulse Frequency Square Wave	f_{GEN1} f_{GEN2} f_{GEN3}	31.25k 4.0M 125k 50% Duty Cycle	Hz
15	Pulse Square Wave	GEN4 GEN5	One 8.0µs positive pulse each 256µs One 64µs positive pulse each 256µs	Vac
16	Positive Supply Voltage (Pin D 26) (Pin F 63)	V_{DD}	5.5(+0−0.5)	V
17	Negative Supply Voltage (Pin D 4) (Pin F 7)	V_{SS}	0	V

NOTES: See Page 44.

TABLE 5 - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS (CONT'D)

NOTES

1. V_{GEN3}

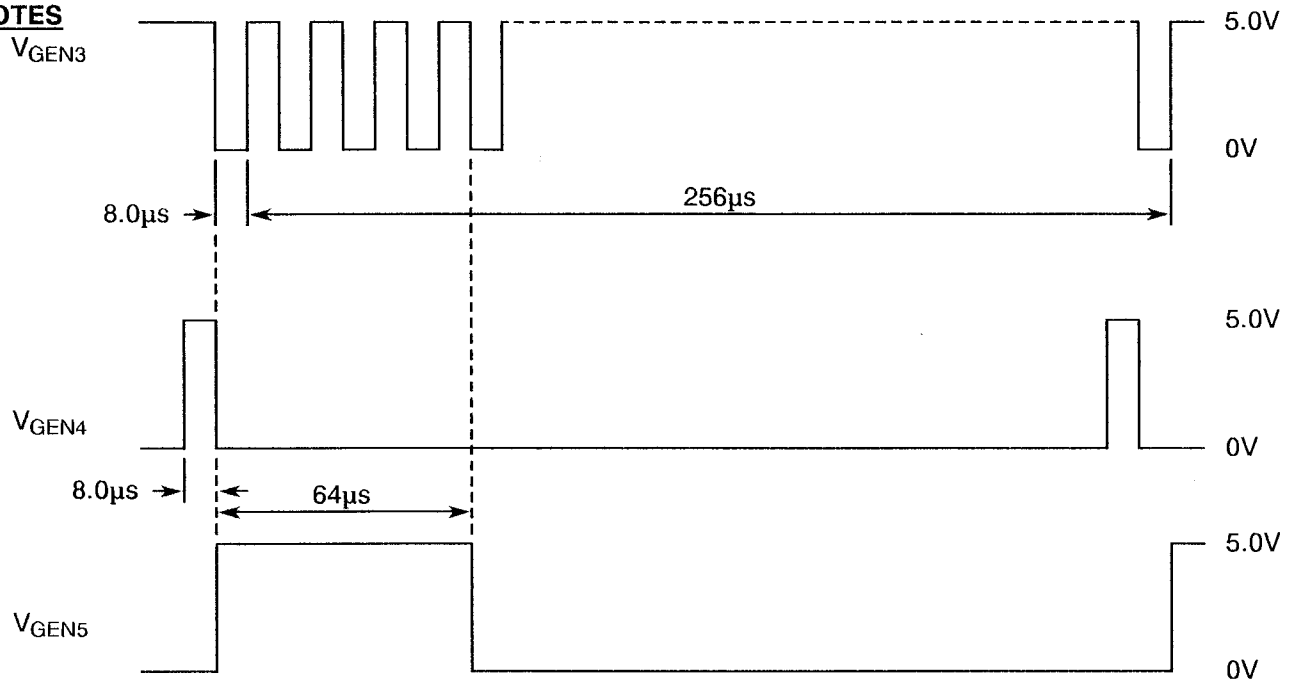
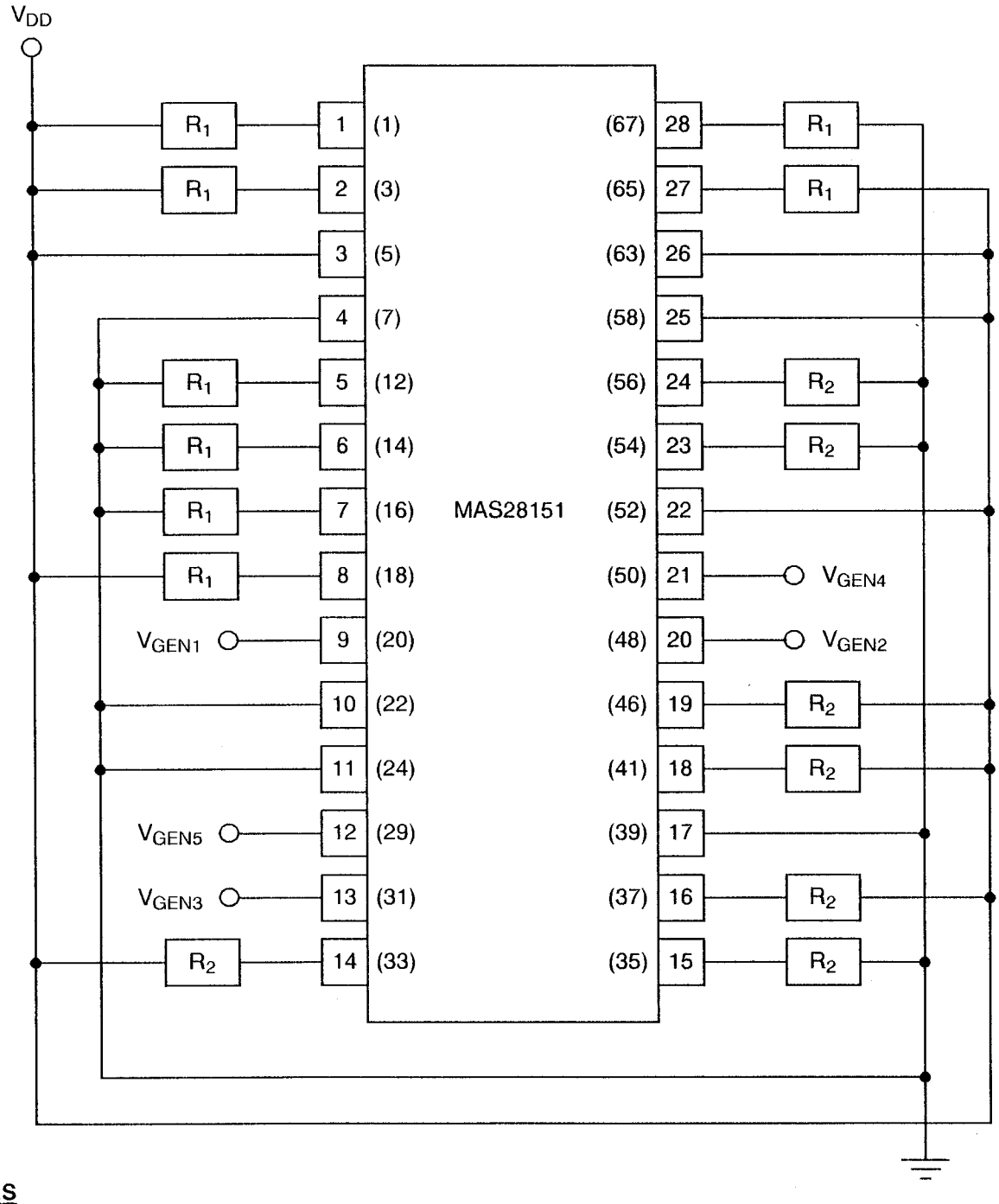


FIGURE 5 - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



NOTES

1. Pin numbers in parenthesis are for the flat package.
2. $R_1 = 1.0k\Omega$, $R_2 = 10k\Omega$.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5 of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5 of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

4.9 TOTAL DOSE IRRADIATION TESTING

4.9.1 Application

If specified in Para. 4.2.1 of this specification, total dose irradiation testing shall be performed in accordance with the requirements of ESA/SCC basic Specification No. 22900.

4.9.2 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6.

4.9.3 Electrical Measurements

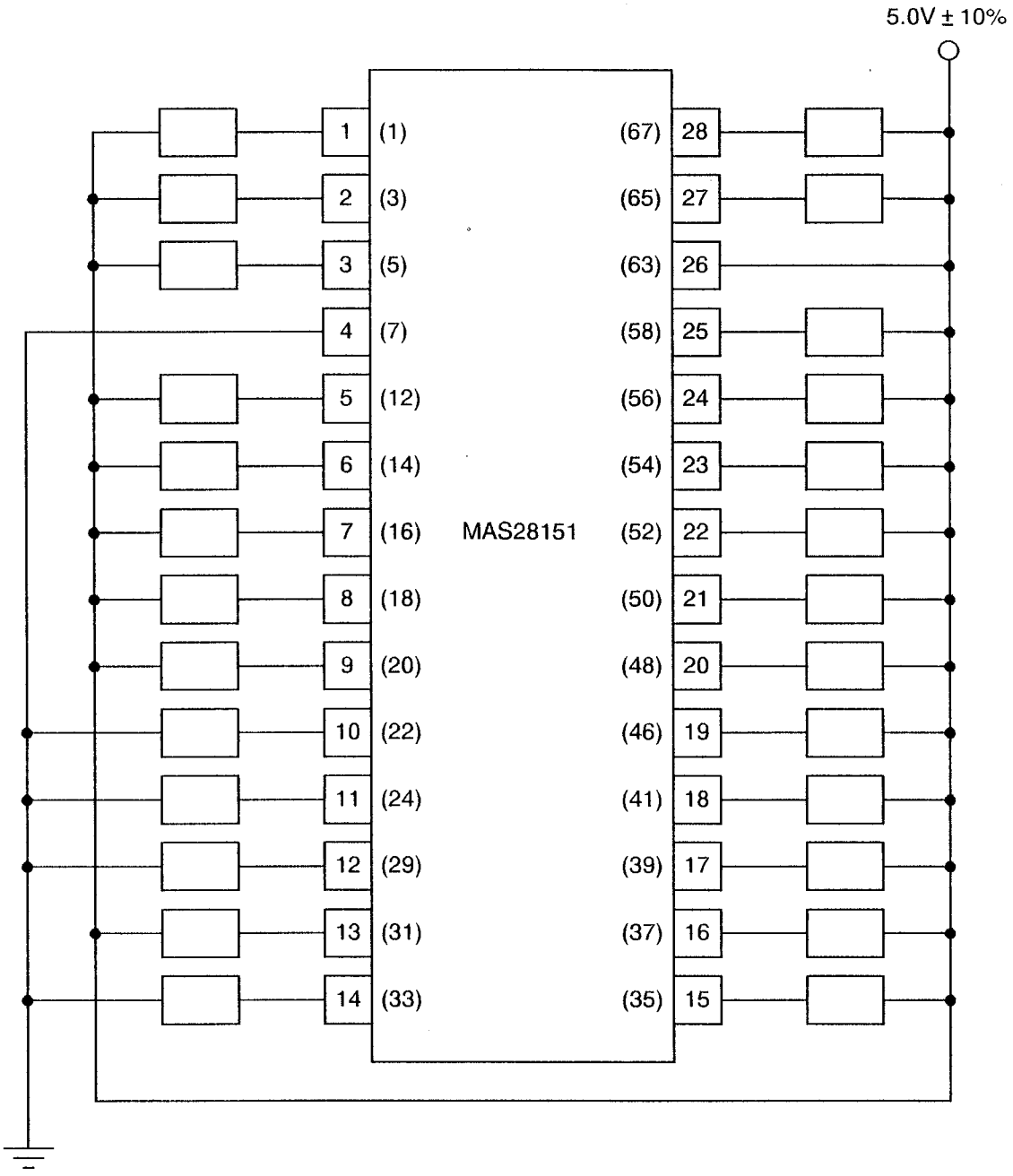
The parameters to be measured prior to irradiation exposure are scheduled in Table 2 of the specification. Only devices which meet the requirements of Table 2 shall be scheduled in the test sample.

The parameters to be measured during and on completion of irradiation testing are scheduled in Table 7 of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1 to 6	Functional Test 1	-	As per Table 2	As per Table 2	-	-	-
7 to 12	Functional Test 2	-	As per Table 2	As per Table 2	-	-	-
13 to 18	Functional Test 3	-	As per Table 2	As per Table 2	-	-	-
19 to 24	Functional Test 4	-	As per Table 2	As per Table 2	-	-	-
25	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	-	2.0	mA
26 to 36	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	-	-1.0	µA
37 to 47	Input Curent High Level	I_{IH}	As per Table 2	As per Table 2	-	1.0	µA
48 to 62	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	–	0.4	V
63 to 77	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	2.4	-	V
78 to 97	Threshold Voltage N-Channel	V_{THN}	As per Table 2	As per Table 2	0.8	-	V
98 to 117	Threshold Voltage P-Channel	V_{THP}	As per Table 2	As per Table 2	–	2.0	V
118 to 135	Input Clamp Voltage (to V_{SS})	V_{IC1}	As per Table 2	As per Table 2	-0.1	-6.0	V
136 to 153	Input Clamp Voltage to (V_{DD})	V_{IC2}	As per Table 2	As per Table 2	0.1	6.0	V
154 to 162	Output Leakage Current Third-State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	-	-10	µA
163 to 171	Output Leakage Current Third-State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	-	10	µA

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING



NOTES

1. Pin numbers in parenthesis are for the flat package.
2. Protection resistor = 10kΩ.

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1 to 6	Functional Test 1	-	As per Table 2	As per Table 2	-	-	-
25	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	-	10	mA
26 to 36	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	-	-10	µA
37 to 47	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	-	10	µA
48 to 62	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	–	0.4	V
63 to 77	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	2.4	-	V
78 to 97	Threshold Voltage N-Channel	V_{THN}	As per Table 2	As per Table 2	0.8	-	V
98 to 117	Threshold Voltage P-Channel	V_{THP}	As per Table 2	As per Table 2	–	2.0	V
154 to 162	Output Leakage Current Third-State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	-	-50	µA
163 to 171	Output Leakage Current Third-State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	-	50	µA

APPENDIX 'A'

AGREED DEVIATIONS FOR GPS (G.B.)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.3	Two additional optional tests may be performed: Static Burn-ins 1 and 2, as specified below. Each burn-in shall be 24 hours and Table 4 Parameter Drift Values shall be applied at 0 and 24 hours and 24 and 48 hours. If these tests are performed, they shall be recorded and counted for PDA.

APPENDIX 'A'

CONDITIONS FOR STATIC BURN-IN 1

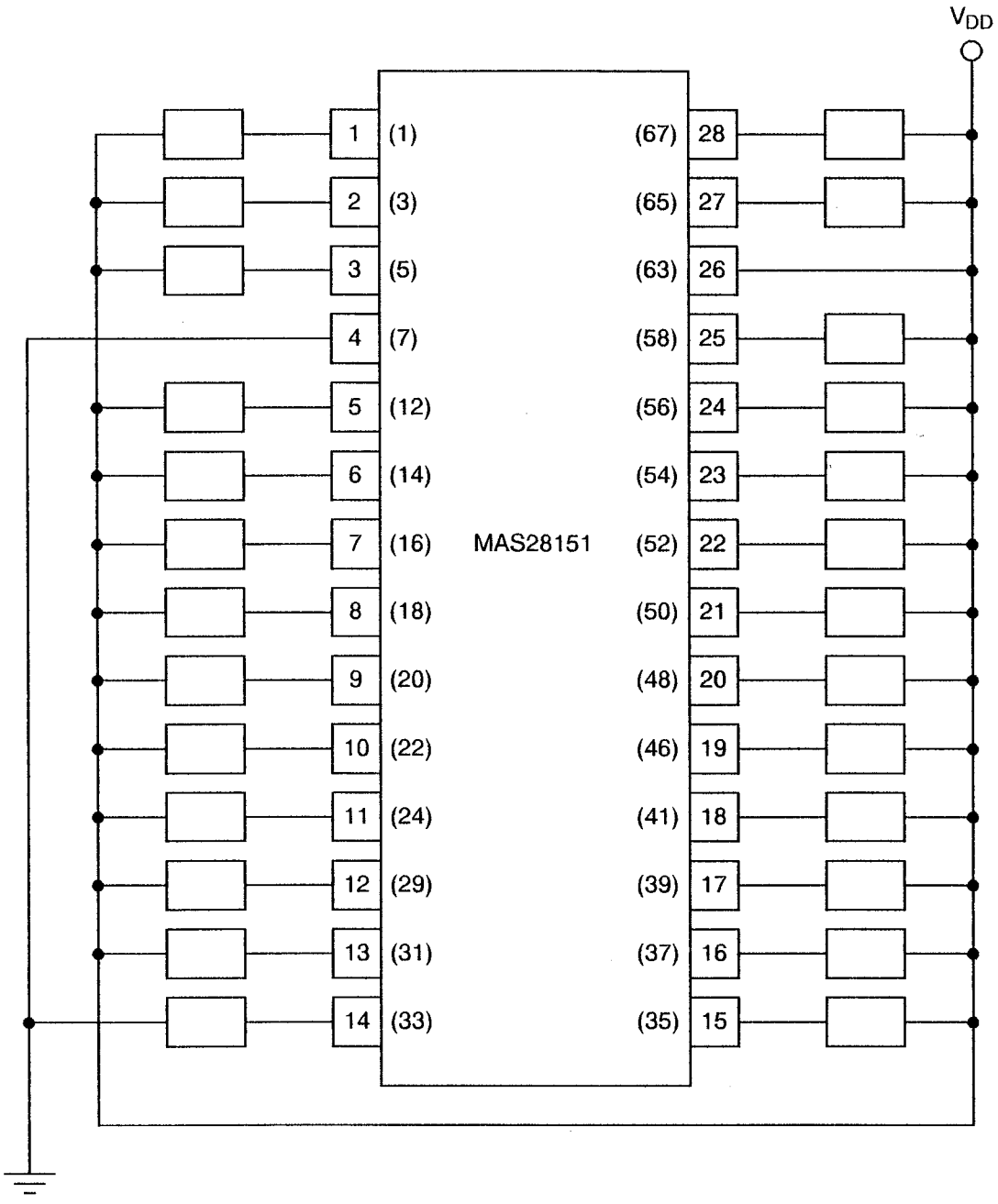
No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0−5)	°C
2	Output - (Pin D 14) - (Pin F 33)	V_{OUT}	V_{SS}	V
3	Outputs - (Pins D 15-18-19-23-24) - (Pins F 35-41-46-54-56)	V_{OUT}	V_{DD}	V
4	Inputs - (Pins D 3-10-11-17-22-25) - (Pins F 5-22-24-39-52-58)	V_{IN}	V_{DD}	V
5	Inputs/Outputs - (Pins D 1-2-5-6-7-8-16-27-28) - (Pins F 1-3-12-14-16-18-37-65-67)	$V_{IN/OUT}$	V_{DD}	V
6	Inputs - (Pins D 9-12-13-20-21) - (Pins F 20-29-31-48-50)	V_{IN}	V_{DD}	V
7	Positive Supply Voltage (Pin D 26) (Pin F 63)	V_{DD}	5.5(+0−0.5)	V
8	Negative Supply Voltage (Pin D 4) (Pin F 7)	V_{SS}	0	V

CONDITIONS FOR STATIC BURN-IN 2

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0−5)	°C
2	Output - (Pin D 15) - (Pin F 35)	V_{OUT}	V_{DD}	V
3	Outputs - (Pins D 14-18-19-23-24) - (Pins F 33-41-46-54-56)	V_{OUT}	V_{SS}	V
4	Inputs - (Pins D 3-10-11-17-22-25) - (Pins F 5-22-24-39-52-58)	V_{IN}	V_{SS}	V
5	Inputs/Outputs - (Pins D 1-2-5-6-7-8-16-27-28) - (Pins F 1-3-12-14-16-18-37-65-67)	$V_{IN/OUT}$	V_{SS}	V
6	Inputs - (Pins D 9-12-13-20-21) - (Pins F 20-29-31-48-50)	V_{IN}	V_{SS}	V
7	Positive Supply Voltage (Pin D 26) (Pin F 63)	V_{DD}	5.5(+0−0.5)	V
8	Negative Supply Voltage (Pin D 4) (Pin F 7)	V_{SS}	0	V

APPENDIX 'A'

ELECTRICAL CIRCUIT FOR STATIC BURN-IN 1

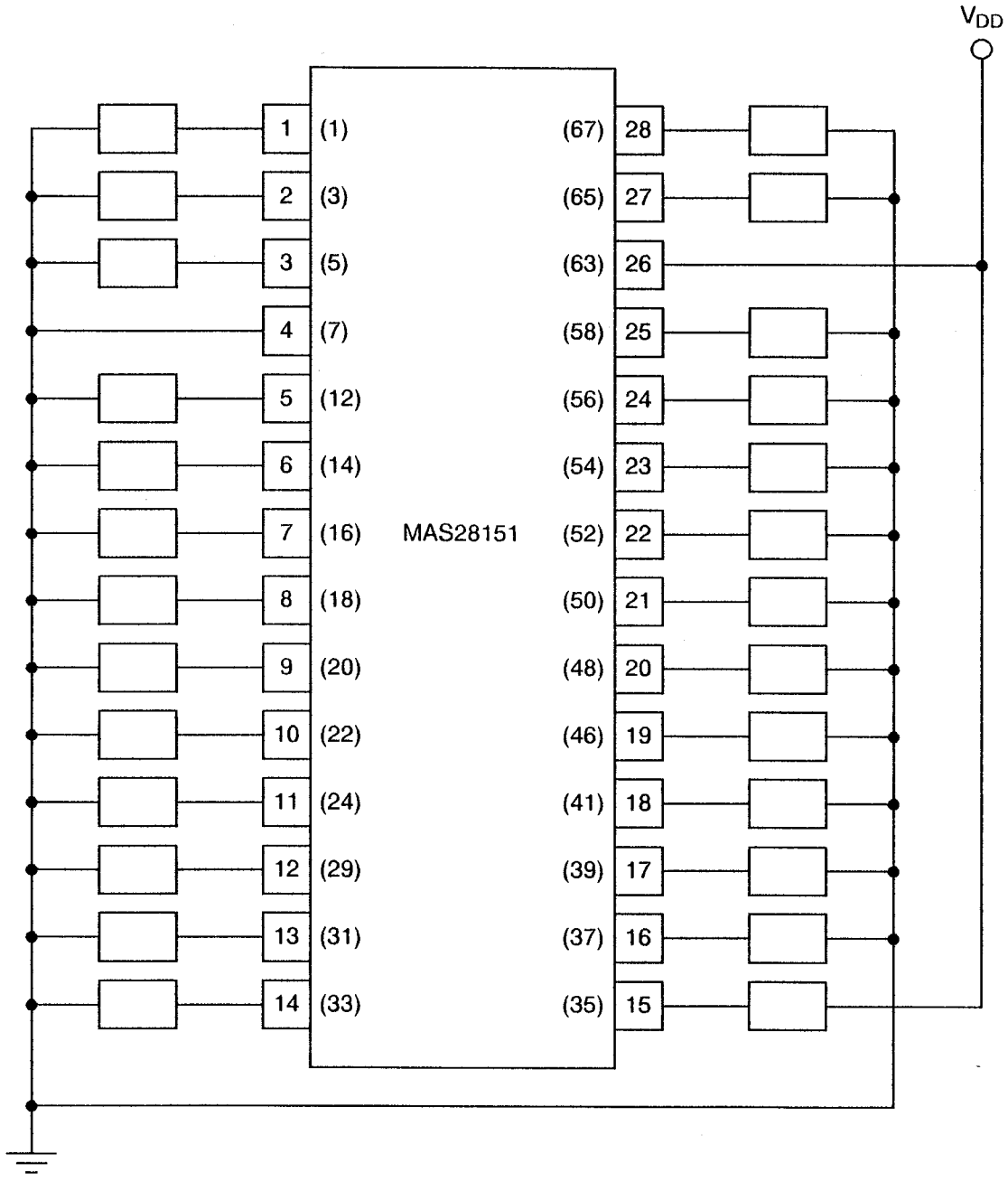


NOTES

1. Pin numbers in parenthesis are for the flat package.
2. Protection resistor = 10kΩ.

APPENDIX 'A'

ELECTRICAL CIRCUIT FOR STATIC BURN-IN 2



NOTES

1. Pin numbers in parenthesis are for the flat package.
2. Protection resistor = 10kΩ.