INTEGRATED CIRCUITS, SILICON MONOLITHIC, ADVANCED CMOS QUAD 2-INPUT NAND GATE WITH TTL COMPATIBLE INPUTS AND FULLY BUFFERED OUTPUTS

BASED ON TYPE 54ACT00

ESCC Detail Specification No. 9201/128

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DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

DCR No.	CHANGE DESCRIPTION
227	Editorial and technical changes as per DCR.

TABLE OF CONTENTS

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.
(b) MIL-STD-883, Test Methods and Procedures for Microelectronics.

1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

1.4.1 The ESCC Component Number

The ESCC Component number shall be constituted as follows:

Example: 920112801A
- Detail Specification Reference: 9201128
- Component Type Variant Number: 01 (as required)
- Total Dose Radiation Level Letter: A (as required)

1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

Variant Number	Based on Type	Case	Terminal Material and /or Finish	Weight max g	Total Dose Radiation Level Letter
01	54ACT00	FP	G2	0.7	A [300kRAD(Si)]
02	54ACT00	FP	G4	0.7	A [300kRAD(Si)]

The terminal material and/or finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.

The Total Dose Radiation Level Letter shall be as defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order, the letter shall be changed accordingly.

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the ESCC Generic Specification.

Characteristics	Symbols	Maximum Ratings	Units	Remarks
Supply Voltage	V_{DD}	-0.5 to 6	V	Note 1
Input Voltage	V_{IN}	-0.5 to V_{DD} +0.5	V	Notes 1, 2
Output Voltage	V_{OUT}	-0.5 to V_{DD} +0.5	V	Notes 1, 3
Device Power Dissipation (Continuous)	P_D	500	mW	
Supply Current	I_{DDop}	50	mA	
Operating Temperature Range	T_{op}	-55 to +125	^oC	T_{amb}
Storage Temperature Range	T_{stg}	-65 to +150	^oC	
Soldering Temperature	T_{sol}	+260	^oC	Note 4

NOTES:

1. Device is functional for $4.5V \leq V_{DD} \leq 5.5V$.
2. Input current limited to $I_{IC}=\pm 20mA$.
3. Output current limited to $I_{OUT}=\pm 50mA$.
4. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same terminal shall not be resoldered until 3 minutes have elapsed.

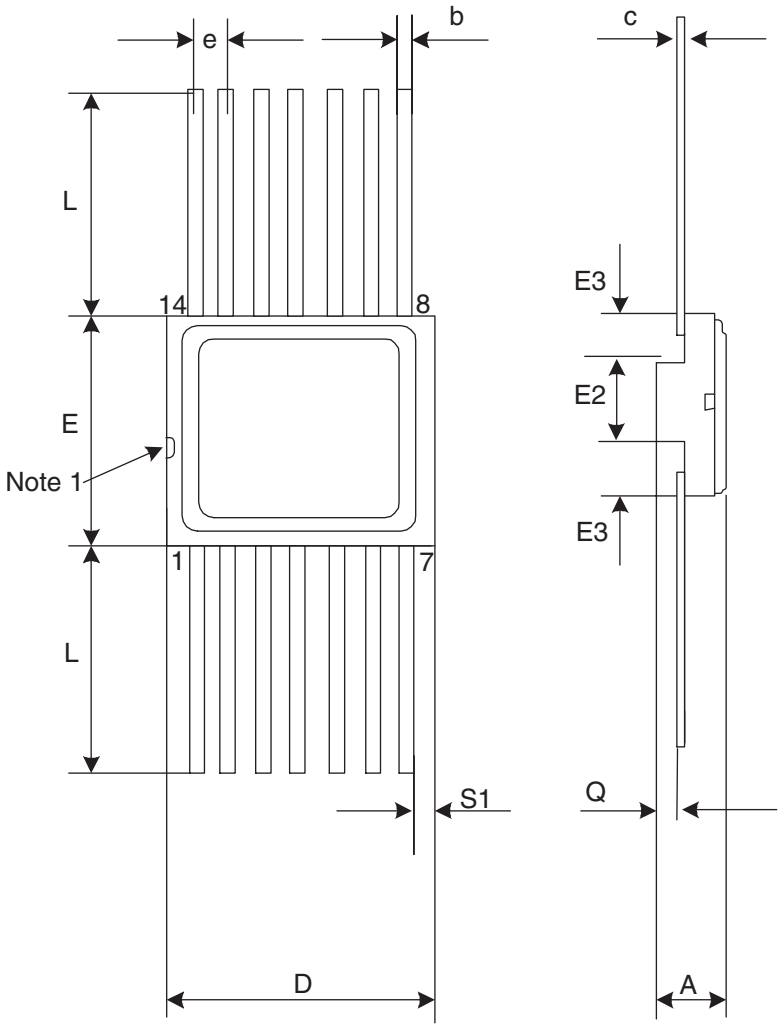
1.6 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of 2000 Volts.

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

Flat Package (FP) - 14 Pin

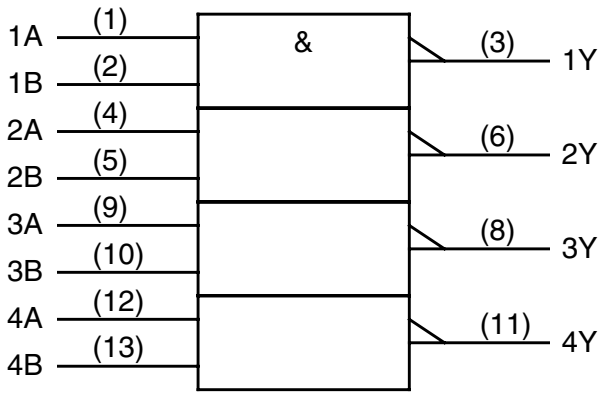

b
e
c
L
14
8
E3
E2
E
Note 1
E3
1
7
L
S1
Q
D
A

Symbols	Dimensions mm		Notes
	Min	Max	
A	2.31	2.72	
b	0.38	0.48	3
c	0.1	0.18	3
D	9.27	9.73	
E	6.19	6.5	
E2	3.68 TYPICAL		
E3	0.76	-	
e	1.27		2, 4
L	6.86	7.62	3
Q	0.66	1.14	3
S1	0.13	-	5

NOTES:

1. Index area; a notch or a dot shall be located adjacent to Pin 1 and shall be within the area shown.
2. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ±0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
3. All terminals.
4. 12 spaces.
5. 4 places.

1.8 FUNCTIONAL DIAGRAM



1.9 PIN ASSIGNMENT

Pin	Function	Pin	Function
1	1A Input	8	3Y Output
2	1B Input	9	3A Input
3	1Y Output	10	3B Input
4	2A Input	11	4Y Output
5	2B Input	12	4A Input
6	2Y Output	13	4B Input
7	V_{SS}	14	V_{DD}

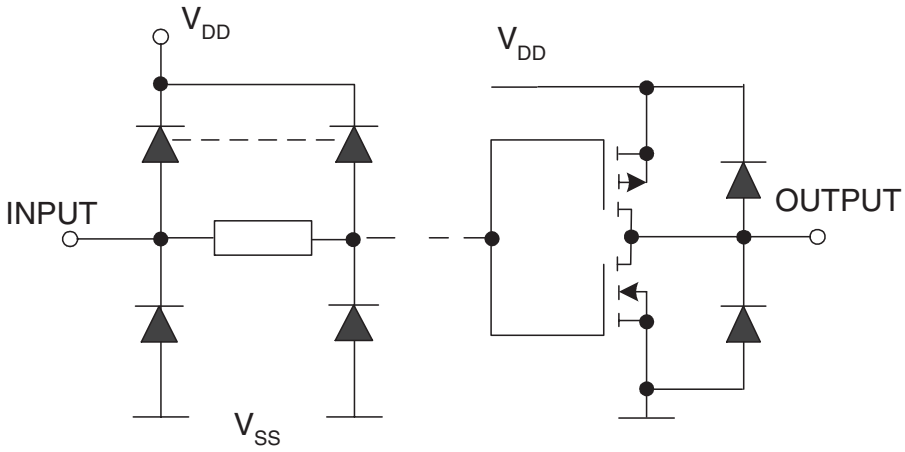
1.10 TRUTH TABLE

1. Logic Level Definitions: L = Low Level, H = High Level
2. Positive Logic: $Y = \overline{A.B}$.

EACH GATE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

1.11 PROTECTION NETWORKS



2. REQUIREMENTS

2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirement and do not affect the component's reliability, are listed in the appendices attached to this specification.

2.1.1 Deviations from the Generic Specification

None.

2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification.
(b) The ESCC qualified components symbol (for ESCC qualified components only).
(c) The ESCC Component Number.
(d) Traceability information.

2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures. Consolidated Notes are given after the tables.

2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at T_{amb}=+22 ± 3°C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table without Load V_{IL}=0.4V,V_{IH}=2.4V V_{DD}=4.5V,V_{SS}=0V Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table without Load V_{IL}=0.4V,V_{IH}=2.4V V_{DD}=5.5V,V_{SS}=0V Note 2	-	-	-

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Quiescent Current 1	I_{DD1}	3005	V_{IL}=0V,V_{IH}=5.5V V_{DD}=5.5V,V_{SS}=0V Note 3	-	1	µA
Quiescent Current 2	I_{DD2}	3005	V_{IN} (Under Test)=3.4V V_{IN} (Remaining Inputs)=5.5V or 0V V_{DD}=5.5V,V_{SS}=0V Note 4	-	1.6	mA
Low Level Input Current	I_{IL}	3009	V_{IN} (Under Test)=0V V_{DD}=5.5V,V_{SS}=0V	-	-100	nA
High Level Input Current	I_{IH}	3010	V_{IN} (Under Test)=5.5V V_{DD}=5.5V,V_{SS}=0V	-	100	nA
Low Level Output Voltage 1	V_{OL1}	3007	V_{IL}=0.8V, V_{IH}=2V I_{OL}=50µA V_{DD}=4.5V, V_{SS}=0V	-	100	mV
Low Level Output Voltage 2	V_{OL2}	3007	V_{IL}=0.8V, V_{IH}=2V I_{OL}=50µA V_{DD}=5.5V, V_{SS}=0V	-	100	mV
Low Level Output Voltage 3	V_{OL3}	3007	V_{IL}=0.8V, V_{IH}=2V I_{OL}=24mA V_{DD}=4.5V, V_{SS}=0V	-	400	mV
Low Level Output Voltage 4	V_{OL4}	3007	V_{IL}=0.8V, V_{IH}=2V I_{OL}=24mA V_{DD}=5.5V, V_{SS}=0V	-	400	mV
Low Level Output Voltage 5	V_{OL5}	3007	V_{IL}=0.8V, V_{IH}=2V I_{OL}=50mA V_{DD}=5.5V, V_{SS}=0V Note 5	-	1.65	V
High Level Output Voltage 1	V_{OH1}	3006	V_{IL}=0.8V, V_{IH}=2V I_{OH}=-50µA V_{DD}=4.5V, V_{SS}=0V	4.4	-	V
High Level Output Voltage 2	V_{OH2}	3006	V_{IL}=0.8V, V_{IH}=2V I_{OH}=-50µA V_{DD}=5.5V, V_{SS}=0V	5.4	-	V
High Level Output Voltage 3	V_{OH3}	3006	V_{IL}=0.8V, V_{IH}=2V I_{OH}=-24mA V_{DD}=5.5V, V_{SS}=0V	5.4	-	V
High Level Output Voltage 4	V_{OH4}	3006	V_{IL}=0.8V, V_{IH}=2V I_{OH}=-24mA V_{DD}=5.5V, V_{SS}=0V	4.7	-	V
High Level Output Voltage 5	V_{OH5}	3006	V_{IL}=0.8V, V_{IH}=2V I_{OH}=-50mA V_{DD}=5.5V, V_{SS}=0V Note 4	3.85	-	V

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Input Clamp Voltage 1, to V_{SS}	V_{IC1}	-	I_{IN} (Under Test)= -1mA V_{DD}=Open, V_{SS}=0V All Other Pins Open	-0.4	-1.5	V
Input Clamp Voltage 2, to V_{DD}	V_{IC2}	-	I_{IN} (Under Test)= 1mA V_{DD}=0V, V_{SS}=Open All Other Pins Open	0.4	1.5	V
Input Capacitance	C_{IN}	3012	V_{IN} (Not Under Test)=0V V_{DD}=5V, V_{SS}=0V f = 100 kHz to 1 MHz Note 6	-	10	pF
Propagation Delay Low to High, mA or mB to mY	t_{PLH}	3003	V_{IN}(Under Test)=Pulse Generator V_{IN}(Remaining Inputs)=Truth Table V_{IL}=0V, V_{IH}=4.5V V_{DD}=4.5V, V_{SS}=0V Note 7	1	9	ns
Propagation Delay High to Low, mA or mB to mY	t_{PHL}	3003	V_{IN}(Under Test)=Pulse Generator V_{IN}(Remaining Inputs)=Truth Table V_{IL}=0V, V_{IH}=4.5V V_{DD}=4.5V, V_{SS}=0V Note 7	1	9	ns

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at T_{amb}=+125 (+0 -5) ^{o}C and T_{amb}=- 55(+5-0)^{o}C.

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Functional Test 1	-	3014	Verify Truth Table without Load V_{IL}=0.4V,V_{IH}=2.4V V_{DD}=4.5V,V_{SS}=0V Note 2	-	-	-
Functional Test 2	-	3014	Verify Truth Table without Load V_{IL}=0.4V,V_{IH}=2.4V V_{DD}=5.5V,V_{SS}=0V Note 2	-	-	-
Quiescent Current 1	I_{DD1}	3005	V_{IL}=0V,V_{IH}=5.5V V_{DD}=5.5V,V_{SS}=0V Note 3	-	425	µA

Characteristics	Symbols	MIL-STD-883 Test Method	Test Conditions Note 1	Limits		Units
				Min	Max	
Quiescent Current 2	I_{DD2}	3005	V_{IN} (Under Test)=3.4V V_{IN} (Remaining Inputs)=5.5V or 0V V_{DD}=5.5V,V_{SS}=0V Note 4	-	1.6	mA
Low Level Input Current	I_{IL}	3009	V_{IN} (Under Test)=0V V_{DD}=5.5V,V_{SS}=0V	-	-1	µA
High Level Input Current	I_{IH}	3010	V_{IN} (Under Test)=5.5V V_{DD}=5.5V,V_{SS}=0V	-	1	µA
Low Level Output Voltage 1	V_{OL1}	3007	V_{IL}=0.8V, V_{IH}=2V I_{OL}=50µA V_{DD}=4.5V, V_{SS}=0V	-	100	mV
Low Level Output Voltage 2	V_{OL2}	3007	V_{IL}=0.8V, V_{IH}=2V I_{OL}=50µA V_{DD}=5.5V, V_{SS}=0V	-	100	mV
Low Level Output Voltage 3	V_{OL3}	3007	V_{IL}=0.8V, V_{IH}=2V I_{OL}=24mA V_{DD}=4.5V, V_{SS}=0V T_{amb}=+125 (+0 -5) °C T_{amb}=- 55(+5-0)°C	- -	500 400	mV mV
Low Level Output Voltage 4	V_{OL4}	3007	V_{IL}=0.8V, V_{IH}=2V I_{OL}=24mA V_{DD}=4.5V, V_{SS}=0V T_{amb}=+125 (+0 -5) °C T_{amb}=- 55(+5-0)°C	- -	500 400	mV mV
Low Level Output Voltage 5	V_{OL5}	3007	V_{IL}=0.8V, V_{IH}=2V I_{OL}=50mA V_{DD}=5.5V, V_{SS}=0V Note 5	-	1.65	V
High Level Output Voltage 1	V_{OH1}	3006	V_{IL}=0.8V, V_{IH}=2V I_{OH}=-50µA V_{DD}=4.5V, V_{SS}=0V	4.4	-	V
High Level Output Voltage 2	V_{OH2}	3006	V_{IL}=0.8V, V_{IH}=2V I_{OH}=-50µA V_{DD}=5.5V, V_{SS}=0V	5.4	-	V
High Level Output Voltage 3	V_{OH3}	3006	V_{IL}=0.8V, V_{IH}=2V I_{OH}=-24mA V_{DD}=4.5V, V_{SS}=0V	5.4	-	V
High Level Output Voltage 4	V_{OH4}	3006	V_{IL}=0.8V, V_{IH}=2V I_{OH}=-24mA V_{DD}=5.5V, V_{SS}=0V	4.7	-	V
High Level Output Voltage 5	V_{OH5}	3006	V_{IL}=0.8V, V_{IH}=2V I_{OH}=-50mA V_{DD}=5.5V, V_{SS}=0V Note 5	3.85	-	V

2.3.3 Notes to Electrical Measurement Tables

1. Unless otherwise specified all inputs and outputs shall be tested for each characteristic. Inputs not under test shall be $V_{IN}=V_{SS}$ or V_{DD} and outputs not under test shall be open.
2. Functional tests shall be performed to verify Truth Table with $V_{OH}\geq 2.5V$, $V_{OL}\leq 2.5V$.
3. Quiescent Current I_{DD1} shall be tested using the following input conditions:
   (a) A Inputs = B Inputs = V_{IH}
   (b) A Inputs = B Inputs = V_{IL}
4. Quiescent Current I_{DD2} shall be tested using the following input conditions:
   (a) Input 1A=3.4V
   (b) Input 1B=3.4V
   (c) Input 2A=3.4V
   (d) Input 2B=3.4V
   (e) Input 3A=3.4V
   (f) Input 3B=3.4V
   (g) Input 4A=3.4V
   (h) Input 4B=3.4V
5. Test shall be performed on only one output at a time with a duration not to exceed 2ms.
6. Guaranteed but not tested.
7. Measurements shall be performed as a go-no-go test on a 100% basis. Read and record measurements shall be performed on a sample of 5 components.
   The pulse generator shall have the following characteristics:
   V_{GEN} = 0 to 3V; f = 1 MHz minimum; t_r and $t_f \leq 3ns$ (10% to 90%); duty cycle = 50%; $R_L = 500\Omega$
   Output load capacitance C_L = 50pF + 5% including scope probe, wiring and stray capacitance without component in the test fixture.
   Propagation delay shall be measured referenced to the 50% of V_{DD}. All paths must be tested.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at T_{amb} =+22±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Quiescent Current 1	I_{DD1}	±0.15	-	1	µA
Quiescent Current 2	I_{DD2}	±0.4	-	1.6	mA
Low Level Input Current	I_{IL}	±20	-	-100	nA
High Level Input Current	I_{IH}	±20	-	100	nA
Low Level Output Voltage 4	V_{OL4}	±40	-	400	mV
High Level Output Voltage 4	V_{OH4}	±0.2	4.7	-	V

NOTES:
Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at T_{amb} =+22±3°C.

The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

Characteristics	Symbols	Limits			Units
		Drift Value Δ	Absolute		
			Min	Max	
Functional Test 1	-	-	-	-	–
Functional Test 2	-	-	-	-	–
Quiescent Current 1	I_{DD1}	±0.15	-	1	µA
Quiescent Current 2	I_{DD2}	±0.4	-	1.6	mA
Low Level Input Current	I_{IL}	±20	-	-100	nA
High Level Input Current	I_{IH}	±20	-	100	nA
Low Level Output Voltage 1	V_{OL1}	±40	-	100	mV
Low Level Output Voltage 2	V_{OL2}	±40	-	100	mV
Low Level Output Voltage 3	V_{OL3}	±40	-	400	mV
Low Level Output Voltage 4	V_{OL4}	±40	-	400	mV
Low Level Output Voltage 5	V_{OL5}	±40	-	1.65	V
High Level Output Voltage 1	V_{OH1}	±0.2	4.4	-	V
High Level Output Voltage 2	V_{OH2}	±0.2	5.4	-	V
High Level Output Voltage 3	V_{OH3}	±0.2	5.4	-	V
High Level Output Voltage 4	V_{OH4}	±0.2	4.7	-	V
High Level Output Voltage 5	V_{OH5}	±0.2	3.85	-	V

NOTES:

1 Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

2 The drift values (Δ) are applicable to the Operating Life Test only.

2.6 HIGH TEMPERATURE REVERSE BIAS BURN-IN CONDITIONS

2.6.1 N-Channel HTRB

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	^{o}C
Outputs Y (all gates)	V_{OUT}	Open or V_{SS}	V
Inputs A, B (all gates)	V_{IN}	V_{SS}	V
Positive Supply Voltage	V_{DD}	5.5 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V
Duration	t	72	Hours

NOTES:
1. Input Protection Resistor = 200Ω min to 47kΩ max.
2. Output Load = 200Ω min to 10kΩ max.

2.6.2 P-Channel HTRB

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	^{o}C
Outputs Y (all gates)	V_{OUT}	Open or V_{SS}	V
Inputs A, B (all gates)	V_{IN}	V_{DD}	V
Positive Supply Voltage	V_{DD}	5.5 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V
Duration	t	72	Hours

NOTES:
1. Input Protection Resistor = 200Ω min to 47kΩ max.
2. Output Load = 200Ω min to 10kΩ max.

2.7 POWER BURN-IN CONDITIONS

Characteristics	Symbols	Test Conditions	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	°C
Outputs Y (all gates)	V_{OUT}	Open	V
Inputs A, B (all gates)	V_{IN}	V_{GEN}	V
Pulse Voltage	V_{GEN}	0V to V_{DD}	V
Pulse Frequency Square Wave	f_{GEN}	100k ± 10% 50 ± 15% Duty Cycle $t_r = t_f \leq 8$ns/V	Hz
Positive Supply Voltage	V_{DD}	5.5 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:
1. Input Protection Resistor = 200Ω min to 47kΩ max.
2. Output Load = 200Ω min to 10kΩ max.

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified for Power Burn-in.

2.9 TOTAL DOSE RADIATION TESTING

2.9.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in the component type variant information herein or in the Purchase Order.

Characteristics	Symbols	Test Conditions (Note 1)	Units
Ambient Temperature	T_{amb}	+125 (+0 -5)	°C
Outputs Y (all gates)	V_{OUT}	Open	V
Inputs A, B (all gates)	V_{IN}	Note 2	V
Positive Supply Voltage	V_{DD}	5.5 (+0 -0.5)	V
Negative Supply Voltage	V_{SS}	0	V

NOTES:
1. Input Protection Resistor = 1kΩ.±20%
2. V_{IN} such that V_{OUT}=0 with a maximum input at V_{DD}.

2.9.2 Electrical Measurements for Total Dose Radiation Testing

Prior to irradiation testing the devices shall have successfully met Room Temperature Electrical Measurements specified herein.

Unless otherwise stated the measurements shall be performed at T_{amb} = +22 ± 3 °C.
The test methods and test conditions shall be as per the corresponding test defined in Room Temperature Electrical Measurements.

The parameters to be measured during and on completion of irradiation testing are shown below.

Unless otherwise specified all inputs and outputs shall be tested for each characteristic.

Characteristics	Symbols	Limits		Units
		Min	Max	
Functional Test 1	-	-	-	–
Functional Test 2	-	-	-	–
Quiescent Current 1	I_{DD1}	-	1	µA
Quiescent Current 2	I_{DD2}	-	1.6	mA
Low Level Input Current	I_{IL}	-	-100	nA
High Level Input Current	I_{IH}	-	100	nA
Low Level Output Voltage 1	V_{OL1}	-	100	mV
Low Level Output Voltage 2	V_{OL2}	-	100	mV
Low Level Output Voltage 3	V_{OL3}	-	400	mV
Low Level Output Voltage 4	V_{OL4}	-	400	mV
Low Level Output Voltage 5	V_{OL5}	-	1.65	V
High Level Output Voltage 1	V_{OH1}	4.4	-	V
High Level Output Voltage 2	V_{OH2}	5.4	-	V
High Level Output Voltage 3	V_{OH3}	5.4	-	V
High Level Output Voltage 4	V_{OH4}	4.7	-	V
High Level Output Voltage 5	V_{OH5}	3.85	-	V

APPENDIX 'A'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Deviations from Production Control - Chart F2	Electrostatic Discharge Sensitivity Test Method: These components are categorised as class 2 (2000 V) per MIL-STD-883 Method 3015.
Deviations from Production Control (Wafer Lot Acceptance) - Chart F2	Total Dose Radiation Testing: The test method and procedure shall be as specified in MIL-STD-883 Method 1019 condition A.
Deviations from Screening Tests - Chart F3	External Visual Inspection: The criteria applicable to chip outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a). High Temperature Reverse Bias Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.
Deviations from Qualification and Periodic Tests - Chart F4	External Visual Inspection: The criteria applicable to chip outs are those described in MIL-STD-883, Test Method 2009, Paras 3.3.6(b) and 3.3.7(a). Operating Life: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.
Deviations from High and Low Temperatures Electrical Measurements	High and Low Temperatures Electrical Measurements may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes High and Low Temperatures Electrical Measurements per the Detail Specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.
Deviations from Room Temperature Electrical Measurements	All AC characteristics (Capacitance and Timings) may be considered guaranteed but not tested if successful pilot lot testing has been performed on the wafer lot which includes AC characteristic measurements per the detail specification. A summary of the pilot lot testing shall be provided if required by the Purchase Order.