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# INTEGRATED CIRCUITS, SILICON MONOLITHIC,

# **ADVANCED CMOS QUAD 2-LINE TO 1-LINE**

# DATA SELECTORS/MULTIPLEXERS

# WITH INVERTED OUTPUTS,

# **BASED ON TYPE 54AC158**

# ESCC Detail Specification No. 9408/074

# ISSUE 1 October 2002



Document Custodian: European Space Agency - see https://escies.org



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# space components coordination group

		Approved by							
Issue/Rev.	Date	SCCG Chairman	ESA Director General or his Deputy						
lssue 1	March 1994	Forman L	4. Jack						



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### **DOCUMENTATION CHANGE NOTICE**

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.
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APPENDICES (Applicable to specific Manufacturers only) 'A' AGREED DEVIATIONS FOR MOTOROLA (F)

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#### 1. <u>GENERAL</u>

#### 1.1 <u>SCOPE</u>

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon, monolithic, advanced CMOS Quad 2-Line to 1-Line Data Selector/Multiplexer, having fully buffered inverted outputs, based on Type 54AC158. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

#### 1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

#### 1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

#### 1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

As per Figure 3(b).

1.8 <u>CIRCUIT SCHEMATIC</u>

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

#### 1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are Categorised as Class 2 with a Minimum Critical Path Failure Voltage of 4000 Volts.

#### 1.11 INPUT AND OUTPUT PROTECTION NETWORKS

Protection networks shall be incorporated into each input and output as shown in Figure 3(e).



### TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
01	D.I.L.	2(a)	G4
02	FLAT	2(b)	G4
03	CHIP CARRIER	2(c)	2
04	CHIP CARRIER	2(c)	4

#### TABLE 1(b) - MAXIMUM RATINGS

NO.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNITS	REMARKS
1	Supply Voltage	V <sub>DD</sub>	-0.5 to +6.0	V	Note 1
2	Input Voltage	V <sub>IN</sub>	-0.5 to V <sub>DD</sub> + 0.5	V	Notes 1, 2
3	Output Voltage	V <sub>OUT</sub>	-0.5 to V <sub>DD</sub> +0.5	V	Notes 1, 3
4	Device Dissipation (Continuous)	PD	528	mW	Note 4
5	Supply Current	I <sub>DDop</sub>	96	mA	
6	Operating Temperature Range	T <sub>op</sub>	-55 to +125	°C	T <sub>amb</sub>
7	Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C	
8	Soldering Temperature For FP and DIP For CCP	T <sub>sol</sub>	+ 265 + 245	°C	Note 5 Note 6

#### **NOTES**

- 1. Device is functional for  $3.0V \le V_{DD} \le 5.5V$ .
- 2. Input current limited to  $I_{IC} = \pm 20$ mA.
- 3. Output current limited to  $I_{OUT} = \pm 50$ mA.
- 4. The maximum device dissipation is determined by IDDop max. (mA) x 5.5V.
- 5. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
- 6. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

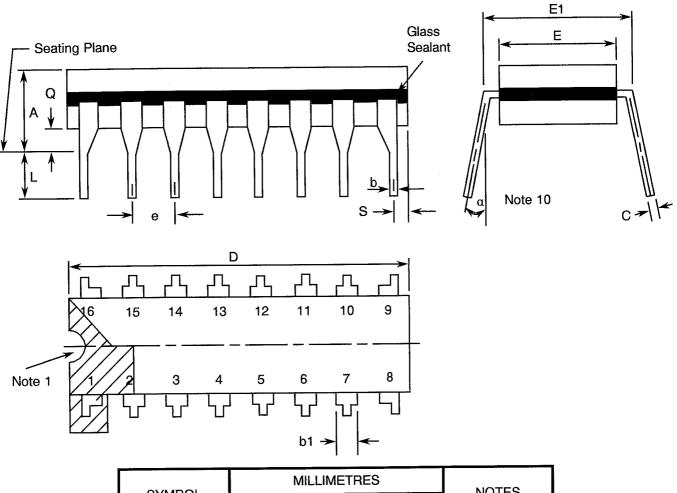
#### FIGURE 1 - PARAMETER DERATING INFORMATION

Not applicable.



### FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - DUAL-IN-LINE PACKAGE, 16-PIN

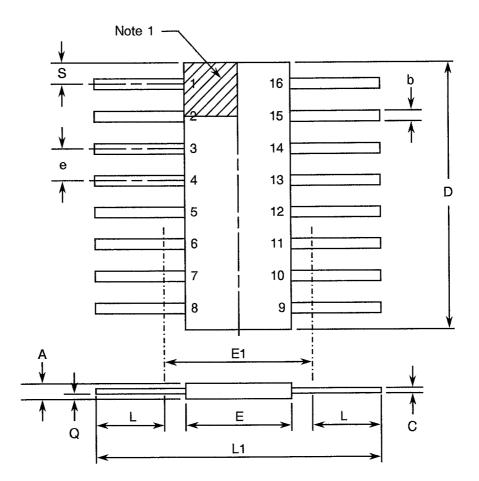


	MILLIM	NOTES	
SYMBOL.	MIN	MAX	NOTES
A	-	5.08	
b	0.35	0.56	8
b1	1.40	1.77	8
С	0.20	0.38	8
D	19.05	19.95	4
E	6.10	7.49	4
E1	7.62TY	PICAL	
е	2.54 T	/PICAL	6, 9
L.	3.10	4.31	8
Q.	0.25	1.02	3
S	0.40	1.10	7
α	0°	15°	10

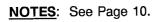


### FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - FLAT PACKAGE, 16-PIN



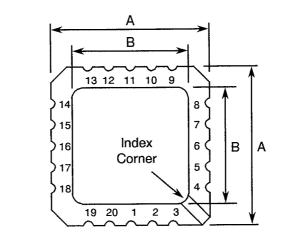
C)/MDOI	MILLIM	NOTES	
SYMBOL	MIN	MAX	NOTES
A	1.52	2.16	
b	0.36	0.56	8
С	0.08	0.17	. 8
D	9.42	10.16	4
E	5.84	7.24	
E1	7.00 T)	PICAL	4
е	1.27 T	PICAL	5, 9
L	5.84	9.14	8
L1	18.93	25.39	
Q.	-	1.02	2
S	-	1.40	7

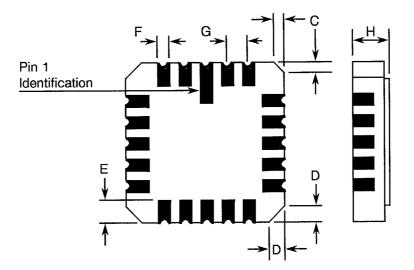




#### FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

# FIGURE 2(c) - SQUARE CHIP CARRIER PACKAGE, 20-TERMINAL





SYMBOL	MILLIM	NOTES	
STWBOL	MIN	MAX	NOTED
A	8.69	9.09	
В	7.80	9.09	
С	0.25	0.51	11
D	0.89	1.14	12
E	1.14	1.40	8
F ·	0.56	0.71	8
G	1.27 T	5, 9	
н	1.63	2.54	



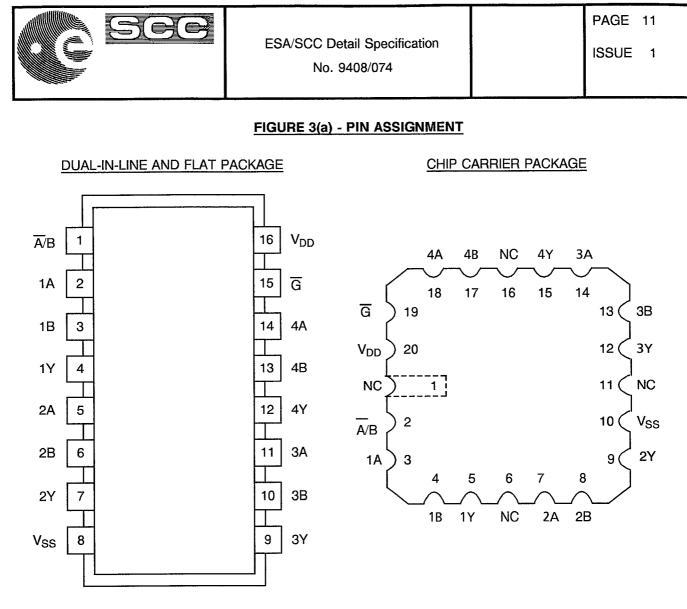
#### FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

#### NOTES TO FIGURES 2(a) TO 2(c) INCLUSIVE

- 1. Index area: a notch, letter or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages the index shall be as defined in Figure 2(c).
- 2. Dimension Q shall be measured at the point of exit of the lead from the body.
- 3. The dimension shall be measured from the seating plane to the base plane.
- 4. The dimension allows for off-centre lids, meniscus and glass overrun.
- 5. The true position pin or terminal spacing is 1.27mm between centrelines. Each pin or terminal centreline shall be located within ±0.13mm of it's true longitudinal position relative to Pin 1 and the highest pin number.
- 6. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of it's true longitudinal position relative to Pin 1 and the highest pin number.
- 7. Applies to all 4 corners.
- 8. All leads or terminals.
- 9. 14 spaces for flat and dual-in-line packages.

16 spaces for chip carrier packages.

- 10. Lead centreline when  $\alpha$  is 0°.
- 11. Index corner only 2 dimensions.
- 12. 3 non-index corners 6 dimensions.



TOP VIEW

TOP VIEW

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#### FLAT PACKAGE AND DUAL-IN-LINE TO CHIP CARRIER PIN ASSIGNMENT

FLAT PACKAGE AND DUAL-IN-LINE PIN OUTS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
CHIP CARRIER PIN OUTS	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20



### FIGURE 3(b) - TRUTH TABLE (EACH SELECTOR/MULTIPLEXER)

	INPUT	OUTPUTS		
STROBE		DA	TA	
G	Ā/B	А	В	Y
Н	Х	Х	Х	Н
L	L	L	Х	Н
L	L	Н	Х	L
L	Н	Х	L	Н
L	Н	Х	Н	L

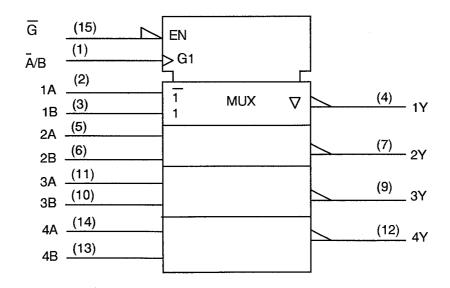
#### **NOTES**

1. Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant.

#### FIGURE 3(c) - CIRCUIT SCHEMATIC

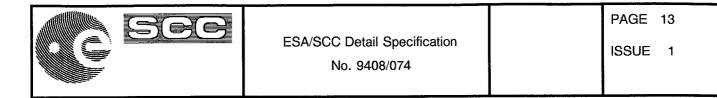
Not applicable.

#### FIGURE 3(d) - FUNCTIONAL DIAGRAM

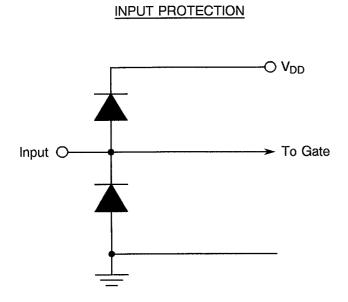


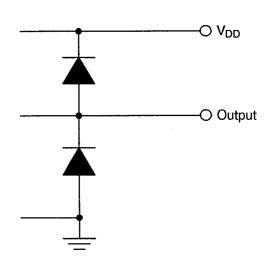
#### **NOTES**

1. Pin numbers shown are for DIP and FP.



# FIGURE 3(e) - INPUT AND OUTPUT PROTECTION NETWORKS





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OUTPUT PROTECTION



#### 2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

- (a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.
- (b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

#### 3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following symbols are used:

V<sub>IC</sub> = Input Clamp Voltage.

I<sub>IC</sub> = Input Clamp Diode Current.

V<sub>OLP</sub> = Ground Bounce Outputs Low.

V<sub>OHV</sub> = Ground Bounce Outputs High.

#### 4. **REQUIREMENTS**

#### 4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalant to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

#### 4.2 DEVIATIONS FROM GENERIC SPECIFICATION

#### 4.2.1 Deviations from Special In-process Controls

- (a) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during qualification and maintenance of qualification.
- (b) Para. 5.2.2, Total Dose Irradiation Testing: If specified in a Purchase Order, shall be performed during procurement on a lot acceptance basis at the total dose irradiation level specified in the Purchase Order.

# 4.2.2 Deviations from Final Production Tests (Chart II)

None.

- 4.2.3 <u>Deviations from Burn-in Tests (Chart III)</u> None.
- 4.2.4 <u>Deviations from Qualification Tests (Chart IV)</u> None.



#### 4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

#### 4.3 MECHANICAL REQUIREMENTS

#### 4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

#### 4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 2.2 grammes for the dual-inline package, 0.7 grammes for the flat package and 0.6 grammes for the chip carrier package.

#### 4.4 MATERIALS AND FINISHES

The materials shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

#### 4.4.1 <u>Case</u>

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body and the lids shall be welded, brazed, preform-soldered or glass frit sealed.

#### 4.4.2 Lead Material and Finish

For dual-in-line and flat packages, the material shall be Type 'G' with Type '4' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. For chip carrier packages the finish shall be Type '2' or Type '4' in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

#### 4.5 MARKING

#### 4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

- (a) Lead Identification.
- (b) The SCC Component Number.
- (c) Traceability Information.

#### 4.5.2 Lead Identification

For dual-in-line and flat packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side. For chip carrier packages, the index shall be as defined by Figure 2(c).



#### 4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows: <u>940807401BF</u>

Detail Specification Number	
Type Variant (see Table 1(a))	
Testing Level (B or C, as applicable)	
Total Dose Irradiation Level (if applicable)	

The Total Dose Irradiation Level designation shall be added for those devices for which a sample has been successfully tested to the level in question. For these devices, a code letter shall be added in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

#### 4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

#### 4.6 ELECTRICAL MEASUREMENTS

#### 4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at  $T_{amb} = +22 \pm 3$  °C.

#### 4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at  $T_{amb} = +125 (+0.5) \text{ °C}$  and -55 (+5.0) °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits and test sequences for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

#### 4.7 BURN-IN TESTS

#### 4.7.1 Parameter Drift Values

The parameter drift values applicable to H.T.R.B. and Power Burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at  $T_{amb} = +22 \pm 3$  °C. The parameter drift values ( $\Delta$ ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

For H.T.R.B. Burn-in, the parameter drift values ( $\Delta$ ) shall be applied before the N-Channel (0 hours) and after the P-Channel (144 hours) burn-in.

#### 4.7.2 Conditions for H.T.R.B. and Power Burn-in

The requirements for H.T.R.B. and Power Burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for H.T.R.B. and Power Burn-in shall be as specified in Tables 5(a), 5(b) and 5(c) of this specification.

#### 4.7.3 Electrical Circuits for H.T.R.B and Power Burn-in

Circuits for use in performing the H.T.R.B. and Power Burn-in tests are shown in Figures 5(a), 5(b) and 5(c) of this specification.



### TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

		0.445.01	TEST METHOD	TEST	TEST CONDITIONS (PINS UNDER TEST	LIM	ITS	
No.	CHARACTERISTICS	SYMBOL	MIL-STD 883	FIG.	D/F = DIP AND FP C = CCP)	MIN	MAX	UNIT
1	Functional Test 1	-		3(b)	Verify Truth Table with Load. $V_{IL} = 0.45V$ , $V_{IH} = 2.5V$ $I_{OL} = 1.0mA$ , $I_{OH} = -1.0mA$ $V_{DD} = 3.0V$ , $V_{SS} = 0V$ $t_r = t_f < 100ns$ f = 10kHz (min) Note 1	-	-	-
2	Functional Test 2	-	-	3(b)	Verify Truth Table with Load. $V_{IL} = 0.6V, V_{IH} = 3.7V$ $I_{OL} = 1.0mA, I_{OH} = -1.0mA$ $V_{DD} = 4.5V, V_{SS} = 0V$ $t_r = t_f < 50ns$ f = 10kHz (min) Note 1	-	-	-
3	Functional Test 3	-	-	3(b)	Verify Truth Table with Load. $V_{IL} = 1.0V$ , $V_{IH} = 4.5V$ $I_{OL} = 1.0mA$ , $I_{OH} = -1.0mA$ $V_{DD} = 5.5V$ , $V_{SS} = 0V$ $t_r = t_f < 50ns$ f = 10kHz (min) Note 1	-	-	-
4 to 5	Quiescent Current	IDD	3005	4(a)	$V_{IL} = 0V, V_{IH} = 5.5V$ $V_{DD} = 5.5V, V_{SS} = 0V$ All Outputs Open Note 2 (Pin D/F 16) (Pin C 20)	-	1.0	μА
6 to 15	Input Current Low Level	Ι <sub>ΙL</sub>	3009	4(b)	$V_{IN} \text{ (Under Test)} = 0V$ $V_{IN} \text{ (Remaining Inputs)} = 5.5V$ $V_{DD} = 5.5V, V_{SS} = 0V$ (Pins D/F 1-2-3-5-6-10-11-13- 14-15) (Pins C 2-3-4-7-8-13-14-17- 18-19)	-	- 100	nA
16 to 25	Input Current High Level	lπ	3010	4(c)	$V_{IN} \text{ (Under Test)} = 5.5V$ $V_{IN} \text{ (Remaining Inputs)} = 0V$ $V_{DD} = 5.5V, V_{SS} = 0V$ (Pins D/F 1-2-3-5-6-10-11-13- 14-15) (Pins C 2-3-4-7-8-13-14-17- 18-19)	-	100	nA



### TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD	TEST	TEST CONDITIONS (PINS UNDER TEST	LIM	ITS	UNIT
140.	CHANAGI ENISTICS	STMBOL	MIL-STD 883	FIG.	D/F = DIP AND FP C = CCP)	MIN	MAX	UNIT
26 to 29	Output Voltage Low Level 1	V <sub>OL1</sub>	3007	4(d)	$V_{IL} = 0.9V, V_{IH} = 2.1V$ $I_{OL} = 50\mu A$ $V_{DD} = 3.0V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	-	0.1	V
30 to 33	Output Voltage Low Level 2	V <sub>OL2</sub>	3007	4(d)	$V_{IL} = 1.35V, V_{IH} = 3.15V$ $I_{OL} = 50\mu A$ $V_{DD} = 4.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	-	0.1	V
34 to 37	Output Voltage Low Level 3	V <sub>OL3</sub>	3007	4(d)	$V_{IL} = 1.65V, V_{IH} = 3.85V$ $I_{OL} = 50\mu A$ $V_{DD} = 5.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	-	0.1	V
38 to 41	Output Voltage Low Level 4	V <sub>OL4</sub>	3007	4(d)	$V_{IL} = 0.9V, V_{IH} = 2.1V$ $I_{OL} = 12mA$ $V_{DD} = 3.0V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	-	0.4	V
42 to 45	Output Voltage Low Level 5	V <sub>OL5</sub>	3007	4(d)	$V_{IL} = 1.35V, V_{IH} = 3.15V$ $I_{OL} = 24mA$ $V_{DD} = 4.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	-	0.4	V
46 to 49	Output Voltage Low Level 6	V <sub>OL6</sub>	3007	4(d)	$V_{IL} = 1.65V, V_{IH} = 3.85V$ $I_{OL} = 24mA$ $V_{DD} = 5.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	-	0.4	V
50 to 53	Output Voltage Low Level 7	V <sub>OL7</sub>	3007	4(d)	$V_{IL} = 1.65V, V_{IH} = 3.85V$ $I_{OL} = 50mA$ $V_{DD} = 5.5V, V_{SS} = 0V$ Note 3 (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	-	1.65	V



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### TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD	TEST	TEST CONDITIONS (PINS UNDER TEST	LIM	ITS	UNIT
INO.	CHARACTERISTICS	STMBOL	MIL-STD 883	FIG.	D/F = DIP AND FP C = CCP)	MIN	MAX	UNIT
54 to 57	Output Voltage High Level 1	V <sub>OH1</sub>	3006	4(e)	$V_{IL} = 0.9V, V_{IH} = 2.1V$ $I_{OH} = -50\mu A$ $V_{DD} = 3.0V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	2.9	-	V
58 to 61	Output Voltage High Level 2	V <sub>OH2</sub>	3006	4(e)	$V_{IL} = 1.35V, V_{IH} = 3.15V$ $I_{OH} = -50\mu A$ $V_{DD} = 4.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	4.4	-	V
62 to 65	Output Voltage High Level 3	V <sub>OH3</sub>	3006	4(e)	$V_{IL} = 1.65V, V_{IH} = 3.85V$ $I_{OH} = -50\mu A$ $V_{DD} = 5.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	5.4	-	V
66 to 69	Output Voltage High Level 4	V <sub>OH4</sub>	3006	4(e)	$V_{IL} = 0.9V, V_{IH} = 2.1V$ $I_{OH} = -4.0mA$ $V_{DD} = 3.0V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	2.4	-	V
70 to 73	Output Voltage High Level 5	V <sub>OH5</sub>	3006	4(e)	$V_{IL} = 1.35V, V_{IH} = 3.15V$ $I_{OH} = -24mA$ $V_{DD} = 4.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	3.7	-	V
74 to 77	Output Voltage High Level 6	V <sub>OH6</sub>	3006	4(e)	$V_{IL} = 1.65V, V_{IH} = 3.85V$ $I_{OH} = -24mA$ $V_{DD} = 5.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	4.7	-	V
78 to 81	Output Voltage High Level 7	V <sub>OH7</sub>	3006	4(e)	$V_{IL} = 1.65V, V_{IH} = 3.85V$ $I_{OH} = -50mA$ $V_{DD} = 5.5V, V_{SS} = 0V$ Note 3 (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	3.85	<b>1</b> .	V



#### TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD	TEST	TEST CONDITIONS (PINS UNDER TEST	LIMITS		UNIT
NO.	CHARACTERISTICS	STIVIDUL	MIL-STD 883	FIG.	D/F = DIP AND FP C = CCP)	MIN	MAX	UNIT
82 to 91	Input Clamp Voltage (to V <sub>SS</sub> )	V <sub>IC1</sub>	3022	4(f)	$\begin{split} &I_{IN} \text{ (Under Test)} = -1.0\text{mA} \\ &V_{DD} = \text{Open}, V_{SS} = 0\text{V} \\ &\text{All Other Pins Open} \\ &(\text{Pins D/F 1-2-3-5-6-10-11-13-14-15}) \\ &(\text{Pins C 2-3-4-7-8-13-14-17-18-19}) \end{split}$	-0.4	- 1.5	V
92 to 101	Input Clamp Voltage (to V <sub>DD</sub> )	V <sub>IC2</sub>	3022	4(f)	$\begin{split} &I_{IN} \text{ (Under Test)} = 1.0\text{mA} \\ &V_{DD} = 0\text{V}, \ V_{SS} = \text{Open} \\ &AII \text{ Other Pins Open} \\ &(\text{Pins D/F 1-2-3-5-6-10-11-13-14-15}) \\ &(\text{Pins C 2-3-4-7-8-13-14-17-18-19}) \end{split}$	0.4	1.5	V

- 1. Maximum time to output comparator strobe 30µs.
- 2. Test each pattern of Figure 4(a).
- 3. No more than one output shall be measured at a time and the duration of the test shall not exceed 2.0ms.
- 4. Guaranteed but not tested.
- 5. Measurements shall be performed on a 100% basis go-no-go, with read and record on a sample basis, LTPD7 (32 pieces) after Chart III (Burn-in) Tests.
- 6. Hand test on 5 samples to be performed during Qualification and Extension of Qualification only.



### TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

			TEST METHOD	TEST	TEST CONDITIONS (PINS UNDER TEST	LIM	ITS	UNIT
No.	CHARACTERISTICS	SYMBOL	MIL-STD 883	FIG.	D/F = DIP AND FP C = CCP)	MIN	MAX	UNIT
102 to 111	Input Capacitance	C <sub>IN</sub>	3012	4(g)	$V_{IN} \text{ (Not Under Test)} = 0Vdc \\ V_{DD} = V_{SS} = 0V \\ \text{Note 4} \\ \text{(Pins D/F 1-2-3-5-6-10-11-13-14-15)} \\ \text{(Pins C 2-3-4-7-8-13-14-17-18-19)} \\ \end{array}$	-	8.0	pF
112 to 113	Propagation Delay Low to High 1 (A to Y) (B to Y)	t <sub>PLH1</sub>	3003	4(h)	$V_{IN} \text{ (Under Test)} = \text{Pulse}$ Generator $V_{IN} \text{ (Remaining Inputs)} =$ Figure 3(b) $V_{DD} = 4.5\text{V}, V_{SS} = 0\text{V}$ Note 5 $\frac{\text{Pins D/F}}{2 \text{ to } 4} = \frac{\text{Pins C}}{3 \text{ to } 5}$ $3 \text{ to } 4 = 4 \text{ to } 5$	-	7.0	ns
114 to 115	Propagation Delay High to Low 1 (A to Y) (B to Y)	t₽HL1	3003	4(h)	$V_{IN} \text{ (Under Test)} = \text{Pulse}$ Generator $V_{IN} \text{ (Remaining Inputs)} =$ Figure 3(b) $V_{DD} = 4.5\text{V}, V_{SS} = 0\text{V}$ Note 5 $\frac{\text{Pins D/F}}{2 \text{ to } 4} = \frac{\text{Pins C}}{3 \text{ to } 5}$ 3 to 4 4 to 5	-	6.5	ns
116	Propagation Delay Low to High 2 (Ā/B to Y)	tplH2	3003	4(h)	$ \begin{array}{l} V_{IN} \mbox{ (Under Test) = Pulse} \\ \mbox{ Generator} \\ V_{IN} \mbox{ (Remaining Inputs) =} \\ \mbox{ Figure 3(b)} \\ V_{DD} = 4.5V, \mbox{ V}_{SS} = 0V \\ \mbox{ Note 5} \\ \hline \\ $	-	9.0	ns
117	Propagation Delay High to Low 2 (Ā/B to Y)	tphl2	3003	4(h)	$V_{IN} \text{ (Under Test) = Pulse}$ Generator $V_{IN} \text{ (Remaining Inputs) =}$ Figure 3(b) $V_{DD} = 4.5V, V_{SS} = 0V$ Note 5 $\frac{Pins D/F}{1 \text{ to } 4} = \frac{Pins C}{2 \text{ to } 5}$	-	9.0	ns



### TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

		SYMBOL	TEST METHOD	TEST	TEST CONDITIONS (PINS UNDER TEST	LIM	ITS	UNIT
No.	CHARACTERISTICS	STMBUL	MIL-STD 883	FIG.	D/F = DIP AND FP C = CCP)	MIN	MAX	UNIT
118	Propagation Delay Low to High 2 (G to Y)	t <sub>PLH3</sub>	3003	4(h)	$V_{IN} \text{ (Under Test)} = \text{Pulse}$ Generator $V_{IN} \text{ (Remaining Inputs)} =$ Figure 3(b) $V_{DD} = 4.5\text{V}, V_{SS} = 0\text{V}$ Note 5 $\frac{\text{Pins D/F}}{15 \text{ to } 12}  \frac{\text{Pins C}}{19 \text{ to } 15}$	-	9.5	ns
119	Propagation Delay High to Low 2 (G to Y)	t₽HL3	3003	4(h)	$V_{IN} \text{ (Under Test)} = \text{Pulse} \\ \text{Generator} \\ V_{IN} \text{ (Remaining Inputs)} = \\ \text{Figure 3(b)} \\ V_{DD} = 4.5 \text{V}, V_{SS} = 0 \text{V} \\ \text{Note 5} \\ \underline{\frac{\text{Pins D/F}}{15 \text{ to 12}}}  \underline{\frac{\text{Pins C}}{19 \text{ to 15}}} \\ \end{array}$	-	8.5	ns
120	Ground Bounce Output Low (High to Low)	V <sub>OLP(H-L)</sub>	-	4(i)	$V_{IN}(\overline{A}/B,4B,\overline{G}) = 1.0V$ $V_{IN}(4A) = 4.0V$ $V_{IN} (Remaining Inputs) =$ Pulse Generator $V_{DD} = 5.5V, V_{SS} = 0V$ Note 6 (Pin D/F 12) (Pin C 15)	-	2.0	V
121	Ground Bounce Output Low (Low to High)	V <sub>OLP(L-H)</sub>	-	4(i)	$V_{IN}(\overline{A}/B,4B,\overline{G}) = 1.0V$ $V_{IN}(4A) = 4.0V$ $V_{IN} (Remaining Inputs) =$ Pulse Generator $V_{DD} = 5.5V, V_{SS} = 0V$ Note 6 (Pin D/F 12) (Pin C 15)	-	1.5	V
122	Ground Bounce Output High (High to Low)	V <sub>OHV(H-L)</sub>	-	4(i)	$V_{IN}(\overline{A}/B,4A,4B,\overline{G}) = 1.0V$ $V_{IN} (Remaining Inputs) =$ Pulse Generator $V_{DD} = 5.5V, V_{SS} = 0V$ Note 6 (Pin D/F 12) (Pin C 15)	-	1.5	V



### TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No		STICS SYMBOL	TEST METHOD		TEST CONDITIONS (PINS UNDER TEST	LIM	ITS	UNIT
No. CHARACTERISTICS	STIVIDUL	MIL-STD 883	FIG.	D/F = DIP AND FP C = CCP)	MIN	MAX	UNIT	
123	Ground Bounce Output High (Low to High)	V <sub>OHV(L-H)</sub>	-	4(i)	$V_{IN}(\overline{A}/B,4A,4B,\overline{G}) = 1.0V$ $V_{IN} (Remaining Inputs) =$ Pulse Generator $V_{DD} = 5.5V, V_{SS} = 0V$ Note 6 (Pin D/F 12) (Pin C 15)	·	2.0	V



# TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE

			TEST METHOD	TEST	TEST CONDITIONS (PINS UNDER TEST	LIM	ITS	UNIT
No.	CHARACTERISTICS	SYMBOL	MIL-STD 883	FIG.	D/F = DIP AND FP C = CCP)	MIN	MAX	UNIT
1	Functional Test 1	-	-	3(b)	Verify Truth Table with Load. $V_{IL} = 0.45V$ , $V_{IH} = 2.5V$ $I_{OL} = 1.0mA$ , $I_{OH} = -1.0mA$ $V_{DD} = 3.0V$ , $V_{SS} = 0V$ $t_r = t_f < 100ns$ f = 10kHz (min) Note 1	-	-	-
2	Functional Test 2	-	-	3(b)	Verify Truth Table with Load. $V_{IL} = 0.6V$ , $V_{IH} = 3.7V$ $I_{OL} = 1.0mA$ , $I_{OH} = -1.0mA$ $V_{DD} = 4.5V$ , $V_{SS} = 0V$ $t_r = t_f < 50ns$ f = 10kHz (min) Note 1	-	-	-
3	Functional Test 3	-	-	3(b)	Verify Truth Table with Load. $V_{IL} = 1.0V, V_{IH} = 4.5V$ $I_{OL} = 1.0mA, I_{OH} = -1.0mA$ $V_{DD} = 5.5V, V_{SS} = 0V$ $t_r = t_f < 50ns$ f = 10kHz (min) Note 1	-	-	-
4 to 5	Quiescent Current	IDD	3005	4(a)	$V_{IL} = 0V, V_{IH} = 5.5V$ $V_{DD} = 5.5V, V_{SS} = 0V$ All Outputs Open Note 2 (Pin D/F 16) (Pin C 20)		20	μА
6 to 15	Input Current Low Level	ΙιL	3009	4(b)	$V_{IN} \text{ (Under Test) = 0V} \\ V_{IN} \text{ (Remaining Inputs) = 5.5V} \\ V_{DD} = 5.5V, V_{SS} = 0V \\ \text{(Pins D/F 1-2-3-5-6-10-11-13-14-15)} \\ \text{(Pins C 2-3-4-7-8-13-14-17-18-19)} \\ \end{array}$	-	- 1.0	μА
16 to 25	Input Current High Level	l <sub>iH</sub>	3010	4(c)	$V_{IN} \text{ (Under Test)} = 5.5V$ $V_{IN} \text{ (Remaining Inputs)} = 0V$ $V_{DD} = 5.5V, V_{SS} = 0V$ (Pins D/F 1-2-3-5-6-10-11-13- 14-15) (Pins C 2-3-4-7-8-13-14-17- 18-19)	-	1.0	μA



### TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD	TEST	TEST CONDITIONS (PINS UNDER TEST	LIM	ITS	UNIT
NO.	CHARACTERIS 103	STNIBUL	MIL-STD 883	FIG.	D/F = DIP AND FP C = CCP)	MIN	MAX	UNIT
26 to 29	Output Voltage Low Level 1	V <sub>OL1</sub>	3007	4(d)	$V_{IL} = 0.9V, V_{IH} = 2.1V$ $I_{OL} = 50\mu A$ $V_{DD} = 3.0V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	F	0.1	V
30 to 33	Output Voltage Low Level 2	V <sub>OL2</sub>	3007	4(d)	$V_{IL} = 1.35V, V_{IH} = 3.15V$ $I_{OL} = 50\mu A$ $V_{DD} = 4.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	-	0.1	V
34 to 37	Output Voltage Low Level 3	V <sub>OL3</sub>	3007	4(d)	$V_{IL} = 1.65V, V_{IH} = 3.85V$ $I_{OL} = 50\mu A$ $V_{DD} = 5.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	-	0.1	V
38 to 41	Output Voltage Low Level 4	V <sub>OL4</sub>	3007	4(d)	$V_{IL} = 0.9V, V_{IH} = 2.1V$ $I_{OL} = 12mA$ $V_{DD} = 3.0V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	-	0.5	V
42 to 45	Output Voltage Low Level 5	V <sub>OL5</sub>	3007	4(d)	$V_{IL} = 1.35V, V_{IH} = 3.15V$ $I_{OL} = 24mA$ $V_{DD} = 4.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	-	0.5	V
46 to 49	Output Voltage Low Level 6	V <sub>OL6</sub>	3007	4(d)	$V_{IL} = 1.65V, V_{IH} = 3.85V$ $I_{OL} = 24mA$ $V_{DD} = 5.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	-	0.5	V
50 to 53	Output Voltage Low Level 7	V <sub>OL7</sub>	3007	4(d)	$V_{IL} = 1.65V, V_{IH} = 3.85V$ $I_{OL} = 50mA$ $V_{DD} = 5.5V, V_{SS} = 0V$ Note 3 (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	-	1.65	V



# TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE (CONT'D)

		SYMPOL	TEST METHOD	TEST	TEST CONDITIONS (PINS UNDER TEST	LIM	ITS	UNIT
No.	CHARACTERISTICS	SYMBOL	MIL-STD 883	FIG.	D/F = DIP AND FP C = CCP)	MIN	MAX	UNIT
54 to 57	Output Voltage High Level 1	V <sub>OH1</sub>	3006	4(e)	$V_{IL} = 0.9V, V_{IH} = 2.1V$ $I_{OH} = -50\mu A$ $V_{DD} = 3.0V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	2.9	-	V
58 to 61	Output Voltage High Level 2	V <sub>OH2</sub>	3006	4(e)	$V_{IL} = 1.35V, V_{IH} = 3.15V$ $I_{OH} = -50\mu A$ $V_{DD} = 4.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	4.4	-	V
62 to 65	Output Voltage High Level 3	V <sub>OH3</sub>	3006	4(e)	$V_{IL} = 1.65V, V_{IH} = 3.85V$ $I_{OH} = -50\mu A$ $V_{DD} = 5.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	5.4	-	V
66 to 69	Output Voltage High Level 4	V <sub>OH4</sub>	3006	4(e)	$V_{IL} = 0.9V, V_{IH} = 2.1V$ $I_{OH} = -4.0mA$ $V_{DD} = 3.0V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	2.4	-	V
70 to 73	Output Voltage High Level 5	V <sub>OH5</sub>	3006	4(e)	$V_{IL} = 1.35V, V_{IH} = 3.15V$ $I_{OH} = -24mA$ $V_{DD} = 4.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	3.7	-	V
74 to 77	Output Voltage High Level 6	V <sub>OH6</sub>	3006	4(e)	$V_{IL} = 1.65V, V_{IH} = 3.85V$ $I_{OH} = -24mA$ $V_{DD} = 5.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	4.7	-	V
78 to 81	Output Voltage High Level 7	V <sub>OH7</sub>	3006	4(e)	$V_{IL} = 1.65V, V_{IH} = 3.85V$ $I_{OH} = -50mA$ $V_{DD} = 5.5V, V_{SS} = 0V$ Note 3 (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	3.85	-	V



# TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE (CONT'D)

			TEST METHOD	test Fig.	TEST CONDITIONS (PINS UNDER TEST	LIM	ITS	UNIT
No.	CHARACTERISTICS	SYMBOL	MIL-STD 883		D/F = DIP AND FP C = CCP)	MIN	MAX	UNIT
82 to 91	Input Clamp Voltage (to V <sub>SS</sub> )	V <sub>IC1</sub>	3022	4(f)	$\begin{split} &I_{IN} \text{ (Under Test)} = -1.0\text{mA} \\ &V_{DD} = \text{Open}, V_{SS} = 0\text{V} \\ &\text{All Other Pins Open} \\ &(\text{Pins D/F } 1\text{-}2\text{-}3\text{-}5\text{-}6\text{-}10\text{-}11\text{-}13\text{-}14\text{-}15)} \\ &(\text{Pins C } 2\text{-}3\text{-}4\text{-}7\text{-}8\text{-}13\text{-}14\text{-}17\text{-}18\text{-}19) \end{split}$	- 0.1	- 1.5	V
92 to 101	Input Clamp Voltage (to V <sub>DD</sub> )	V <sub>IC2</sub>	3022	4(f)	$\begin{split} &I_{IN} \text{ (Under Test)} = 1.0\text{mA} \\ &V_{DD} = 0\text{V}, \ V_{SS} = \text{Open} \\ &\text{All Other Pins Open} \\ &(\text{Pins D/F 1-2-3-5-6-10-11-13-14-15}) \\ &(\text{Pins C 2-3-4-7-8-13-14-17-18-19}) \end{split}$	0.1	1.5	V



### TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE

			TEST METHOD	TEST	TEST CONDITIONS (PINS UNDER TEST	LIM	ITS	
No.	CHARACTERISTICS	SYMBOL	MIL-STD 883	FIG.	D/F = DIP AND FP C = CCP)	MIN	MAX	UNIT
1	Functional Test 1	•	-	3(b)	Verify Truth Table with Load. $V_{IL} = 0.45V$ , $V_{IH} = 2.5V$ $I_{OL} = 1.0mA$ , $I_{OH} = -1.0mA$ $V_{DD} = 3.0V$ , $V_{SS} = 0V$ $t_r = t_f < 100ns$ f = 10kHz (min) Note 1	-	-	-
2	Functional Test 2	-	-	3(b)	Verify Truth Table with Load. $V_{IL} = 0.6V$ , $V_{IH} = 3.7V$ $I_{OL} = 1.0mA$ , $I_{OH} = -1.0mA$ $V_{DD} = 4.5V$ , $V_{SS} = 0V$ $t_r = t_f < 50ns$ f = 10kHz (min) Note 1	_	-	-
3	Functional Test 3	-	-	3(b)	Verify Truth Table with Load. $V_{IL} = 1.0V$ , $V_{IH} = 4.5V$ $I_{OL} = 1.0mA$ , $I_{OH} = -1.0mA$ $V_{DD} = 5.5V$ , $V_{SS} = 0V$ $t_r = t_f < 50ns$ f = 10kHz (min) Note 1	-	-	-
4 to 5	Quiescent Current	IDD	3005	4(a)	$V_{IL} = 0V, V_{IH} = 5.5V$ $V_{DD} = 5.5V, V_{SS} = 0V$ All Outputs Open Note 2 (Pin D/F 16) (Pin C 20)	-	1.0	μА
6 to 15	Input Current Low Level	Ι <sub>ΙL</sub>	3009	4(b)	$V_{IN} \text{ (Under Test)} = 0V$ $V_{IN} \text{ (Remaining Inputs)} = 5.5V$ $V_{DD} = 5.5V, V_{SS} = 0V$ (Pins D/F 1-2-3-5-6-10-11-13- 14-15) (Pins C 2-3-4-7-8-13-14-17- 18-19)	-	- 100	nA
16 to 25	Input Current High Level	I <sub>IH</sub>	3010	4(c)	$V_{IN} \text{ (Under Test)} = 5.5V$ $V_{IN} \text{ (Remaining Inputs)} = 0V$ $V_{DD} = 5.5V, V_{SS} = 0V$ (Pins D/F 1-2-3-5-6-10-11-13- 14-15) (Pins C 2-3-4-7-8-13-14-17- 18-19)	-	100	nA



# TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE (CONT'D)

No	CHARACTERISTICS	SYMBOL	TEST METHOD	TEST	TEST CONDITIONS (PINS UNDER TEST	LIM	ITS	UNIT
No.	CHARACTERISTICS	STNDUL	MIL-STD 883	FIG.	D/F = DIP AND FP C = CCP)	MIN	MAX	UNIT
26 to 29	Output Voltage Low Level 1	V <sub>OL1</sub>	3007	4(d)	$V_{IL} = 0.9V, V_{IH} = 2.1V$ $I_{OL} = 50\mu A$ $V_{DD} = 3.0V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	-	0.1	V
30 to 33	Output Voltage Low Level 2	V <sub>OL2</sub>	3007	4(d)	$V_{IL} = 1.35V, V_{IH} = 3.15V$ $I_{OL} = 50\mu A$ $V_{DD} = 4.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)		0.1	V
34 to 37	Output Voltage Low Level 3	V <sub>OL3</sub>	3007	4(d)	$V_{IL} = 1.65V, V_{IH} = 3.85V$ $I_{OL} = 50\mu A$ $V_{DD} = 5.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	-	0.1	V
38 to 41	Output Voltage Low Level 4	V <sub>OL4</sub>	3007	4(d)	$V_{IL} = 0.9V, V_{IH} = 2.1V$ $I_{OL} = 12mA$ $V_{DD} = 3.0V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	-	0.4	V
42 to 45	Output Voltage Low Level 5	V <sub>OL5</sub>	3007	4(d)	$V_{IL} = 1.35V, V_{IH} = 3.15V$ $I_{OL} = 24mA$ $V_{DD} = 4.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	-	0.4	V
46 to 49	Output Voltage Low Level 6	V <sub>OL6</sub>	3007	4(d)	$V_{IL} = 1.65V, V_{IH} = 3.85V$ $I_{OL} = 24mA$ $V_{DD} = 5.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	-	0.4	V
50 to 53	Output Voltage Low Level 7	V <sub>OL7</sub>	3007	4(d)	$V_{IL} = 1.65V, V_{IH} = 3.85V$ $I_{OL} = 50mA$ $V_{DD} = 5.5V, V_{SS} = 0V$ Note 3 (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	-	1.65	V



# TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE (CONT'D)

	CHARACTERISTICS		TEST METHOD	TEST	TEST CONDITIONS (PINS UNDER TEST	LIM	ITS	UNIT
No.	CHARACTERISTICS	SYMBOL	MIL-STD 883	FIG.	D/F = DIP AND FP C = CCP)	MIN	MAX	UNIT
54 to 57	Output Voltage High Level 1	V <sub>OH1</sub>	3006	4(e)	$V_{IL} = 0.9V, V_{IH} = 2.1V$ $I_{OH} = -50\mu A$ $V_{DD} = 3.0V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	2.9	-	V
58 to 61	Output Voltage High Level 2	V <sub>OH2</sub>	3006	4(e)	$V_{IL} = 1.35V, V_{IH} = 3.15V$ $I_{OH} = -50\mu A$ $V_{DD} = 4.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	4.4	-	V
62 to 65	Output Voltage High Level 3	V <sub>OH3</sub>	3006	4(e)	$V_{IL} = 1.65V, V_{IH} = 3.85V$ $I_{OH} = -50\mu A$ $V_{DD} = 5.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	5.4	-	V
66 to 69	Output Voltage High Level 4	V <sub>OH4</sub>	3006	4(e)	$V_{IL} = 0.9V, V_{IH} = 2.1V$ $I_{OH} = -4.0mA$ $V_{DD} = 3.0V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	2.4	-	V
70 to 73	Output Voltage High Level 5	V <sub>OH5</sub>	3006	4(e)	$V_{IL} = 1.35V, V_{IH} = 3.15V$ $I_{OH} = -24mA$ $V_{DD} = 4.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	3.7	1	V
74 to 77	Output Voltage High Level 6	V <sub>OH6</sub>	3006	4(e)	$V_{IL} = 1.65V, V_{IH} = 3.85V$ $I_{OH} = -24mA$ $V_{DD} = 5.5V, V_{SS} = 0V$ (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	4.7	-	V
78 to 81	Output Voltage High Level 7	V <sub>OH7</sub>	3006	4(e)	$V_{IL} = 1.65V, V_{IH} = 3.85V$ $I_{OH} = -50mA$ $V_{DD} = 5.5V, V_{SS} = 0V$ Note 3 (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	3.85		V

NOTES: See Page 20.

.



# TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE (CONT'D)

No. CHARACTERISTICS	SYMBOL	TEST METHOD	TEST	TEST CONDITIONS (PINS UNDER TEST	LIM	ITS	UNIT	
NO.	CHARACTERISTICS	STNBUL	MIL-STD 883	FIG.	D/F = DIP AND FP C = CCP)	MIN	MAX	UNIT
82 to 91	Input Clamp Voltage (to V <sub>SS</sub> )	V <sub>IC1</sub>	3022	4(f)	$\begin{split} &I_{IN} \text{ (Under Test)} = -1.0\text{mA} \\ &V_{DD} = \text{Open}, \ &V_{SS} = 0\text{V} \\ &\text{All Other Pins Open} \\ &(\text{Pins D/F 1-2-3-5-6-10-11-13-14-15}) \\ &(\text{Pins C 2-3-4-7-8-13-14-17-18-19}) \end{split}$	- 0.1	- 1.5	V
92 to 101	Input Clamp Voltage (to V <sub>DD</sub> )	V <sub>IC2</sub>	3022	4(f)	$\begin{split} &I_{IN} \text{ (Under Test)} = 1.0\text{mA} \\ &V_{DD} = 0\text{V}, \ V_{SS} = \text{Open} \\ &All \ Other \ Pins \ Open \\ &(\text{Pins D/F } 1\text{-}2\text{-}3\text{-}5\text{-}6\text{-}10\text{-}11\text{-}13\text{-}14\text{-}15) \\ &(\text{Pins C } 2\text{-}3\text{-}4\text{-}7\text{-}8\text{-}13\text{-}14\text{-}17\text{-}18\text{-}19) \end{split}$	0.1	1.5	V



#### FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

### FIGURE 4(a) - QUIESCENT CURRENT TEST TABLE

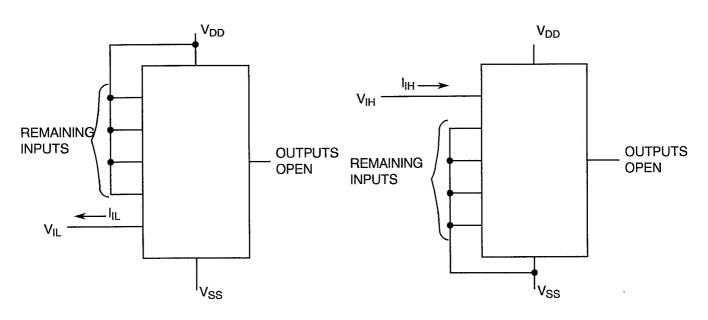
		INPUTS								OUTPUTS	PACKAGE	AGE D.C. SUPP			
	PATTERN NO.	1 2	2 3	3 4	5 7	6 8	10 13	11 14	13 17	14 18	15 19	4 7 9 12 5 9 12 15	DIL, FP CCP	8 10	16 20
ſ	1	1	1	1	1	1	1	1	1	1	0	OPEN		V <sub>SS</sub>	V <sub>DD</sub>
	2	0	0	0	0	0	0	0	0	0	0	OPEN		$\downarrow$	$\downarrow$

#### **NOTES**

- 1. Figure 4(a) illustrates one series of test patterns. Any other pattern series must be agreed with the Qualifying Space Agency and shall be included as an Appendix.
- Qualifying Space Agency and shall be included as an Appendix. 2. Logic Level Definitions:  $1 = V_{IH} = V_{DD}$ ,  $0 = V_{IL} = V_{SS}$ .

FIGURE 4(b) - INPUT CURRENT LOW LEVEL

FIGURE 4(c) - INPUT CURRENT HIGH LEVEL

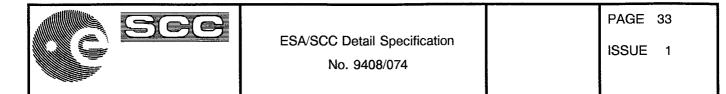


#### **NOTES**

1. Each input to be tested separately

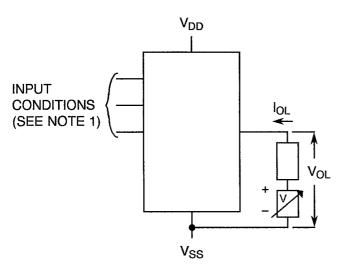
#### **NOTES**

1. Each input to be tested separately



### FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

#### FIGURE 4(d) - OUTPUT VOLTAGE LOW LEVEL



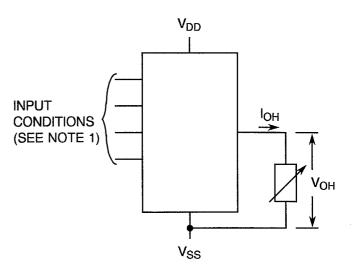
#### NOTES

1. V<sub>IN</sub> = V<sub>IL</sub> (max.) and/or V<sub>IH</sub> (min.) as per Truth Table to give V<sub>OL</sub>.

FIGURE 4(f) - INPUT CLAMP VOLTAGE

2. Each output to be tested separately.

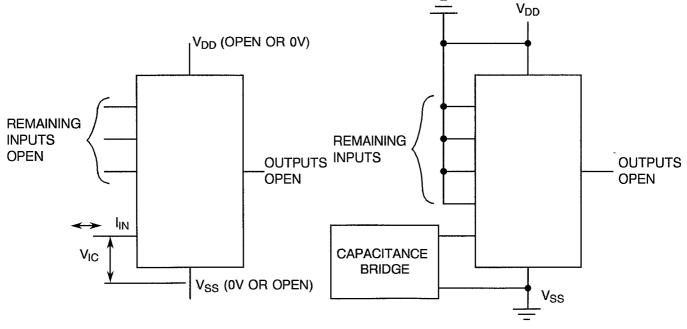
#### FIGURE 4(e) - OUTPUT VOLTAGE HIGH LEVEL



#### NOTES

- V<sub>IN</sub> = V<sub>IL</sub> (max.) and/or V<sub>IH</sub> (min.) as per Truth Table to give V<sub>OH</sub>.
- 2. Each output to be tested separately.

#### FIGURE 4(g) - INPUT CAPACITANCE



#### **NOTES**

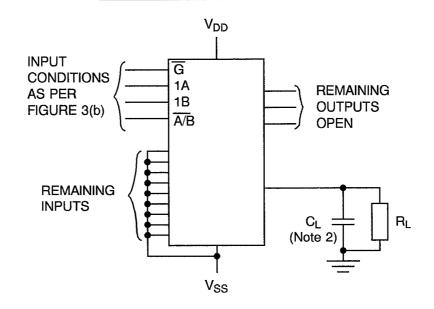
1. Each input to be tested separately.

- 1. Each input to be tested separately.
- 2. f = 100kHz to 1MHz.

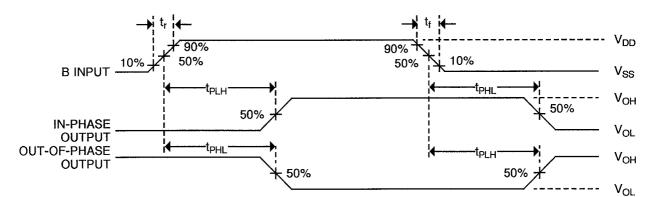


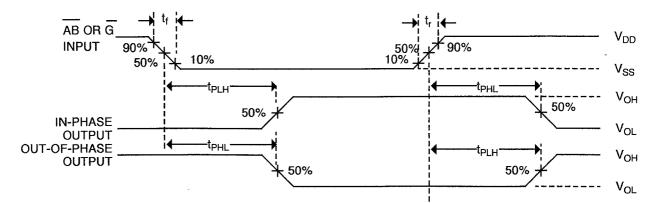
#### FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

#### FIGURE 4(h) - PROPAGATION DELAY

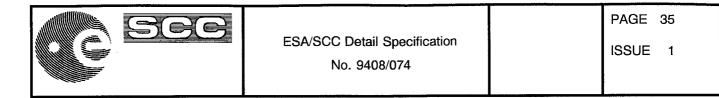


#### VOLTAGE WAVEFORMS



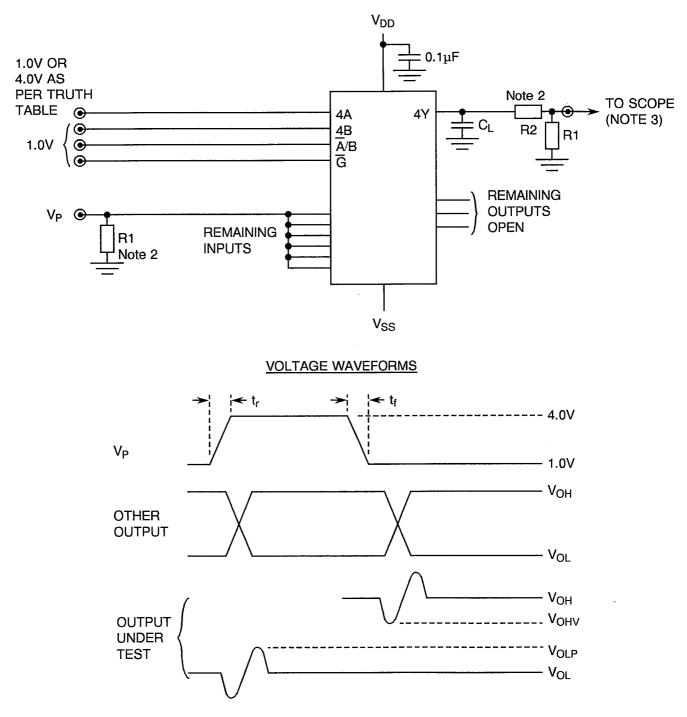


- 1. Pulse Generator V<sub>P</sub> = 0V to V<sub>DD</sub>, t<sub>r</sub> and t<sub>f</sub> ≤ 6ns, f = 1.0MHz minimum, 50% Duty Cycle, Z<sub>OUT</sub> = 50 $\Omega$ .
- 2.  $C_L = 50 pF \pm 5\%$  including scope, wiring and stray capacitance without package in test fixture,  $R_L = 500\Omega \pm 5\%$ .



#### FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

#### FIGURE 4(i) - GROUND BOUNCE



- 1. Pulse Generator  $V_P$  = 1.0V to 4.0V, t<sub>r</sub> and t<sub>f</sub> ≤ 6.0ns, f = 1.0MHz, 50% Duty Cycle, Z<sub>OUT</sub> = 50Ω.
- 2.  $C_L = 50 pF \pm 5\%$ ,  $R1 = 51\Omega \pm 5\%$ ,  $R2 = 450\Omega \pm 5\%$ .
- 3. Oscilloscope  $Z_{IN} = 50\Omega$ , Bandwidth  $\ge 1.0$ GHz with memory capability.



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### TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
4 to 5	Quiescent Current	I <sub>DD</sub>	As per Table 2	As per Table 2	± 300	nA
6 to 15	Input Current Low Level	lιL	As per Table 2	As per Table 2	±20	nA
16 to 25	Input Current High Level	ĥн	As per Table 2	As per Table 2	±20	nA ,
46 to 49	Output Voltage Low Level 6	V <sub>OL6</sub>	As per Table 2	As per Table 2	±0.04	V
74 to 77	Output Voltage High Level 6	V <sub>OH6</sub>	As per Table 2	As per Table 2	±0.2	V



# TABLE 5(a) - CONDITIONS FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, N-CHANNELS

NO.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T <sub>amb</sub>	+ 125( + 0-5)	°C
2	Outputs - (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	V <sub>OUT</sub>	-	
3	Inputs - (Pins D/F 1-2-3-5-6-10-11-13-14-15) (Pins C 2-3-4-7-8-13-14-17-18-19)	V <sub>IN</sub>	V <sub>SS</sub>	V
4	Positive Supply Voltage (Pin D/F 16) (Pin C 20)	V <sub>DD</sub>	5.5( + 0-0.5)	V
5	Negative Supply Voltage (Pin D/F 8) (Pin C 10)	V <sub>SS</sub>	0	V
6	Duration	t	72	Hours

### **NOTES**

- 1. Input Protection Resistor =  $R1 = 1.0k\Omega$ .
- 2. Output Load =  $R2 = 10k\Omega$ .

### TABLE 5(b) - CONDITIONS FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, P-CHANNELS

NO.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T <sub>amb</sub>	+ 125( + 0-5)	°C
2	Outputs - (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	V <sub>OUT</sub>	Open	-
3	Inputs - (Pins D/F 1-2-3-5-6-10-11-13-14-15) (Pins C 2-3-4-7-8-13-14-17-18-19)	V <sub>IN</sub>	V <sub>DD</sub>	V
4	Positive Supply Voltage (Pin D/F 16) (Pin C 20)	V <sub>DD</sub>	5.5( + 0-0.5)	. V
5	Negative Supply Voltage (Pin D/F 8) (Pin C 10)	V <sub>SS</sub>	0	V
6	Duration	t	72	Hours

- 1. Input Protection Resistor = R1 =  $1.0k\Omega$ .
- 2. Output Load =  $R2 = 10k\Omega$ .



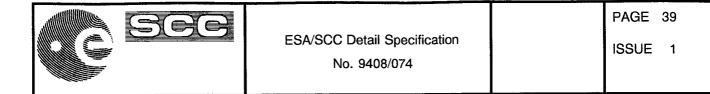
ISSUE 1

# TABLE 5(c) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

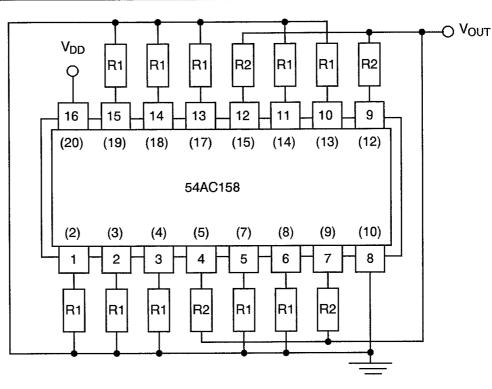
No.	CHARACTERISTICS	SYMBOL	CONDITIONS	UNIT
1	Ambient Temperature	T <sub>amb</sub>	+ 125( + 0 - 5)	°C
2	Outputs - (Pins D/F 4-7-9-12) (Pins C 5-9-12-15)	V <sub>OUT</sub>	V <sub>DD</sub> /2	V
3	Inputs - (Pins D/F 1-2-5-11-14) (Pins C 2-3-7-14-18)	V <sub>IN</sub>	V <sub>DD</sub>	V
4	Inputs - (Pins D/F 3-6-10-13) (Pins C 4-8-13-17)	V <sub>IN</sub>	V <sub>GEN</sub>	Vac
5	Input - (Pin D/F 15) (Pin C 19)	V <sub>IN</sub>	V <sub>SS</sub>	V
6	Pulse Voltage	V <sub>GEN</sub>	0V to V <sub>DD</sub>	Vac
7	Pulse Frequency Square Wave	f	100k ± 10% 50 ± 15% Duty Cycle t <sub>r</sub> = t <sub>f</sub> < 100ns	Hz
8	Positive Supply Voltage (Pin D/F 16) (Pin C 20)	V <sub>DD</sub>	5.5( + 0 - 0.5)	V
9	Negative Supply Voltage (Pin D/F 16) (Pin C 20)	V <sub>SS</sub>	0	V

### NOTES

1. Input Protection Resistor = Output Load =  $220\Omega$ .



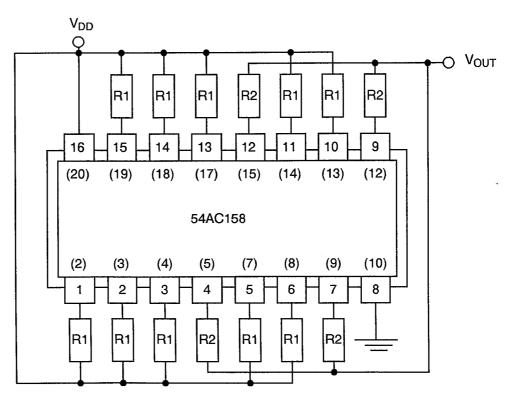
#### FIGURE 5(a) - ELECTRICAL CIRCUIT FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, N-CHANNELS



#### **NOTES**

1. Pin numbers in parenthesis are for the chip carrier package.

### FIGURE 5(b) - ELECTRICAL CIRCUIT FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, P-CHANNELS

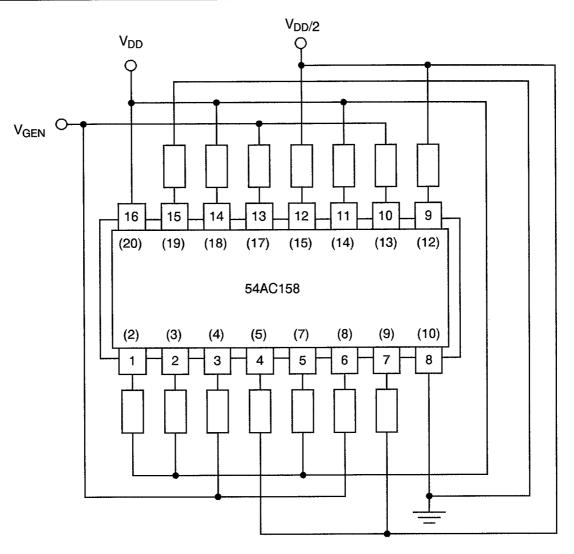


#### NOTES

1. Pin numbers in parenthesis are for the chip carrier package.



### FIGURE 5(c) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



#### NOTES

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1. Pin numbers in parenthesis are for the chip carrier package.



#### 4.8 <u>ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC</u> SPECIFICATION NO. 9000)

#### 4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at  $T_{amb} = +22 \pm 3$  °C.

#### 4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at  $T_{amb}I = +22 \pm 3$  °C.

#### 4.8.3 <u>Electrical Measurements on Completion of Endurance Tests</u>

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at  $T_{amb} = +22 \pm 3$  °C.

#### 4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(c) of this specification.

#### 4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(c) of this specification.

#### 4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

#### 4.9 TOTAL DOSE IRRADIATION TESTING

#### 4.9.1 Application

If specified in Para. 4.2.1 of this specification, total dose irradiation testing shall be performed in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

#### 4.9.2 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6 of this specification.

#### 4.9.3 Electrical Measurements

The parameters to be measured prior to irradiation exposure are scheduled in Table 2 of this specification. Only devices which meet the requirements of Table 2 shall be included in the test sample.

The parameters to be measured during and on completion of irradiation testing are scheduled in Table 7 of this specification.



### TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

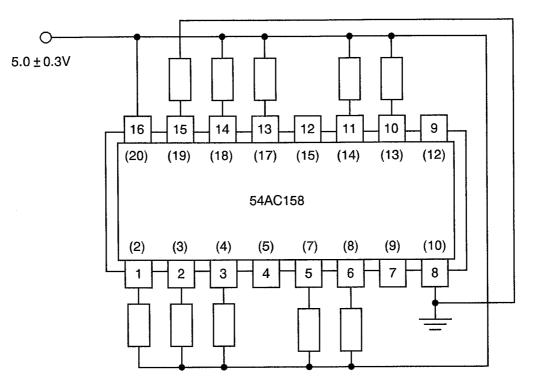
Nia	CHARACTERISTICS	SYMBOL	SPEC. AND/OR	TEST	CHANGE LIMITS	ABSO	LUTE	UNIT
No.	CHARACTERISTICS	STNDUL	TEST METHOD	CONDITIONS	(Δ) (NOTE 1)	MIN	MAX	UNIT
1	Functional Test 1	-	As per Table 2	As per Table 2	-	-	-	-
2	Functional Test 2	-	As per Table 2	As per Table 2	-	-	-	-
3	Functional Test 3	-	As per Table 2	As per Table 2	-	-	-	-
4 to 5	Quiescent Current	I <sub>DD</sub>	As per Table 2	As per Table 2	±0.3	-	1.0	μA
6 to 15	Input Current Low Level	IIL	As per Table 2	As per Table 2	±20	-	- 100	nA
16 to 25	Input Current High Level	lιH	As per Table 2	As per Table 2	±20	-	100	nA
38 to 41	Output Voltage Low Level 4	V <sub>OL4</sub>	As per Table 2	As per Table 2	±0.04	-	0.4	V
46 to 49	Output Voltage Low Level 6	V <sub>OL6</sub>	As per Table 2	As per Table 2	±0.04	-	0.4	V
66 to 69	Output Voltage High Level 4	V <sub>OH4</sub>	As per Table 2	As per Table 2	±0.2	2.4	-	V
74 to 77	Output Voltage High Level 6	V <sub>OH6</sub>	As per Table 2	As per Table 2	±0.2	4.7	-	V

#### **NOTES**

1. The change limits  $\Delta$  are applicable to the Operating Life test only. The change in parameters between initial and end point measurements shall not exceed the limits given. In addition, the absolute limits shall not be exceeded.



### FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING



### <u>NOTES</u>

- 1. Pin numbers in parenthesis are for the chip carrier package.
- 2. Input Protection Resistor =  $1.0k\Omega$ .

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON	
COMPLETION OF IRRADIATION TESTING	

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	ABSOLUTE		UNIT
						MIN	MAX	UNIT
1	Functional Test 1	_	As per Table 2	As per Table 2	-	-	-	-
2	Functional Test 2	-	As per Table 2	As per Table 2	-	-	-	-
3	Functional Test 3	-	As per Table 2	As per Table 2	-	-	-	-
4 to 5	Quiescent Current	I <sub>DD</sub>	As per Table 2	As per Table 2	-	-	100	μA



### APPENDIX 'A'

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### AGREED DEVIATIONS FOR MOTOROLA (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS							
Para. 4.2.1(a)	Para. 5.2.2, Total Dose Irradiation Testing: Shall not be performed during qualification and maintenance of qualification.							