INTEGRATED CIRCUITS, SILICON MONOLITHIC,

BIPOLAR OPERATIONAL AMPLIFIERS,

BASED ON TYPE OP400A

ESCC Detail Specification No. 9101/033

ISSUE 1

October 2002

Document Custodian: European Space Agency - see https://escies.org

LEGAL DISCLAIMER AND COPYRIGHT

european space agency
agence spatiale européenne

Pages 1 to 28

INTEGRATED CIRCUITS, SILICON MONOLITHIC,

BIPOLAR OPERATIONAL AMPLIFIERS,

BASED ON TYPE OP400A

ESA/SCC Detail Specification No. 9101/033

space components
coordination group

Issue/Rev.	Date	Approved by	
		SCCG Chairman	ESA Director General or his Deputy
Issue 1	June 1994		
Revision 'A'	December 1994		
Revision 'B'	May 1997		

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.
'A'	Dec. '94	P1. Cover Page		None
		P2. DCN		None
		P6. Table 1(b)	: In Note 1 second sentence, '<' corrected to '>'	23688

TABLE OF CONTENTS

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, quad low offset, low power, operational amplifier, based on Type OP400A. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The parameter derating information of the integrated circuits specified herein is shown in Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the integrated circuits specified herein are shown in Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE (FIGURE 3(b))

Not applicable.

1.8 CIRCUIT SCHEMATIC

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 with a Minimum Critical Path Failure Voltage of 1000 Volts.

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
01	D.I.L.	2(a)	G4
02	CHIP CARRIER	2(b)	7

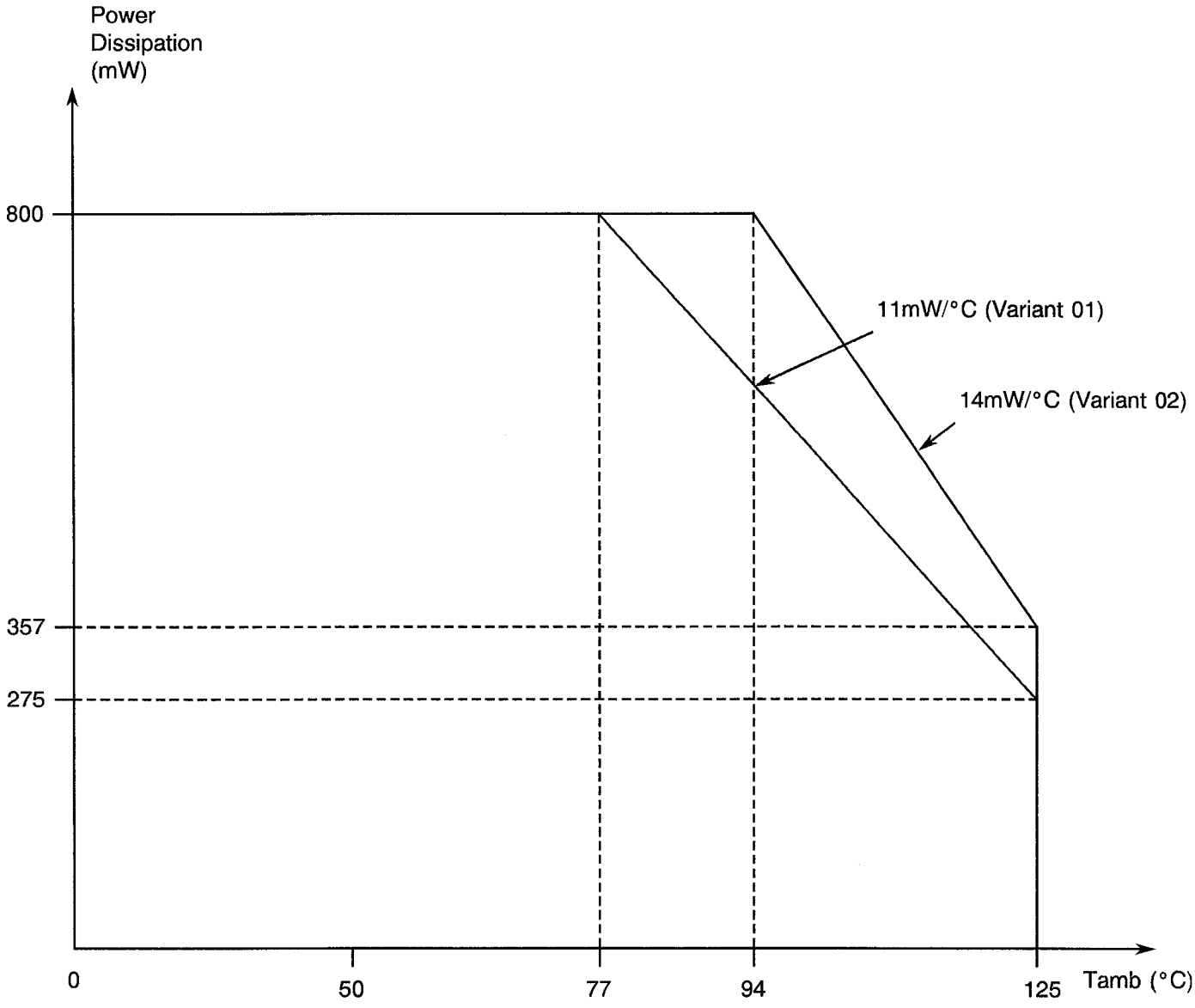
TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage Range	V_{CC}	±20	V	-
2	Differential Input Voltage Range	V_{ID}	±30	V	-
3	Input Voltage Range	V_{IN}	±20	V	-
4	Device Power Dissipation (Continuous)	P_D	800	mW	Note 1
5	Operating Temperature Range	T_{op}	−55 to +125	°C	-
6	Storage Temperature Range	T_{stg}	−65 to +150	°C	-
7	Soldering Temperature For DIP For CCP	T_{sol}	 +265 +245	°C	 Note 2 Note 3
8	Junction Temperature	T_J	+150	°C	-
9	Thermal Resistance For DIP For CCP	$R_{TH(J-C)}$	 29 35	°C/W	-

NOTES

1. At T_{amb} = +77°C for Variant 01 and +94°C for Variant 02. For derating at T_{amb} > +77°C and +94°C, see Figure 1.
2. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
3. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

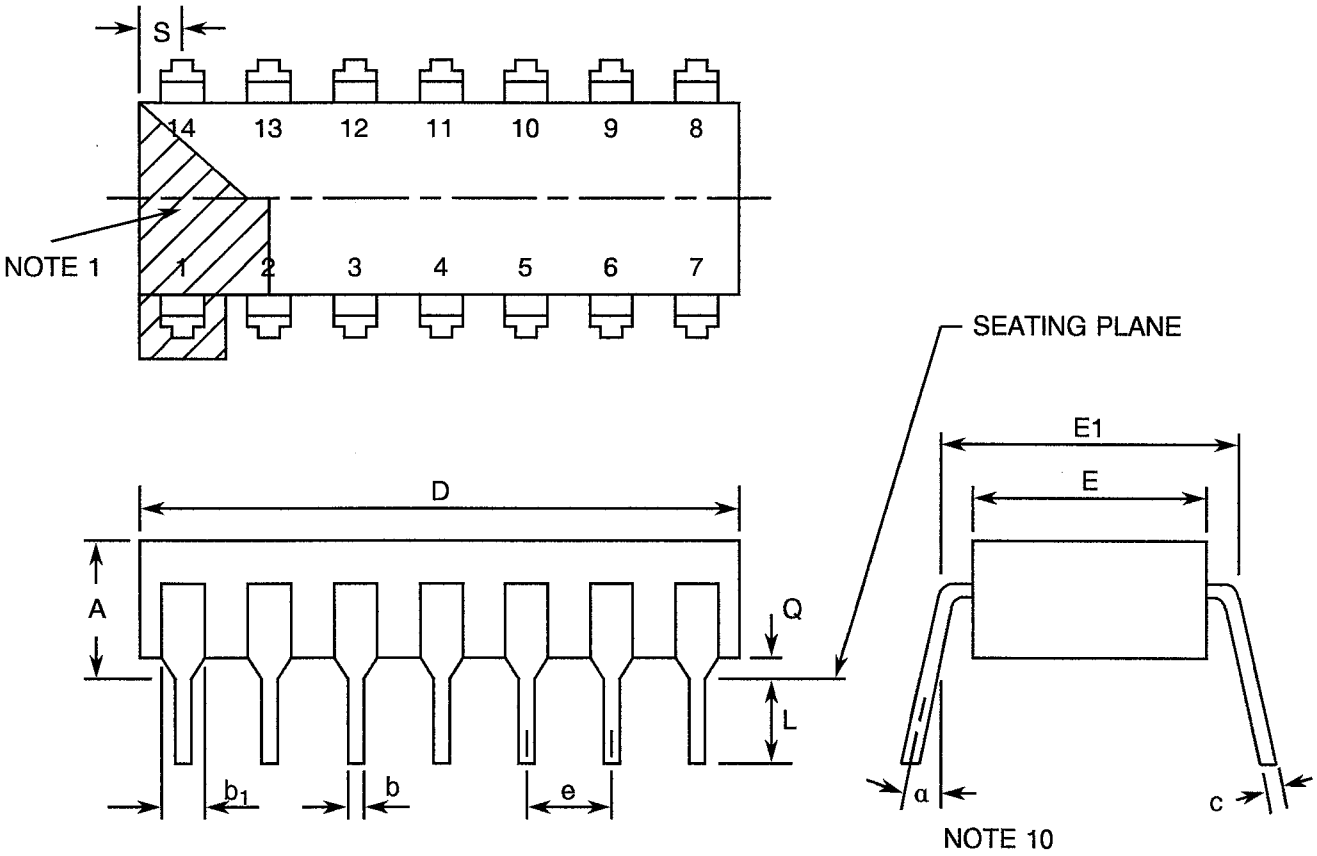
FIGURE 1 - PARAMETER DERATING INFORMATION



Power Dissipation versus Temperature

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - DUAL-IN-LINE PACKAGE, 14-PIN

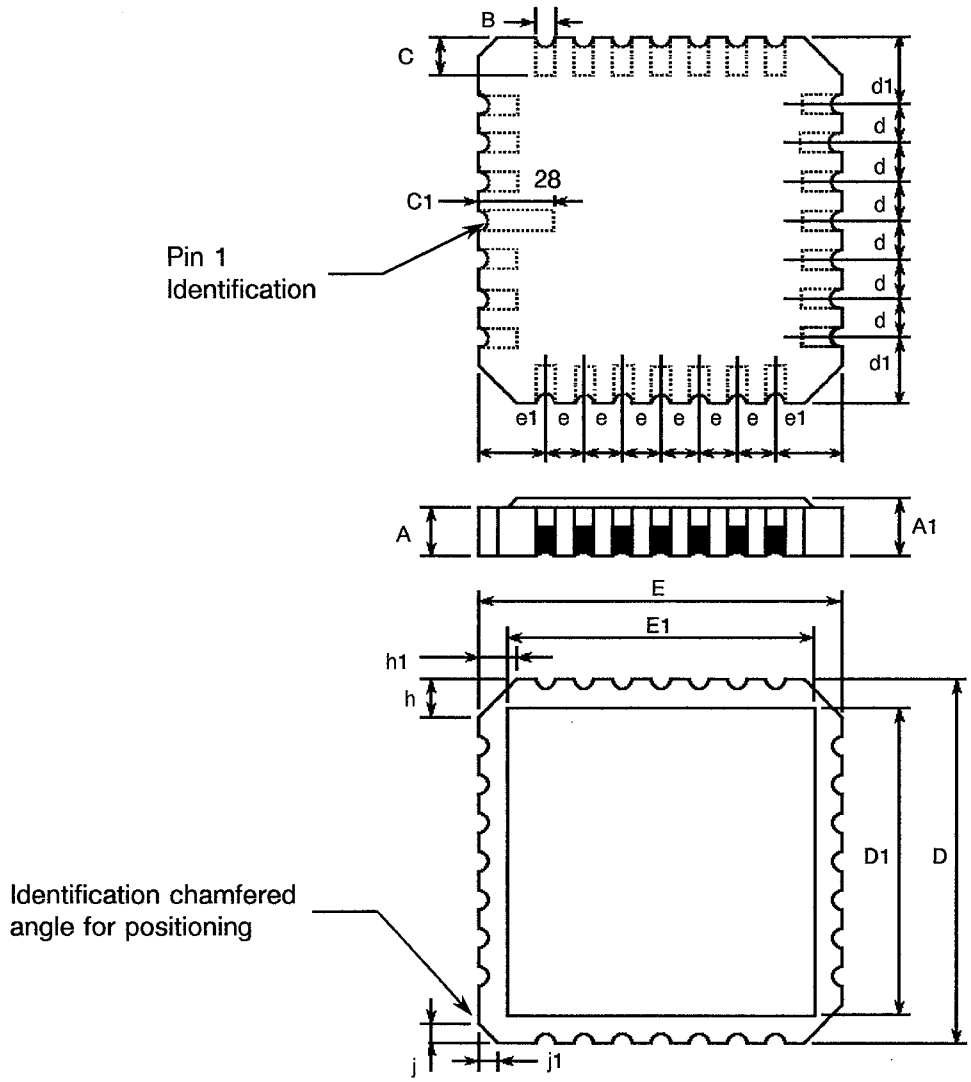


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	-	5.08	
b	0.38	0.58	8
b_1	-	1.78	8
c	0.20	0.38	8
D	-	19.94	
E	5.59	7.87	
E1	7.37	8.13	4
e	2.54 TYPICAL		6, 9
L	3.18	5.08	
Q	0.38	1.52	3
S	1.78	2.54	7
α	0°	15°	10

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - CHIP CARRIER, 28-TERMINAL



DIMENSIONS	MILLIMETRES		NOTES
	MIN	MAX	
A	1.63	2.54	
A1	1.37	2.24	
B	0.56	0.71	8
C	1.14	1.40	8
C1	1.96	2.36	
D	11.23	11.63	
D1	-	11.63	
d	1.27 TYPICAL		6, 9
d1	1.91 TYPICAL		
E	11.23	11.63	
E1	-	11.63	
e	1.27 TYPICAL		6, 9
e1	1.91 TYPICAL		
h, h1	1.016 TYPICAL		11
j, j1	0.51 TYPICAL		12

NOTES: See Page 10.

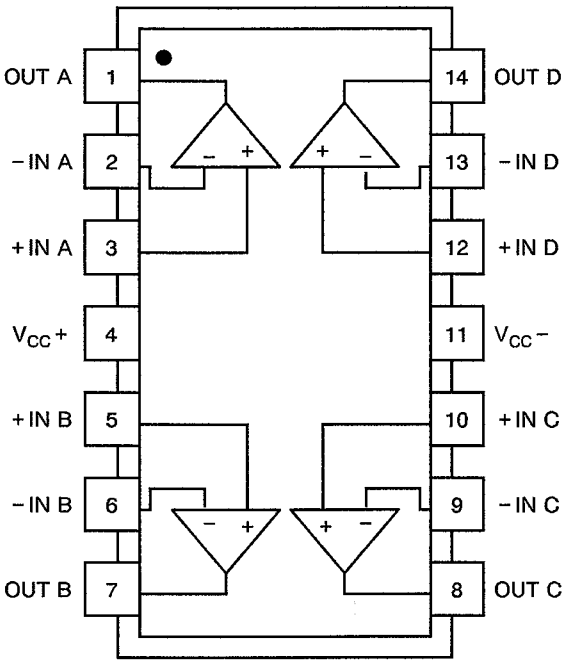
FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURES 2(a) TO 2(b) INCLUSIVE

1. Index area: a notch or a dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown in Figure 2(b).
2. Not applicable.
3. The dimension shall be measured from the seating plane to the base plane.
4. This dimension allows for off-centre lids, meniscus and glass overrun.
5. Not applicable.
6. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ± 0.25mm of its true longitudinal position relative to Pins 1 and the highest pin number.
7. Applies to all 4 corners.
8. All leads or terminals.
9. 12 spaces for dual-in-line packages.
   24 spaces for chip carrier packages.
10. Lead centreline when α is 0°.
11. 3 non-index corners - 6 dimensions.
12. Index corner only - 2 dimensions.

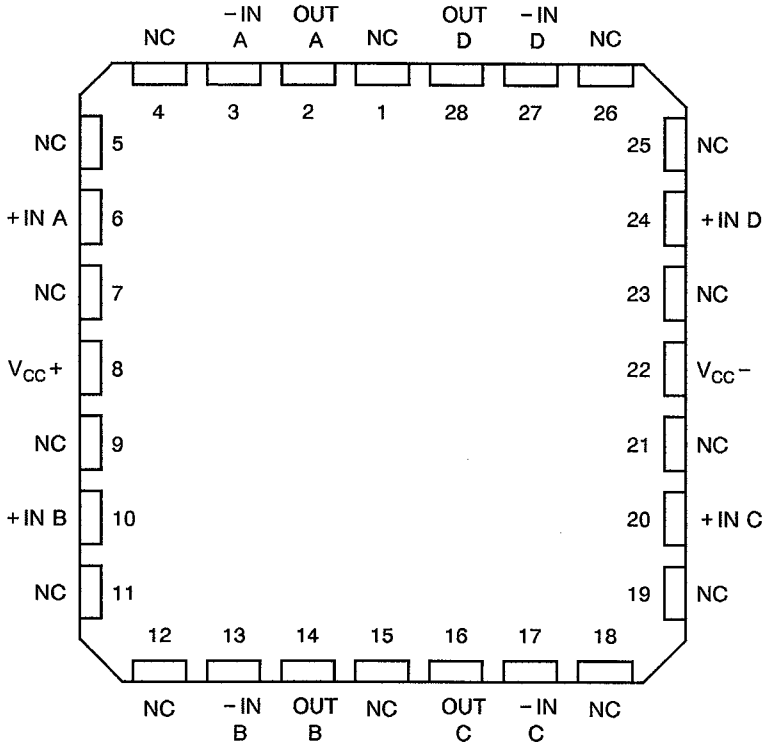
FIGURE 3(a) - PIN ASSIGNMENT

DUAL-IN-LINE PACKAGE



(TOP VIEW)

CHIP CARRIER PACKAGE



(TOP VIEW)

DUAL-IN-LINE TO CHIP CARRIER PIN ASSIGNMENT

DUAL-IN-LINE PIN OUTS	1	2	3	4	5	6	7	8	9	10	11	12	13	14
CHIP CARRIER PIN OUTS	2	3	6	8	10	13	14	16	17	20	22	24	27	28

FIGURE 3(b) - TRUTH TABLE

Not applicable.

FIGURE 3(c) - CIRCUIT SCHEMATIC

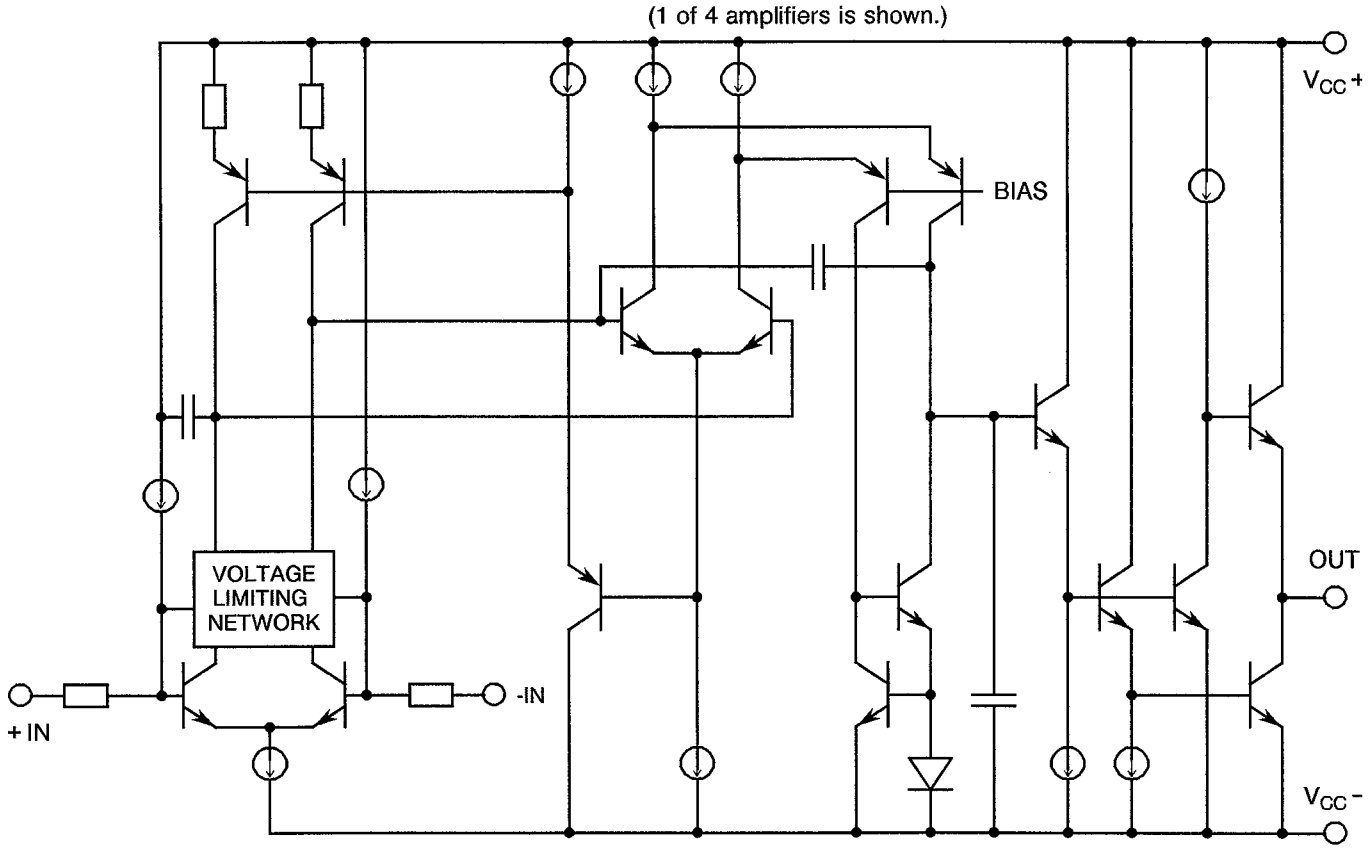
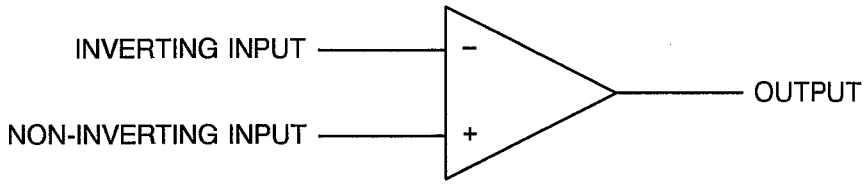


FIGURE 3(d) - FUNCTIONAL DIAGRAM



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

V_{CC} = Supply voltage of the device under test.
AV = Gain of the device under test.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

(a) Para. 7.1.1(a), "High Temperature Reverse Bias tests" and subsequent electrical measurements related to this test shall be omitted.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 2.2 grammes for the dual-in-line package and 0.85 grammes for the chip carrier package.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body and the lids shall be welded, brazed, preform-soldered or glass frit-sealed.

4.4.2 Lead Material and Finish

For dual-in-line packages, the material shall be Type 'G' with Type '4' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. For chip carrier packages, the finish shall be Type '7' in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700 and the following paragraphs. When the component is too small to accommodate all of the marking specified, as much as space permits shall be marked and the marking information, in full, shall accompany the component in its primary package.

The information to be marked and the order of precedence shall be as follows:-

(a) Lead Identification.

(b) The SCC Component Number.

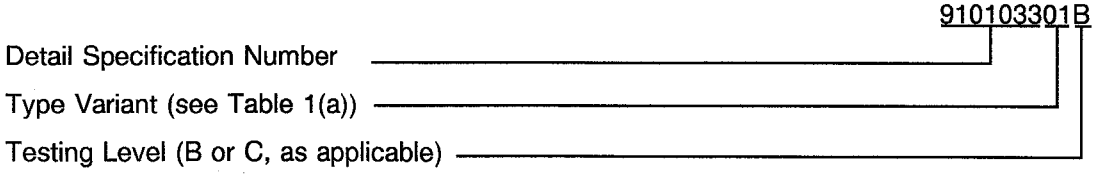
(c) Traceability Information.

4.5.2 Lead Identification

For dual-in-line packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side. For chip carrier packages, the index shall be as defined by Figure 2(b).

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:-



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ °C and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits and test sequences for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-in

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for power burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for High Temperature Reverse Bias Burn-in

Not applicable.

4.7.5 Electrical Circuits for Power Burn-in

Circuits for use in performing the power burn-in tests are shown in Figure 5(b) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL (NOTE 1)	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
1 to 4	Input Offset Voltage	V_{IOi}	4001	4(a)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_1 = 0V$	-	150	µV
5 to 8	Input Offset Current	I_{IOi}	4001	4(b)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_1 = 0V$	-	1.0	nA
9 to 12	Input Bias Current	I_{IBi}	4001	4(c)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_1 = 0V$	-	±3.0	nA
13 to 16	Output Voltage Swing (Plus)	$+V_{OPi}$	4004	4(d)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_1 = +15V$, $R_L = 10k\Omega$	+12	-	V
17 to 20	Output Voltage Swing (Minus)	$-V_{OPi}$	4004	4(d)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_1 = -15V$, $R_L = 10k\Omega$	-	−12	V
21 to 24	Output Voltage Swing (Plus)	$+V_{OPi}$	4004	4(d)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_1 = +15V$, $R_L = 2.0k\Omega$	+11	-	V
25 to 28	Output Voltage Swing (Minus)	$-V_{OPi}$	4004	4(d)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_1 = -15V$, $R_L = 2.0k\Omega$	-	−11	V
29	Power Supply Current	I_{CC}	4005	4(e)	$+V_{CC} = 15V$, $-V_{CC} = -15V$	-	2.9	mA
30 to 33	Open Loop Voltage Gain	A_{VSi}	4004	4(f)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_1 = +10V$ or $V_1 = -10V$ $R_L = 10k\Omega$	5000	-	V/mV
34 to 37	Open Loop Voltage Gain	A_{VSi}	4004	4(f)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_1 = +10V$ or $V_1 = -10V$ $R_L = 2.0k\Omega$	2000	-	V/mV
38 to 41	Power Supply Rejection Ratio	$+PSRR_i$	4003	4(g)	$+V_{CC} = 3V$ or $18V$ $-V_{CC} = -18V$	-	1.8	µV/V
42 to 45	Power Supply Rejection Ratio	$-PSRR_i$	4003	4(g)	$-V_{CC} = -3V$ or $-18V$ $+V_{CC} = +18V$	-	1.8	µV/V
46 to 49	Common Mode Rejection Ratio	$CMRR_i$	4003	4(h)	$+V_{CC} = +27V$ or $+3V$ $-V_{CC} = -3V$ or $-27V$ $V_1 = -12V$ or $+12V$	120	-	dB

NOTES: See Page 17.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL (NOTE 1)	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
50 to 53	Slew Rate (Plus)	$SR_i(+)$	4002	4(i)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{IN} = +5V$ to $-5V$ AV = 1.0	0.1	-	V/µs
54 to 57	Slew Rate (Minus)	$SR_i(-)$	4002	4(i)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{IN} = +5V$ to $-5V$ AV = 1.0	0.1	-	V/µs
58 to 61	Input Noise Voltage	e_{NT}	-	4(j)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ f = 10 to 100Hz	-	438	nVrms

NOTES

1. A parameter with an index 'i' ('i' = 1 to 4) means that a measurement for each of the 4 amplifiers must be performed.

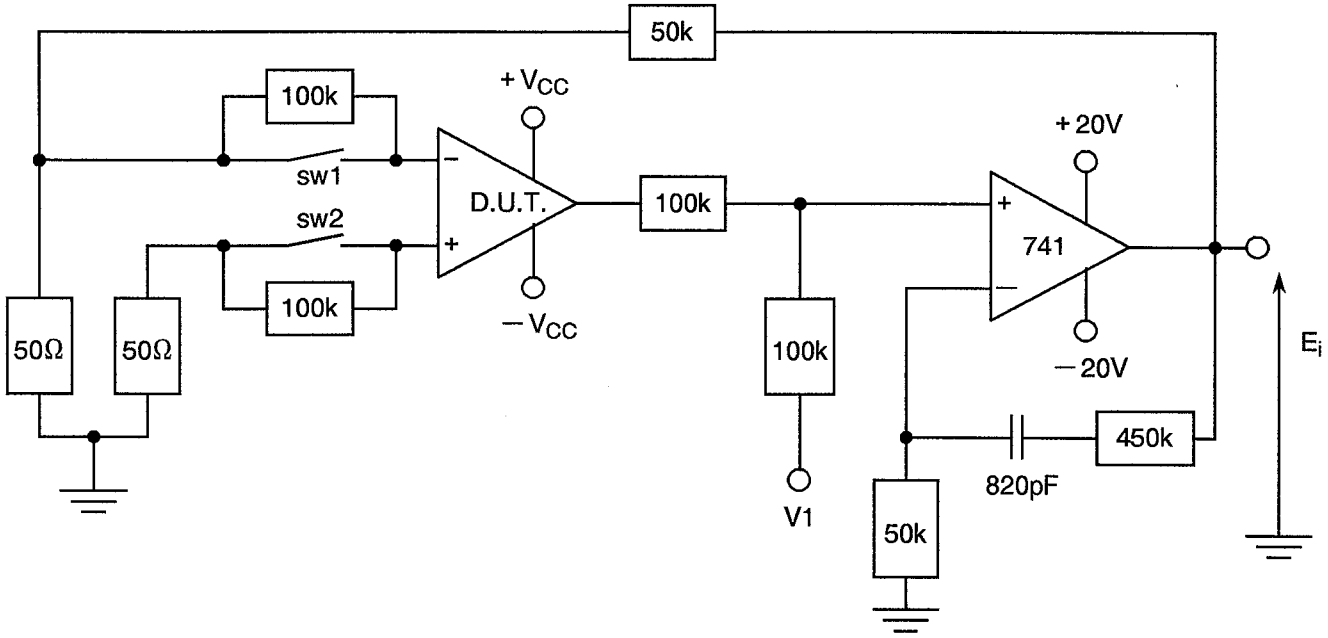
TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES

No.	CHARACTERISTICS	SYMBOL (NOTE 1)	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
1 to 4	Input Offset Voltage	V_{IOi}	4001	4(a)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_1 = 0V	-	270	µV
5 to 8	Input Offset Current	I_{IOi}	4001	4(b)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_1 = 0V	-	2.5	nA
9 to 12	Input Bias Current	I_{IBi}	4001	4(c)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_1 = 0V	-	±5.0	nA
13 to 16	Output Voltage Swing (Plus)	$+V_{OPi}$	4004	4(d)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_1 = +15V, R_L = 10kΩ	+12	-	V
17 to 20	Output Voltage Swing (Minus)	$-V_{OPi}$	4004	4(d)	$+V_{CC}$ = 15V, $-V_{CC}$ = −15V V_1 = −15V, R_L = 10kΩ	-	−12	V
21 to 24	Output Voltage Swing (Plus)	$+V_{OPi}$	4004	4(d)	$+V_{CC}$ = 15V, $-V_{CC}$ = −15V V_1 = +15V, R_L = 2.0kΩ	+11	-	V
25 to 28	Output Voltage Swing (Minus)	$-V_{OPi}$	4004	4(d)	$+V_{CC}$ = 15V, $-V_{CC}$ = −15V V_1 = −15V, R_L = 2.0kΩ	-	−11	V
29	Power Supply Current	I_{CC}	4005	4(e)	$+V_{CC}$ = 15V, $-V_{CC}$ = −15V	-	3.1	mA
30 to 33	Open Loop Voltage Gain	A_{VSi}	4004	4(f)	$+V_{CC}$ = 15V, $-V_{CC}$ = −15V V_1 = +10V or V_1 = −10V R_L = 10kΩ	3000	-	V/mV
34 to 37	Open Loop Voltage Gain	A_{VSi}	4004	4(f)	$+V_{CC}$ = 15V, $-V_{CC}$ = −15V V_1 = +10V or V_1 = −10V R_L = 2.0kΩ	1000	-	V/mV
38 to 41	Power Supply Rejection Ratio	$+PSRR_i$	4003	4(g)	$+V_{CC}$ = 3V or 18V $-V_{CC}$ = −18V	-	3.2	µV/V
42 to 45	Power Supply Rejection Ratio	$-PSRR_i$	4003	4(g)	$-V_{CC}$ = −3V or −18V $+V_{CC}$ = +18V	-	3.2	µV/V
46 to 49	Common Mode Rejection Ratio	$CMRR_i$	4003	4(h)	$+V_{CC}$ = +27V or +3V $-V_{CC}$ = −3V or −27V V_1 = −12V or +12V	115	-	dB

NOTES: See Page 17.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - INPUT OFFSET VOLTAGE

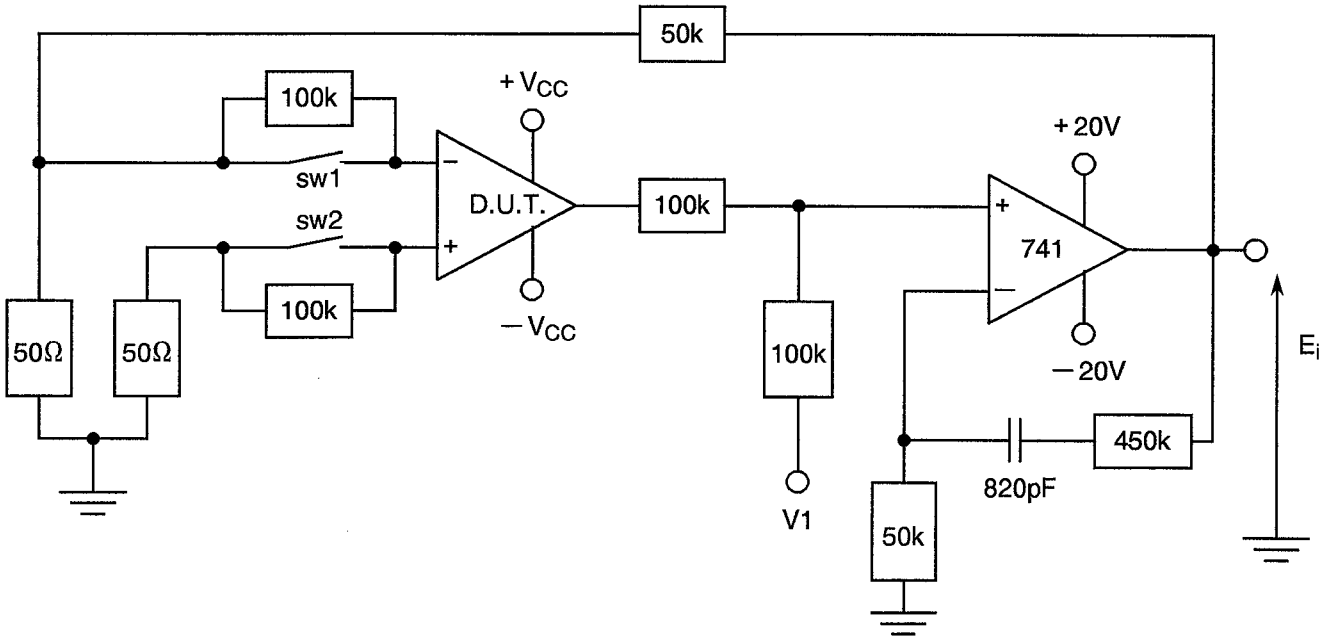


NOTES

1. Close sw1 and sw2, measure E_i for each amplifier.

$$V_{IOi} = \frac{E_i}{1000}$$

FIGURE 4(b) - INPUT OFFSET CURRENT



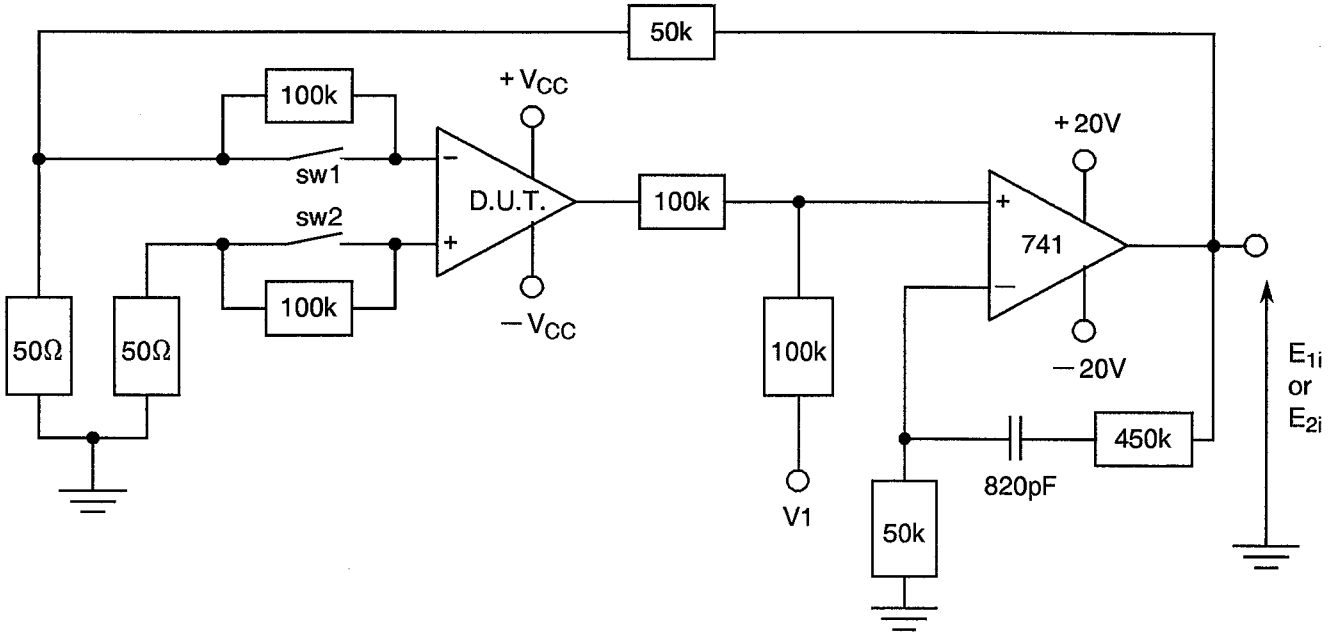
NOTES

1. Open sw1 and sw2, measure E_i for each amplifier.

$$I_{IOi} = \frac{E_i/1000 - V_{IOi}}{100k\Omega}$$

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(c) - INPUT BIAS CURRENT



NOTES

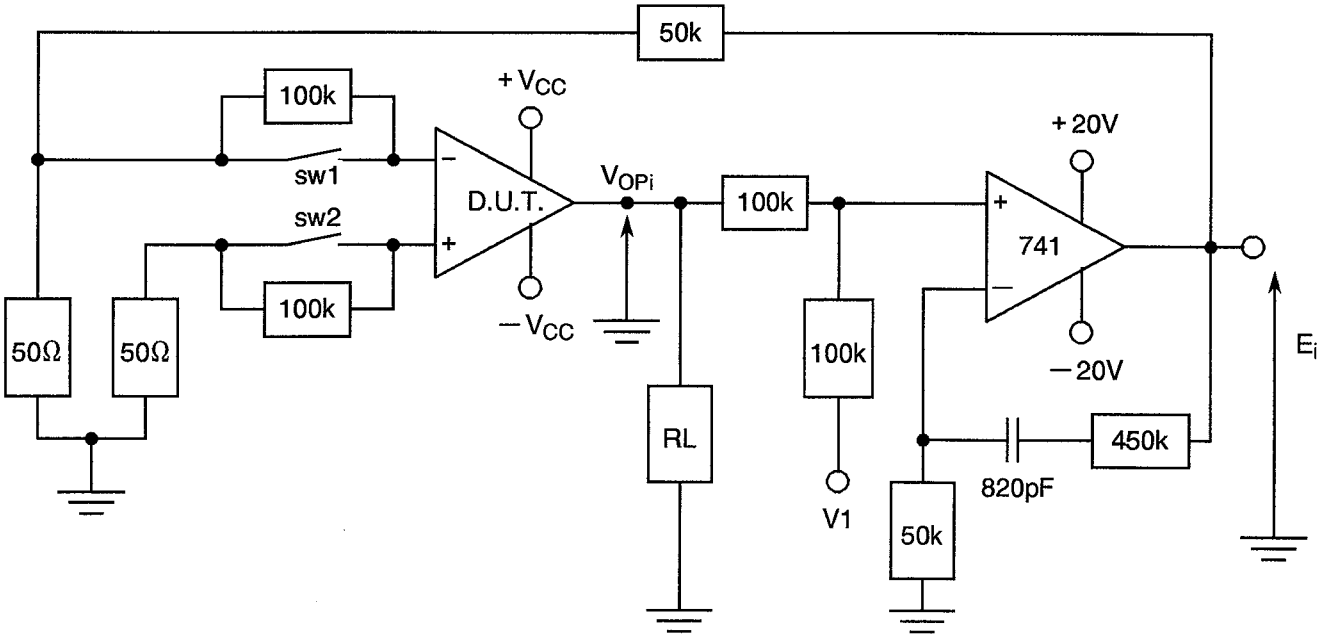
1. Close sw1 and open sw2, measure E_{1i}.
2. Open sw1 and close sw2, measure E_{2i}

$$I_{+IBi} = \frac{V_{IOi} - E_{1i}/1000}{100k\Omega}$$

$$I_{-IBi} = \frac{V_{IOi} - E_{2i}/1000}{100k\Omega}$$

$$I_{IBi} = \frac{|I_{+IBi}| + |I_{-IBi}|}{2}$$

FIGURE 4(d) - OUTPUT VOLTAGE SWING

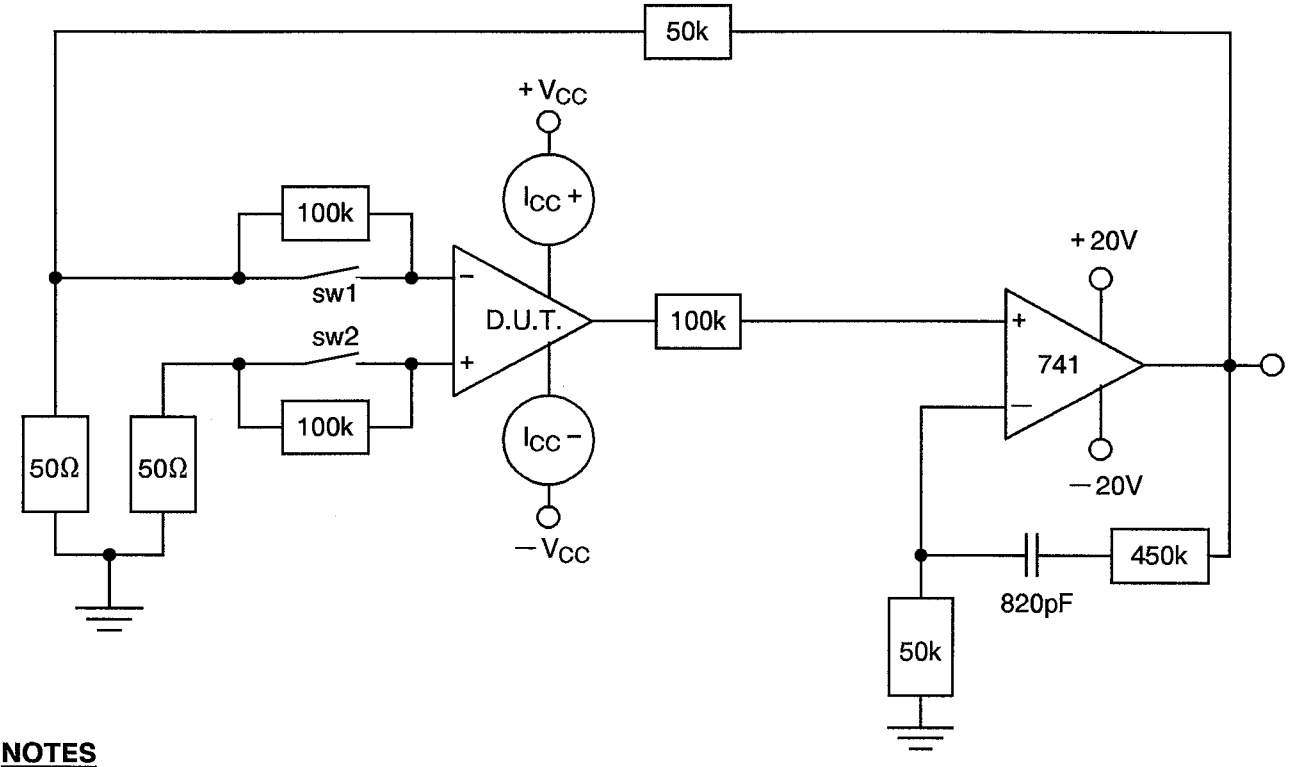


NOTES

1. Close sw1 and sw2, measure V_{OPi} for each amplifier.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

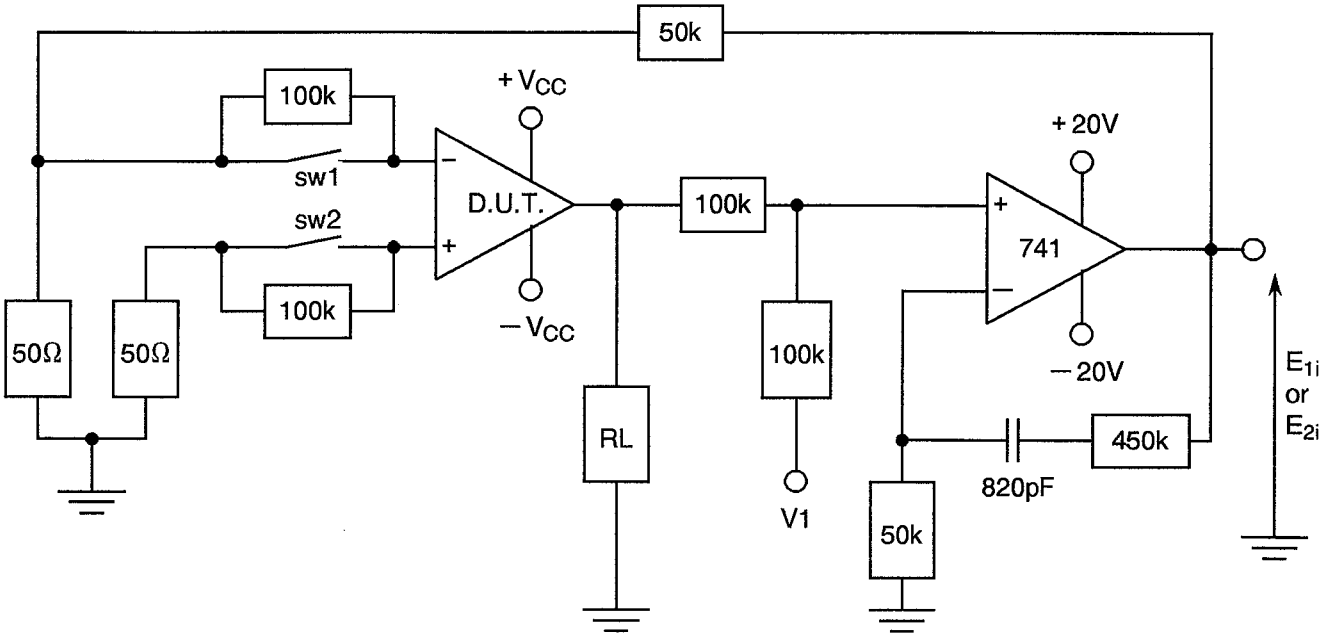
FIGURE 4(e) - POWER SUPPLY CURRENT



NOTES

1. Close sw1 and sw2, measure I_{CC} for the four amplifiers.

FIGURE 4(f) - OPEN LOOP VOLTAGE GAIN



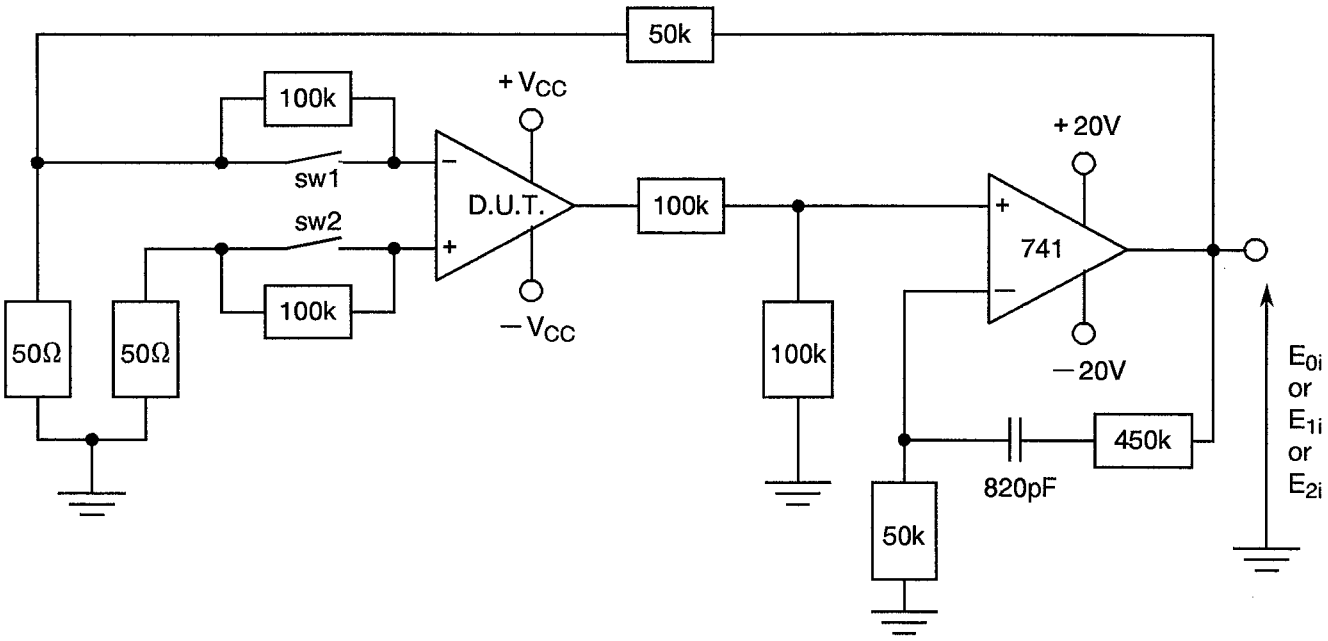
NOTES

1. Close sw1 and sw2, measure E_{1i} when $V_1 = -10V$ and measure E_{2i} when $V_1 = +10V$.

$$A_{VSi} = 1000 \times \frac{20}{E_{2i} - E_{1i}}$$

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(g) - POWER SUPPLY REJECTION RATIO



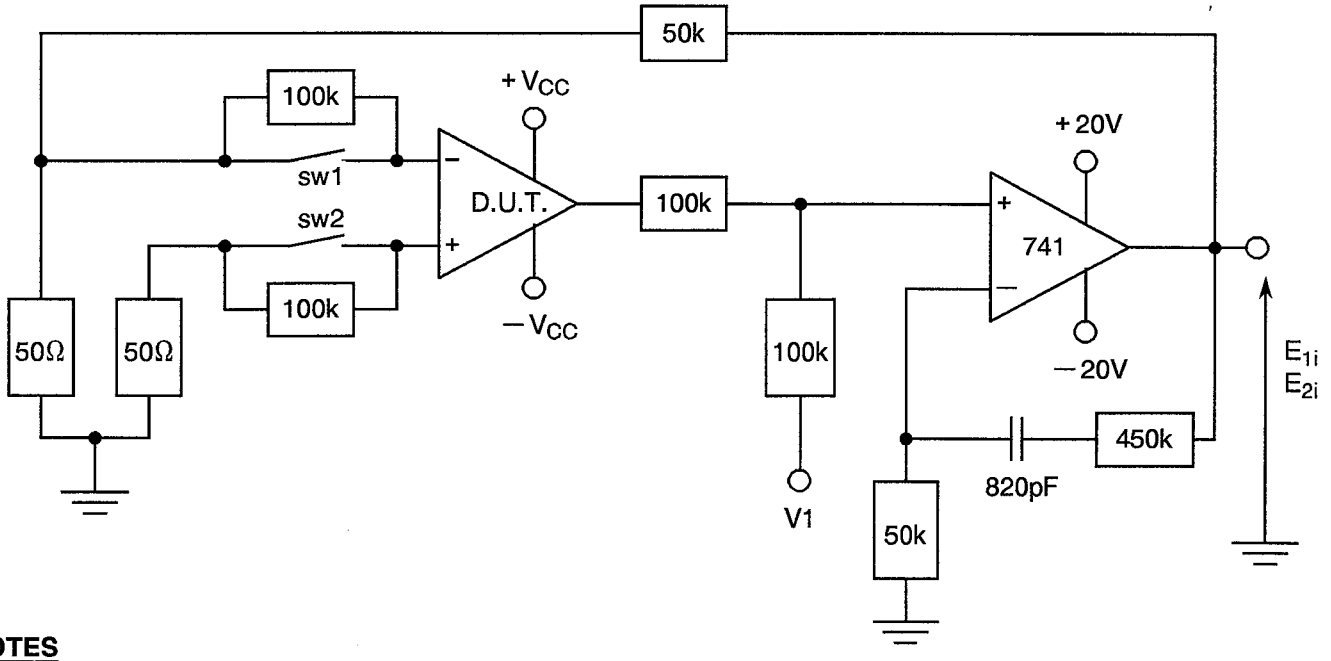
NOTES

1. Close sw1 and sw2, measure E_{0i} when $+V_{CC} = +18V$ and $-V_{CC} = -18V$.
2. Close sw1 and sw2, measure E_{1i} when $+V_{CC} = +3V$ and $-V_{CC} = -18V$.
3. Close sw1 and sw2, measure E_{2i} when $+V_{CC} = +18V$ and $-V_{CC} = -3V$.
4. $\Delta V_{CC} = 15V$.

$$+PSRR_i = \frac{E_{1i} - E_{0i}}{15 \times 1000}$$

$$-PSRR_i = \frac{E_{2i} - E_{0i}}{15 \times 1000}$$

FIGURE 4(h) - COMMON MODE REJECTION RATIO



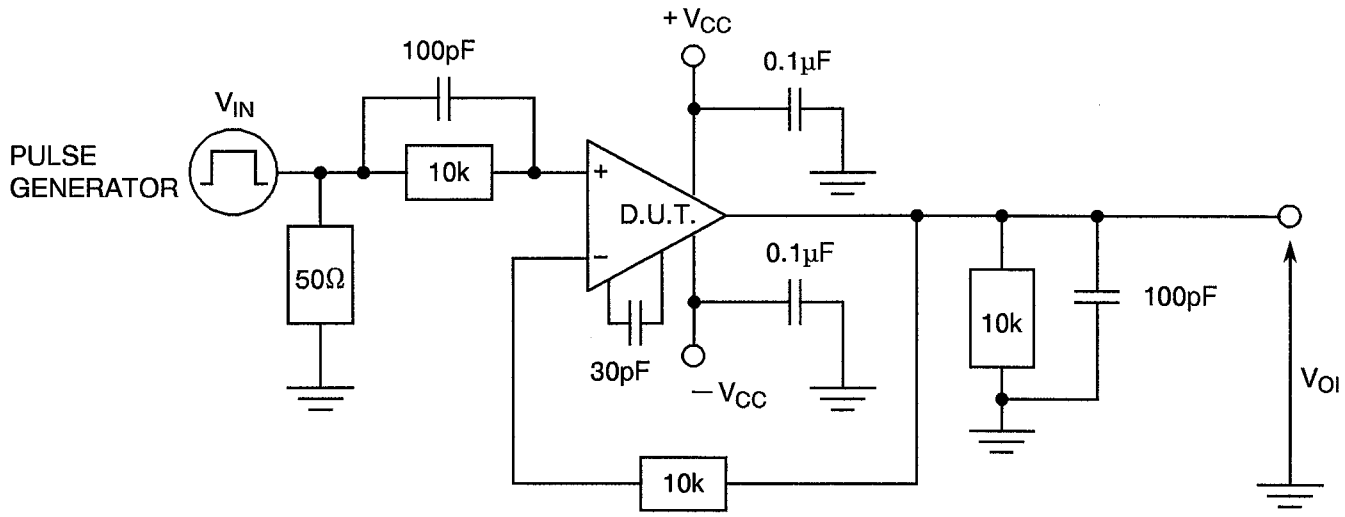
NOTES

1. Close sw1 and sw2, measure E_{1i} when $V_1 = -12V$, $+V_{CC} = +27V$ and $-V_{CC} = -3V$.
2. Close sw1 and sw2, measure E_{2i} when $V_1 = +12V$, $+V_{CC} = +3V$ and $-V_{CC} = -27V$.

$$CMRR_i = 20\log \frac{E_{2i}-E_{1i}}{1000 \times 24}$$

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - SLEW RATE

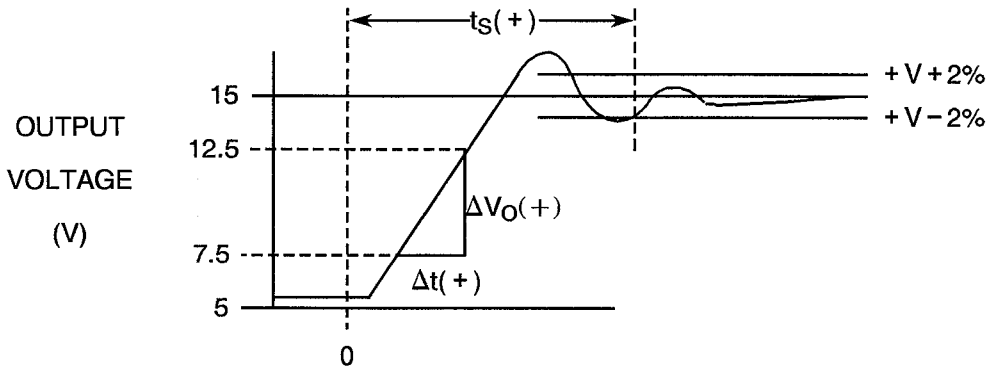


NOTES

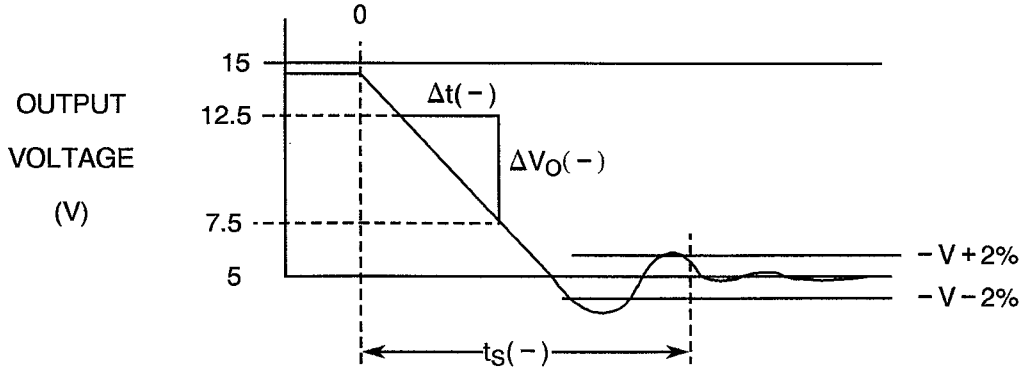
1. Pulse Generator:- Rise Time ≤ 10ns.
   Repetition Rate 1.0kHz (Max.).
   Pulse Voltage V_{IN} = −5V to +5V.

$$SR = \frac{|\Delta V_{OI}|}{|\Delta t|}$$

WAVEFORM 1 - SR(+)



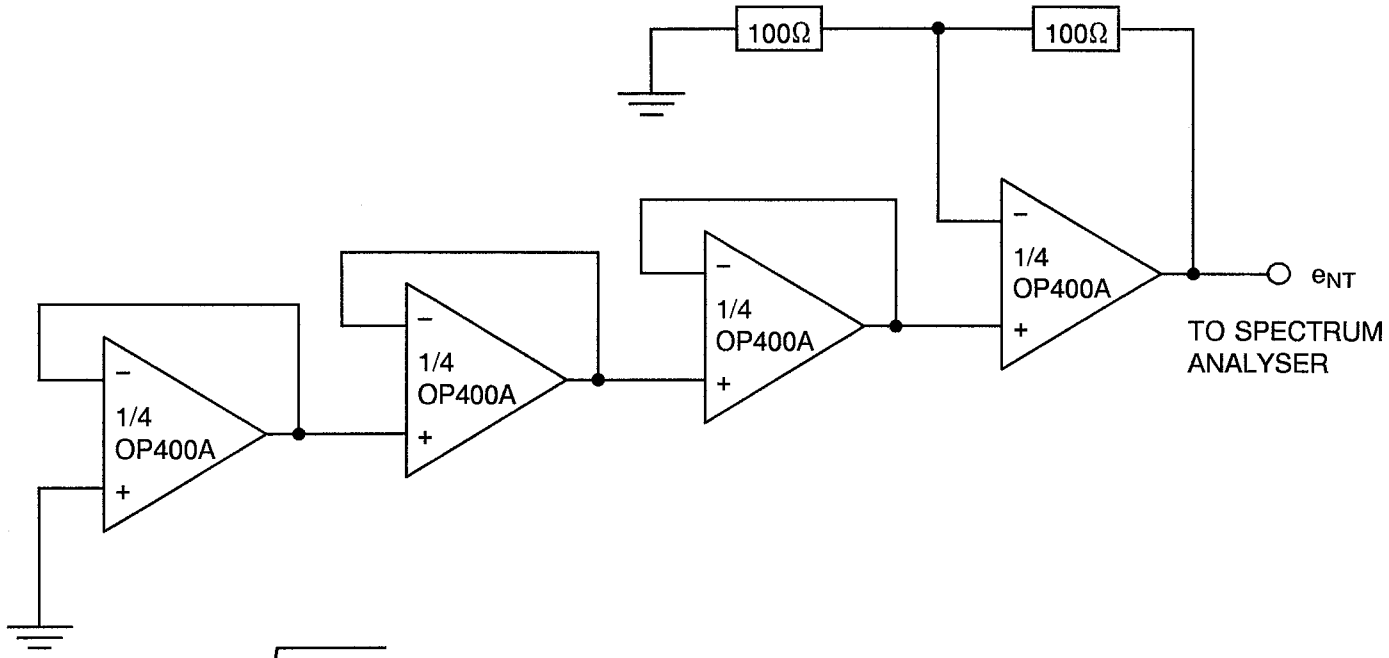
WAVEFORM 2 - SR(−)



NOTES 1. t_S = Time stabilisation

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(j) - INPUT NOISE VOLTAGE



$e_{NT} = \sqrt{\sum Ai^2}$

Where $A_i = e_N(f_{High} - f_{Low})$ for each of the 4 amplifiers.

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
1 to 4	Input Offset Voltage	V_{IOi}	As per Table 2	As per Table 2	± 30	μV
5 to 8	Input Offset Current	I_{IOi}	As per Table 2	As per Table 2	± 0.3	nA
9 to 12	Input Bias Current	I_{IBi}	As per Table 2	As per Table 2	± 0.3	nA
29	Power Supply Current	I_{CC}	As per Table 2	As per Table 2	± 10	%

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

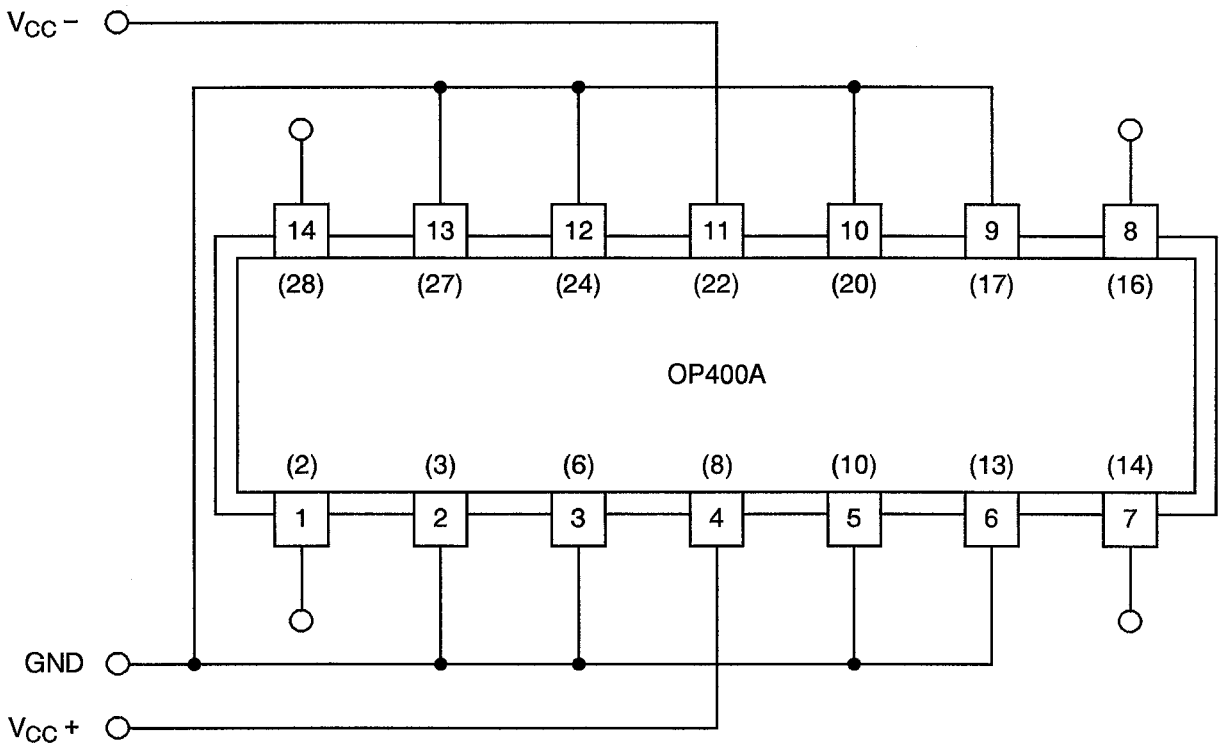
TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+ 125(+ 5 − 0)	°C
2	Power Supply Voltage	V_{CC}	± 18	V

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



NOTES

1. Pin numbers in parenthesis are for the chip carrier package.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(b) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL (NOTE 1)	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	ABSOLUTE		UNIT
					MIN	MAX	
1 to 4	Input Offset Voltage	V_{IOi}	As per Table 2	As per Table 2	-	150	µV
5 to 8	Input Offset Current	I_{IOi}	As per Table 2	As per Table 2	-	1.0	nA
9 to 12	Input Bias Current	I_{IBi}	As per Table 2	As per Table 2	-	±3.0	nA
13 to 16	Output Voltage Swing (Plus)	$+V_{OPi}$	As per Table 2	As per Table 2	+12	-	V
17 to 20	Output Voltage Swing (Minus)	$-V_{OPi}$	As per Table 2	As per Table 2	-	−12	V
21 to 24	Output Voltage Swing (Plus)	$+V_{OPi}$	As per Table 2	As per Table 2	+11	-	V
25 to 28	Output Voltage Swing (Minus)	$-V_{OPi}$	As per Table 2	As per Table 2	-	−11	V
29	Power Supply Current	I_{CC}	As per Table 2	As per Table 2	-	2.9	mA
30 to 33	Open Loop Voltage Gain	A_{VSi}	As per Table 2	As per Table 2	5000	-	V/mV
34 to 37	Open Loop Voltage Gain	A_{VSi}	As per Table 2	As per Table 2	2000	-	V/mV
38 to 41	Power Supply Rejection Ratio	$+PSRR_i$	As per Table 2	As per Table 2	-	1.8	µV/V
42 to 45	Power Supply Rejection Ratio	$-PSRR_i$	As per Table 2	As per Table 2	-	1.8	µV/V
46 to 49	Common Mode Rejection Ratio	$CMRR_i$	As per Table 2	As per Table 2	120	-	dB