INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS SILICON GATE, STATIC 256K (262144×1 BIT) ASYNCHRONOUS RANDOM ACCESS MEMORY WITH 3-STATE OUTPUTS, BASED ON TYPE M65697

ESCC Detail Specification No. 9301/038

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Pages 1 to 48

INTEGRATED CIRCUITS, SILICON MONOLITHIC, CMOS SILICON GATE, STATIC 256K (262144 × 1 BIT) ASYNCHRONOUS RANDOM ACCESS MEMORY WITH 3-STATE OUTPUTS, BASED ON TYPE M65697EV

ESA/SCC Detail Specification No. 9301/038

SCC

space components
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DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE Reference		CHANGE Item	Approved DCR No.
'A'	Apr. '96	P1.	Cover page	"EV" deleted from part number	221330
		P2.	DCN		None
		P5.	Para. 1.1	"EV" deleted from part number	221330
		P6.	Table 1(a)	Variant numbers amended	221330
				"EV" deleted from Based on Type	221330
				Note 1 added	221330
		P17.	Para. 4.5.3	Type Variant amended	221330
		P22.	Table 2 a.c.	Nos. 116 to 117, 118 to 119, 120 to 121, Variant numbers amended	221330
		P23.	Table 2 a.c.	Nos. 126 to 127, 130 to 131, 134 to 135, 142 to 143, Variant numbers amended	221330
		P24.	Note 1	In Functional Test 1, "(2)" added to MARCH	221330
				In Functional Test 3, "(2)" amended to "(3)"	221330
				In N.B., new No. 2 added and existing 2 amended to "3".	221330
		P25.	Note 6(e)	Variant numbers amended	221330
			Note 8	In headings, Variant numbers amended	221330
		P29.	Table 3 a.c.	Nos. 116 to 117, 118 to 119, 120 to 121, Variant numbers amended	221330
		P30.	Table 3 a.c.	Nos. 126 to 127, 130 to 131, 134 to 135, 142 to 143, Variant numbers amended	221330
		P38.	Figure 5(b)	"EV" deleted from part number	221330
		P42.	Figure 6	"EV" deleted from part number	221330

TABLE OF CONTENTS

TABLES

FIGURES

APPENDICES (Applicable to specific Manufacturers only)

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon, monolithic, CMOS Silicon Gate, Static, 256K (262144 × 1 BIT) Asynchronous Random Access Memory with 3-State Outputs, based on Type M65697. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

As per Figure 3(b).

1.8 CIRCUIT DESCRIPTION

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 with a Minimum Critical Path Failure Voltage of 1 000 Volts.

1.11 INPUT PROTECTION NETWORK

Double transistor protection shall be incorporated into each input as shown in Figure 3(e).

TABLE 1(a) - TYPE VARIANTS

VARIANT	BASED ON TYPE	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
05	M65697-55	D.I.L.	2(a)	G2
06	M65697-55	FLAT PACK	2(b)	G2
07	M65697-45	D.I.L.	2(a)	G2
08	M65697-45	FLAT PACK	2(b)	G2

NOTES

1. Variants 01 to 04 deleted; not to be used.

TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage	V_{DD}	−0.3 to +7.0	V	Note 1
2	Input Voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V	Note 2 Power On
3	Output Current	± I_{OUT}	$V_{OUT} = V_{DD}$: +110 $V_{OUT} = V_{SS}$: −60	mA	Note 3
4	Device Dissipation (Continuous)	P_D	1.66	W	Per Package
5	Operating Temperature Range	T_{op}	−55 to +125	°C	T_{amb}
6	Storage Temperature Range	T_{stg}	−65 to +150	°C	
7	Soldering Temperature For DIL and FP	T_{sol}	+265	°C	Note 4
8	Thermal Resistance	$R_{TH(J-A)}$	24	°C/W	
9	Junction Temperature	T_J	+165	°C	

NOTES

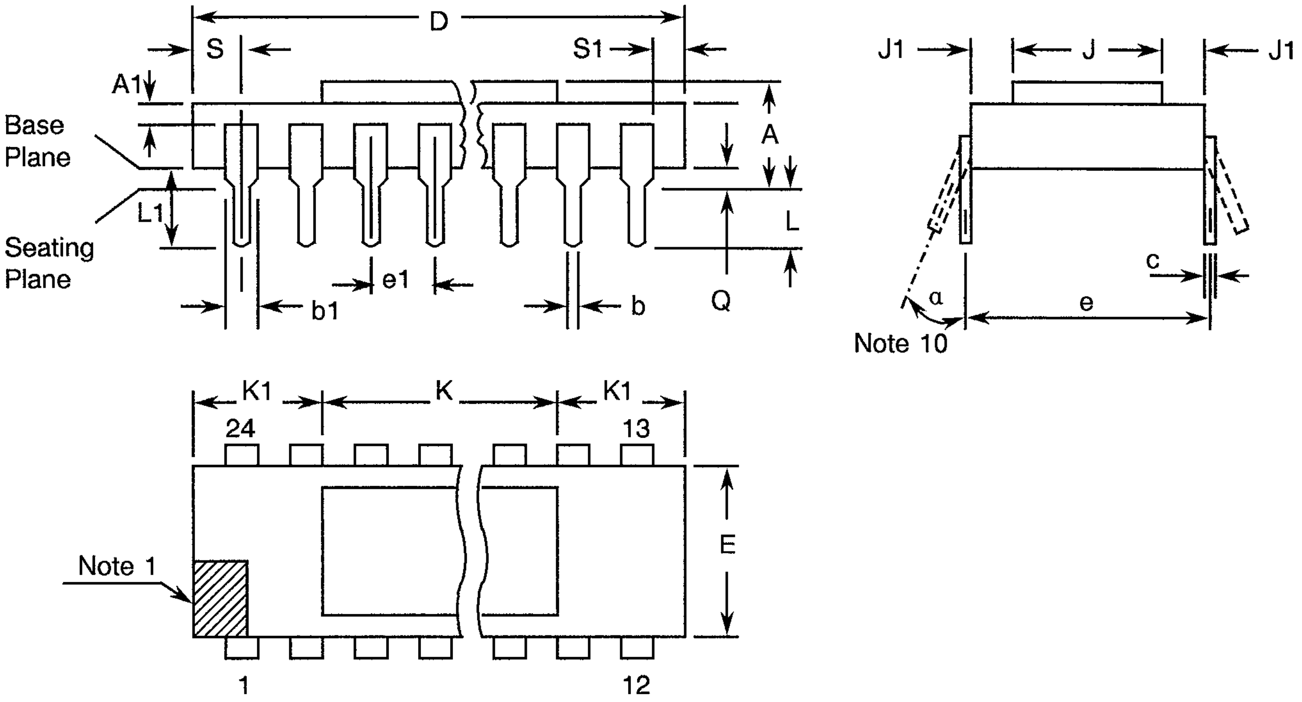
1. Device is functional from +4.5V to +5.5V with reference to Ground.
2. V_{DD} +0.3V should not exceed +7.0V.
3. The maximum output current of any single output.
4. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION

Not applicable.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - DUAL-IN-LINE PACKAGE, 24-PIN

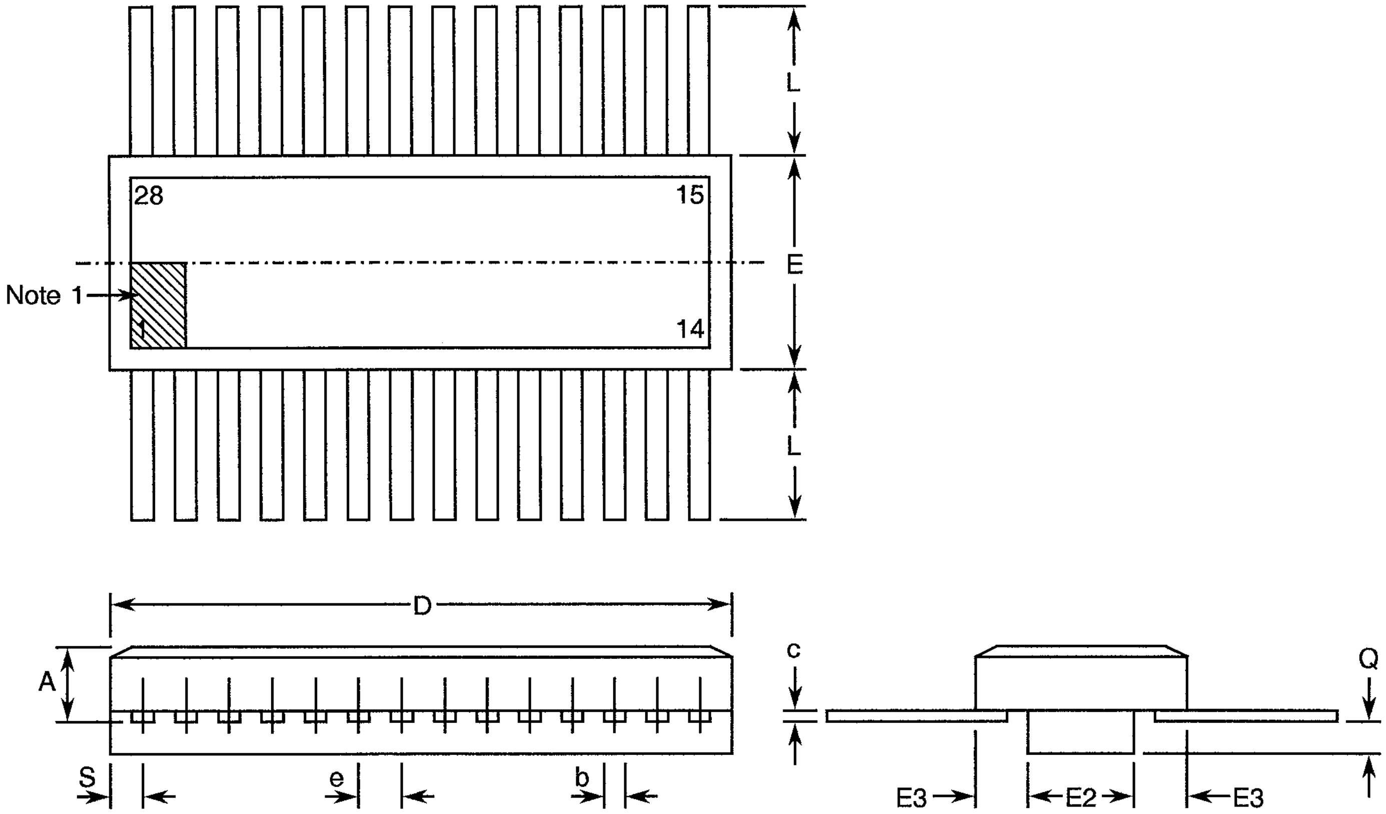


SYMBOL	MILLIMETERS		NOTES
	MIN.	MAX.	
A	3.30	5.84	-
A1	0.13	-	-
b	0.36	0.58	8
b1	0.96	1.65	8
c	0.20	0.38	8
D	-	30.80	-
E	6.10	7.87	4
e	7.37	8.13	-
e1	2.54 TYPICAL		6,9
J	7.03 TYPICAL		-
J1	0.23 TYPICAL		-
K	11.43 TYPICAL		-
K1	9.70 TYPICAL		-
L	2.92	5.08	8
L1	3.30	-	8
S	-	2.97	7
S1	0.13	-	7
Q	0.38	2.54	3
α	0°	15°	10

NOTES: See Page 9.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - FLAT PACKAGE, 28-PIN



SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	2.29	3.30	-
b	0.38	0.48	8
c	0.08	0.15	8
D	-	18.80	-
E	9.65	10.67	-
E2	4.57	-	-
E3	0.76	-	-
e	1.27 TYPICAL		5, 9
L	6.35	9.40	8
Q	0.66	-	2
S	-	1.30	7

NOTES: See Page 9.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURES 2(a) TO 2(b) INCLUSIVE

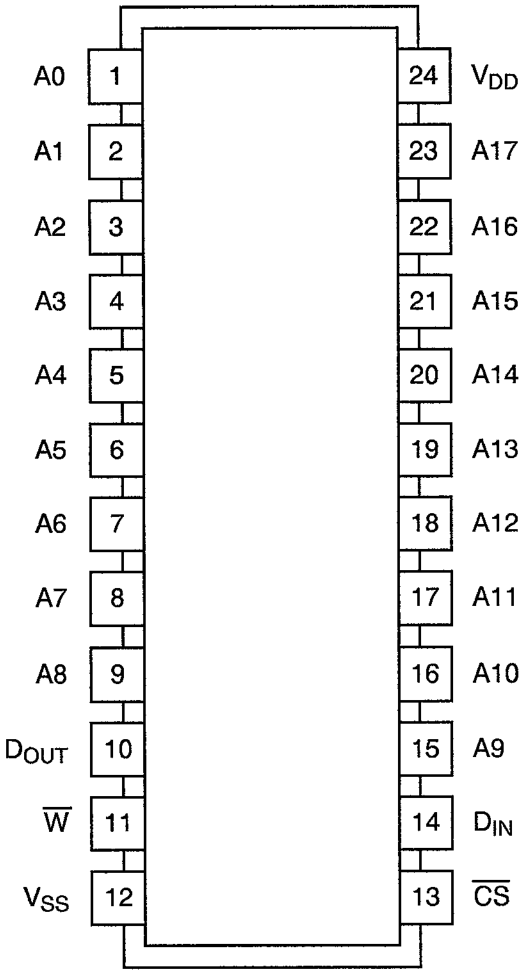
1. Index area: a notch, letter or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. The dimension shall be measured from the seating plane to the base plane.
4. The dimension allows for off-centre lids, meniscus and glass overrun.
5. The true position pin or terminal spacing is 1.27mm between centrelines. Each pin or terminal centreline shall be located within 0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
6. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within 0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.
7. Applies to all 4 corners.
8. All leads or terminals.
9. 22 spaces for dual-in-line packages

   26 spaces for flat packages.

10 Lead centre when α is 0°.

FIGURE 3(a) - PIN ASSIGNMENT

DUAL-IN-LINE PACKAGE



TOP VIEW

NOTES

1. A0 to A17 = Address Inputs.
2. D_{IN} = Data Input.
4. $\overline{W}$ = Write Enable.
3. $\overline{CS}$ = Chip Select.
5. D_{OUT} = Data Output.

DUAL-IN-LINE TO FLAT PACKAGE PIN ASSIGNMENT

DUAL-IN-LINE PACKAGE PIN OUTS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
FLAT PACKAGE PIN OUTS	1	2	3	5	6	7	8	9	10	12	13	14	15	16	17	19	20	21	22	23	24	26	27	28

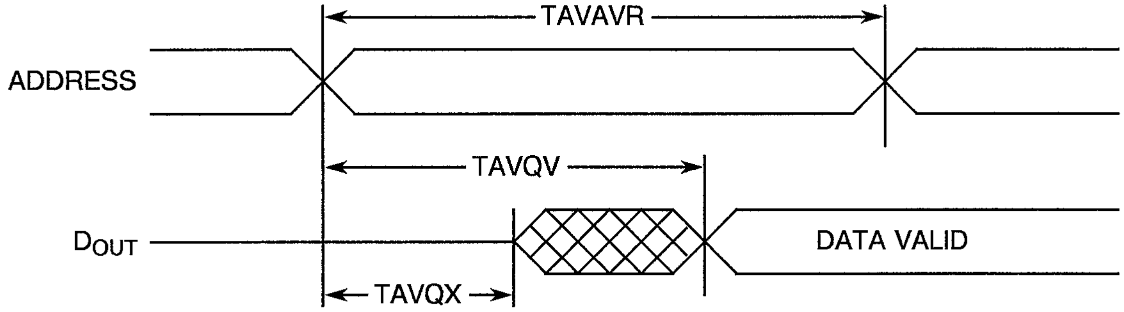
FIGURE 3(b) - TRUTH TABLE

$\overline{CS}$	$\overline{W}$	D_{IN}	D_{OUT}	MODE
H	X	Z	Z	Deselect
L	H	Z	Valid	Read
L	L	Valid	Z	Write

NOTES
1. Logic Level Definitions, L = Low Level, H = High Level, Z = High Impedance, X = Irrelevant.

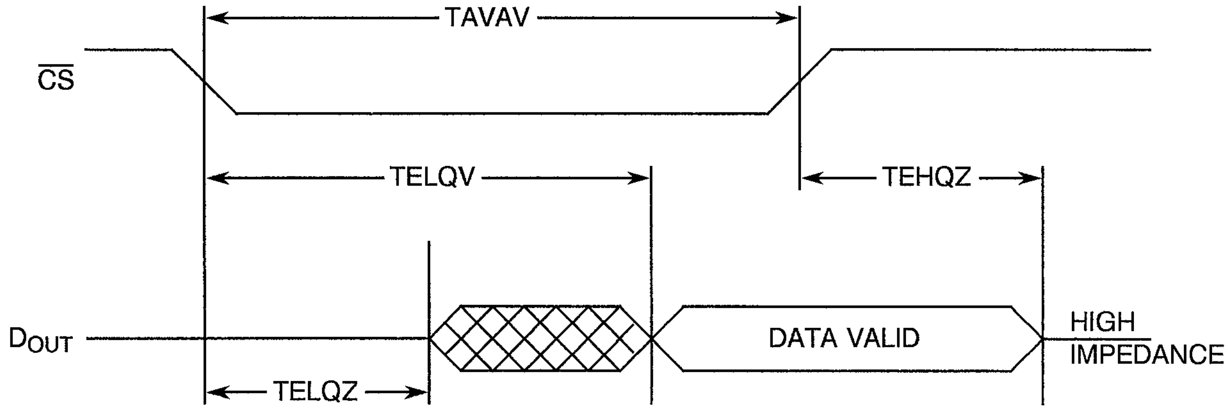
TIMING WAVEFORMS

READ CYCLE 1



NOTES
1. $\overline{W}$ is High throughout Read Cycle.
2. Device is continuously selected for $\overline{CS} = V_{IL}$.

READ CYCLE 2

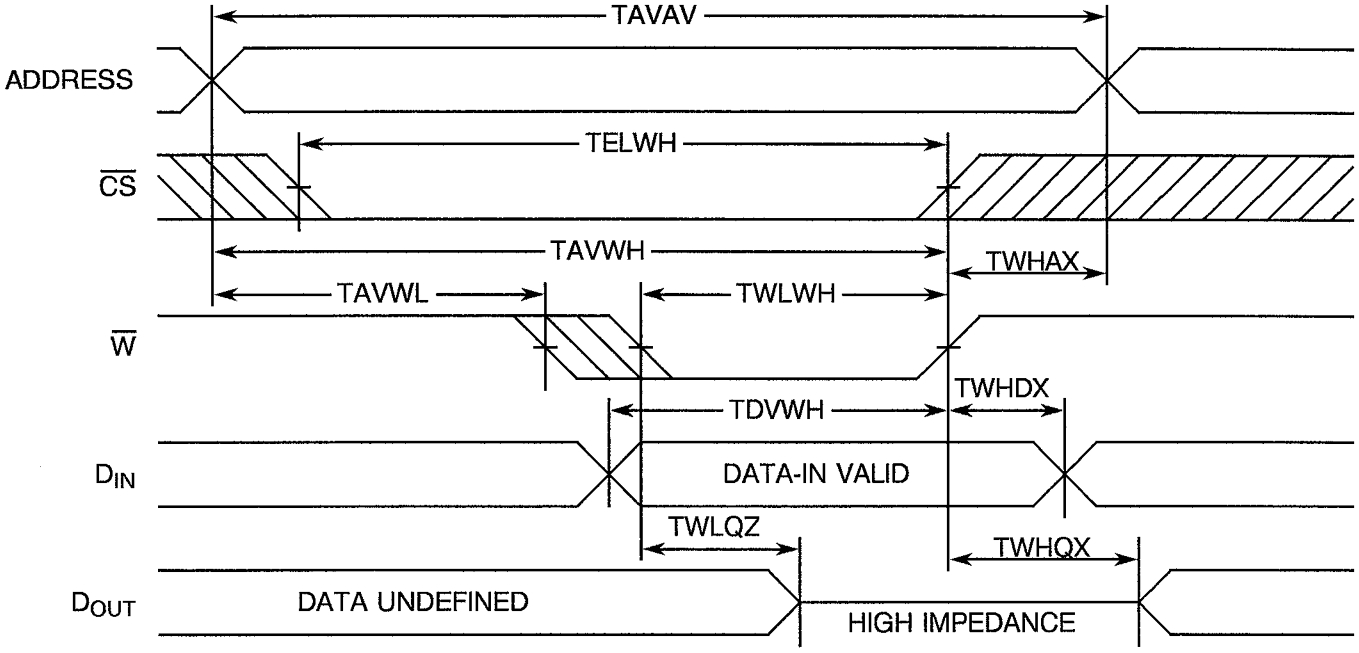


NOTES
1. W is High throughout Read Cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transition Low.

FIGURE 3(b) - TRUTH TABLE (CONTINUED)

TIMING WAVEFORMS (CONTINUED)

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



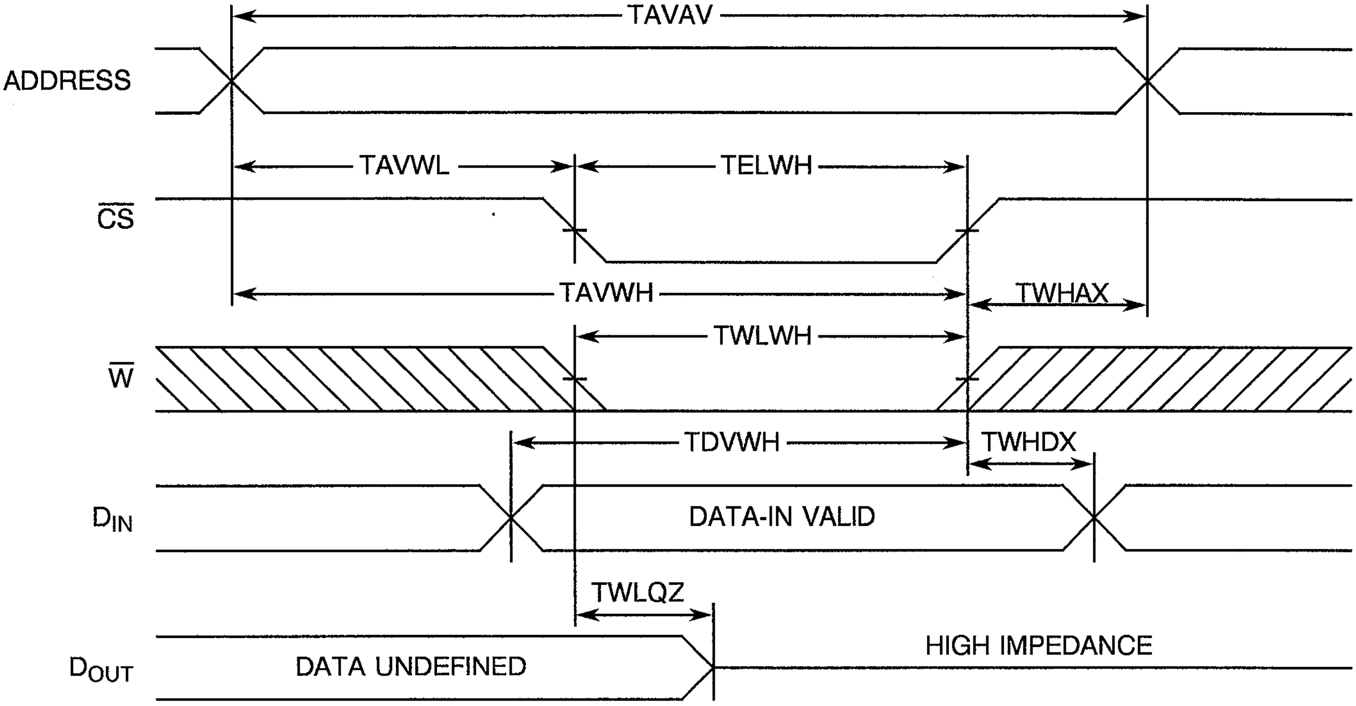
NOTES

1. The internal write time of the memory is defined by the overlap of $\overline{CS}$ Low and $\overline{W}$ Low. Both signals must be Low to initiate a write and either signal can terminate a write by going High. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

FIGURE 3(b) - TRUTH TABLE (CONTINUED)

TIMING WAVEFORMS (CONTINUED)

WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED)



NOTES

1. The internal write time of the memory is defined by the overlap of $\overline{CS}$ Low and $\overline{W}$ Low. Both signals must be Low to initiate a write and either signal can terminate a write by going High. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

FIGURE 3(c) - CIRCUIT SCHEMATIC

Not applicable.

FIGURE 3(d) - FUNCTIONAL DIAGRAM

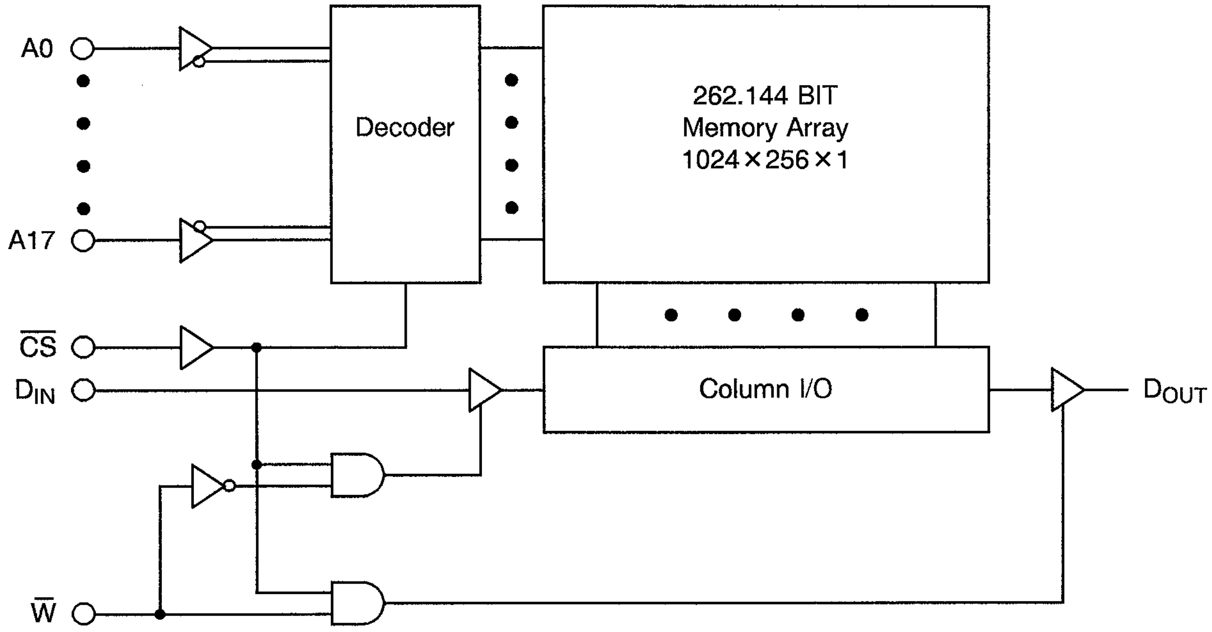
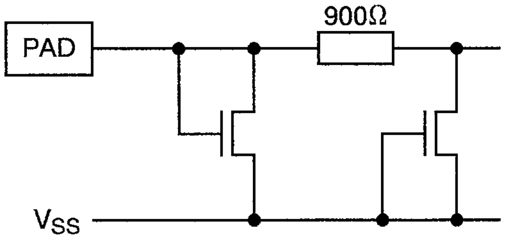
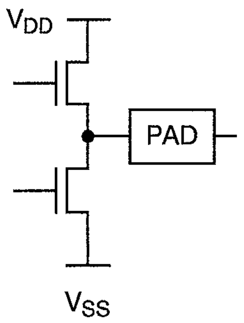


FIGURE 3(e) - INPUT/OUTPUT PROTECTION NETWORKS

EQUIVALENT OF EACH INPUT



EQUIVALENT OF EACH OUTPUT



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:

V_{IC} = Input Clamp Voltage.
I_{OZL} = Output Leakage Current Third State (Low Level Applied)
I_{OZH} = Output Leakage Current Third State (High Level Applied)
C_{IN} = Input Capacitance.
C_{OUT} = Output Capacitance
TAVAV = Cycle Time.
TAVQV = Address Access Time.
TAVQX = Output Change from Address Time.
TAVWH = Address Valid to End of Write.
TAVWL = Address Set-up Time.
TDVWH = Data Set-up Time.
TEHQZ = $\overline{CS}$ High Output Disable Time.
TELQV = $\overline{CS}$ Access Time.
TELQX = $\overline{CS}$ Low Output Enable Time.
TELWH = $\overline{CS}$ Low to End of Write.
TWHAX = Address Hold from Write End Time.
TWHDX = Data Hold Time.
TWHQX = $\overline{W}$ High Output Enable Time.
TWLQZ = $\overline{W}$ Low Output Disable Time.
TWLWH = $\overline{W}$ Low Pulse Width.
DR = Data Retention.
t_{CDR} = Chip Select to Start of Data Retention.
t_r = Recovery Time from Data Retention.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

(a) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during qualification and extension of qualification.

(b) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during procurement on a lot acceptance basis at the total dose irradiation level specified in the Purchase Order.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

(a) Para. 7.1.1(a), "High Temperature Reverse Bias" test and subsequent electrical measurements related to this test shall be omitted.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 3.5 grammes for the dual-in-line package and 4.0 grammes for the flat package.

4.4 MATERIALS AND FINISHES

The materials shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body and the lids shall be welded, brazed, preform-soldered or glass-frit-sealed.

4.4.2 Lead Material and Finish

For dual-in-line and flat packages, the material shall be Type 'G' with Type '2' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500.

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

4.5.2 Lead Identification

For dual-in-line and flat packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:

930103805BF

Detail Specification Number
Type Variant (see Table 1(a))
Testing Level (B or C, as applicable)
Total Dose Irradiation Level (if applicable)

The Total Dose Irradiation Level designation shall be added for those devices for which a sample has been successfully tested to the level in question. For these devices, a code letter shall be added in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ °C and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to Power Burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ), applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-in

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for Power Burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for Power Burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for High Temperature Reverse Bias Burn-in

Not applicable.

4.7.5 Electrical Circuits for Power Burn-in

Circuits for use in performing the Power Burn-in tests are shown in Figure 5(b) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP AND F = FP)	LIMITS		UNIT
						MIN	MAX	
1 to 7	Functional Test 1 (Nominal Inputs)	-	3014	3(b)	Verify Truth Table. For Input/Output Conditions and Test Patterns, see Note 1	-	-	-
8 to 12	Functional Test 2 (Worst Case Inputs)	-	3014	3(b)	Verify Truth Table. For Input/Output Conditions and Test Patterns, see Note 1	-	-	-
13	Functional Test 3 (Worst Case Outputs)	-	3014	3(b)	Verify Truth Table. For Input/Output Conditions and Test Patterns, see Note 1	-	-	-
14 to 34	Input Current Low Level	I_{IL}	3009	4(a)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 1-2-3-4-5-6-7-8-9-11-13-14-15-16-17-18-19-20-21-22-23) (Pins F 1-2-3-5-6-7-8-9-10-13-15-16-17-19-20-21-22-23-24-26-27)	-	−1.0	µA
35 to 55	Input Current High Level	I_{IH}	3010	4(b)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 1-2-3-4-5-6-7-8-9-11-13-14-15-16-17-18-19-20-21-22-23) (Pins F 1-2-3-5-6-7-8-9-10-13-15-16-17-19-20-21-22-23-24-26-27)		1.0	µA
56	Output Voltage Low Level	V_{OL}	3007	4(c)	V_{IL} = 0.8V, V_{IH} = 2.2V $V_{IN(\overline{CS})}$ = 0V, $V_{IN(\overline{W})}$ = 4.5V I_{OL} = 8.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 2 (Pin D 10) (Pin F 12)	-	0.4	V

NOTES: See Page 24.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP AND F = FP)	LIMITS		UNIT
						MIN	MAX	
57	Output Voltage High Level	V_{OH}	3007	4(d)	$V_{IL} = 0.8V$, $V_{IH} = 2.2V$ $V_{IN(\overline{CS})} = 0V$, $V_{IN(\overline{W})} = 4.5V$ $I_{OH} = -4.0mA$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 3 (Pin D 10) (Pin F 12)	2.4	-	V
58 to 78	Input Clamp Voltage (to V_{SS})	V_{IC}	3008	4(e)	I_{IN} (Under Test) = −200μA V_{IN} (Remaining Inputs) = 0V $V_{DD} = V_{SS} = 0V$ (Pins D 1-2-3-4-5-6-7-8-9-11-13-14-15-16-17-18-19-20-21-22-23) (Pins F 1-2-3-5-6-7-8-9-10-13-15-16-17-19-20-21-22-23-24-26-27)	−0.1	−1.9	V
79	Output Leakage Current Third State 1 (Low Level Applied)	I_{OZL1}	-	4(f)	$V_{IN(\overline{CS})} = 3.0V$, $V_{OUT} = 0V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ (Pin D 10) (Pin F 12)	-	−1.0	μA
80	Output Leakage Current Third State 1 (High Level Applied)	I_{OZH1}	-	4(f)	$V_{IN(\overline{CS})} = 3.0V$, $V_{OUT} = 5.5V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ (Pin D 10) (Pin F 12)	-	1.0	μA
81	Output Leakage Current Third State 2 (Low Level Applied)	I_{OZL2}	-	4(f)	$V_{IN(\overline{CS}, \overline{W})} = 0V$, $V_{OUT} = 0V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ (Pin D 10) (Pin F 12)	-	−1.0	μA
82	Output Leakage Current Third State 2 (High Level Applied)	I_{OZH2}	-	4(f)	$V_{IN(\overline{CS}, \overline{W})} = 0V$, $V_{OUT} = 5.5V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ (Pin D 10) (Pin F 12)	-	1.0	μA
83	Supply Current (Operating)	I_{DDop}	3005	4(g)	$V_{IN(\overline{W})} = 5.5V$ V_{IN} (Remaining Inputs) = 0V to 5.5V Pattern = ICCACT f = 5.0MHz, $I_{OUT} = 0mA$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 4 (Pin D 24) (Pin F 28)	-	70	mA

NOTES: See Page 24.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP AND F = FP)	LIMITS		UNIT
						MIN	MAX	
84	Supply Current 1 (Standby)	I_{DDSB1}	3005	4(g)	$V_{IN(\overline{CS})} = 2.2V$ V_{IN} (Remaining Inputs) = 0.8V $I_{OUT} = 0mA$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ (Pin D 24) (Pin F 28)	-	15	mA
85	Supply Current 2 (Standby)	I_{DDSB2}	3005	4(g)	$V_{IN(\overline{CS})} = V_{DD} - 0.3V$ V_{IN} (Remaining Inputs) = $V_{DD} - 0.3V$ to 0.3V $I_{OUT} = 0mA$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 5 (Pin D 24) (Pin F 28)	-	100	µA
86	Data Retention Current	I_{DDDR}	3005	4(h)	$V_{IL} = 0V$, $V_{IH} = 2.0V$ $V_{IN(\overline{CS})} = V_{DD} - 0.3V$ $I_{OUT} = 0mA$ $V_{DD} = 2.0V$, $V_{SS} = 0V$ Note 5 (Pin D 24) (Pin F 28)	-	80	µA
87	Data Retention	DR	-	-	$V_{IL} = 0V$, $V_{IH} = 2.0V$ $V_{IN(\overline{CS})} \geq V_{DD} - 0.3V$ $I_{OUT} = 0mA$ $V_{DD} = 2.0V$, $V_{SS} = 0V$ Note 6 (Pin D 10) (Pin F 12)	-	-	-

NOTES: See Page 24.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP AND F = FP)	LIMITS		UNIT
						MIN	MAX	
88 to 108	Input Capacitance	C_{IN}	3012	4(i)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 7 (Pins D 1-2-3-4-5-6-7-8-9-11-13-14-15-16-17-18-19-20-21-22-23) (Pins F 1-2-3-5-6-7-8-9-10-13-15-16-17-19-20-21-22-23-24-26-27)	-	5.0	pF
109	Output Capacitance	C_{OUT}	3012	4(j)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 7 (Pin D 10) (Pin F 12)	-	7.0	pF
110 to 115	Functional Test 4 (Nominal Inputs)	-	3014	3(b)	Verify Truth Table. For Input and Output Conditions, see Note 8 $V_{SS} = 0V$	-	-	-
116 to 117	Access Time (Address)	TAVQV	-	4(k)	V_{DD} = 4.5V and 5.5V $V_{SS} = 0V$ Notes 8 and 10 Variants 5-6 Variants 7-8	- -	55 45	ns
118 to 119	Access Time (Chip Select)	TELQV	-	4(k)	V_{DD} = 4.5V and 5.5V $V_{SS} = 0V$ Notes 8 and 10 Variants 5-6 Variants 7-8	- -	55 45	ns
120 to 121	Write Pulse Width ($\overline{W}$ Low)	TWLWH	-	4(k)	V_{DD} = 4.5V and 5.5V $V_{SS} = 0V$ Notes 8 and 10 Variants 5-6 Variants 7-8	- -	50 40	ns
122 to 123	Data Set-up Time	TDVWH	-	4(k)	V_{DD} = 4.5V and 5.5V $V_{SS} = 0V$ Notes 8 and 10	-	25	ns
124 to 125	Data Hold Time	TWHDX	-	4(k)	V_{DD} = 4.5V and 5.5V $V_{SS} = 0V$ Notes 8 and 10	0	-	ns

NOTES: See Page 24.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP AND F = FP)	LIMITS		UNIT
						MIN	MAX	
126 to 127	Read/Write Cycle Time	TAVAV	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 8 and 11			ns
					Variants 5-6	55	-	
					Variants 7-8	45	-	
128 to 129	Output Change from Address Cycle	TAVQX	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 8 and 11	5.0	-	ns
130 to 131	$\overline{CS}$ Low to End of Write	TELWH	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 8 and 11			ns
					Variants 5-6	50	-	
					Variants 7-8	40	-	
132 to 133	Address Set-up Time	TAVWL	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 8 and 11	0	-	ns
134 to 135	Address Valid to End of Write	TAVWH	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 8 and 11			ns
					Variants 5-6	50	-	
					Variants 7-8	40	-	
136 to 137	Address Hold from Write End	TWHAX	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 8 and 11	0	-	ns
138 to 139	Output Enable Time ($\overline{CS}$ Low)	TELQX	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8	5.0	-	ns
140 to 141	Output Disable Time ($\overline{CS}$ High)	TEHQZ	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8	-	15	ns
142 to 143	Output Disable Time ($\overline{W}$ Low)	TWLQZ	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8			ns
					Variants 5-6	20	-	
					Variants 7-8	15	-	
144 to 145	Output Enable Time ($\overline{W}$ High)	TWHQX	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8	0	-	ns

NOTES: See Page 24.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE (CONT'D)

NOTES

1. Functional test go-no-go with the following test sequences:-

FUNCTIONAL TEST 1

Pattern	Timing (1) (ns)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{OUT\ COMP}$ (V)
MARCH (2)	155	4.5 and 5.5	0	0	3.0	0.5	-0.5	1.5
CHECKERBOARD	155	4.5	0	0	3.0	0.5	-0.5	1.5
IMAG	155	4.5 and 5.5	0	0	3.0	0.5	-0.5	1.5
LONG CHIP SELECT	155	4.5 and 5.5	0	0	3.0	0.5	-0.5	1.5

FUNCTIONAL TEST 2

Pattern	Timing (1) (ns)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{OUT\ COMP}$ (V)
MARCH	155	5.5	0	-0.5	5.8	0.5	-0.5	1.5
MARCH	155	6.0	0	0	6.0	0.5	-0.5	1.5
MARCH	155	4.0	0	0	4.0	0.5	-0.5	1.5
MARCH	155	5.5	0	0	2.2	0.5	-0.5	1.5
MARCH	155	4.5	0	0.8	3.0	0.5	-0.5	1.5

FUNCTIONAL TEST 3

Pattern	Timing (1) (ns)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{OUT\ COMP}$ (V)
MARCH	155	4.5	0	0	3.0	4.0	-1.0	(3)

N.B.

1. A Write cycle is followed by a Read cycle. The time between start of Write according to Figure 3(b) and start of Read is the specified "Timing" parameter.
2. $\overline{CS}$ Low, Gray Code, TWMAX = 70ns.
3. 0.4V for Low Output Level
   2.4V for High Output Level.

2. Select Address Inputs to produce low level output at the pin under test in accordance with Figure 3(b).

3. Select Address Inputs to produce high level output at the pin under test in accordance with Figure 3(b).

4. Derating is 10mA/MHz.

5. Measurement is performed with the memory loaded with a background of zero and then with a background of ones. For all inputs high then low. Only the worst case is recorded.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE (CONT'D)

NOTES

6. Data Retention Procedure:-
   - (a) Write Memory with Checkerboard pattern with Timing = 155ns at the conditions given.
   - (b) Power Down to $V_{DD} = 1.6 \pm 0V$ for 250ms. (This is a test condition only. Memory retention cannot be guaranteed if V_{DD} is reduced below 2.0V).
   - (c) Restore to original condition given, read Memory and compare with original pattern.
   - (d) Repeat the procedure with $\overline{\text{Checkerboard}}$ pattern with Timing = 155ns at the conditions given.
   - (e) For Variants 05, 06: $t_r = 55ns$.
     For Variants 07, 08: $t_r = 45ns$.

7. Guaranteed but not tested. Characterised at initial design and after major process changes.

8. **FUNCTIONAL TEST 4**

Pattern	Timing (1) (ns) Variants 5-6	Timing (1) (ns) Variants 7-8	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	$V_{OUT\ COMP}$ (V)
MARCH/COMARCH	145	120	4.5	0	0	3.0	0.5	-0.5	1.5
IMAG	145	120	4.5	0	0	3.0	0.5	-0.5	1.5
MARCH/COMARCH	145	120	5.5	0	0	3.0	0.5	-0.5	1.5
IMAG	200	165	4.5	0	0	3.0	0.5	-0.5	1.5

N.B.

1. A Write cycle is followed by a Read cycle. The time between start of Write according to Figure 3(b) and start of Read is the specified "Timing" parameter.
2. Output load 1 TTL Gate equivalent + $C_L \leq 30pF$.
   $t_r = t_f = 5.0ns$ max.

9. Tested go-no-go using MARCH and IMAG patterns.

10. Parameters measured using MARCH pattern during Functional Test 4.

11. Parameters tested go-no-go during Functional Test 4.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP AND F = FP)	LIMITS		UNIT
						MIN	MAX	
1 to 7	Functional Test 1 (Nominal Inputs)	-	3014	3(b)	Verify Truth Table. For Input/Output Conditions and Test Patterns, see Note 1	-	-	-
8 to 12	Functional Test 2 (Worst Case Inputs)	-	3014	3(b)	Verify Truth Table. For Input/Output Conditions and Test Patterns, see Note 1	-	-	-
13	Functional Test 3 (Worst Case Outputs)	-	3014	3(b)	Verify Truth Table. For Input/Output Conditions and Test Patterns, see Note 1	-	-	-
14 to 34	Input Current Low Level	I_{IL}	3009	4(a)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 1-2-3-4-5-6-7-8-9-11-13-14-15-16-17-18-19-20-21-22-23) (Pins F 1-2-3-5-6-7-8-9-10-13-15-16-17-19-20-21-22-23-24-26-27)	-	− 1.0	µA
35 to 55	Input Current High Level	I_{IH}	3010	4(b)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins D 1-2-3-4-5-6-7-8-9-11-13-14-15-16-17-18-19-20-21-22-23) (Pins F 1-2-3-5-6-7-8-9-10-13-15-16-17-19-20-21-22-23-24-26-27)		1.0	µA
56	Output Voltage Low Level	V_{OL}	3007	4(c)	V_{IL} = 0.8V, V_{IH} = 2.2V $V_{IN(\overline{CS})}$ = 0V, $V_{IN(\overline{W})}$ = 4.5V I_{OL} = 8.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 2 (Pin D 10) (Pin F 12)	-	0.4	V

NOTES: See Page 24.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP AND F = FP)	LIMITS		UNIT
						MIN	MAX	
57	Output Voltage High Level	V_{OH}	3007	4(d)	$V_{IL} = 0.8V$, $V_{IH} = 2.2V$ $V_{IN(\overline{CS})} = 0V$, $V_{IN(\overline{W})} = 4.5V$ $I_{OH} = -4.0mA$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 3 (Pin D 10) (Pin F 12)	2.4	-	V
58 to 78	Input Clamp Voltage (to V_{SS})	V_{IC}	3008	4(e)	I_{IN} (Under Test) = $-200\mu A$ V_{IN} (Remaining Inputs) = 0V $V_{DD} = V_{SS} = 0V$ (Pins D 1-2-3-4-5-6-7-8-9-11-13-14-15-16-17-18-19-20-21-22-23) (Pins F 1-2-3-5-6-7-8-9-10-13-15-16-17-19-20-21-22-23-24-26-27)	− 0.1	− 1.9	V
79	Output Leakage Current Third State 1 (Low Level Applied)	I_{OZL1}	-	4(f)	$V_{IN(\overline{CS})} = 3.0V$, $V_{OUT} = 0V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ (Pin D 10) (Pin F 12)	-	− 1.0	µA
80	Output Leakage Current Third State 1 (High Level Applied)	I_{OZH1}	-	4(f)	$V_{IN(\overline{CS})} = 3.0V$, $V_{OUT} = 5.5V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ (Pin D 10) (Pin F 12)	-	1.0	µA
81	Output Leakage Current Third State 2 (Low Level Applied)	I_{OZL2}	-	4(f)	$V_{IN(\overline{CS}, \overline{W})} = 0V$, $V_{OUT} = 0V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ (Pin D 10) (Pin F 12)	-	− 1.0	µA
82	Output Leakage Current Third State 2 (High Level Applied)	I_{OZH2}	-	4(f)	$V_{IN(\overline{CS}, \overline{W})} = 0V$, $V_{OUT} = 5.5V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ (Pin D 10) (Pin F 12)	-	1.0	µA
83	Supply Current (Operating)	I_{DDop}	3005	4(g)	$V_{IN(\overline{W})} = 5.5V$ V_{IN} (Remaining Inputs) = 0V to 5.5V Pattern = ICCACT f = 5.0MHz, $I_{OUT} = 0mA$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 4 (Pin D 24) (Pin F 28)	-	70	mA

NOTES: See Page 24.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP AND F = FP)	LIMITS		UNIT
						MIN	MAX	
84	Supply Current 1 (Standby)	I_{DDSB1}	3005	4(g)	$V_{IN(\overline{CS})} = 2.2V$ V_{IN} (Remaining Inputs) = 0.8V $I_{OUT} = 0mA$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ (Pin D 24) (Pin F 28)	-	15	mA
85	Supply Current 2 (Standby)	I_{DDSB2}	3005	4(g)	$V_{IN(\overline{CS})} = V_{DD} - 0.3V$ V_{IN} (Remaining Inputs) $= V_{DD} - 0.3V$ to 0.3V $I_{OUT} = 0mA$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 5 (Pin D 24) (Pin F 28)	-	100	µA
86	Data Retention Current	I_{DDDR}	3005	4(h)	$V_{IL} = 0V$, $V_{IH} = 2.0V$ $V_{IN(\overline{CS})} = V_{DD} - 0.3V$ $I_{OUT} = 0mA$ $V_{DD} = 2.0V$, $V_{SS} = 0V$ Note 5 (Pin D 24) (Pin F 28)	-	80	µA
87	Data Retention	DR	-	-	$V_{IL} = 0V$, $V_{IH} = 2.0V$ $V_{IN(\overline{CS})} \geq V_{DD} - 0.3V$ $I_{OUT} = 0mA$ $V_{DD} = 2.0V$, $V_{SS} = 0V$ Note 6 (Pin D 10) (Pin F 12)	-	-	-

NOTES: See Page 24.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP AND F = FP)	LIMITS		UNIT
						MIN	MAX	
88 to 108	Input Capacitance	C_{IN}	3012	4(i)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 7 (Pins D 1-2-3-4-5-6-7-8-9-11-13-14-15-16-17-18-19-20-21-22-23) (Pins F 1-2-3-5-6-7-8-9-10-13-15-16-17-19-20-21-22-23-24-26-27)	-	5.0	pF
109	Output Capacitance	C_{OUT}	3012	4(j)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 7 (Pin D 10) (Pin F 12)	-	7.0	pF
110 to 115	Functional Test 4 (Nominal Inputs)	-	3014	3(b)	Verify Truth Table. For Input and Output Conditions, see Note 8 $V_{SS} = 0V$	-	-	-
116 to 117	Access Time (Address)	TAVQV	-	4(k)	$V_{DD} = 4.5V$ and 5.5V $V_{SS} = 0V$ Notes 8 and 10 Variants 5-6 Variants 7-8	- -	55 45	ns
118 to 119	Access Time (Chip Select)	TELQV	-	4(k)	$V_{DD} = 4.5V$ and 5.5V $V_{SS} = 0V$ Notes 8 and 10 Variants 5-6 Variants 7-8	- -	55 45	ns
120 to 121	Write Pulse Width ($\overline{W}$ Low)	TWLWH	-	4(k)	$V_{DD} = 4.5V$ and 5.5V $V_{SS} = 0V$ Notes 8 and 10 Variants 5-6 Variants 7-8	- -	50 40	ns
122 to 123	Data Set-up Time	TDVWH	-	4(k)	$V_{DD} = 4.5V$ and 5.5V $V_{SS} = 0V$ Notes 8 and 10	-	25	ns
124 to 125	Data Hold Time	TWHDX	-	4(k)	$V_{DD} = 4.5V$ and 5.5V $V_{SS} = 0V$ Notes 8 and 10	0	-	ns

NOTES: See Page 24.

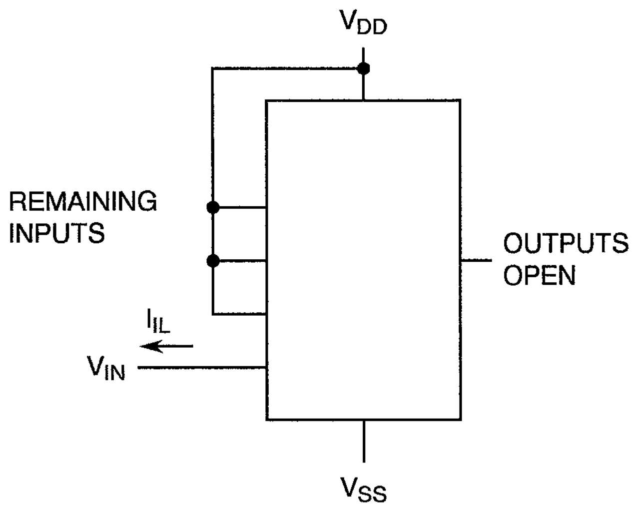
TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D = DIP AND F = FP)	LIMITS		UNIT
						MIN	MAX	
126 to 127	Read/Write Cycle Time	TAVAV	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 8 and 11 Variants 5-6 Variants 7-8	55 45	- -	ns
128 to 129	Output Change from Address Cycle	TAVQX	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 8 and 11	5.0	-	ns
130 to 131	$\overline{\text{CS}}$ Low to End of Write	TELWH	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 8 and 11 Variants 5-6 Variants 7-8	50 40	- -	ns
132 to 133	Address Set-up Time	TAVWL	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 8 and 11	0	-	ns
134 to 135	Address Valid to End of Write	TAVWH	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 8 and 11 Variants 5-6 Variants 7-8	50 40	- -	ns
136 to 137	Address Hold from Write End	TWHAX	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 8 and 11	0	-	ns
138 to 139	Output Enable Time ($\overline{\text{CS}}$ Low)	TELQX	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8	5.0	-	ns
140 to 141	Output Disable Time ($\overline{\text{CS}}$ High)	TEHQZ	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8	-	15	ns
142 to 143	Output Disable Time ($\overline{\text{W}}$ Low)	TWLQZ	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 5-6 Variants 7-8	20 15	- -	ns
144 to 145	Output Enable Time ($\overline{\text{W}}$ High)	TWHQX	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8	0	-	ns

NOTES: See Page 24.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

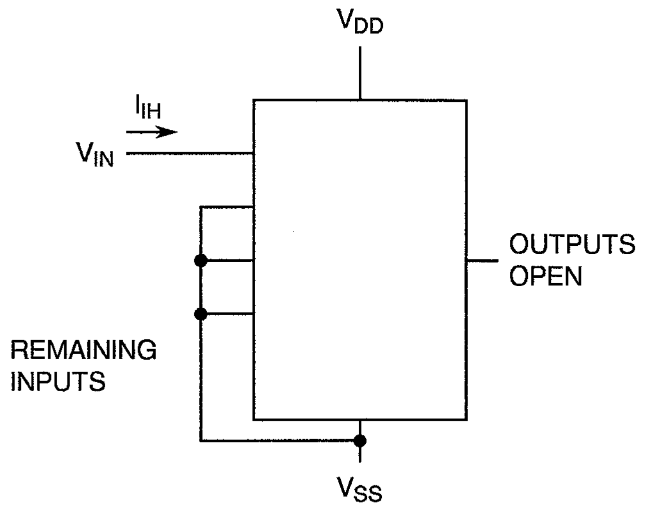
FIGURE 4(a) - INPUT CURRENT LOW LEVEL



NOTES

1. Each input to be tested separately.

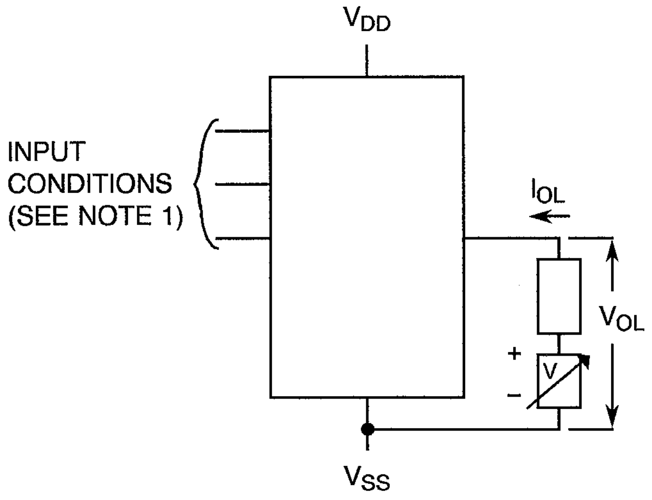
FIGURE 4(b) - INPUT CURRENT HIGH LEVEL



NOTES

1. Each input to be tested separately.

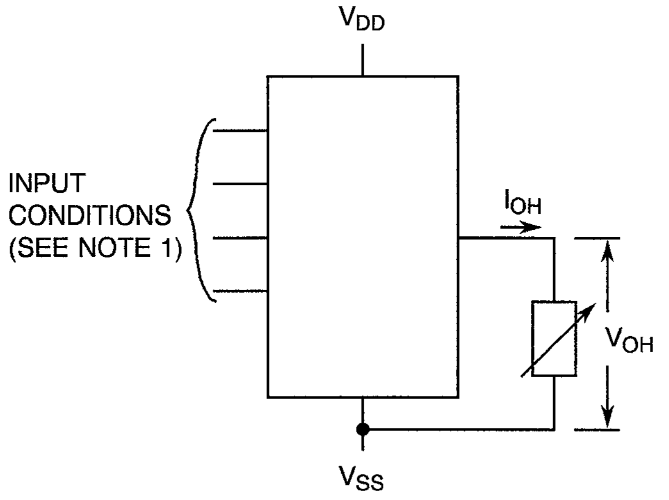
FIGURE 4(c) - OUTPUT VOLTAGE LOW LEVEL



NOTES

1. See Note 2 to Table 2.
2. Each output to be tested separately.

FIGURE 4(d) - OUTPUT VOLTAGE HIGH LEVEL

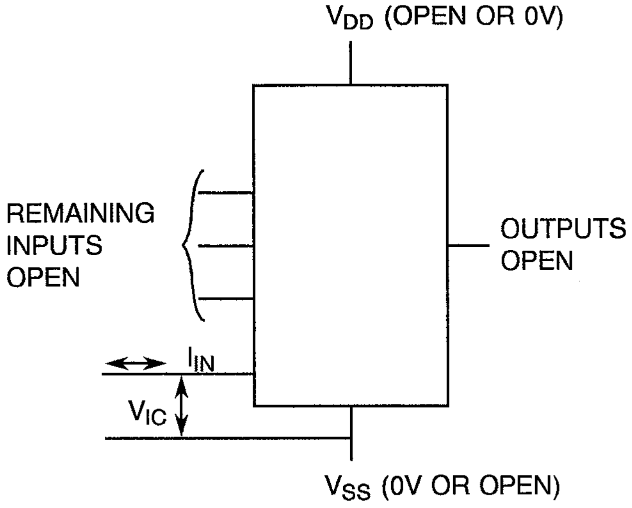


NOTES

1. See Note 3 to Table 2.
2. Each output to be tested separately.

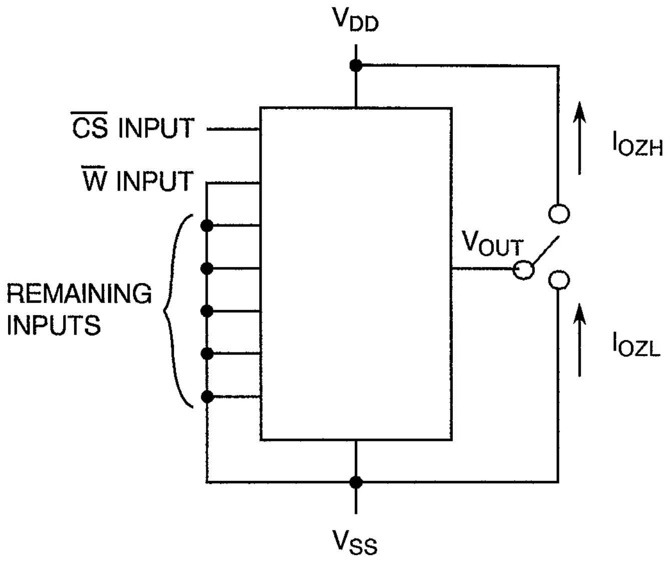
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(e) - INPUT CLAMP VOLTAGE



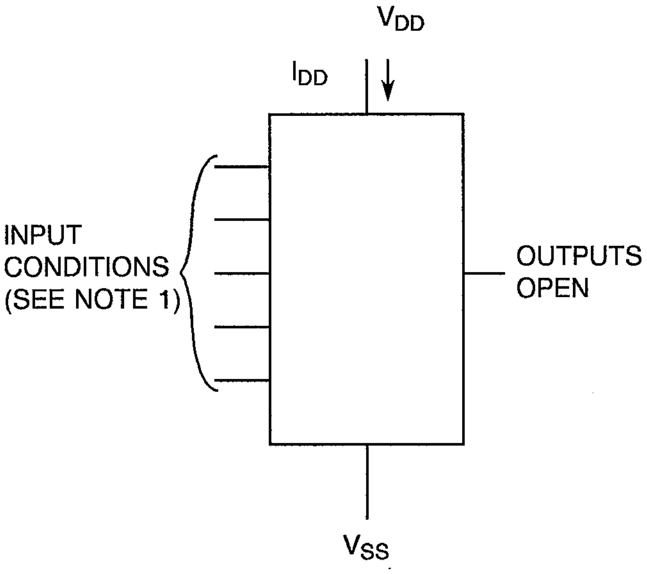
NOTES
1. Each input to be tested separately.

FIGURE 4(f) - OUTPUT LEAKAGE CURRENT THIRD STATE



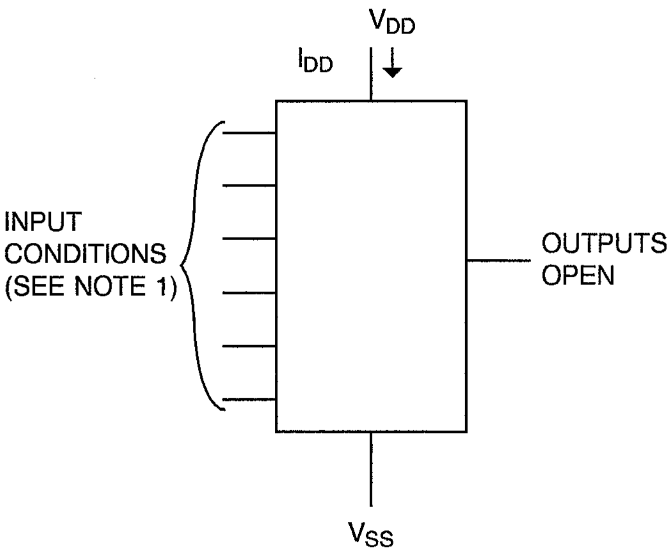
NOTES
1. Each output to be tested separately.

FIGURE 4(g) - SUPPLY CURRENT



NOTES
1. As per Table 2 or 3.

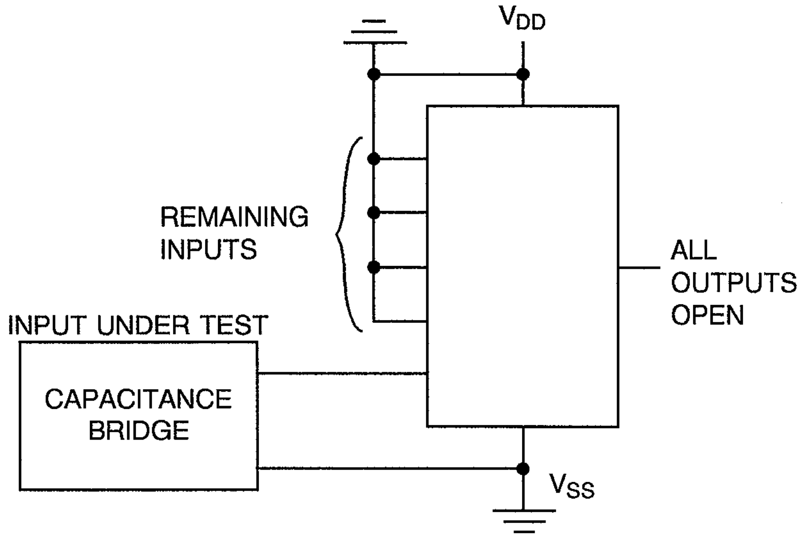
FIGURE 4(h) - DATA RETENTION CURRENT



NOTES
1. Procedure as per Note 6 to Table 2.

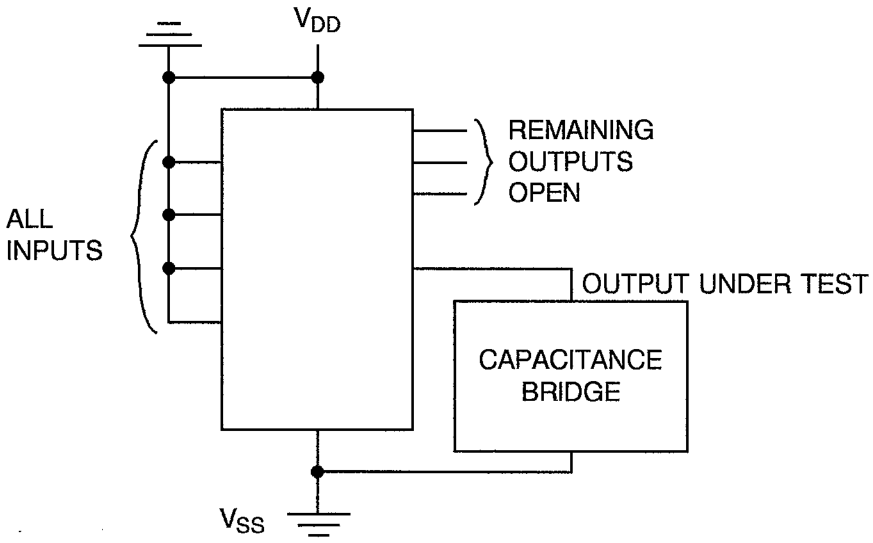
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - INPUT CAPACITANCE



NOTES
1. Each input to be tested separately.
2. f = 100kHz to 1MHz.

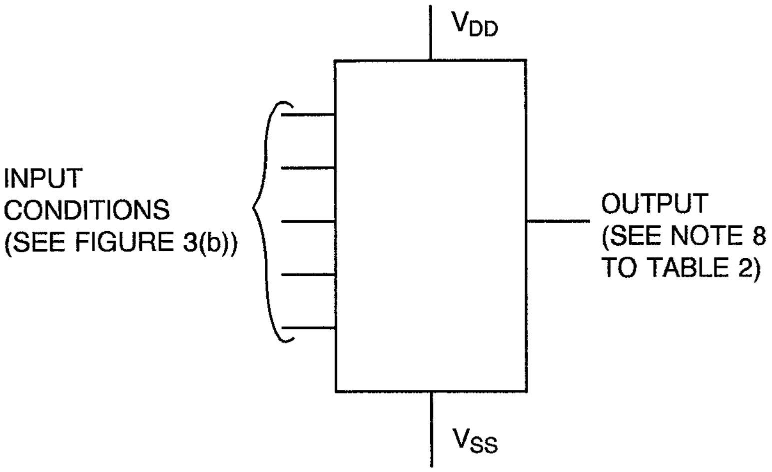
FIGURE 4(j) - OUTPUT CAPACITANCE



NOTES
1. Each output to be tested separately.
2. f = 100kHz to 1MHz.

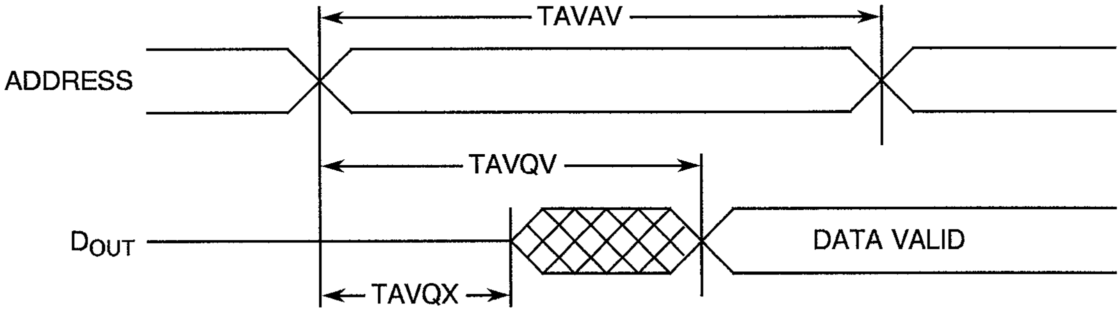
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(k) - PROPAGATION DELAY



VOLTAGE WAVEFORMS

READ CYCLE 1



READ CYCLE 2

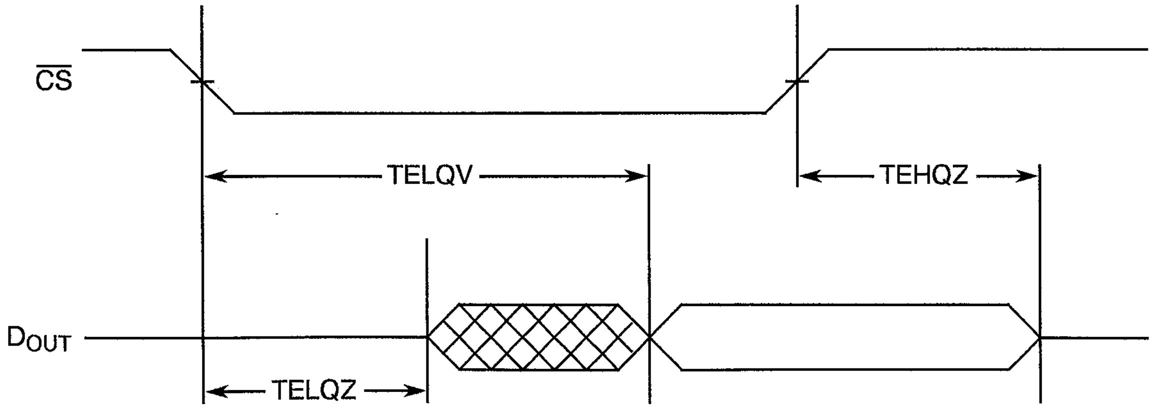
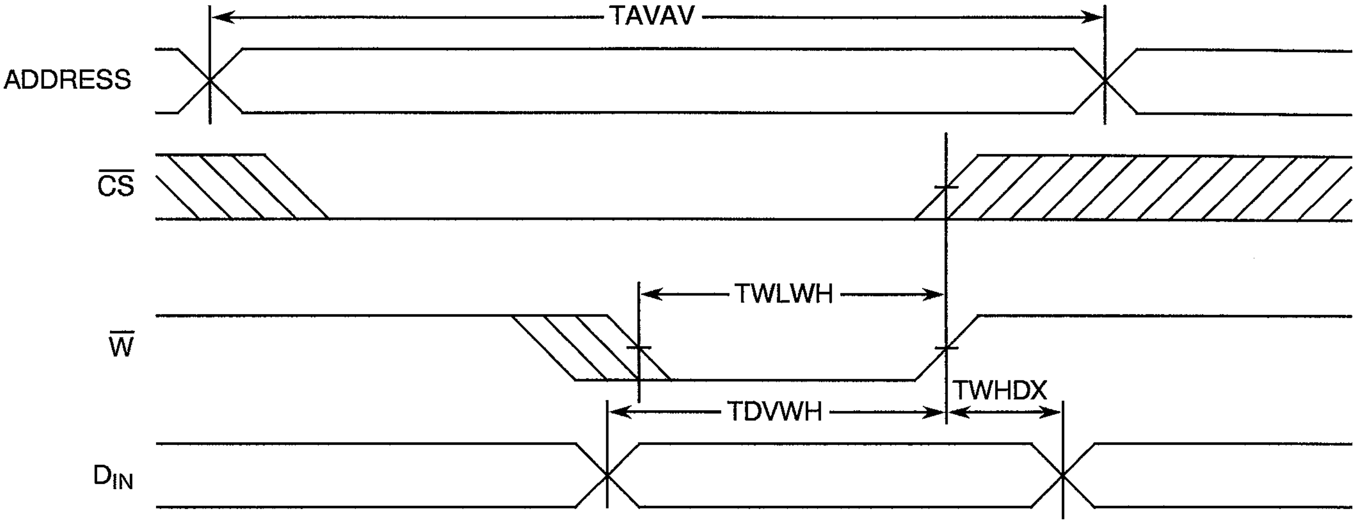


FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

VOLTAGE WAVEFORMS (CONTINUED)

WRITE CYCLE 1



WRITE CYCLE 2

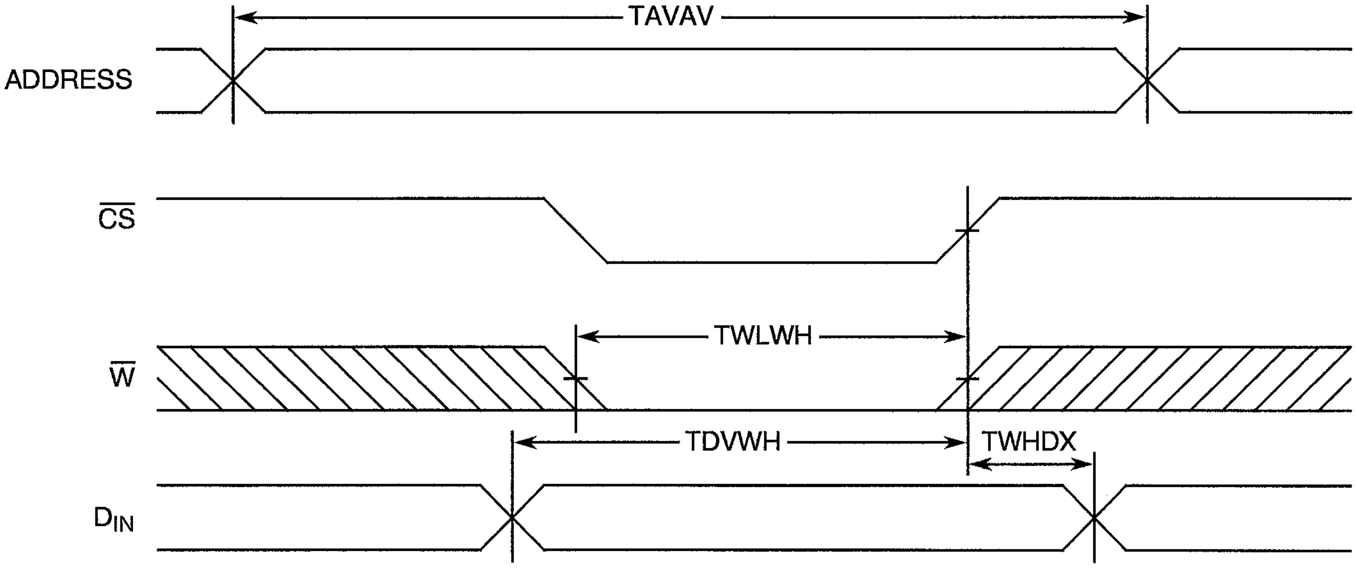


TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
14 to 34	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	± 100	nA
35 to 55	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	± 100	nA
56	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	± 100	mV
57	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	± 100	mV
79	Output Leakage Current Third State 1 (Low Level Applied)	I_{OZL1}	As per Table 2	As per Table 2	± 100	nA
80	Output Leakage Current Third State 1 (High Level Applied)	I_{OZH1}	As per Table 2	As per Table 2	± 100	nA
81	Output Leakage Current Third State 2 (Low Level Applied)	I_{OZL2}	As per Table 2	As per Table 2	± 100	nA
82	Output Leakage Current Third State 2 (High Level Applied)	I_{OZH2}	As per Table 2	As per Table 2	± 100	nA
84	Supply Current 1 (Standby)	I_{DDSB1}	As per Table 2	As per Table 2	± 1.5	mA
85	Supply Current 2 (Standby)	I_{DDSB2}	As per Table 2	As per Table 2	± 10	µA
86	Data Retention Current	I_{DDDR}	As per Table 2	As per Table 2	± 5.0	µA

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0−5)	°C
2	Output - (Pin D 10) (Pin F 12)	V_{OUT}	V_{SS}	V
3	Inputs - (Pins D 1-2-3-4-5-6-7-8-9-14-15-16-17-18-19-20-21-22-23) (Pins F 1-2-3-5-6-7-8-9-10-16-17-19-20-21-22-23-24-26-27)	V_{IN}	f0 to f14 as per Figure 5 (Note 1)	Vac
4	Input - (Pin D 13) (Pin F 15)	V_{IN}	V_{SS}	Vac
5	Input - (Pin D 11) (Pin F 13)	V_{IN}	$\overline{W}$ (Note 2)	Vac
6	Pulse Voltage	V_{GEN}	0V to V_{DD}	Vac
7	Pulse Frequency Square Wave	f0	275k ± 20% 50 ± 15% Duty Cycle	Hz
8	Positive Supply Voltage (Pin D 24) (Pin F 28)	V_{DD}	5.0(+0.5−0)	V
9	Negative Supply Voltage (Pin D 12) (Pin F 14)	V_{SS}	0	V

NOTES

1. $f_n = 1/2\ (f_n - 1)$.
2. Input Timing.

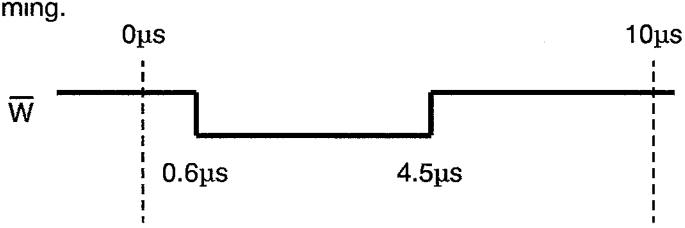
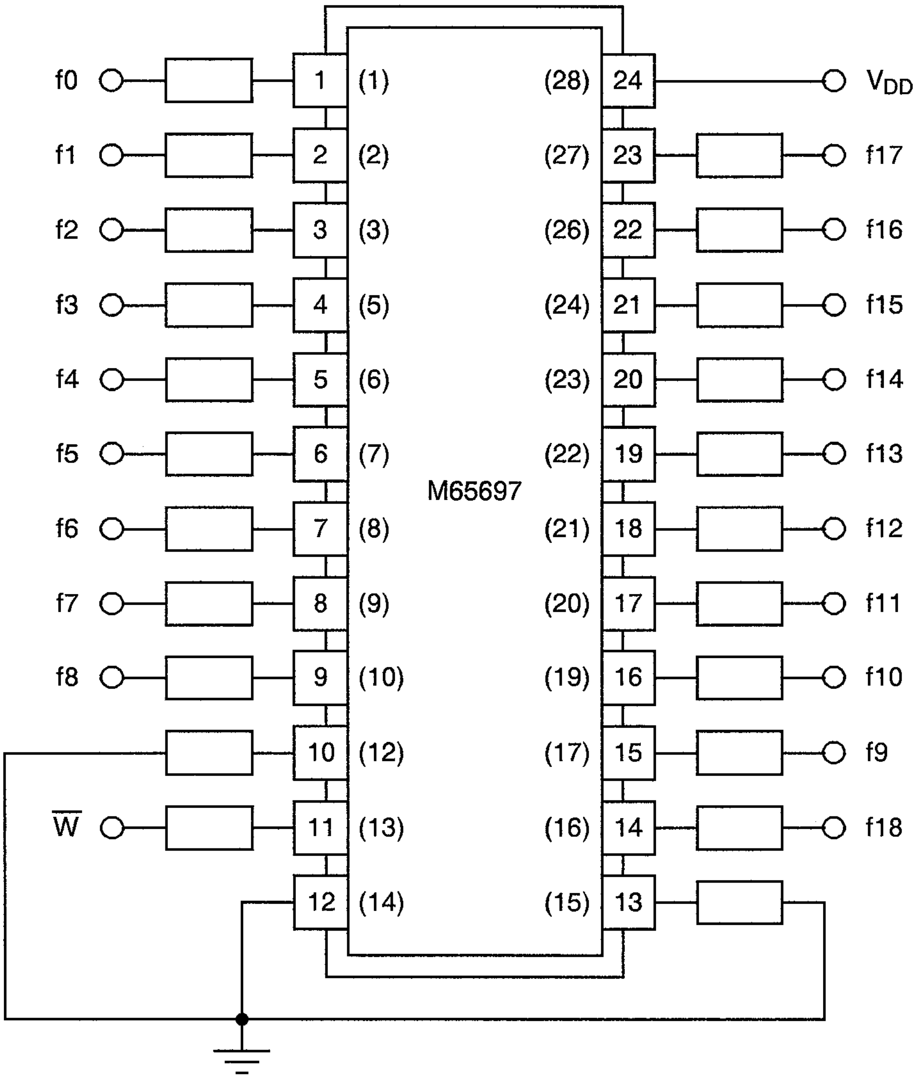


FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



NOTES

1. Input Protection Resistor = 1.0kΩ.
2. Pin numbers in parenthesis are for flat package.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION No. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(b) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

4.9 TOTAL DOSE IRRADIATION TESTING

4.9.1 Application

If specified in Para. 4.2.1 of this specification, total dose irradiation testing shall be performed in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.9.2 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6 of this specification.

4.9.3 Electrical Measurements

The parameters to be measured prior to irradiation exposure are scheduled in Table 2 of this specification. Only devices which meet the requirements of Table 2 shall be included in the test sample.

The parameters to be measured during and on completion of irradiation testing are scheduled in Table 7 of this specification.

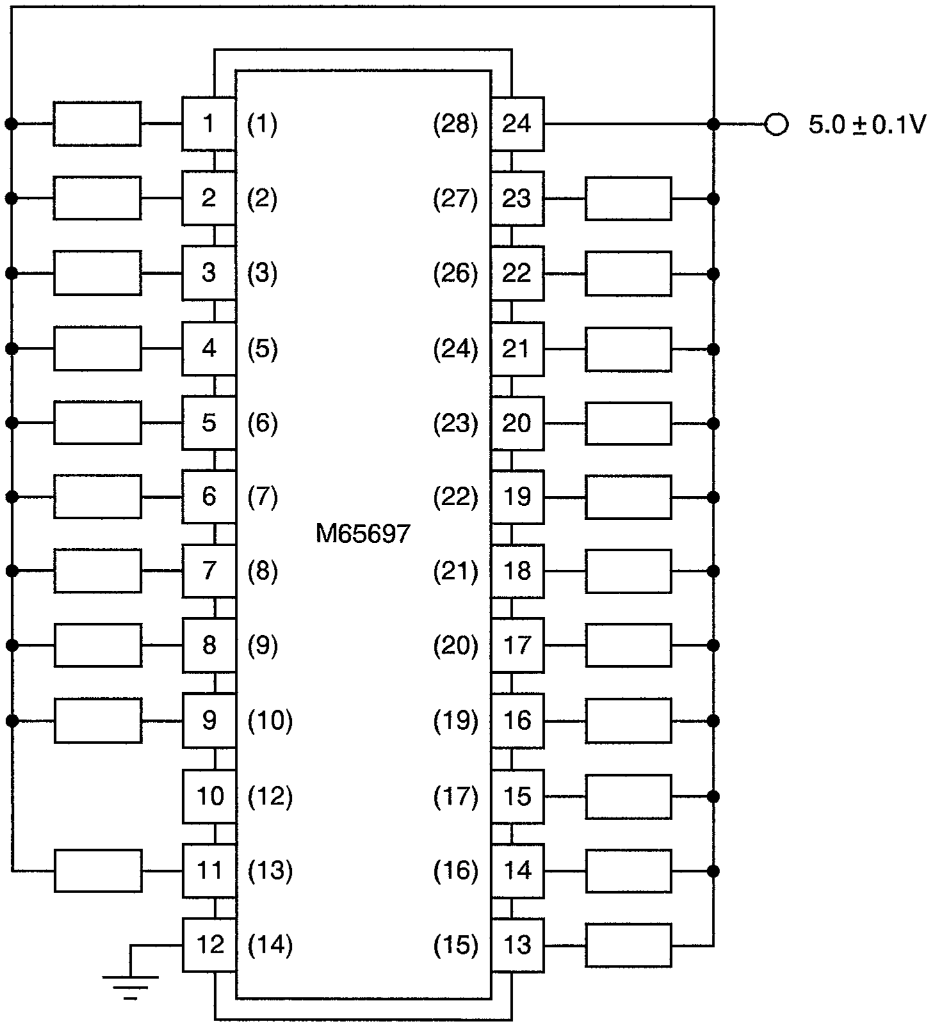
TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	ABSOLUTE LIMITS		UNIT
						MIN	MAX	
1 to 7	Functional Test 1 (Nominal Inputs)	-	As per Table 2	As per Table 2	-	-	-	-
8 to 12	Functional Test 2 (Worst Case Inputs)	-	As per Table 2	As per Table 2	-	-	-	-
13	Functional Test 3 (Worst Case Outputs)	-	As per Table 2	As per Table 2	-	-	-	-
14 to 34	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	±0.1	-	−1.0	µA
35 to 55	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	±0.1	-	1.0	µA
56	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	±0.1	-	0.4	V
57	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	±0.1	2.4	-	V
58 to 78	Input Clamp Voltage (to V_{SS})	V_{IC}	As per Table 2	As per Table 2	-	−2.0	−0.2	V
79	Output Leakage Current Third State 1 (Low Level Applied)	I_{OZL1}	As per Table 2	As per Table 2	±0.1	-	−1.0	µA
80	Output Leakage Current Third State 1 (High Level Applied)	I_{OZH1}	As per Table 2	As per Table 2	±0.1	-	1.0	µA
81	Output Leakage Current Third State 2 (Low Level Applied)	I_{OZL2}	As per Table 2	As per Table 2	±0.1	-	−1.0	µA
82	Output Leakage Current Third State 2 (High Level Applied)	I_{OZH2}	As per Table 2	As per Table 2	±0.1	-	1.0	µA
83	Supply Current (Operating)	I_{DDop}	As per Table 2	As per Table 2	-	-	70	mA
84	Supply Current 1 (Standby)	I_{DDSB1}	As per Table 2	As per Table 2	-	-	15	mA
85	Supply Current 2 (Standby)	I_{DDSB2}	As per Table 2	As per Table 2	±10	-	100	µA

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	ABSOLUTE LIMITS		UNIT
						MIN	MAX	
86	Data Retention Current	I_{DDDR}	As per Table 2	As per Table 2	-	-	80	µA
87	Data Retention	DR	As per Table 2	As per Table 2	-	-	-	-

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING



NOTES

1. Input Protection Resistor = 1.0kΩ.
2. Pin numbers in parenthesis are for flat package.

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
1 to 7	Functional Test 1 (Nominal Inputs)	-	As per Table 2	As per Table 2	-	-	-
14 to 34	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	-	−5.0	µA
35 to 55	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	-	5.0	µA
56	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	-	0.4	V
57	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	2.4	-	V
79	Output Leakage Current Third State 1 (Low Level Applied)	I_{OZL1}	As per Table 2	As per Table 2	-	−5.0	µA
80	Output Leakage Current Third State 1 (High Level Applied)	I_{OZH1}	As per Table 2	As per Table 2	-	5.0	µA
81	Output Leakage Current Third State 2 (Low Level Applied)	I_{OZL2}	As per Table 2	As per Table 2	-	−5.0	µA
82	Output Leakage Current Third State 2 (High Level Applied)	I_{OZH2}	As per Table 2	As per Table 2	-	5.0	µA
85	Supply Current 2 (Standby)	I_{DDSB2}	As per Table 2	As per Table 2	-	5.0	mA

<u>APPENDIX 'A'</u>

AGREED DEVIATIONS FOR MATRA-MHS (F)

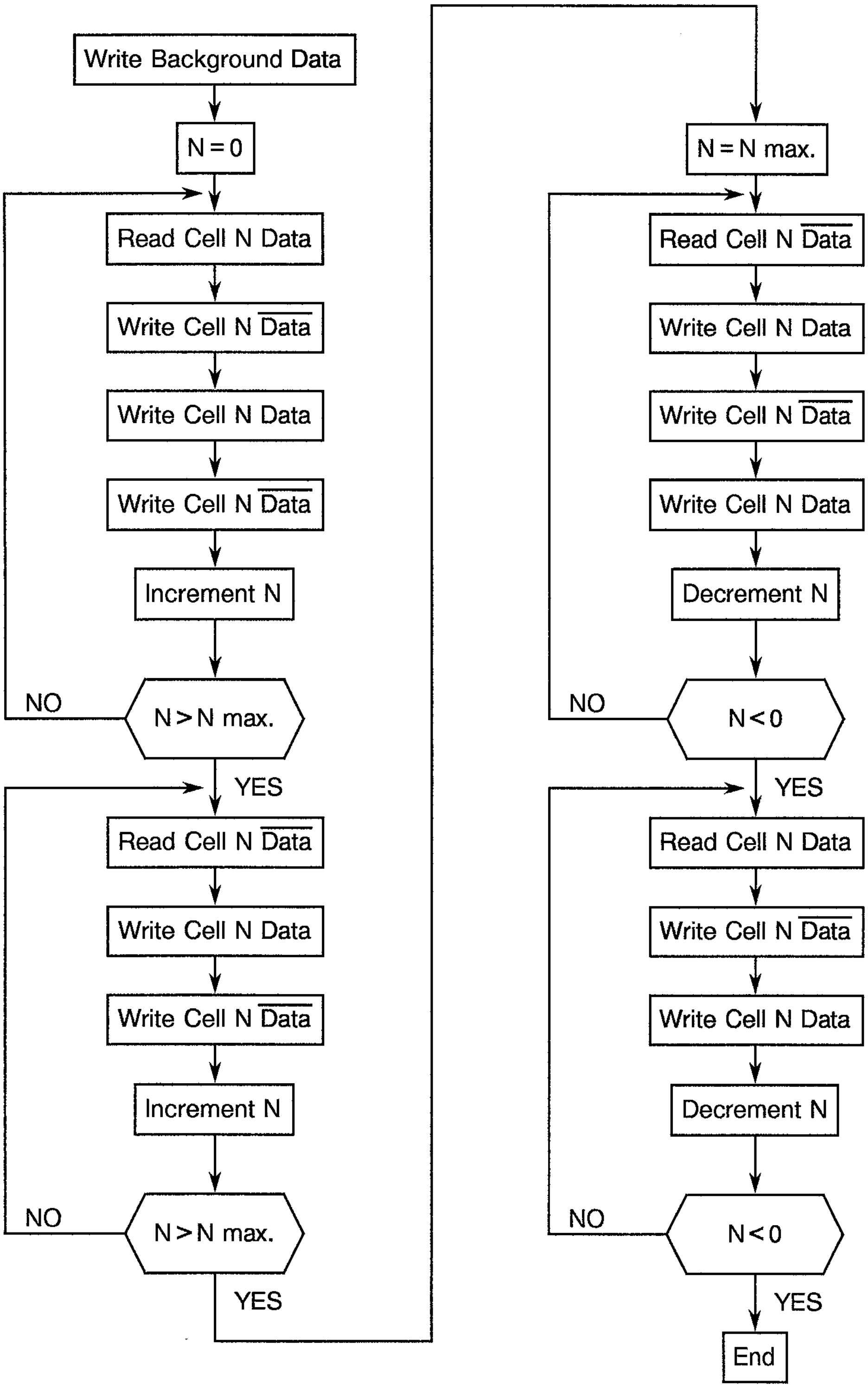
ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.2	Para. 9.9.3, "Electrical Measurements at Room Temperature". May be performed at High Temperature.
Para. 4.2.4 and 4.2.5	Para. 9.9.4, "Electrical Measurements at Room Temperature". May be performed in accordance with Table 2, but Parameter Drift Values must be calculated in accordance with Table 6 of this specification

The following test patterns may be used:-

1. ICCACT Pattern
   (a) Write loop pattern between N min. and N max.
2. LONG CHIP SELECT Pattern
   (a) Checkerboard pattern with timing unspecified.

APPENDIX 'A'

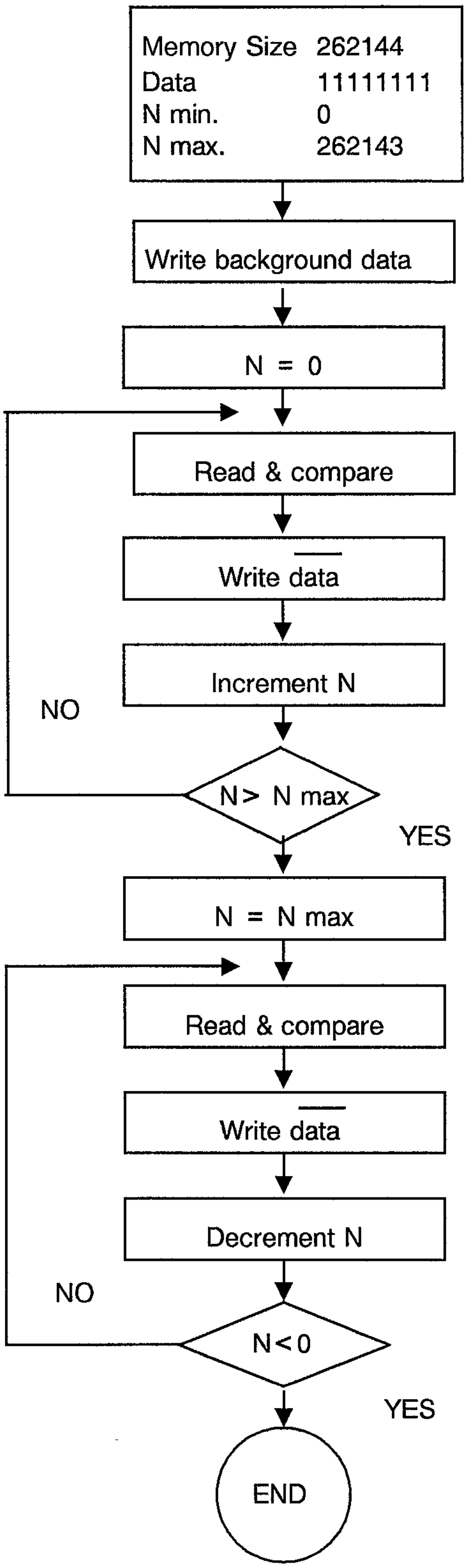
3. IMAG Pattern



Memory Size (Address space) = 262144
Data = 1111 1111
N Max. = 262143

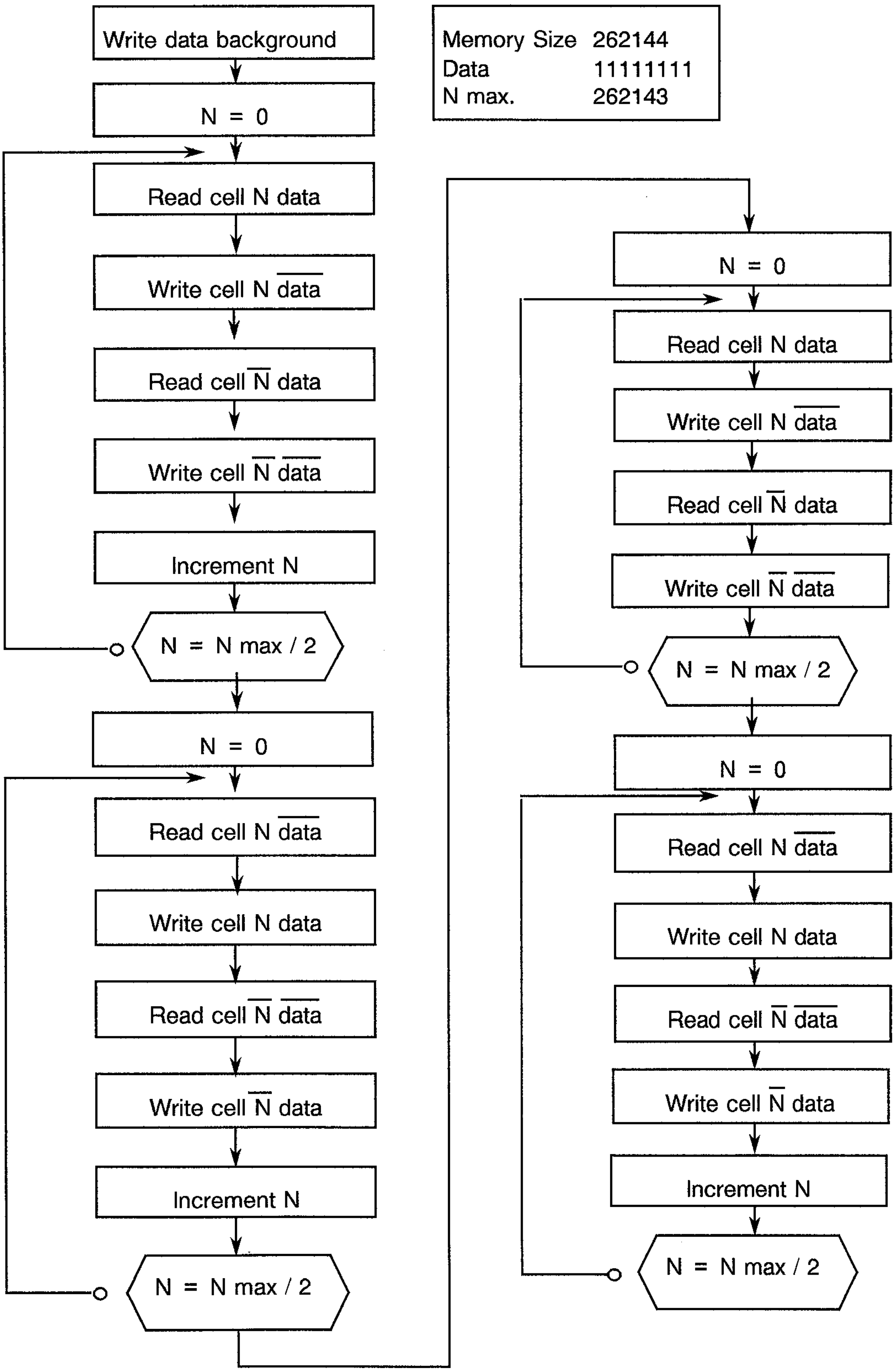
APPENDIX 'A'

4. MARCH Pattern



APPENDIX 'A'

5. COMARCH Pattern



6. CHECKERBOARD Pattern