INTEGRATED CIRCUITS, MONOLITHIC,

SILICON ON SAPPHIRE, CMOS VIRTUAL

CHANNEL MULTIPLEXER,

BASED ON TYPE 12396

ESCC Detail Specification No. 9544/004

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DOCUMENTATION CHANGE NOTICE

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'A'	Oct. '94	P1. Cover page		None
		P2. DCN		None
		P11. Figure 3(a)	: Pin 65 description corrected	23682
		P27. Para. 4.3.3	: In first sentence, 'Basic' corrected to 'Generic'	23682
		P77. Header	: Specification Number corrected	23682
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'B'	Jan. '97	P1. Cover page	: Part Number amended	221374
		P2. DCN		None
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		P5. Para. 1.1	: In the first sentence, Part Number amended	221374
		P59. Table 5(b)	: No. 2, in Characteristics, Pin 62 added	221374
			: No. 4, in Characteristics, Pin 42 added	221374
			: No. 5, in Characteristics, Pins 12 and 38 added and 42 deleted	221374
		P61. Figure 5(b)	: Part Number amended	221374
			: Pin 42 disconnected from V_{GEN1} and connected to V_{SS}	221374
		P68. Figure 6	: No. 2, in Characteristics, Pin 62 added	221374
			: No. 4, in Characteristics, Pin 42 added	221374
			: No. 5, in Characteristics, Pins 12 and 38 added and 42 deleted	221374
		P70. Figure 6	: Part Number amended	221374
			: Pin 42 disconnected from V_{GEN1} and connected to V_{SS}	221374
		P76. Appendix 'A'	: Title amended	221374
			: For Para. 4.2.3 entry, item "(b)" added	221374
'C'	Mar. '98	P1. Cover page		None
		P2. DCN		None
		P8. Figure 2	: In Note 4, "0.6" corrected to "0.635"	23883

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1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a monolithic, Silicon on Sapphire CMOS Virtual Channel Multiplexer, based on Type 12396. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

As per Figure 3(b).

1.8 CIRCUIT DESCRIPTION

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 with a Minimum Critical Path Failure Voltage of 1500Volts.

1.11 INPUT/OUTPUT PROTECTION NETWORKS

Protection networks shall be incorporated into each input and output as shown in Figure 3(e).

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND FINISH
01	FLAT	2(a)	D2

TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage	V_{DD}	−0.5 to +7.0	V	-
2	Input Voltage	V_{IN}	−0.5 to V_{DD} + 0.5	V	-
3	DC Input Current	I_{IN}	20	mA	-
4	DC Output Current	I_{OUT}	10	mA	Note 1
5	Device Dissipation (Continuous)	P_D	200	mWdc	-
6	Output Dissipation	P_{DSO}	50	mWdc	Note 1
7	Operating Temperature Range	T_{op}	−55 to +125	°C	T_{amb}
8	Storage Temperature Range	T_{stg}	−65 to +150	°C	-
9	Soldering Temperature	T_{sol}	+260	°C	Note 2

NOTES

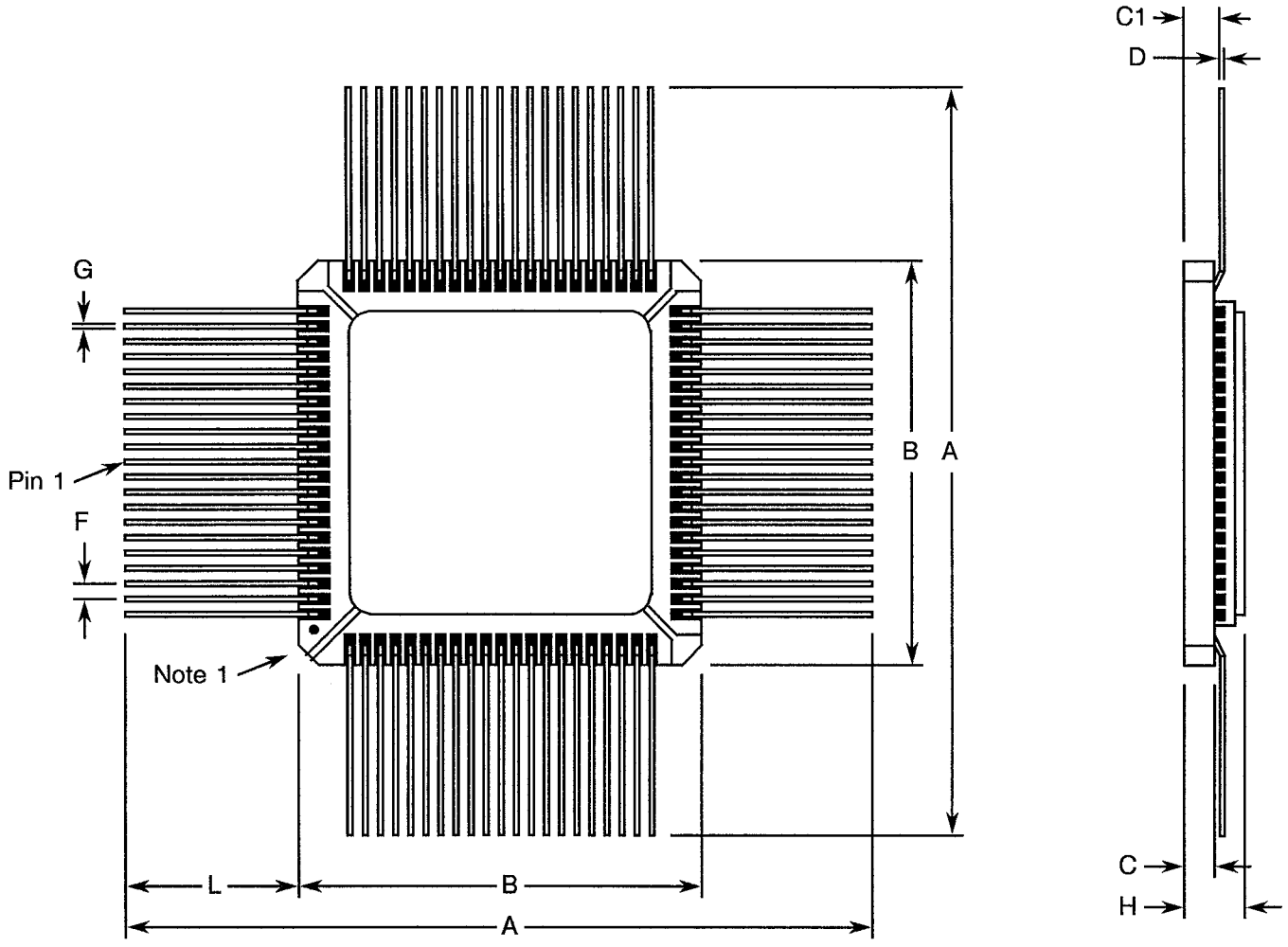
1. Single output.
2. Duration 5 seconds maximum at a distance of not less than 1.0mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION

Not applicable.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - FLAT PACKAGE, 84-PIN



SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	33.5	35.0	
B	16.2	16.7	
C	1.0	1.5	
C1	1.2	1.7	2, 5
D	0.1	0.2	
F	0.5	0.7	3, 4
G	0.2	0.3	2
H	1.9	2.4	
L	8.2	9.5	2

NOTES: See Page 8.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURE 2(a)

1. Index area; the index shall be as defined in Figure 2(a).
2. All leads.
3. 80 spaces for flat packages.
4. The true position pin spacing is 0.635mm between centre lines. Each pin centreline shall be located within ±0.1mm of its true longitudinal position relative to Pin 1 and the highest pin number.
5. The dimension shall be measured at the point of exit of the lead from the body.

FIGURE 3(a) - PIN ASSIGNMENT

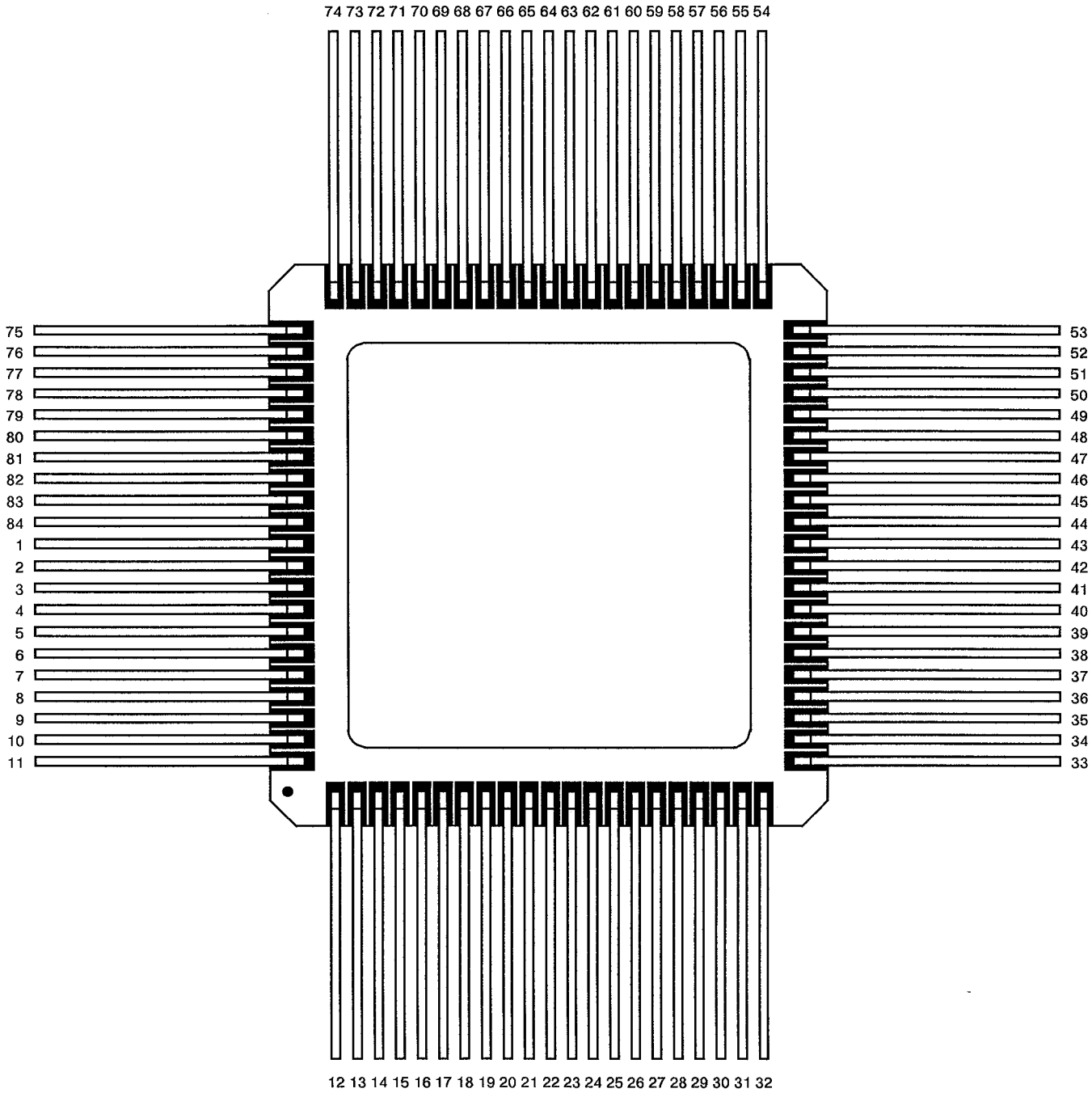


FIGURE 3(a) - PIN ASSIGNMENT (CONTINUED)

PIN DESCRIPTION

SYMBOL	FUNCTION	DESCRIPTION	PIN NUMBER
V_{DD}	Input	Positive Supply	1
POLL3	VCA Polled	Output	2
CTS3	Clear to Send	Output	3
PVCF3	VCA Serial PVCF Input	CMOS Input	4
RTS3	VCA Ready to Send	CMOS Input	5
POLL2	VCA Polled	Output	6
CTS2	Clear to Send	Output	7
PVCF2	VCA Serial PVCF Input	CMOS Input	8
RTS2	VCA Ready to Send	CMOS Input	9
POLL1	VCA Polled	Output	10
CTS1	Clear to Send	Output	11
PVCF1	VCA Serial PVCF Input	CMOS Input	12
RTS1	VCA Ready to Send	CMOS Input	13
POLL0	VCA Polled	Output	14
CTS0	Clear to Send	Output	15
PVCF0	VCA Serial PVCF Input	CMOS Input	16
RTS0	VCA Ready to Send	CMOS Input	17
D2	Data Bus	Input/Output	18
D1	Data Bus	Input/Output	19
D0	Data Bus	Input/Output	20
V_{DD}	Input	Positive Supply	21
V_{SS}	Input	Negative Supply	22
A4	Address Bus	TTL Input	23
A3	Address Bus	TTL Input	24
A2	Address Bus	TTL Input	25
A1	Address Bus	TTL Input	26
A0	Address Bus	TTL Input	27
$R/\overline{W}$	Read/Write Control	TTL Input	28
$\overline{CS}$	Chip Select	TTL Input	29
$\overline{RESET}$	Reset	Schmitt Trigger Input	30
TEST1	Test Control	CMOS Input	31
TEST0	Test Control	CMOS Input	32
$\overline{ERR}$	Internal Error Detected	Output	33
TCID4	Part of CLCW Virtual Channel Identifier Field	CMOS Input	34
TCID3	Part of CLCW Virtual Channel Identifier Field	CMOS Input	35
SELCLCW	Select CLCW	CMOS Input	36
D1TTC	Serial Data	Schmitt Trigger Input	37

FIGURE 3(a) - PIN ASSIGNMENT (CONTINUED)

PIN DESCRIPTION (CONTINUED)

SYMBOL	FUNCTION	DESCRIPTION	PIN NUMBER
D0TTC	Serial Data	Schmitt Trigger Input	38
V_{SS}	Input	Negative Supply	39
SAMPLE	Sample Signal	Output	40
ODDFRAME	Odd Master Frame Counter Indication	Output	41
CLCWCLK	Clock for Generating CLCW Control Signals	CMOS Input	42
CLKTTC	Clock for TTC-B-01 Data	Output	43
BITCLK	Clock	CMOS Input	44
BITLOCK	Demodulator Achieved Bit Lock	Schmitt Trigger Input	45
RFAVAIL	RF Signal Present	Schmitt Trigger Input	46
SCID9	Spacecraft Identifier	CMOS Input	47
SCID8	Spacecraft Identifier	CMOS Input	48
SCID7	Spacecraft Identifier	CMOS Input	49
SCID6	Spacecraft Identifier	CMOS Input	50
SCID5	Spacecraft Identifier	CMOS Input	51
SCID4	Spacecraft Identifier	CMOS Input	52
SCID3	Spacecraft Identifier	CMOS Input	53
SCID2	Spacecraft Identifier	CMOS Input	54
SCID1	Spacecraft Identifier	CMOS Input	55
SCID0	Spacecraft Identifier	CMOS Input	56
RSSPACE	Insertion of Space for Reed-Solomon Check Codes	CMOS Input	57
OPCF	Trailer Insertion	CMOS Input	58
FECW	Trailer Insertion	CMOS Input	59
LEN1	Transfer Frame Length	CMOS Input	60
LEN0	Transfer Frame Length	CMOS Input	61
ALTSOUT	Alternate Serial Transfer Frame Output	Output	62
SOUT	Serial Transfer Frame Output	Output	63
V_{SS}	Input	Negative Supply	64
V_{DD}	Input	Positive Supply	65
FRAME	Frame Indication	Output	66
SYNCMARK	Synchronisation Marker	Output	67
EXTSEL	External Selection of Next Virtual Channel	CMOS Input	68
POLL7	VCA Polled	Output	69
CTS7	Clear to Send	Output	70
PVCF7	VCA Serial PVCF Input	CMOS Input	71
RTS7	VCA Ready to Send	CMOS Input	72
POLL6	VCA Polled	Output	73

FIGURE 3(a) - PIN ASSIGNMENT (CONTINUED)

PIN DESCRIPTION (CONTINUED)

SYMBOL	FUNCTION	DESCRIPTION	PIN NUMBER
CTS6	Clear to Send	Output	74
PVCF6	VCA Serial PVCF Input	CMOS Input	75
RTS6	VCA Ready to Send	CMOS Input	76
POLL5	VCA Polled	Output	77
CTS5	Clear to Send	Output	78
PVCF5	VCA Serial PVCF Input	CMOS Input	79
RTS5	VCA Ready to Send	CMOS Input	80
POLL4	VCA Polled	Output	81
CTS4	Clear to Send	Output	82
PVCF4	VCA Serial PVCF Input	CMOS Input	83
RTS4	VCA Ready to Send	CMOS Input	84

FIGURE 3(b) - TRUTH TABLE

TIMING DIAGRAMS

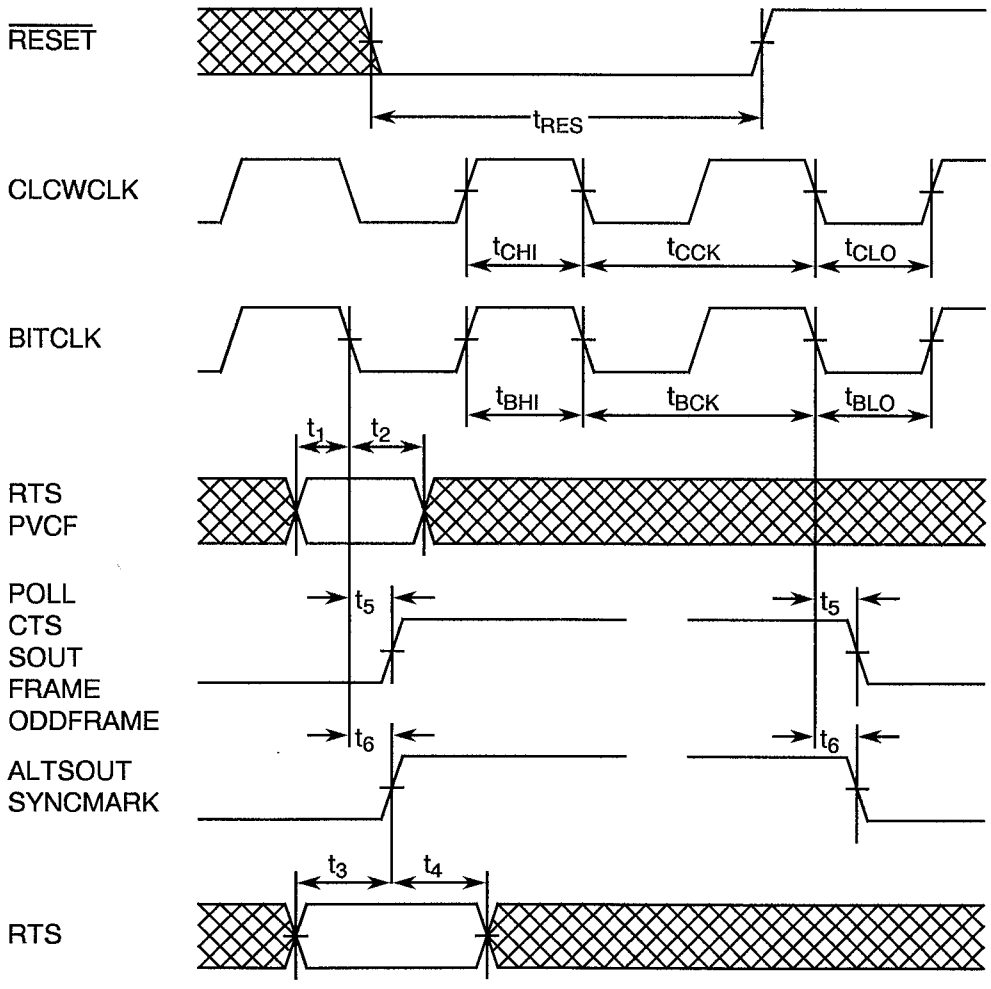


FIGURE 3(b) - TRUTH TABLE (CONTINUED)

TIMING DIAGRAMS (CONTINUED)

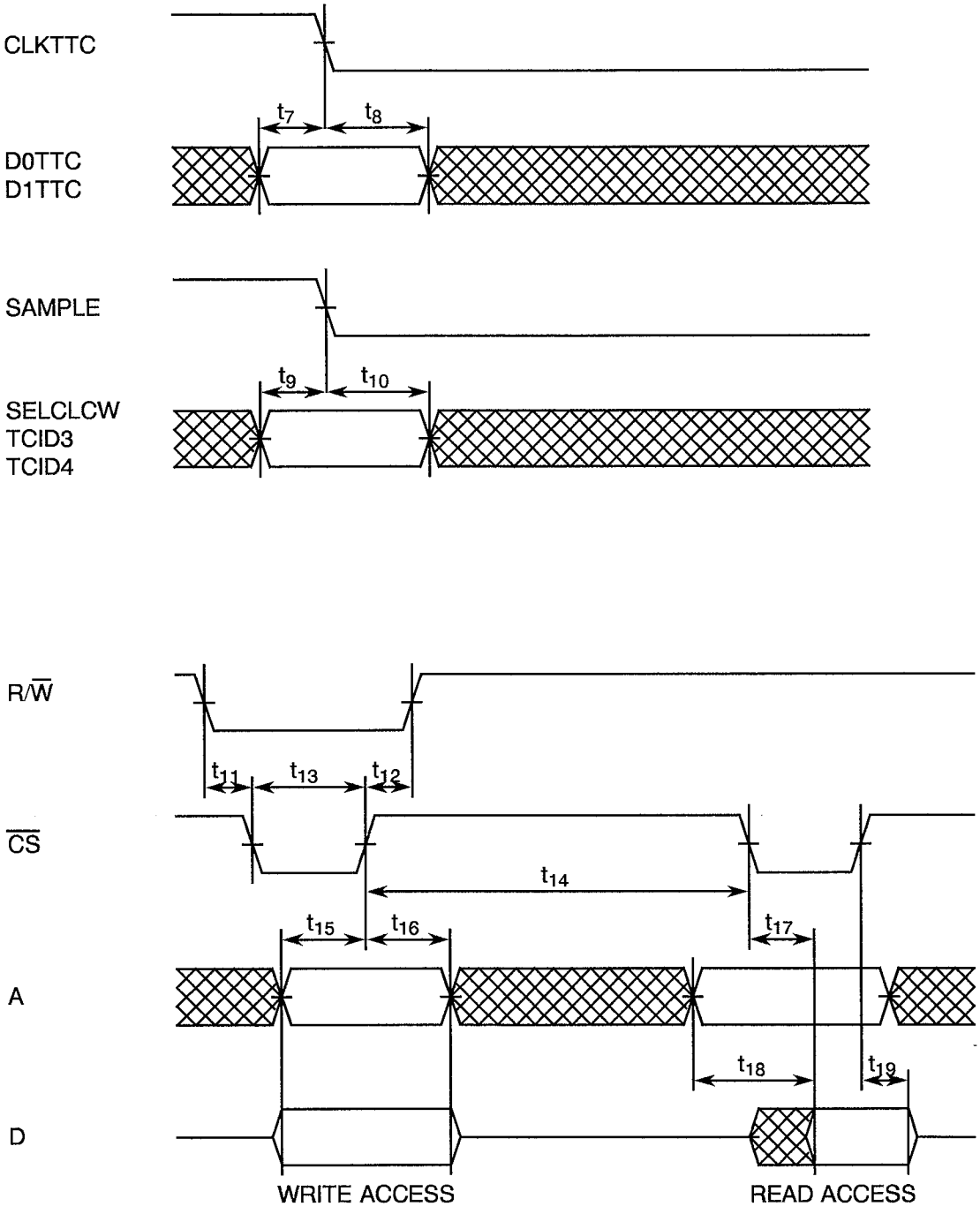


FIGURE 3(c) - CIRCUIT DESCRIPTION

SUMMARY OF OPERATION

After reset, the VCM performs a self-test (optionally) and then automatically starts outputting Transfer Frames continuously:

- Generates and outputs the 32 bit Attached Synchronisation Marker.
- Generates and outputs the Frame Identification and the Master Channel Frame Count fields of the Transfer Frame Primary Header.
- Feeds through the Partial Virtual Channel Frame from the selected VCA.
- Optionally generates and outputs the Transfer Frame Trailer.
- Optionally leaves space for the Reed-Solomon check codes, and generates the control signals for the MA1916 Reed-Solomon encoder.

If the built-in selection algorithms are used, the VCM selects which VCA is to output the next Partial Virtual Channel Frame (PVCF). If no PVCF was found to be available, the VCM demands the VCA for Virtual Channel 7 to produce a PVCF, normally resulting in an idle Transfer Frame.

If external selection is employed, the VCA specified by 3 input pins is demanded to provide a PVCF. If the selected VCA cannot provide a normal PVCF, an idle PVCF is sent, resulting in an idle Transfer Time being output for that Virtual Channel.

During operation, the bandwidth allocation (or the priority order) for the selection of the next Virtual Channel to be output may be reprogrammed.

The VCM retrieves part of the Command Link Control Word (CLCW) from the Packet Telecommand Decoder, using the TTC-B-01 interface. The retrieved data will form part of the OPCF in the trailer.

FUNCTIONS NOT INCLUDED IN THE VCM

The VCM does not produce idle frames. Instead, if the selected VCA does not have a complete PVCF available, it will output an idle PVCF, resulting in an idle Transfer Frame being output from the VCM.

The VCM does not generate or insert the Reed-Solomon check block, or perform any interleaving functions. This is handled by a Reed-Solomon encoder such as the MA1916. The same applies for convolutional encoding.

VCA/VCM INTERFACE

The VCM has 2 inputs and 2 outputs for each of the 8 VCAs than can be connected. 1 VCA is required per Virtual Channel. The inputs are Ready to Send (RTS0 to RTS7) and Partial Virtual Channel Frame (PVCF0 to PVCF7). The outputs are Clear to Send (CTS0 to CTS7) and Device Polled (POLL0 to POLL7). The POLL signals are described in Bandwidth Allocation. The VCM operates on the falling BITCLK edge, whereas the VCA operates on the rising BITCLK edge, to avoid skew problems.

When the VCA is ready to transfer a complete PVCF, it activates its RTS signal. If the built-in selection algorithms are used, the VCM selects one of the VCAs whose RTS input is activated. With external selection the VCA indicated by RTS0 to RTS2 is selected.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

The VCM activates the CTS output corresponding to the selected VCA. 4 BITCLK cycles later, the VCM samples the data from the VCA present on the corresponding PVCF input, to be output at the SOUT and ALTSOUT outputs. A new bit value is sampled every BITCLK cycle until the complete PVCF has been fed through. The CTS signal remains activated for 461 BITCLK cycles.

A schematic view of the interface as seen by the VCM is presented in Figure I. In this example, 1 of the internal selection algorithms is used.

The size of the PVCF depends on both the length of the Transfer Frame, defined by the LEN0 and LEN1 inputs, and whether the Operational Control Field (OPCF) and/or the Frame Error Correction Word (FECW) shall be generated, as determined by the OPCF and FECW inputs. The PVCF lengths are as given in the Table below.

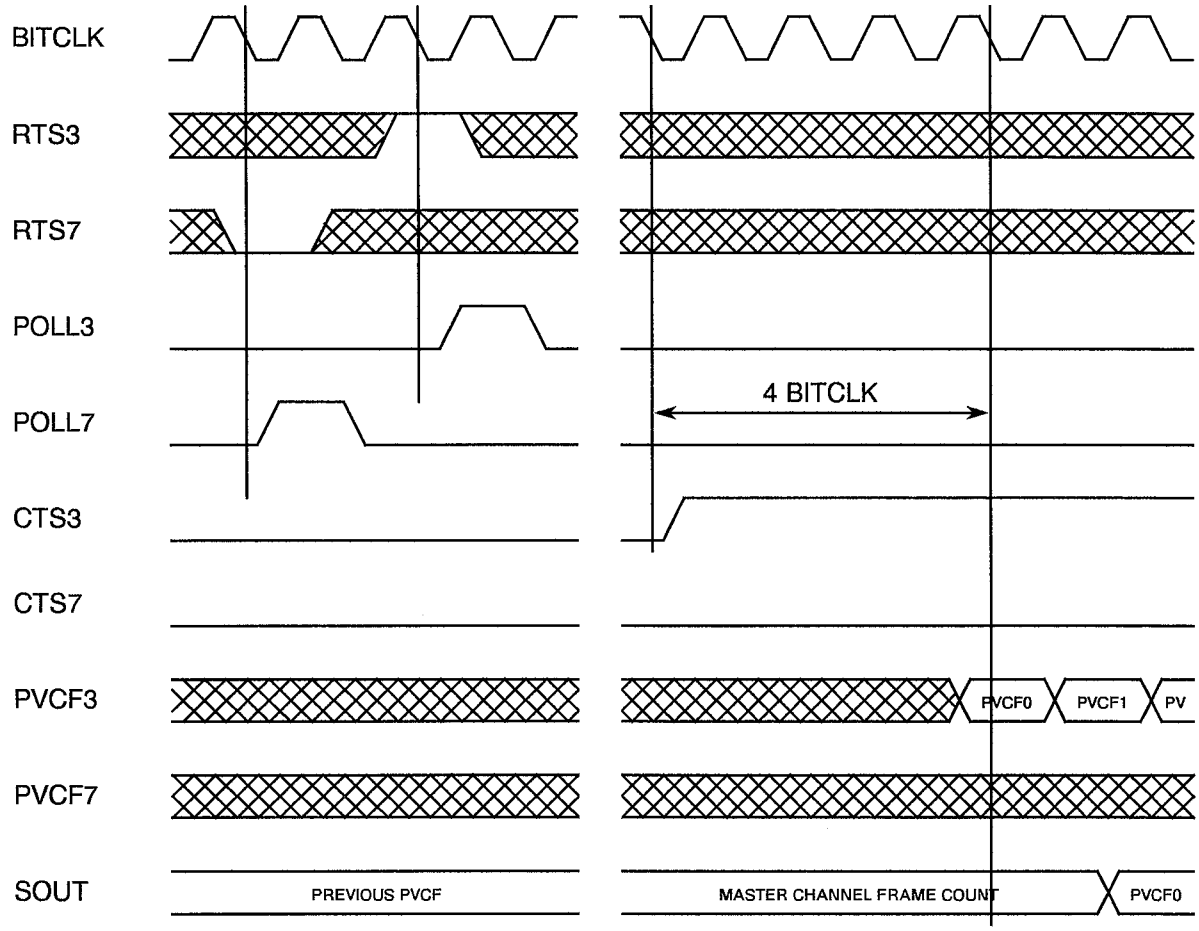
Transfer Frame Length	LEN0	LEN1	OPCF	FECW	PVCF Length
223 octets	0	0	0	0	220 octets
223 octets	0	0	0	1	218 octets
223 octets	0	0	1	0	216 octets
223 octets	0	0	1	1	214 octets
446 octets	0	1	0	0	443 octets
446 octets	0	1	0	1	441 octets
446 octets	0	1	1	0	439 octets
446 octets	0	1	1	1	437 octets
892 octets	1	0	0	0	889 octets
892 octets	1	0	0	1	887 octets
892 octets	1	0	1	0	885 octets
892 octets	1	0	1	1	883 octets
1115 octets	1	1	0	0	1112 octets
1115 octets	1	1	0	1	1110 octets
1115 octets	1	1	1	0	1108 octets
1115 octets	1	1	1	1	1106 octets

NOTES

1. Logic Level Definitions: 0 = Low Level, 1 = High Level.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

FIGURE I - VCA/VCM INTERFACE



BANDWIDTH ALLOCATION TABLE INTERFACE

The Bandwidth Allocation Table (BAT) is used by the built-in selection algorithms, described in the Selection of Next Virtual Channel to Output a Transfer Frame.

Data can be written to the BAT using a 3-bit parallel bus. The data consists of 32 entries of 3 bits each. Which entry is read or written is selected by the 5-bit address bus A0 to A4.

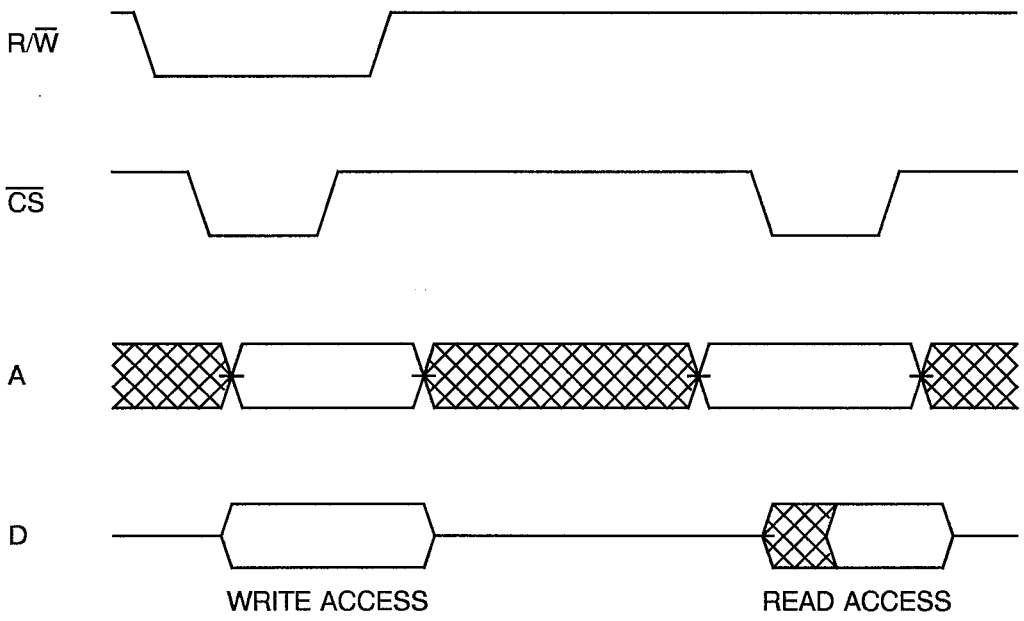
N.B.
D0 and A0 are the most significant bits of the data bus and the address bus, respectively.

The BAT interface is asynchronous. It is possible to both read and write data while the VCM is operating. $\overline{CS}$ must be de-activated for a minimum of 4 BITCLK cycles after a write, to allow for internal updating of the BAT. The interface is shown in Figure II.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

After reset, the BAT contains 0, 1, 2, 3, 4, 5, 6, 7, 0, 1, 2 ..., so that all Virtual Channels will have an equal bandwidth allocated. In the case of Priority Selection, this will mean that Virtual Channel 0 then has the highest priority, and Virtual Channel 7 the lowest.

FIGURE II - BAT INTERFACE



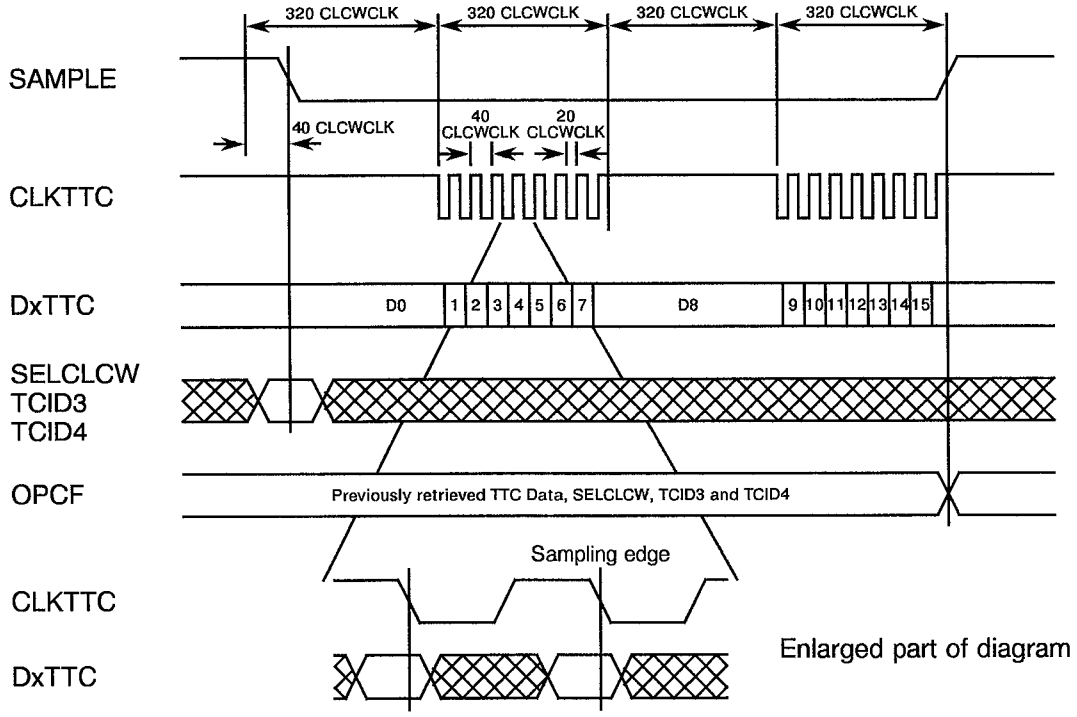
CLCW INTERFACE

The 32-bit Command Link Control Word (CLCW), as specified in ESA PSS-04-107, consists of, in output order:

- Control Word Type (bit 0) is "0".
- CLCW Version Number (bits 1 to 2) is "00".
- Status Field (bits 3 to 5) is "000".
- COP in Effect (bits 6 to 7) is "01".
- Virtual Channel Identifier (bits 8 to 13) describes which Packet TC decoder is used for the CLCW. For the VCM, bits 8 - 10 are fixed to "000", bit 11 gets its value from the TCID3 input, bit 12 gets its value from the TCID4 input and bit 13 gets its value from the SELCLCW input (also used for selecting the CLCW source).
- Reserved Field (bits 14 to 15) is "00".
- No RF Available Flag (bit 16) has the same value as the $\overline{\text{RFAVAIL}}$ input.
- No Bit Lock Flag (bit 17) has the same value as the $\overline{\text{BITLOCK}}$ input.
- Bits 18 to 31 are retrieved from the Packet TC decoder using a TTC-B-01 interface, as shown in Figure III. This part of the CLCW is normally retrieved once per transmitted frame, depending on the CLCWCLK frequency. Bit 18 gets its value from bit 2 of the retrieved word, and bit 31 gets its value from bit 15 of the retrieved word (the LSB).

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

FIGURE III - TTC B-01 INTERFACE FOR THE CLCW



The VCM generates the CLKTTC and SAMPLE output signals for controlling the CLCW interface, and inputs the D0TTC or the D1TTC signal from the Packet TC decoder. The retrieval starts at the same time as the frame starts to be output. All signals related to the CLCW interface are proportional to the CLCWCLK frequency. The transfer rate equals CLCWCLK divided by 80, e.g. if CLCWCLK is 10MHz the CLCW interface is operating at 125kbit/s. CLCWCLK is normally connected to the same clock as BITCLCK. However, in the case that another frequency is desired, a separate clock signal can be connected to CLCWCLK as explained in Asynchronous CLCW Input Interface.

The interface has been designed to retrieve 1 CLCW per Transfer Frame generated, regardless of the frame length, when CLCWCLK is connected to the same clock as BITCLCK. The interface allows direct connection to a Packet TC decoder chip without additional components. Alternatively, another electrical interface can be designed using external components.

Since the SELCLCW, TCID3 and TCID4 inputs indicate which Packet TC decoder the CLCW originates from, they are latched on the falling SAMPLE edge, so as not to change while the CLCW is acquired. These 3 latched signals, together with the 14 bits retrieved from the TTC-B-01 interface, are transferred to the OPCF register on the rising SAMPLE edge. In case SAMPLE is rising while the OPCF is being output, the update is delayed until the old OPCF has been output.

The VCM provides a mechanism for multiplexing the CLCW from 2 Packet TC decoders. Which data input is used is determined by the SELCLCW signal, latched as described above. D1TTC is used when the latched SELCLCW="1", otherwise D0TTC is used. If 3 to 8 Packet TC decoders are used, they can be multiplexed externally, the source being indicated by the TCID3 and TCID4 inputs.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

The ODDFRAME output can be connected to the SELCLCW input to automatically toggle between the 2 Packet TC decoders as CLCW source, provided that an odd number of Transfer Frames are output per CLCW acquisition. When CLCWCLK is connected to BITCLK, each Transfer Frame with an even Master Channel Frame Count will have a CLCW retrieved from the D0TTC and D1TTC inputs for odd Transfer Frames.

SELECTION OF NEXT VIRTUAL CHANNEL TO OUTPUT A TRANSFER FRAME

The VCM features 2 built-in algorithms for selecting the next Virtual Channel to output a Transfer Frame: Bandwidth Allocation and Priority Selection. Alternatively, a user-defined algorithm can be implemented externally if the built-in algorithms are not suitable.

BANDWIDTH ALLOCATION

This mode is enabled when the EXTSEL input is logic "0". In this mode the VCM uses adaptive frame ordering, as described in Selected Algorithm Examples. The Bandwidth Allocation Table (BAT) contains 32 internal 3-bit registers whose value (0 to 7) indicates the number of the Virtual Channel to be considered.

While outputting a Transfer Frame the VCM scans the BAT for the next ready frame to be output in a round-robin fashion. The algorithm selects the next entry in the BAT which points to a VCA that has activated its corresponding RTS signal. If a Virtual Channel does not have an entry in the BAT that points to it, no Transfer Frames from that Virtual Channel will be output, even if no other Transfer Frames are available.

The round-robin scanning continues until 1 activated RTS has been found, or all 33 entries in the BAT have been examined. If none of the VCAs pointed to by the BAT entries had activated their RTS signal, the VCM activates the CTS7 output, requesting the VCA for Virtual Channel 7 to produce a PVCF. VCA7 then produces an idle PVCF, resulting in an Idle Transfer Frame being output from the VCM (if VCA7 is also used for sending normal data, and enough data has become available, a normal PVCF is supplied instead).

This function can be used to send low-priority data instead of idle frames; if data is fed to VCA7, but no entry in the BAT points to it, Virtual Channel 7 will have the lowest priority; all other Virtual Channels have their guaranteed Bandwidth, but VCA7 will use the spare bandwidth when no other VCA can provide a normal PVCF.

The selection starts when approximately 80% of the previous frame has been output to allow the algorithm to complete before the next frame. The exact figures are: 1536 BITCLK cycles after the first bit of the Synchronisation Marker for a frame length of 223 octets; 3072 cycles for 446 octets; 6144 cycles for 892 octets and 8192 cycles for 1115 octets. Since the selection occurs while the previous Transfer Frame is being output, the first frame after reset has been chosen to be from VCA7.

For each entry in the BAT that is scanned, the VCM activates the corresponding POLL output for the duration of 1 BITCLK cycle. Consequently a VCA may receive between 0 and 33 polls for each Transfer Frame being output, depending on the BAT programming. The POLL signal may be used by a VCA to recognise that it has been considered for outputting a PVCF.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

PRIORITY SELECTION

This mode is enabled when the SYNCMARK output is connected to the EXTSEL input. On the falling SYNCMARK edge the BAT pointer is reset to restart at the first entry in the BAT (address 0). Since this occurs after each selection (Transfer Frame), the result will effectively be a priority selection. Except for the repeated resetting, the selection process works exactly as in the case of Bandwidth Allocation.

EXTERNAL SELECTION

This mode is enabled when EXTSEL is connected to logic "1". In this mode the selection has to be external and should be provided through RTS0 to RTS2. RTS0 is the most significant bit. The value at RTS0 to RTS2 is sampled on the rising SYNCMARK edge. The RTS3 to RTS7 signals are not used but should be connected to a defined logic level.

If the selected VCA has a PVCF available it will provide a normal PVCF, otherwise an idle PVCF is sent resulting in an idle Transfer Frame being output for that Virtual Channel. The selection also applies for the first Transfer Frame after reset, which will normally be an Idle Transfer Frame since the VCA has not received enough data.

N.B.
In this mode the selection algorithm still operates internally, toggling the POLL outputs according to the BAT programming.

ATTACHED SYNCHRONISATION MARKER

Before outputting the Transfer Frame the VCM generates and sends the 32 bit Attached Synchronisation Marker. The VCM has 2 outputs, SOUT and ALTSOUT, which continuously output the same Transfer Frames, but with different Synchronisation Markers. For the SOUT output, the value of the Attached Synchronisation Marker is hex 1ACFFC1D.

For applications that use a tape recorder that plays back a recorded data stream in forward order, the ALTSOUT output can be used instead of the SOUT output for the data to be recorded. This pin outputs the value hex 352EF853 for the Attached Synchronisation Marker, but is otherwise identical to the SOUT output.

If Reed-Solomon encoding is used, a space will be present on both the SOUT and ALTSOUT outputs. If only one Reed-Solomon encoder is used both for the SOUT and ALTSOUT outputs (e.g. for error correction for the tape recorder), the synchronisation marker, or the check codes, have to be multiplexed externally.

TRANSFER FRAME PRIMARY HEADER

The fields in the first 3 octets of the Primary Header generated by the VCM are, in the order they are output:

- Version number, always "00".
- Spacecraft Identifier (S/C Id), has the same value as inputs SCID0 to SCID9.
- Virtual Channel Identifier (VC Id) is the number of the Virtual Channel currently being output.
- Operational Control Field Flag (OPCF Flag), indicates whether the Operational Control Field is present in the Trailer or not. This flag has the same value as the input pin OPCF.
- Master Channel Frame Count retrieved from the Master Frame Counter. This 8-bit counter is incremented by 1 for each frame that is output.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

TRANSFER FRAME TRAILER

The Trailer consists of 2 optional fields:

- The 4 octet Operational Control Field (OPCF) is present when the input OPCF = "1". This field contains the Command Link Control Word (CLCW), updated on the rising SAMPLE edge, as described in CLCW Interface.
- The 2 octet Frame Error Control Word (FECW) is present when the input FECW = "1". It consists of the CRC checksum over the whole Transfer Frame (excluding the FECW and the Synchronisation Marker) using the generator polynomial $g(x) = x^{16} + x^{12} + x^5 + 1$. The shift register is initialised to all "1s" before each frame.

SPACE FOR REED-SOLOMON CHECK CODES

A space for Reed-Solomon check codes between the Transfer Frames can be selected with the RSSPACE input. When RSSPACE = "1", the space is present and both the SOUT and ALTSOUT outputs are logic "0" after the Transfer Frame has been output. The space is output after normal as well as after idle Transfer Frames. The length of this space depends on the inputs LEN0 and LEN1 as given in the Table below.

LEN0	LEN1	TRANSFER FRAME LENGTH	LENGTH OF SPACE FOR CHECK CODES
0	0	223 octets	32 octets
0	1	446 octets	64 octets
1	0	892 octets	128 octets
1	1	1115 octets	160 octets

NOTES
1. Logic Level Definitions: 0 = Low Level, 1 = High Level.

IDLE TRANSFER FRAMES

If the VCA for which CTS is activated has a complete PVCF available it will provide a normal PVCF, otherwise an idle PVCF will be generated, resulting in an idle Transfer Frame being output for that Virtual Channel.

All fields generated by the VCM are the same as for a normal frame. The VCA will generate the correct flags and counter values and provide an adequate fill pattern for the data field.

TRANSFER FRAME OUTPUTS

The Attached Synchronisation Marker, the complete Transfer Frames and the optional space for Reed-Solomon check codes are output through the SOUT and ALTSOUT outputs.

The VCM is designed to suit the interface of the MA1916 Reed-Solomon encoder, if Reed-Solomon encoding is used. The output signal FRAME is intended to be connected to the SMC input of the MA1916 to control the generation and output of the check codes. FRAME is activated when the first part of the transfer frame is being output. It is de-activated when the last bit of the Transfer Frame has been output. It is also de-activated when the Attached Synchronisation Marker is being output, so that it is not included in the generation of check symbols.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

TEST

The VCM features Built-In Self Test (BIST) with a fault coverage of 92%. The BIST runs for 4997 BITCLK cycles after $\overline{\text{RESET}}$ has been released. The BIST result does not depend on the state on any of the input pins. The BIST can be disabled by connecting the TEST0 input to logic "1"; after releasing $\overline{\text{RESET}}$ the VCM will be reset but no BIST will be performed.

If an error is detected by the BIST, the $\overline{\text{ERR}}$ signal remains activated ($\overline{\text{ERR}}$="0"), until the next reset occurs. The VCM will try to continue to operate in normal mode. If no internal error was detected, the $\overline{\text{ERR}}$ signal is de-activated and the VCM starts working in normal mode.

When $\overline{\text{RESET}}$ is activated and during BIST, the CLKTTC and SAMPLE outputs are driven to logic "1", the D data bus is 3-Stated, and all other outputs set to logic "0" so as not to trigger connected devices.

The production test for the VCM has a fault coverage of 99%, and is performed at a BITCLK frequency of 10MHz. The TEST1 pin is used for the production test and shall be tied to logic "0" during normal operation.

The fault coverage figures are based on stuck-at-"0"/"1" faults at the gate level, faulting all nets (gate outputs).

STATE AFTER RESET

After reset, or after reset and the completion of BIST, the VCM is initialised as follows:

- The BAT contains 0, 1, 2, 3, 4, 5, 6, 7, 0, 1, 2 ..., so that all Virtual Channels will have an equal bandwidth allocated. In the case of Priority Selection, this will mean that Virtual Channel 0 then has the highest priority and Virtual Channel 7 the lowest.
- The Master Channel Frame Count field has the value "0". The ODDFRAME signal has the value "0". Finally, bits 18 to 31 of the CLCW are set to "0", though normally data will be retrieved from the Packet TC decoder before the CLCW is output.
- The VCM starts outputting the Synchronisation Marker of the first Transfer Frame after reset. If internal selection is used this frame will come from VCA7, which is normally an Idle Transfer Frame since the VCA has not received enough data, otherwise it will come from the VCA defined by the external selection.

The selection also applies for the first Transfer Frame after reset, which normally will be idle, since the VCAs have not received enough data.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

EXAMPLE OF NEXT VIRTUAL CHANNEL TO OUTPUT A TRANSFER FRAME SELECTION

For the examples below, the entries in the BAT are:

- 0, 1, 0, 2, 0, 3, 0, 1, 0, 2, 0, 3, 0 ... etc.

The following number of complete PVCFs will become available from the VCAs:

- VC0: 3 PVCFs.
- VC1: 1 PVCF.
- VC2: none.
- VC3: 2 PVCFs.
- VC4: 2 PVCFs.
- VC7: none.

The examples below show what would be output directly after reset, with the BAT programmed as described above before the selection starts. The value of the BAT pointer is initially "0", i.e. pointing to the first entry in the list above.

Using the Bandwidth Allocation algorithm, the Transfer Frames output from the VCM will be from:

- (First after reset) **VC7(Idle) VC0 VC1 VC0** (VC2 no frame) **VC0 VC3** (VC0, VC1, VC0, VC2, VC0 no frame) **VC3** (none of the entries in the BAT has a frame) **VC7(Idle) VC7(Idle)** ...

Similarly, by employing the Priority Selection algorithm, the Transfer Frames output from the VCM will be from:

- **VC7(Idle) VC0 VC0 VC0 VC1 VC3 VC3 VC7(Idle) VC7(Idle)** ...

Finally, using External Selection with RTS0 = RTS1 = RTS2 = "0" as an example in a simple system using only 1 VCA, the following Transfer Frames will be output (the first Transfer Frame is idle since no data has been gathered after reset):

- **VC0(Idle) VC0 VC0 VC0 VC0(Idle) VC0(Idle)** ...

N.B.
No Transfer Frames are generated for Virtual Channel 4 since there is no entry in the BAT indicating VC4.

ADAPTIVE FRAME ORDERING VERSUS FIXED FRAME ORDERING

Fixed frame ordering has the following characteristics:

- The sequence of Virtual Channels to output a Transfer Frame is fixed, though this sequence may be changed for different phases of a mission.
- If a Virtual Channel selected for output has not enough data to output a Transfer Frame, it instead generates an idle frame which can be regarded as originating from the Virtual Channel, but without any valid data. The Virtual Channel Count is updated.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

This means that some of the bandwidth may not be utilised, if the data source(s) associated with a Virtual Channel continuously do not produce exactly the amount of data that is has bandwidth allocated for. Therefore, the VCM built-in algorithms use adaptive frame ordering that may dynamically alter the frame ordering:

- As long as all Virtual Channels in the sequence can output a Transfer Frame, the sequence is followed.
- If the Virtual Channel selected for output is not able to output a Transfer Frame, that Virtual Channel is considered as being in the OFF state and the next Virtual Channel in the sequence is selected for output. Thus, in the normal case, the Transfer Frame Generator does not produce idle frames and the bandwidth can be used for Transfer Frames from other Virtual Channels.
- In the case that none of the Virtual Channels can output a Transfer Frame, the VCM has to output an idle frame, which thus is not associated with any particular Virtual Channel. However, in order to be compliant with ESA PSS-04-106, the VCM built-in selection algorithms use VCA7 for producing an idle PVCF.

ASYNCHRONOUS CLCW INPUT INTERFACE

Although normally intended to be connected to the same clock as BITCLK, CLCWCLK may be connected to a different asynchronous clock, allowing a transfer rate independent of the bit rate.

If CLCWCLK has a lower frequency than BITCLK, the acquisition may span several Transfer Frames. The number of Transfer Frames output for each acquisition can be calculated as the nearest integer higher than

$$\frac{160 \times f_{BCK}}{(4 + (\text{frame length}) + (\text{RS length})) \times f_{CCK}}$$

For example, if $f_{BCK} = 10\text{MHz}$, $f_{CCK} = 1.0\text{MHz}$, and 223 octet Transfer Frames with Reed-Solomon encoding are used, $(160 \times 10/((4 + 223 + 32) \times 1) = 6.18 \Rightarrow 7$ Transfer Frames will be output for each acquired CLCW. Combinations that give a ratio close to the integer limit (e.g. 1.99 or 2.0) should be avoided; it can give a varying number of Transfer Frames per CLCW acquisition (or in very rare cases without FECW and Reed-Solomon check codes, leading to the OPCF not being updated due to a design shortcoming).

In the case that the CLCW acquisition spans several Transfer Frames, the VCA will output the previously retrieved CLCW value until a new acquisition is completed. The first Transfer Frame after reset would then have bits 18 to 31 equal to "0". In case SAMPLE is rising while the CLCW is being output, the update is delayed until the old CLCW has been output.

FIGURE 3(d) - FUNCTIONAL DIAGRAM

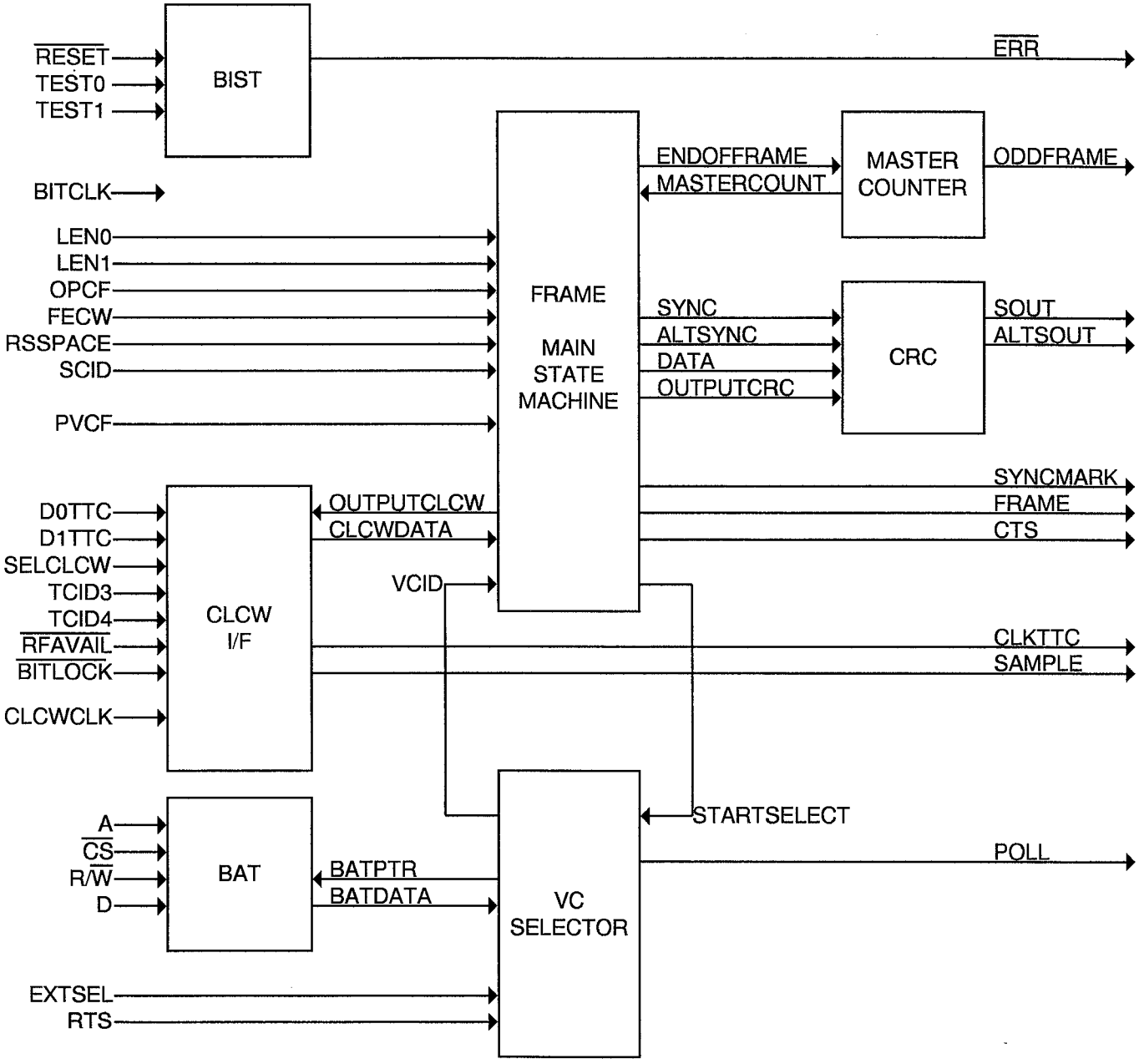
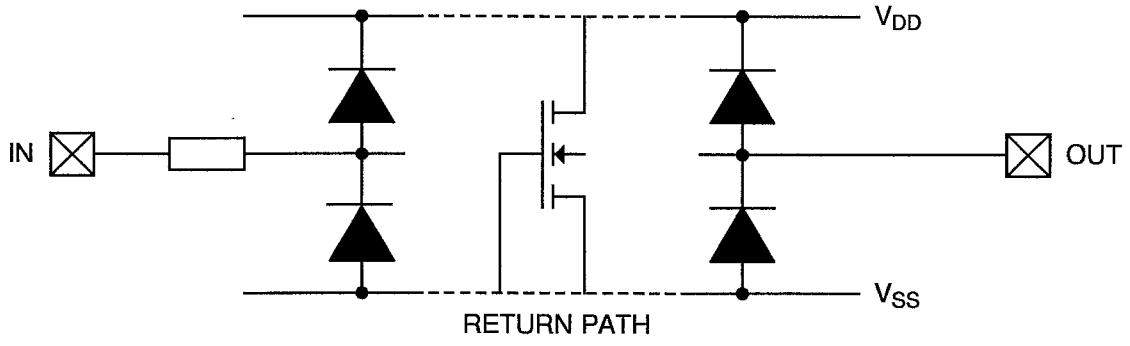


FIGURE 3(e) - INPUT/OUTPUT PROTECTION NETWORKS



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

(c) ESA PSS-04-106, Packet Telemetry Standard.

(d) ESA PSS-04-107, Packet Telecommand Standard.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviation is used:-

V_{IC} - Input/Output Clamp Voltage.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

(a) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during qualification and maintenance of qualification.

(b) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during procurement on a lot acceptance basis at the total dose irradiation level specified in the Purchase Order.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

(a) Para. 7.1.1(a), "High Temperature Reverse Bias" test and subsequent electrical measurements related to this test shall be omitted.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 5.0 grammes.

4.3.3 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The test conditions shall be as follows:-

Applied Force: 1.0 ± 0.1 Newtons, 3 bends at 45°.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body and the lids shall be pre-form soldered.

4.4.2 Lead Material and Finish

The material shall be Type 'D' with Type '2' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

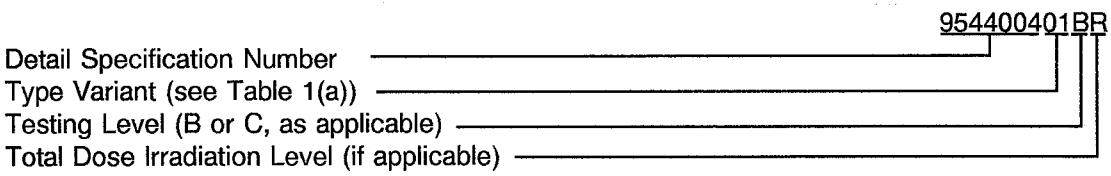
(c) Traceability Information.

4.5.2 Lead Identification

An index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



The Total Dose Irradiation Level designation shall be added for those devices for which a sample has been successfully tested to the level in question. For these devices, a code shall be added in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ °C and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for H.T.R.B. Burn-in

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for Power Burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for Power Burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for H.T.R.B. Burn-in

Not applicable.

4.7.5 Electrical Circuits for Power Burn-in

A circuit for use in performing the Power Burn-in test is shown in Figure 5(b) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
1 to 4	V_{SS} and V_{DD} Continuity	-	-	4(a)	I_{OUT} = 10µA V_{DD} = V_{SS} = 0V (Pins 1-21-22-39 to 64 + 65)	-	100	mV
5	Functional Test 1 (Basic)	-	3014	-	Verify Device Operation with Load V_{IL} = 0V, V_{IH} = 5.0V V_{OL} = 1.0V, V_{OH} = 4.0V I_{OUT} = ±2.0mA C_L = 100pF ± 20% V_{DD} = 5.0V, V_{SS} = 0V Pattern: M1 at 1.0MHz	-	-	-
6	Functional Test 2 (Nominal Voltage)	-	3014	-	Verify Device Operation with Load V_{IL}, V_{IH} = Note 1 V_{OL} = 1.0V, V_{OH} = 4.0V I_{OUT} = ±2.0mA C_L = 100pF ± 20% V_{DD} = 5.0V, V_{SS} = 0V Pattern: M1 at 10MHz	-	-	-
7	Functional Test 3 (High Voltage)	-	3014	-	Verify Device Operation with Load V_{IL}, V_{IH} = Note 1 V_{OL} = 1.0V, V_{OH} = 4.5V I_{OUT} = ±2.0mA C_L = 100pF ± 20% V_{DD} = 5.5V, V_{SS} = 0V Pattern: M1 at 10MHz	-	-	-
8	Functional Test 4 (Low Voltage)	-	3014	-	Verify Device Operation with Load V_{IL}, V_{IH} = Note 1 V_{OL} = 1.0V, V_{OH} = 3.5V I_{OUT} = ±2.0mA C_L = 100pF ± 20% V_{DD} = 4.5V, V_{SS} = 0V Pattern: M1 at 10MHz	-	-	-
9	Quiescent Current	I_{DD}	3005	4(b)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V All Outputs Open Note 2 (Pins 1 + 21 + 65)	-	0.5	mA

NOTES: See Page 33.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
10 to 60	Input Current Low Level	I_{IL}	3009	4(c)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 4-5-8-9-12-13-16-17-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-44-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84)	-	− 1.0	µA
61 to 111	Input Current High Level	I_{IH}	3009	4(d)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 4-5-8-9-12-13-16-17-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-44-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84)	-	1.0	µA
112 to 138	Output Voltage Low Level	V_{OL}	3007	4(e)	V_{IL}, V_{IH} = Note 1 I_{OL} = 4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pins 2-3-6-7-10-11-14-15-18-19-20-33-40-41-43-62-63-66-67-69-70-73-74-77-78-81-82)	-	0.4	V
139 to 165	Output Voltage High Level 1	V_{OH1}	3006	4(f)	V_{IL}, V_{IH} = Note 1 I_{OL} = − 4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pins 2-3-6-7-10-11-14-15-18-19-20-33-40-41-43-62-63-66-67-69-70-73-74-77-78-81-82)	3.9	-	V
166 to 192	Output Voltage High Level 2	V_{OH2}	3006	4(f)	V_{IL}, V_{IH} = Note 1 I_{OL} = − 0.5mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pins 2-3-6-7-10-11-14-15-18-19-20-33-40-41-43-62-63-66-67-69-70-73-74-77-78-81-82)	4.2	-	V

NOTES: See Page 33.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
193 to 200	Threshold Voltage Low Level 1 (TTL Inputs)	V_{THN1}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 18-19-20, Note 4) (Pins 23-24-25-26-27-28-29)	0.8	-	V
201 to 208	Threshold Voltage High Level 1 (TTL Inputs)	V_{THP1}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 18-19-20, Note 5) (Pins 23-24-25-26-27-28-29)	-	2.0	V
209	Threshold Voltage Low Level 2 (CMOS Inputs)	V_{THN2}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 4-5-8-9-12-13-16-17-31-32-34-35-36-42-44-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84, Note 4)	1.3	-	V
210	Threshold Voltage High Level 2 (CMOS Inputs)	V_{THP2}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 4-5-8-9-12-13-16-17-31-32-34-35-36-42-44-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84, Note 5)	-	3.2	V
211 to 215	Threshold Voltage Low Level 3 (SCHMITT Trigger Inputs)	V_{THN3}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 30-37-38-45-46)	1.0	2.8	V
216 to 220	Threshold Voltage High Level 3 (SCHMITT Trigger Inputs)	V_{THP3}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 30-37-38-45-46)	1.5	3.3	V
221 to 225	Hysteresis Voltage	V_H	-	4(h)	V_{DD} = 4.5V, V_{SS} = 0V Note 6 (Pins 30-37-38-45-46)	0.5	-	V
226 to 233	Threshold Voltage Low Level 4 (TTL Inputs)	V_{THN4}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 18-19-20, Note 4) (Pins 23-24-25-26-27-28-29)	0.8	-	V
234 to 241	Threshold Voltage High Level 4 (TTL Inputs)	V_{THP4}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 18-19-20, Note 5) (Pins 23-24-25-26-27-28-29)	-	2.0	V

NOTES: See Page 33.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
242	Threshold Voltage Low Level 5 (CMOS Inputs)	V_{THN5}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 4-5-8-9-12-13-16-17-31-32-34-35-36-42-44-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84, Note 4)	1.7	-	V
243	Threshold Voltage High Level 5 (CMOS Inputs)	V_{THP5}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 4-5-8-9-12-13-16-17-31-32-34-35-36-42-44-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84, Note 5)	-	3.9	V
244 to 248	Threshold Voltage Low Level 6 (SCHMITT Trigger Inputs)	V_{THN6}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 30-37-38-45-46)	1.2	3.8	V
249 to 253	Threshold Voltage High Level 6 (SCHMITT Trigger Inputs)	V_{THP6}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 30-37-38-45-46)	1.7	4.3	V
254 to 331	Input/Output Clamp Voltage (to V_{SS})	V_{IC1}	3022	4(i)	I_{IN} = −100µA V_{DD} = V_{SS} = 0V (Pins 2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-33-34-35-36-37-38-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-62-63-66-67-68-69-70-71-72-73-74-75-76-77-78-79-80-81-82-83-84)	-	−2.0	V
332 to 409	Input/Output Clamp Voltage (to V_{DD})	V_{IC2}	3022	4(i)	I_{IN} = 100µA V_{DD} = V_{SS} = 0V (Pins 2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-33-34-35-36-37-38-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-62-63-66-67-68-69-70-71-72-73-74-75-76-77-78-79-80-81-82-83-84)	-	2.0	V

NOTES: See Page 33.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
410 to 412	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	3006	4(j)	V_{IN} (3-State Control) = Note 7 V_{OUT} = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 18-19-20)	-	−10	µA
413 to 415	Output Leakage Current Third State (High Level Applied)	I_{OZH}	3006	4(j)	V_{IN} (3-State Control) = Note 7 V_{OUT} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 18-19-20)	-	10	µA
416	Supply Current 1 (During BIST)	I_{DDS1}	3005	4(b)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V Pattern M1 at 10MHz (Note 8)	-	60	mA
417	Supply Current 2 (During Normal Operation)	I_{DDS2}	3005	4(b)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V Pattern M1 at 10MHz (Note 8)	-	15	mA

NOTES

1. During Functional Tests 2, 3 and 4:-

   V_{IL} = 0.4V, V_{IH} = 2.4V for Pins 18, 19, 20.

   Functional Test 2: V_{IL} = 0.5V, V_{IH} = 4.5V,
   Functional Test 3: V_{IL} = 0.5V, V_{IH} = 5.0V,
   Functional Test 4: V_{IL} = 0.5V, V_{IH} = 4.0V,
   for Pins 4, 5, 8, 9, 12, 13, 16, 17, 30, 31, 32, 34, 35, 36, 37, 38, 42, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 68, 71, 72, 75, 76, 79, 80, 83, 84.

2. Measurement is performed with the device having been initialised using functional test pattern M1, stopped at test vector 16379. Total combined current for all V_{DD} Pins.
3. The output pin under test is configured into correct state for the measurement by using a functional test pattern on the inputs which produces a low or high at the pin, as appropriate.
4. Minimum value of pin group.
5. Maximum value of pin group.
6. Hysteresis is a calculated value from measurements for each pin from $V_{THP3} - V_{THN3} = V_H$.
7. The device is configured using a functional test pattern so that the pin under test is in the Third-State condition for the measurement. The measurement includes the input currents I_{IL} and I_{IH}.
8. Test vectors 0 to 4990 of functional test pattern M1 are used for measurement of I_{DDS1}.
9. Guaranteed but not tested. Characterised after major process changes.
10. Parameters tested go-no-go during Functional Tests 2, 3 and 4.
11. Guaranteed but not tested.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
418 to 457	Input Capacitance 1	C_{IN1}	3012	4(k)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 9 (Pins 4-5-8-9-12-13-16-17-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84)	-	5.0	pF
458	Input Capacitance 2	C_{IN2}	3012	4(k)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 9 (Pin 44)	-	10	pF
459 to 461	Input/Output Capacitance	C_{IN}/C_{OUT}	3012	4(k)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 9 (Pins 18-19-20)	-	10	pF
462 to 464	Rise and Fall Time (TTL and CMOS Inputs)	t_r1/t_f1	3004	-	Note 9	-	100	ns
465 to 467	Rise and Fall Time (SCHMITT Trigger Inputs)	t_r2/t_f2	3004	-	Note 9	-	1.0	µs
468 to 470	Clock Period for CLCWCLK	t_{CCK}	3003	-	Note 10	100	-	ns
471 to 473	Clock High Pulse Width for CLCWCLK	t_{CHI}	3003	-	Note 10	50	-	ns
474 to 476	Clock Low Pulse Width for CLCWCLK	t_{CLO}	3003	-	Note 10	50	-	ns
477 to 479	Clock Period for BITCLK	t_{BCK}	3003	-	Note 10	100	-	ns
480 to 482	Clock High Pulse Width for BITCLK	t_{BHI}	3003	-	Note 10	50	-	ns

NOTES: See Page 33.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
483 to 485	Clock Low Pulse Width for BITCLK	t_{BLO}	3003	-	Note 10	50	-	ns
486 to 488	RESET Activated	t_{RES}	3003	-	Note 10	$3t_{BCK}$	-	-
489 to 491	PVCF Setup to Falling Edge of BITCLK	$t_{1(PVCF)}$	3003	-	Note 10	3.0	-	ns
492 to 494	PVCF Hold after Falling Edge of BITCLK	$t_{2(PVCF)}$	3003	-	Note 10	97	-	ns
495 to 497	RTS Setup to Falling Edge of BITCLK	$t_{1(RTS)}$	3003	-	Note 10	3.0	-	ns
498 to 500	RTS Hold after Falling Edge of BITCLK	$t_{2(RTS)}$	3003	-	Note 10	97	-	ns
501 to 503	RTS Setup to Rising Edge of SYNCMARK (Ext. Selection)	t_3	3003	-	Note 10	$2t_{BCK}$	-	-
504 to 506	RTS Hold after Rising Edge of SYNCMARK (Ext. Selection)	t_4	3003	-	Note 10	$2t_{BCK}$	-	-
507 to 509	POLL Valid from Falling Edge of BITCLK	$t_{5(POLL)}$	3003	-	$I_{OUT} \pm 2.0$mA $C_L = 100$pF $\pm 20\%$ Note 10	-	53	ns
510 to 512	CTS Valid from Falling Edge of BITCLK	$t_{5(CTS)}$	3003	-	$I_{OUT} \pm 2.0$mA $C_L = 100$pF $\pm 20\%$ Note 10	-	53	ns
513 to 515	SOUT Valid from Falling Edge of BITCLK	$t_{5(SOUT)}$	3003	-	$I_{OUT} \pm 2.0$mA $C_L = 100$pF $\pm 20\%$ Note 10	-	53	ns
516 to 518	FRAME Valid from Falling Edge of BITCLK	$t_{5(FRAME)}$	3003	-	$I_{OUT} \pm 2.0$mA $C_L = 100$pF $\pm 20\%$ Note 10	-	54	ns

NOTES: See Page 33.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
519 to 521	ODDFRAME Valid from Falling Edge of BITCLK	$t_{5(ODD-FRAME)}$	3003	-	$I_{OUT} \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 10	-	54	ns
522 to 524	ALTSOUT Valid from Falling Edge of BITCLK	$t_{6(ALT-SOUT)}$	3003	-	$I_{OUT} \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 10	-	56	ns
525 to 527	SYNCMARK Valid from Falling Edge of BITCLK	$t_{6(SYNC-MARK)}$	3003	-	$I_{OUT} \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 10	-	57	ns
528 to 530	D0TTC, D1TTC Setup to CLKTTC Low	t_7	3003	-	Note 11	60	-	ns
531 to 533	D0TTC, D1TTC Hold after CLKTTC Low	t_8	3003	-	Note 11	0	-	ns
534 to 536	SELCLCW Setup to SAMPLE Low	$t_{9(SEL-CLCW)}$	3003	-	Note 11	$2t_{BCK}$	-	-
537 to 539	TCID Setup to SAMPLE Low	$t_{9(TCID)}$	3003	-	Note 11	$2t_{BCK}$	-	-
540 to 542	SELCLCW Hold after SAMPLE Low	$t_{10(SEL-CLCW)}$	3003	-	Note 11	$2t_{BCK}$	-	-
543 to 545	TCID Hold after SAMPLE Low	$t_{10(TCID)}$	3003	-	Note 11	$2t_{BCK}$	-	-
546 to 548	R/$\overline{W}$ Low to $\overline{CS}$ Low	t_{11}	3003	-	Note 10	100	-	ns
549 to 551	$\overline{CS}$ High to R/$\overline{W}$ High	t_{12}	3003	-	Note 10	100	-	ns
552 to 554	$\overline{CS}$ Width	t_{13}	3003	-	Note 10	100	-	ns
555 to 557	$\overline{CS}$ Width De-activated after Write	t_{14}	3003	-	Note 10	$4t_{BCK}$	-	-

NOTES: See Page 33.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
558 to 560	A to $\overline{CS}$ Rising Edge during Write	$t_{15(A)}$	3003	-	Note 10	200	-	ns
561 to 563	D to $\overline{CS}$ Rising Edge during Write	$t_{15(D)}$	3003	-	Note 10	200	-	ns
564 to 566	A Hold after $\overline{CS}$ Rising Edge during Write	$t_{16(A)}$	3003	-	Note 10	100	-	ns
567 to 569	D Hold after $\overline{CS}$ Rising Edge during Write	$t_{16(D)}$	3003	-	Note 10	100	-	ns
570 to 572	D Valid from Falling Edge of $\overline{CS}$ during Read	t_{17}	3003	-	Note 10	81	-	ns
573 to 575	D Valid from A Stable during Read	t_{18}	3003	-	Note 10	81	-	ns
576 to 578	$\overline{CS}$ Rising Edge to D 3-State after Read	t_{19}	3003	-	Note 10	81	-	ns

NOTES: See Page 33.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
5	Functional Test 1 (Basic)	-	3014	-	Verify Device Operation with Load V_{IL} = 0V, V_{IH} = 5.0V V_{OL} = 1.0V, V_{OH} = 4.0V I_{OUT} = ±2.0mA C_L = 100pF ± 20% V_{DD} = 5.0V, V_{SS} = 0V Pattern: M1 at 1.0MHz	-	-	-
6	Functional Test 2 (Nominal Voltage)	-	3014	-	Verify Device Operation with Load V_{IL}, V_{IH} = Note 1 V_{OL} = 1.0V, V_{OH} = 4.0V I_{OUT} = ±2.0mA C_L = 100pF ± 20% V_{DD} = 5.0V, V_{SS} = 0V Pattern: M1 at 10MHz	-	-	-
7	Functional Test 3 (High Voltage)	-	3014	-	Verify Device Operation with Load V_{IL}, V_{IH} = Note 1 V_{OL} = 1.0V, V_{OH} = 4.5V I_{OUT} = ±2.0mA C_L = 100pF ± 20% V_{DD} = 5.5V, V_{SS} = 0V Pattern: M1 at 10MHz	-	-	-
8	Functional Test 4 (Low Voltage)	-	3014	-	Verify Device Operation with Load V_{IL}, V_{IH} = Note 1 V_{OL} = 1.0V, V_{OH} = 3.5V I_{OUT} = ±2.0mA C_L = 100pF ± 20% V_{DD} = 4.5V, V_{SS} = 0V Pattern: M1 at 10MHz	-	-	-
9	Quiescent Current	I_{DD}	3005	4(b)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V All Outputs Open Note 2 (Pins 1 + 21 + 65)	-	3.5	mA

NOTES: See Page 33.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
10 to 60	Input Current Low Level	I_{IL}	3009	4(c)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 4-5-8-9-12-13-16-17-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-44-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84)	-	− 1.0	µA
61 to 111	Input Current High Level	I_{IH}	3009	4(d)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 4-5-8-9-12-13-16-17-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-44-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84)	-	1.0	µA
112 to 138	Output Voltage Low Level	V_{OL}	3007	4(e)	V_{IL}, V_{IH} = Note 1 I_{OL} = 4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pins 2-3-6-7-10-11-14-15-18-19-20-33-40-41-43-62-63-66-67-69-70-73-74-77-78-81-82)	-	0.4	V
139 to 165	Output Voltage High Level 1	V_{OH1}	3006	4(f)	V_{IL}, V_{IH} = Note 1 I_{OL} = − 4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pins 2-3-6-7-10-11-14-15-18-19-20-33-40-41-43-62-63-66-67-69-70-73-74-77-78-81-82)	3.9	-	V
166 to 192	Output Voltage High Level 2	V_{OH2}	3006	4(f)	V_{IL}, V_{IH} = Note 1 I_{OL} = − 0.5mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pins 2-3-6-7-10-11-14-15-18-19-20-33-40-41-43-62-63-66-67-69-70-73-74-77-78-81-82)	4.2	-	V

NOTES: See Page 33.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
193 to 200	Threshold Voltage Low Level 1 (TTL Inputs)	V_{THN1}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 18-19-20, Note 4) (Pins 23-24-25-26-27-28-29)	0.8	-	V
201 to 208	Threshold Voltage High Level 1 (TTL Inputs)	V_{THP1}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 18-19-20, Note 5) (Pins 23-24-25-26-27-28-29)	-	2.0	V
209	Threshold Voltage Low Level 2 (CMOS Inputs)	V_{THN2}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 4-5-8-9-12-13-16-17-31-32-34-35-36-42-44-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84, Note 4)	1.3	-	V
210	Threshold Voltage High Level 2 (CMOS Inputs)	V_{THP2}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 4-5-8-9-12-13-16-17-31-32-34-35-36-42-44-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84, Note 5)	-	3.2	V
211 to 215	Threshold Voltage Low Level 3 (SCHMITT Trigger Inputs)	V_{THN3}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 30-37-38-45-46)	1.0	2.8	V
216 to 220	Threshold Voltage High Level 3 (SCHMITT Trigger Inputs)	V_{THP3}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 30-37-38-45-46)	1.5	3.3	V
221 to 225	Hysteresis Voltage	V_H	-	4(h)	V_{DD} = 4.5V, V_{SS} = 0V Note 6 (Pins 30-37-38-45-46)	0.5	-	V
226 to 233	Threshold Voltage Low Level 4 (TTL Inputs)	V_{THN4}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 18-19-20, Note 4) (Pins 23-24-25-26-27-28-29)	0.8	-	V
234 to 241	Threshold Voltage High Level 4 (TTL Inputs)	V_{THP4}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 18-19-20, Note 5) (Pins 23-24-25-26-27-28-29)	-	2.0	V

NOTES: See Page 33.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
242	Threshold Voltage Low Level 5 (CMOS Inputs)	V_{THN5}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 4-5-8-9-12-13-16-17-31-32-34-35-36-42-44-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84, Note 4)	1.7	-	V
243	Threshold Voltage High Level 5 (CMOS Inputs)	V_{THP5}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 4-5-8-9-12-13-16-17-31-32-34-35-36-42-44-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84, Note 5)	-	3.9	V
244 to 248	Threshold Voltage Low Level 6 (SCHMITT Trigger Inputs)	V_{THN6}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 30-37-38-45-46)	1.2	3.8	V
249 to 253	Threshold Voltage High Level 6 (SCHMITT Trigger Inputs)	V_{THP6}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 30-37-38-45-46)	1.7	4.3	V
254 to 331	Input/Output Clamp Voltage (to V_{SS})	V_{IC1}	3022	4(i)	I_{IN} = −100µA V_{DD} = V_{SS} = 0V (Pins 2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-33-34-35-36-37-38-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-62-63-66-67-68-69-70-71-72-73-74-75-76-77-78-79-80-81-82-83-84)	-	−2.0	V
332 to 409	Input/Output Clamp Voltage (to V_{DD})	V_{IC2}	3022	4(i)	I_{IN} = 100µA V_{DD} = V_{SS} = 0V (Pins 2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-33-34-35-36-37-38-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-62-63-66-67-68-69-70-71-72-73-74-75-76-77-78-79-80-81-82-83-84)	-	2.0	V

NOTES: See Page 33.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
410 to 412	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	3006	4(j)	V_{IN} (3-State Control) = Note 7 V_{OUT} = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 18-19-20)	-	−20	µA
413 to 415	Output Leakage Current Third State (High Level Applied)	I_{OZH}	3006	4(j)	V_{IN} (3-State Control) = Note 7 V_{OUT} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 18-19-20)	-	20	µA
416	Supply Current 1 (During BIST)	I_{DDS1}	3005	4(b)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V Pattern M1 at 10MHz (Note 8)	-	63	mA
417	Supply Current 2 (During Normal Operation)	I_{DDS2}	3005	4(b)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V Pattern M1 at 10MHz (Note 8)	-	18	mA

NOTES: See Page 33.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
462 to 464	Rise and Fall Time (TTL and CMOS Inputs)	t_r1/t_f1	3004	-	Note 9	-	100	ns
465 to 467	Rise and Fall Time (SCHMITT Trigger Inputs)	t_r2/t_f2	3004	-	Note 9	-	1.0	µs
468 to 470	Clock Period for CLCWCLK	t_{CCK}	3003	-	Note 10	100	-	ns
471 to 473	Clock High Pulse Width for CLCWCLK	t_{CHI}	3003	-	Note 10	50	-	ns
474 to 476	Clock Low Pulse Width for CLCWCLK	t_{CLO}	3003	-	Note 10	50	-	ns
477 to 479	Clock Period for BITCLK	t_{BCK}	3003	-	Note 10	100	-	ns
480 to 482	Clock High Pulse Width for BITCLK	t_{BHI}	3003	-	Note 10	50	-	ns
483 to 485	Clock Low Pulse Width for BITCLK	t_{BLO}	3003	-	Note 10	50	-	ns
486 to 488	RESET Activated	t_{RES}	3003	-	Note 10	$3t_{BCK}$	-	-
489 to 491	PVCF Setup to Falling Edge of BITCLK	$t_{1(PVCF)}$	3003	-	Note 10	3.0	-	ns
492 to 494	PVCF Hold after Falling Edge of BITCLK	$t_{2(PVCF)}$	3003	-	Note 10	97	-	ns
495 to 497	RTS Setup to Falling Edge of BITCLK	$t_{1(RTS)}$	3003	-	Note 10	3.0	-	ns
498 to 500	RTS Hold after Falling Edge of BITCLK	$t_{2(RTS)}$	3003	-	Note 10	97	-	ns

NOTES: See Page 33.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
501 to 503	RTS Setup to Rising Edge of SYNCMARK (Ext. Selection)	t_3	3003	-	Note 10	$2t_{BCK}$	-	-
504 to 506	RTS Hold after Rising Edge of SYNCMARK (Ext. Selection)	t_4	3003	-	Note 10	$2t_{BCK}$	-	-
507 to 509	POLL Valid from Falling Edge of BITCLK	$t_{5(POLL)}$	3003	-	$I_{OUT} \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 10	-	53	ns
510 to 512	CTS Valid from Falling Edge of BITCLK	$t_{5(CTS)}$	3003	-	$I_{OUT} \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 10	-	53	ns
513 to 515	SOUT Valid from Falling Edge of BITCLK	$t_{5(SOUT)}$	3003	-	$I_{OUT} \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 10	-	53	ns
516 to 518	FRAME Valid from Falling Edge of BITCLK	$t_{5(FRAME)}$	3003	-	$I_{OUT} \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 10	-	54	ns
519 to 521	ODDFRAME Valid from Falling Edge of BITCLK	$t_{5(ODD-FRAME)}$	3003	-	$I_{OUT} \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 10	-	54	ns
522 to 524	ALTSOUT Valid from Falling Edge of BITCLK	$t_{6(ALT-SOUT)}$	3003	-	$I_{OUT} \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 10	-	56	ns
525 to 527	SYNCMARK Valid from Falling Edge of BITCLK	$t_{6(SYNC-MARK)}$	3003	-	$I_{OUT} \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 10	-	57	ns
528 to 530	D0TTC, D1TTC Setup to CLKTTC Low	t_7	3003	-	Note 11	60	-	ns
531 to 533	D0TTC, D1TTC Hold after CLKTTC Low	t_8	3003	-	Note 11	0	-	ns
534 to 536	SELCLCW Setup to SAMPLE Low	$t_{9(SEL-CLCW)}$	3003	-	Note 11	$2t_{BCK}$	-	-

NOTES: See Page 33.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
537 to 539	TCID Setup to SAMPLE Low	$t_{9(TCID)}$	3003	-	Note 11	$2t_{BCK}$	-	-
540 to 542	SELCLCW Hold after SAMPLE Low	$t_{10(SEL-CLCW)}$	3003	-	Note 11	$2t_{BCK}$	-	-
543 to 545	TCID Hold after SAMPLE Low	$t_{10(TCID)}$	3003	-	Note 11	$2t_{BCK}$	-	-
546 to 548	R/$\overline{W}$ Low to $\overline{CS}$ Low	t_{11}	3003	-	Note 10	100	-	ns
549 to 551	$\overline{CS}$ High to R/$\overline{W}$ High	t_{12}	3003	-	Note 10	100	-	ns
552 to 554	$\overline{CS}$ Width	t_{13}	3003	-	Note 10	100	-	ns
555 to 557	$\overline{CS}$ Width De-activated after Write	t_{14}	3003	-	Note 10	$4t_{BCK}$	-	-
558 to 560	A to $\overline{CS}$ Rising Edge during Write	$t_{15(A)}$	3003	-	Note 10	200	-	ns
561 to 563	D to $\overline{CS}$ Rising Edge during Write	$t_{15(D)}$	3003	-	Note 10	200	-	ns
564 to 566	A Hold after $\overline{CS}$ Rising Edge during Write	$t_{16(A)}$	3003	-	Note 10	100	-	ns
567 to 569	D Hold after $\overline{CS}$ Rising Edge during Write	$t_{16(D)}$	3003	-	Note 10	100	-	ns
570 to 572	D Valid from Falling Edge of $\overline{CS}$ during Read	t_{17}	3003	-	Note 10	81	-	ns
573 to 575	D Valid from A Stable during Read	t_{18}	3003	-	Note 10	81	-	ns
576 to 578	$\overline{CS}$ Rising Edge to D 3-State after Read	t_{19}	3003	-	Note 10	81	-	ns

NOTES: See Page 33.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
5	Functional Test 1 (Basic)	-	3014	-	Verify Device Operation with Load V_{IL} = 0V, V_{IH} = 5.0V V_{OL} = 1.0V, V_{OH} = 4.0V I_{OUT} = ±2.0mA C_L = 100pF ± 20% V_{DD} = 5.0V, V_{SS} = 0V Pattern: M1 at 1.0MHz	-	-	-
6	Functional Test 2 (Nominal Voltage)	-	3014	-	Verify Device Operation with Load V_{IL}, V_{IH} = Note 1 V_{OL} = 1.0V, V_{OH} = 4.0V I_{OUT} = ±2.0mA C_L = 100pF ± 20% V_{DD} = 5.0V, V_{SS} = 0V Pattern: M1 at 10MHz	-	-	-
7	Functional Test 3 (High Voltage)	-	3014	-	Verify Device Operation with Load V_{IL}, V_{IH} = Note 1 V_{OL} = 1.0V, V_{OH} = 4.5V I_{OUT} = ±2.0mA C_L = 100pF ± 20% V_{DD} = 5.5V, V_{SS} = 0V Pattern: M1 at 10MHz	-	-	-
8	Functional Test 4 (Low Voltage)	-	3014	-	Verify Device Operation with Load V_{IL}, V_{IH} = Note 1 V_{OL} = 1.0V, V_{OH} = 3.5V I_{OUT} = ±2.0mA C_L = 100pF ± 20% V_{DD} = 4.5V, V_{SS} = 0V Pattern: M1 at 10MHz	-	-	-
9	Quiescent Current	I_{DD}	3005	4(b)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V All Outputs Open Note 2 (Pins 1 + 21 + 65)	-	0.5	mA

NOTES: See Page 33.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
10 to 60	Input Current Low Level	I_{IL}	3009	4(c)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 4-5-8-9-12-13-16-17-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-44-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84)	-	−1.0	µA
61 to 111	Input Current High Level	I_{IH}	3009	4(d)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 4-5-8-9-12-13-16-17-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-44-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84)	-	1.0	µA
112 to 138	Output Voltage Low Level	V_{OL}	3007	4(e)	V_{IL}, V_{IH} = Note 1 I_{OL} = 4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pins 2-3-6-7-10-11-14-15-18-19-20-33-40-41-43-62-63-66-67-69-70-73-74-77-78-81-82)	-	0.4	V
139 to 165	Output Voltage High Level 1	V_{OH1}	3006	4(f)	V_{IL}, V_{IH} = Note 1 I_{OL} = −4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pins 2-3-6-7-10-11-14-15-18-19-20-33-40-41-43-62-63-66-67-69-70-73-74-77-78-81-82)	3.9	-	V
166 to 192	Output Voltage High Level 2	V_{OH2}	3006	4(f)	V_{IL}, V_{IH} = Note 1 I_{OL} = −0.5mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pins 2-3-6-7-10-11-14-15-18-19-20-33-40-41-43-62-63-66-67-69-70-73-74-77-78-81-82)	4.2	-	V

NOTES: See Page 33.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
193 to 200	Threshold Voltage Low Level 1 (TTL Inputs)	V_{THN1}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 18-19-20, Note 4) (Pins 23-24-25-26-27-28-29)	0.8	-	V
201 to 208	Threshold Voltage High Level 1 (TTL Inputs)	V_{THP1}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 18-19-20, Note 5) (Pins 23-24-25-26-27-28-29)	-	2.0	V
209	Threshold Voltage Low Level 2 (CMOS Inputs)	V_{THN2}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 4-5-8-9-12-13-16-17-31-32-34-35-36-42-44-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84, Note 4)	1.3	-	V
210	Threshold Voltage High Level 2 (CMOS Inputs)	V_{THP2}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 4-5-8-9-12-13-16-17-31-32-34-35-36-42-44-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84, Note 5)	-	3.2	V
211 to 215	Threshold Voltage Low Level 3 (SCHMITT Trigger Inputs)	V_{THN3}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 30-37-38-45-46)	1.0	2.8	V
216 to 220	Threshold Voltage High Level 3 (SCHMITT Trigger Inputs)	V_{THP3}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 30-37-38-45-46)	1.5	3.3	V
221 to 225	Hysteresis Voltage	V_H	-	4(h)	V_{DD} = 4.5V, V_{SS} = 0V Note 6 (Pins 30-37-38-45-46)	0.5	-	V
226 to 233	Threshold Voltage Low Level 4 (TTL Inputs)	V_{THN4}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 18-19-20, Note 4) (Pins 23-24-25-26-27-28-29)	0.8	-	V
234 to 241	Threshold Voltage High Level 4 (TTL Inputs)	V_{THP4}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 18-19-20, Note 5) (Pins 23-24-25-26-27-28-29)	-	2.0	V

NOTES: See Page 33.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
242	Threshold Voltage Low Level 5 (CMOS Inputs)	V_{THN5}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 4-5-8-9-12-13-16-17-31-32-34-35-36-42-44-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84, Note 4)	1.7	-	V
243	Threshold Voltage High Level 5 (CMOS Inputs)	V_{THP5}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 4-5-8-9-12-13-16-17-31-32-34-35-36-42-44-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84, Note 5)	-	3.9	V
244 to 248	Threshold Voltage Low Level 6 (SCHMITT Trigger Inputs)	V_{THN6}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 30-37-38-45-46)	1.2	3.8	V
249 to 253	Threshold Voltage High Level 6 (SCHMITT Trigger Inputs)	V_{THP6}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 30-37-38-45-46)	1.7	4.3	V
254 to 331	Input/Output Clamp Voltage (to V_{SS})	V_{IC1}	3022	4(i)	I_{IN} = −100μA V_{DD} = V_{SS} = 0V (Pins 2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-33-34-35-36-37-38-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-62-63-66-67-68-69-70-71-72-73-74-75-76-77-78-79-80-81-82-83-84)	-	−2.0	V
332 to 409	Input/Output Clamp Voltage (to V_{DD})	V_{IC2}	3022	4(i)	I_{IN} = 100μA V_{DD} = V_{SS} = 0V (Pins 2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-33-34-35-36-37-38-40-41-42-43-44-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-62-63-66-67-68-69-70-71-72-73-74-75-76-77-78-79-80-81-82-83-84)	-	2.0	V

NOTES: See Page 33.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
410 to 412	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	3006	4(j)	V_{IN} (3-State Control) = Note 7 V_{OUT} = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 18-19-20)	-	−10	µA
413 to 415	Output Leakage Current Third State (High Level Applied)	I_{OZH}	3006	4(j)	V_{IN} (3-State Control) = Note 7 V_{OUT} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 18-19-20)	-	10	µA
416	Supply Current 1 (During BIST)	I_{DDS1}	3005	4(b)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V Pattern M1 at 10MHz (Note 8)	-	60	mA
417	Supply Current 2 (During Normal Operation)	I_{DDS2}	3005	4(b)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V Pattern M1 at 10MHz (Note 8)	-	15	mA

NOTES: See Page 33.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
462 to 464	Rise and Fall Time (TTL and CMOS Inputs)	t_r1/t_f1	3004	-	Note 9	-	100	ns
465 to 467	Rise and Fall Time (SCHMITT Trigger Inputs)	t_r2/t_f2	3004	-	Note 9	-	1.0	µs
468 to 470	Clock Period for CLCWCLK	t_{CCK}	3003	-	Note 10	100	-	ns
471 to 473	Clock High Pulse Width for CLCWCLK	t_{CHI}	3003	-	Note 10	50	-	ns
474 to 476	Clock Low Pulse Width for CLCWCLK	t_{CLO}	3003	-	Note 10	50	-	ns
477 to 479	Clock Period for BITCLK	t_{BCK}	3003	-	Note 10	100	-	ns
480 to 482	Clock High Pulse Width for BITCLK	t_{BHI}	3003	-	Note 10	50	-	ns
483 to 485	Clock Low Pulse Width for BITCLK	t_{BLO}	3003	-	Note 10	50	-	ns
486 to 488	RESET Activated	t_{RES}	3003	-	Note 10	$3t_{BCK}$	-	-
489 to 491	PVCF Setup to Falling Edge of BITCLK	$t_{1(PVCF)}$	3003	-	Note 10	3.0	-	ns
492 to 494	PVCF Hold after Falling Edge of BITCLK	$t_{2(PVCF)}$	3003	-	Note 10	97	-	ns
495 to 497	RTS Setup to Falling Edge of BITCLK	$t_{1(RTS)}$	3003	-	Note 10	3.0	-	ns
498 to 500	RTS Hold after Falling Edge of BITCLK	$t_{2(RTS)}$	3003	-	Note 10	97	-	ns

NOTES: See Page 33.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
501 to 503	RTS Setup to Rising Edge of SYNCMARK (Ext. Selection)	t_3	3003	-	Note 10	$2t_{BCK}$	-	-
504 to 506	RTS Hold after Rising Edge of SYNCMARK (Ext. Selection)	t_4	3003	-	Note 10	$2t_{BCK}$	-	-
507 to 509	POLL Valid from Falling Edge of BITCLK	$t_{5(POLL)}$	3003	-	$I_{OUT} \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 10	-	53	ns
510 to 512	CTS Valid from Falling Edge of BITCLK	$t_{5(CTS)}$	3003	-	$I_{OUT} \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 10	-	53	ns
513 to 515	SOUT Valid from Falling Edge of BITCLK	$t_{5(SOUT)}$	3003	-	$I_{OUT} \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 10	-	53	ns
516 to 518	FRAME Valid from Falling Edge of BITCLK	$t_{5(FRAME)}$	3003	-	$I_{OUT} \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 10	-	54	ns
519 to 521	ODDFRAME Valid from Falling Edge of BITCLK	$t_{5(ODD-FRAME)}$	3003	-	$I_{OUT} \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 10	-	54	ns
522 to 524	ALTSOUT Valid from Falling Edge of BITCLK	$t_{6(ALT-SOUT)}$	3003	-	$I_{OUT} \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 10	-	56	ns
525 to 527	SYNCMARK Valid from Falling Edge of BITCLK	$t_{6(SYNC-MARK)}$	3003	-	$I_{OUT} \pm 2.0mA$ $C_L = 100pF \pm 20\%$ Note 10	-	57	ns
528 to 530	D0TTC, D1TTC Setup to CLKTTC Low	t_7	3003	-	Note 11	60	-	ns
531 to 533	D0TTC, D1TTC Hold after CLKTTC Low	t_8	3003	-	Note 11	0	-	ns
534 to 536	SELCLCW Setup to SAMPLE Low	$t_{9(SEL-CLCW)}$	3003	-	Note 11	$2t_{BCK}$	-	-

NOTES: See Page 33.

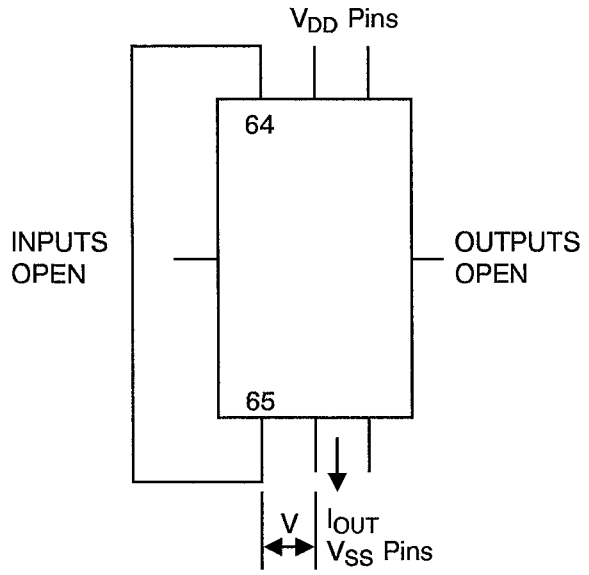
TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
537 to 539	TCID Setup to SAMPLE Low	$t_{9(TCID)}$	3003	-	Note 11	$2t_{BCK}$	-	-
540 to 542	SELCLCW Hold after SAMPLE Low	$t_{10(SEL-CLCW)}$	3003	-	Note 11	$2t_{BCK}$	-	-
543 to 545	TCID Hold after SAMPLE Low	$t_{10(TCID)}$	3003	-	Note 11	$2t_{BCK}$	-	-
546 to 548	R/$\overline{W}$ Low to $\overline{CS}$ Low	t_{11}	3003	-	Note 10	100	-	ns
549 to 551	$\overline{CS}$ High to R/$\overline{W}$ High	t_{12}	3003	-	Note 10	100	-	ns
552 to 554	$\overline{CS}$ Width	t_{13}	3003	-	Note 10	100	-	ns
555 to 557	$\overline{CS}$ Width De-activated after Write	t_{14}	3003	-	Note 10	$4t_{BCK}$	-	-
558 to 560	A to $\overline{CS}$ Rising Edge during Write	$t_{15(A)}$	3003	-	Note 10	200	-	ns
561 to 563	D to $\overline{CS}$ Rising Edge during Write	$t_{15(D)}$	3003	-	Note 10	200	-	ns
564 to 566	A Hold after $\overline{CS}$ Rising Edge during Write	$t_{16(A)}$	3003	-	Note 10	100	-	ns
567 to 569	D Hold after $\overline{CS}$ Rising Edge during Write	$t_{16(D)}$	3003	-	Note 10	100	-	ns
570 to 572	D Valid from Falling Edge of $\overline{CS}$ during Read	t_{17}	3003	-	Note 10	81	-	ns
573 to 575	D Valid from A Stable during Read	t_{18}	3003	-	Note 10	81	-	ns
576 to 578	$\overline{CS}$ Rising Edge to D 3-State after Read	t_{19}	3003	-	Note 10	81	-	ns

NOTES: See Page 33.

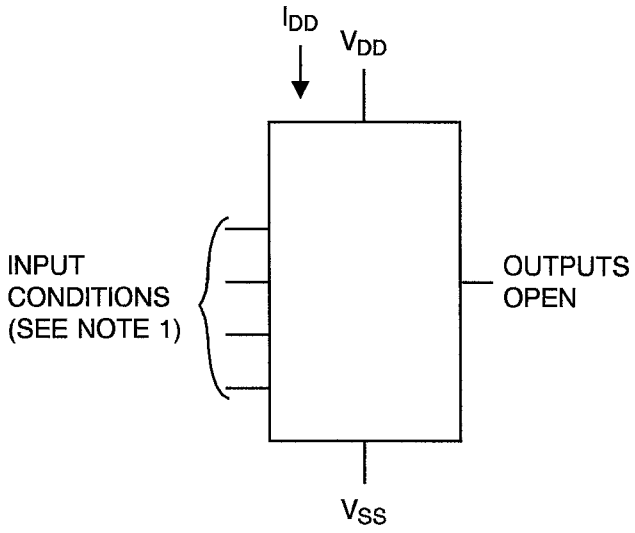
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - V_{SS}, V_{DD} CONTINUITY



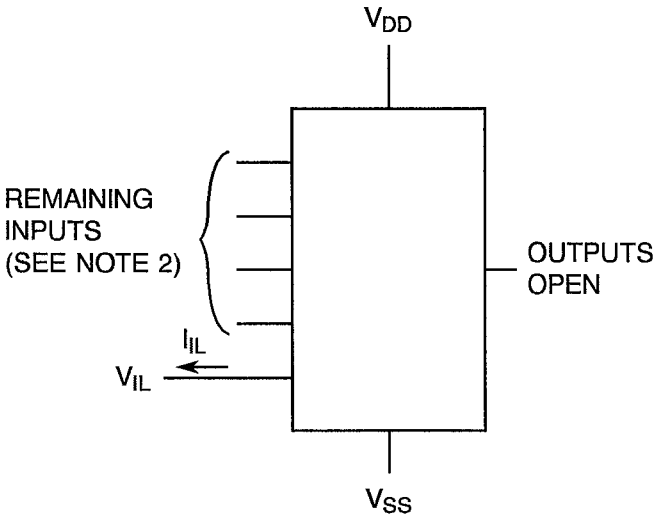
NOTES
1. Each power pin tested separately.

FIGURE 4(b) - QUIESCENT CURRENT



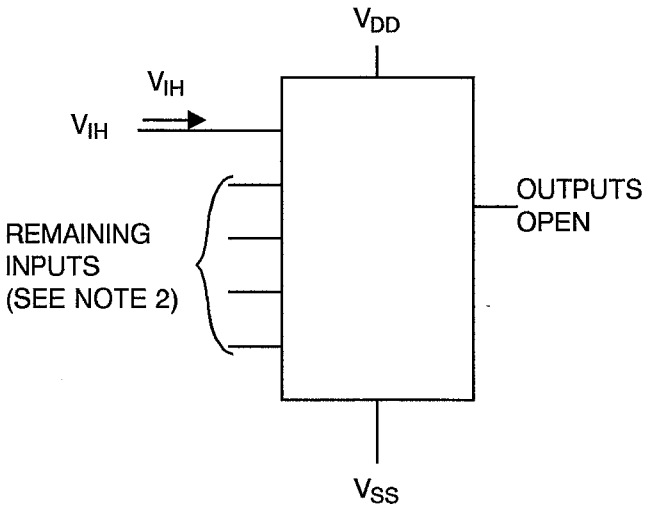
NOTES
1. Input conditions as per Table 2.

FIGURE 4(c) - INPUT CURRENT LOW LEVEL



NOTES
1. Each input to be tested separately.
2. Input conditions as per Table 2.

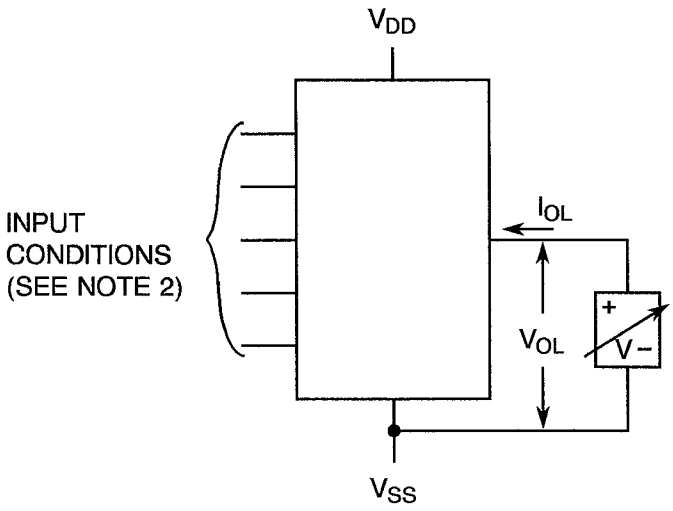
FIGURE 4(d) - INPUT CURRENT HIGH LEVEL



NOTES
1. Each input to be tested separately.
2. Input conditions as per Table 2.

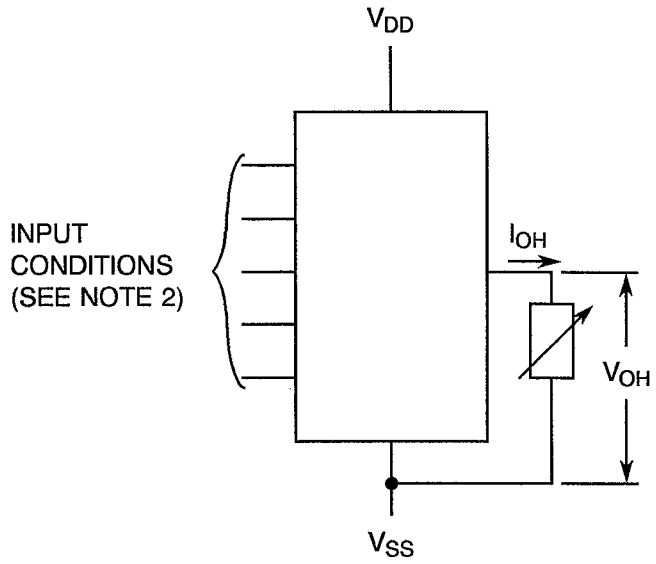
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(e) - OUTPUT VOLTAGE LOW LEVEL



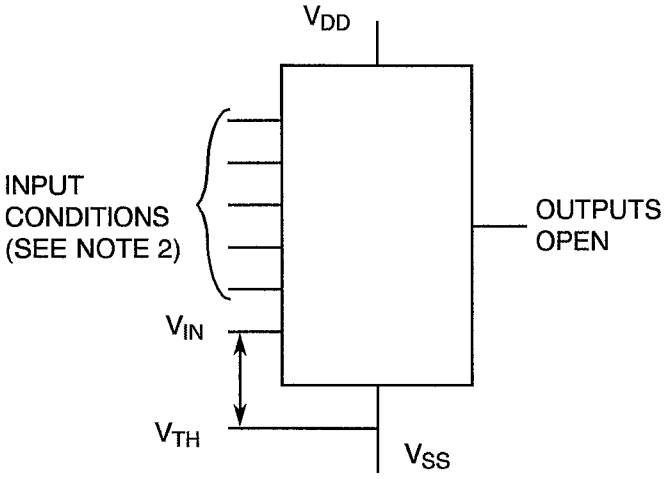
NOTES
1. Each output to be tested separately.
2. Input conditions as per Table 2.

FIGURE 4(f) - OUTPUT VOLTAGE HIGH LEVEL



NOTES
1. Each output to be tested separately.
2. Input conditions as per Table 2.

FIGURE 4(g) - THRESHOLD VOLTAGE



NOTES
1. Each input to be tested separately.
2. Input conditions as per Table 2.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(h) - HYSTERESIS VOLTAGE

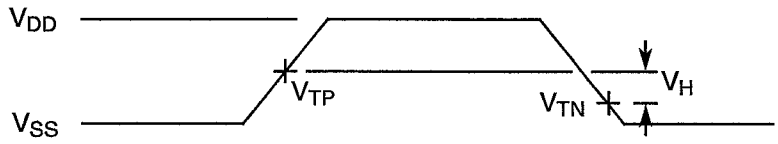
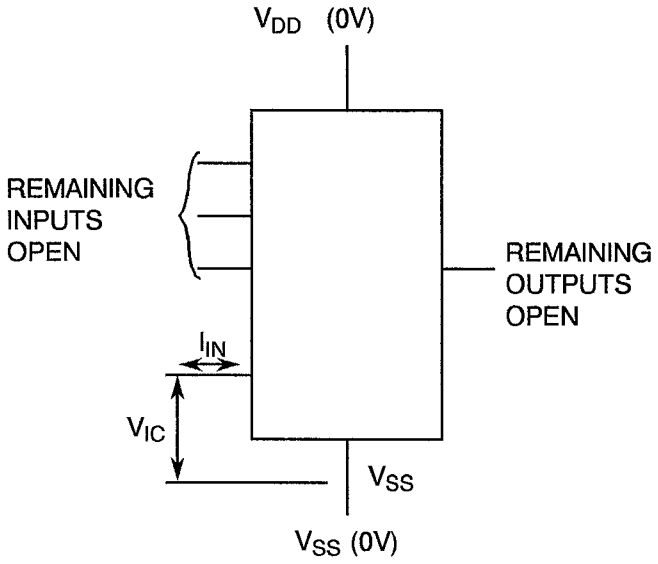


FIGURE 4(i) - INPUT/OUTPUT CLAMP VOLTAGE

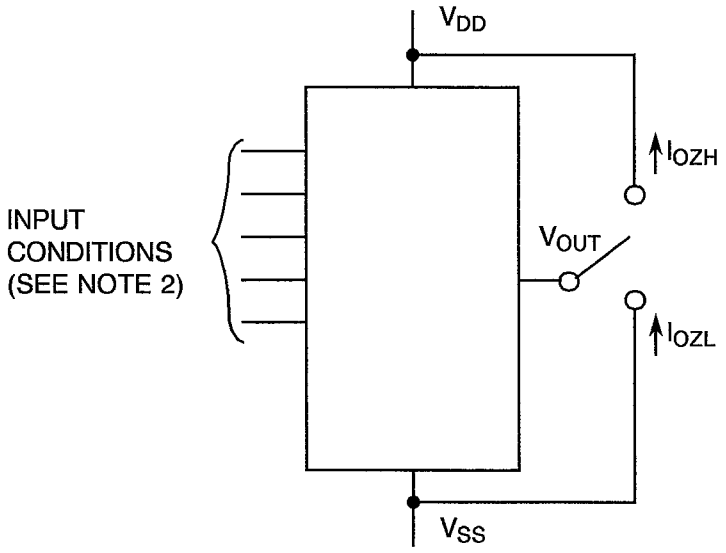


NOTES

1. Each input and output to be tested separately.

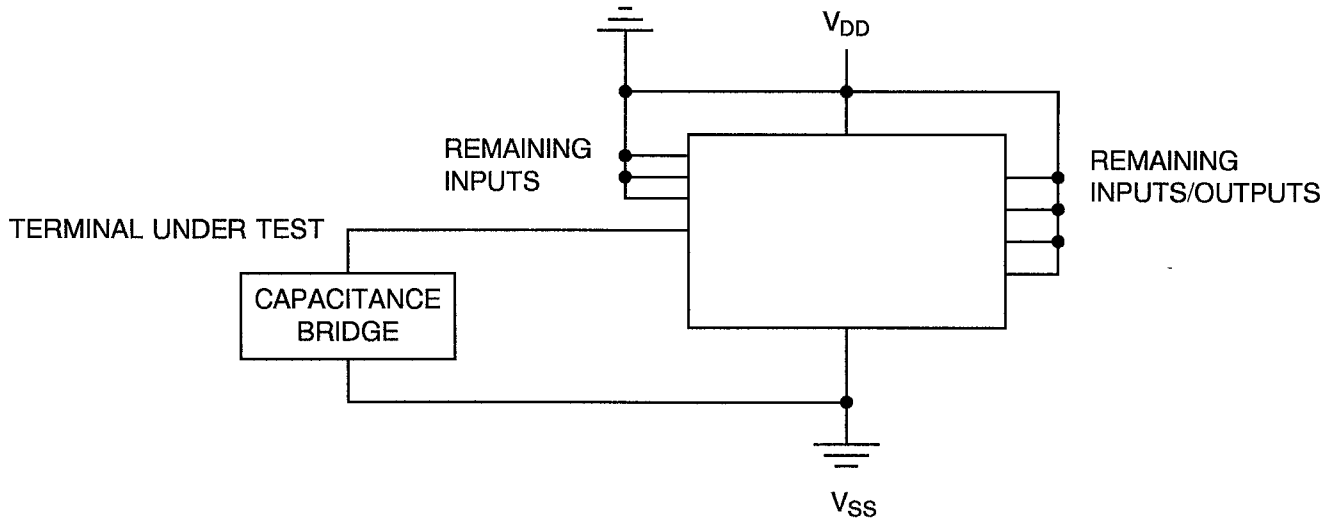
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(j) - OUTPUT LEAKAGE CURRENT THIRD STATE



NOTES
1. Each output to be tested separately.
2. Input conditions as per Table 2.

FIGURE 4(k) - INPUT AND INPUT/OUTPUT CAPACITANCE



NOTES
1. Test frequency = 1.0MHz.
2. Each input and input/output is to be tested separately.

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
9	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	±250	µA
10 to 60	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	±200	nA
61 to 111	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	±200	nA
112 to 138	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	±200	mV
139 to 165	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	±300	mV
410 to 412	Output Leakage Current (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	±2.0	µA
413 to 415	Output Leakage Current (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	±2.0	µA

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0−5)	°C
2	Outputs - (Pins 2-3-6-7-10-11-14-15-33-40-41-43-62-63-66-67-69-70-73-74-77-78-81-82)	V_{OUT}	$V_{DD}/2$	V
3	Input - (Pin 31)	V_{IN}	V_{DD}	V
4	Input - (Pins 32-42)	V_{IN}	V_{SS}	V
5	Inputs - (Pins 4-5-8-9-12-13-16-17-18-19-20-23-24-25-26-27-28-29-34-35-36-37-38-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84)	V_{IN}	V_{GEN1}	V
6	Input - (Pin 30)	V_{IN}	V_{GEN3}	Vac
7	Input - (Pin 44)	V_{IN}	V_{GEN2}	Vac
8	Pulse Voltage	V_{GEN}	0V to V_{DD}	Vac
9	Pulse Frequency Square Wave	f_{GEN1} f_{GEN2}	$f_{GEN2}/2$ 250k 50% Duty Cycle	Hz
10	Pulse Square Wave	GEN3	Pulse width at lower level = 3 cycles of GEN2 repeated after 1000 cycles of GEN2	-
11	Positive Supply Voltage (Pins 1-21-65)	V_{DD}	5.5(+0−0.5)	V
12	Negative Supply Voltage (Pins 22-39-64)	V_{SS}	0	V

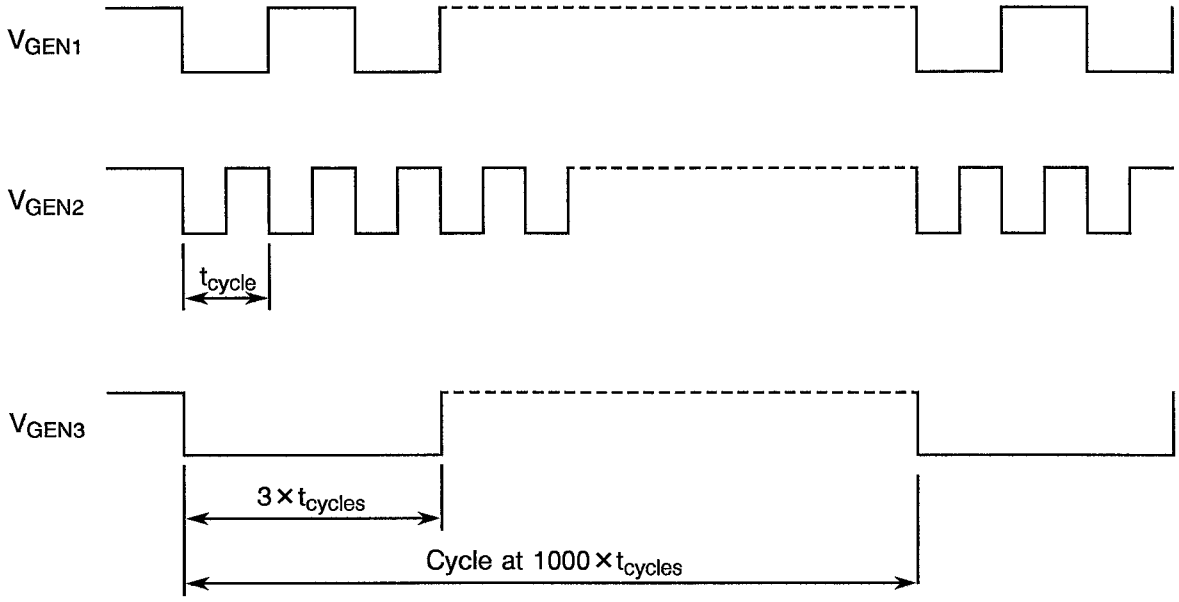
NOTES

1. Input Protection Resistor = Output Load = 10kΩ.

TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS (CONT'D)

NOTES

1.

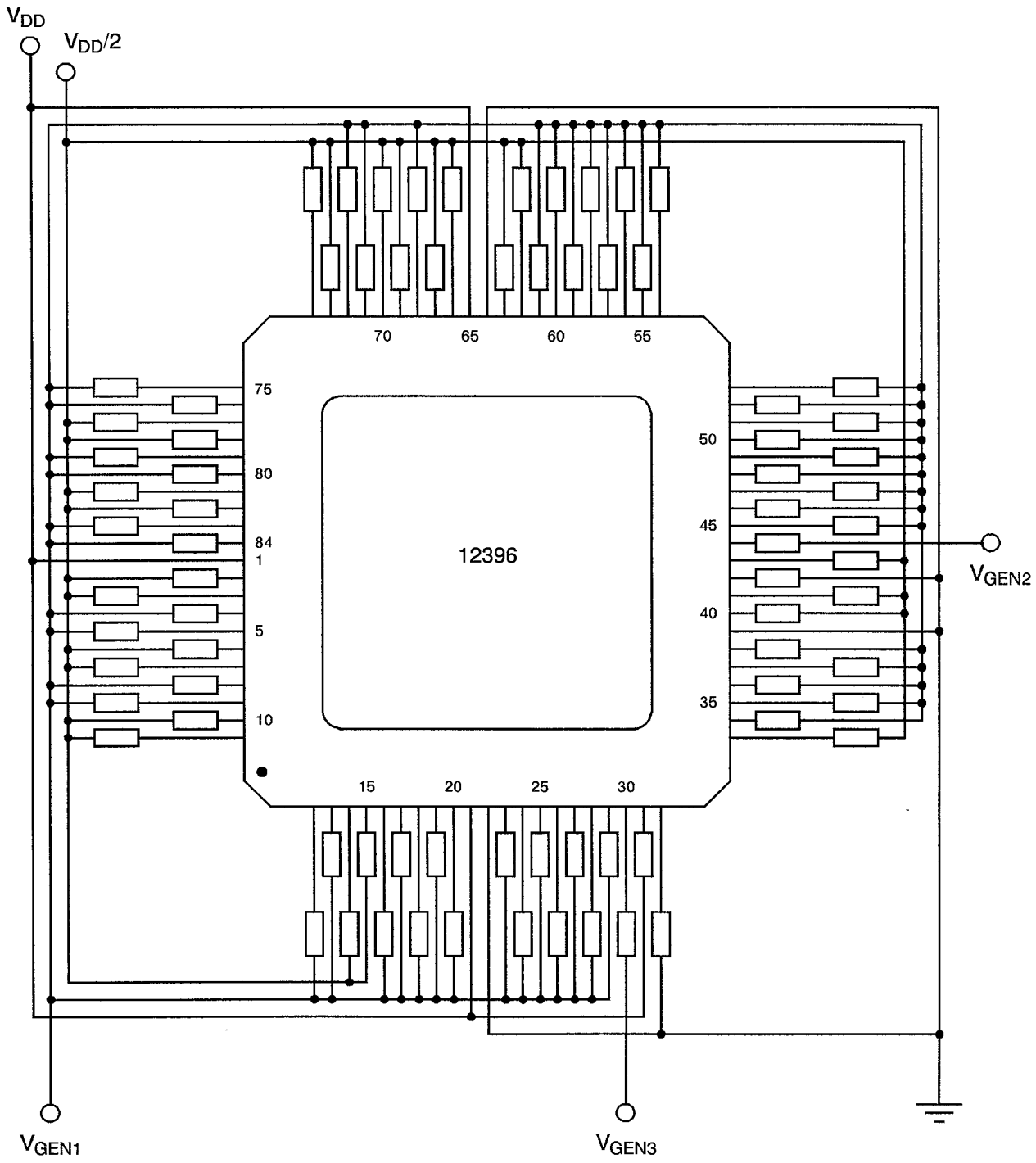


$t_{cycle} = 4.0\mu s.$

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(b) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

4.9 TOTAL DOSE IRRADIATION TESTING

4.9.1 Application

If specified in Para. 4.2.1 of this specification, total dose irradiation testing shall be performed in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.9.2 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6.

4.9.3 Electrical Measurements

The parameters to be measured prior to irradiation exposure are scheduled in Table 2 of this specification. Only devices which meet the requirements of Table 2 shall be scheduled in the test sample.

The parameters to be measured during and on completion of irradiation testing are scheduled in Table 7 of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
5	Functional Test 1 (Basic)	-	As per Table 2	As per Table 2	-	-	-
6	Functional Test 2 (Nominal Voltage)	-	As per Table 2	As per Table 2	-	-	-
7	Functional Test 3 (High Voltage)	-	As per Table 2	As per Table 2	-	-	-
8	Functional Test 4 (Low Voltage)	-	As per Table 2	As per Table 2	-	-	-
9	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	-	0.5	mA
10 to 60	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	-	−1.0	µA
61 to 111	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	-	1.0	µA
112 to 138	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	-	0.4	V
139 to 165	Output Voltage High Level 1	V_{OH1}	As per Table 2	As per Table 2	3.9	-	V
166 to 192	Output Voltage High Level 2	V_{OH2}	As per Table 2	As per Table 2	4.2	-	V
193 to 200	Threshold Voltage Low Level 1 (TTL Inputs)	V_{THN1}	As per Table 2	As per Table 2	0.8	-	V
201 to 208	Threshold Voltage High Level 1 (TTL Inputs)	V_{THP1}	As per Table 2	As per Table 2	-	2.0	V
209	Threshold Voltage Low Level 2 (CMOS Inputs)	V_{THN2}	As per Table 2	As per Table 2	1.3	-	V
210	Threshold Voltage High Level 2 (CMOS Inputs)	V_{THP2}	As per Table 2	As per Table 2	-	3.2	V
211 to 215	Threshold Voltage Low Level 3 (SCHMITT Trigger Inputs)	V_{THN3}	As per Table 2	As per Table 2	1.0	2.8	V

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
216 to 220	Threshold Voltage High Level 3 (SCHMITT Trigger Inputs)	V_{THP3}	As per Table 2	As per Table 2	1.5	3.3	V
221 to 225	Hysteresis Voltage	V_H	As per Table 2	As per Table 2	0.5	-	V
226 to 233	Threshold Voltage Low Level 4 (TTL Inputs)	V_{THN4}	As per Table 2	As per Table 2	0.8	-	V
234 to 241	Threshold Voltage High Level 4 (TTL Inputs)	V_{THP4}	As per Table 2	As per Table 2	-	2.0	V
242	Threshold Voltage Low Level 5 (CMOS Inputs)	V_{THN5}	As per Table 2	As per Table 2	1.7	-	V
243	Threshold Voltage High Level 5 (CMOS Inputs)	V_{THP5}	As per Table 2	As per Table 2	-	3.9	V
244 to 248	Threshold Voltage Low Level 6 (SCHMITT Trigger Inputs)	V_{THN6}	As per Table 2	As per Table 2	1.2	3.8	V
249 to 253	Threshold Voltage High Level 6 (SCHMITT Trigger Inputs)	V_{THP6}	As per Table 2	As per Table 2	1.7	4.3	V
254 to 331	Input/Output Clamp Voltage (to V_{SS})	V_{IC1}	As per Table 2	As per Table 2	-	−2.0	V
332 to 409	Input/Output Clamp Voltage (to V_{DD})	V_{IC2}	As per Table 2	As per Table 2	-	2.0	V
410 to 412	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	-	−10	µA
413 to 415	Output Leakage Current Third State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	-	10	µA
416	Supply Current 1 (During BIST)	I_{DDS1}	As per Table 2	As per Table 2	-	60	mA

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
417	Supply Current 2 (During Normal Operation)	I_{DDS2}	As per Table 2	As per Table 2	-	15	mA
486 to 488	RESET Activated	t_{RES}	As per Table 2	As per Table 2	$3t_{BCK}$	-	-
489 to 491	PVCF Setup to Falling Edge of BITCLK	$t_{1(PVCF)}$	As per Table 2	As per Table 2	3.0	-	ns
492 to 494	PVCF Hold after Falling Edge of BITCLK	$t_{2(PVCF)}$	As per Table 2	As per Table 2	97	-	ns
495 to 497	RTS Setup to Falling Edge of BITCLK	$t_{1(RTS)}$	As per Table 2	As per Table 2	3.0	-	ns
498 to 500	RTS Hold after Falling Edge of BITCLK	$t_{2(RTS)}$	As per Table 2	As per Table 2	97	-	ns
501 to 503	RTS Setup to Rising Edge of SYNCMARK (Ext. Selection)	t_3	As per Table 2	As per Table 2	$2t_{BCK}$	-	-
504 to 506	RTS Hold after Rising Edge of SYNCMARK (Ext. Selection)	t_4	As per Table 2	As per Table 2	$2t_{BCK}$	-	-
507 to 509	POLL Valid from Falling Edge of BITCLK	$t_{5(POLL)}$	As per Table 2	As per Table 2	-	53	ns
510 to 512	CTS Valid from Falling Edge of BITCLK	$t_{5(CTS)}$	As per Table 2	As per Table 2	-	53	ns
513 to 515	SOUT Valid from Falling Edge of BITCLK	$t_{5(SOUT)}$	As per Table 2	As per Table 2	-	53	ns
516 to 518	FRAME Valid from Falling Edge of BITCLK	$t_{5(FRAME)}$	As per Table 2	As per Table 2	-	54	ns
519 to 521	ODDFRAME Valid from Falling Edge of BITCLK	$t_{5(ODD-FRAME)}$	As per Table 2	As per Table 2	-	54	ns

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
522 to 524	ALTSOUT Valid from Falling Edge of BITCLK	$t_{6(ALT-SOUT)}$	As per Table 2	As per Table 2	-	56	ns
525 to 527	SYNCMARK Valid from Falling Edge of BITCLK	$t_{6(SYNC-MARK)}$	As per Table 2	As per Table 2	-	57	ns
528 to 530	D0TTC, D1TTC Setup to CLKTTC Low	t_7	As per Table 2	As per Table 2	60	-	ns
531 to 533	D0TTC, D1TTC Hold after CLKTTC Low	t_8	As per Table 2	As per Table 2	0	-	ns
534 to 536	SELCLCW Setup to SAMPLE Low	$t_{9(SEL-CLCW)}$	As per Table 2	As per Table 2	$2t_{BCK}$	-	-
537 to 539	TCID Setup to SAMPLE Low	$t_{9(TCID)}$	As per Table 2	As per Table 2	$2t_{BCK}$	-	-
540 to 542	SELCLCW Hold after SAMPLE Low	$t_{10(SEL-CLCW)}$	As per Table 2	As per Table 2	$2t_{BCK}$	-	-
543 to 545	TCID Hold after SAMPLE Low	$t_{10(TCID)}$	As per Table 2	As per Table 2	$2t_{BCK}$	-	-
546 to 548	R/$\overline{W}$ Low to $\overline{CS}$ Low	t_{11}	As per Table 2	As per Table 2	100	-	ns
549 to 551	$\overline{CS}$ High to R/$\overline{W}$ High	t_{12}	As per Table 2	As per Table 2	100	-	ns
552 to 554	$\overline{CS}$ Width	t_{13}	As per Table 2	As per Table 2	100	-	ns
555 to 557	$\overline{CS}$ Width De-activated after Write	t_{14}	As per Table 2	As per Table 2	$4t_{BCK}$	-	-
558 to 560	A to $\overline{CS}$ Rising Edge during Write	$t_{15(A)}$	As per Table 2	As per Table 2	200	-	ns

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
561 to 563	D to $\overline{CS}$ Rising Edge during Write	$t_{15(D)}$	As per Table 2	As per Table 2	200	-	ns
564 to 566	A Hold after $\overline{CS}$ Rising Edge during Write	$t_{16(A)}$	As per Table 2	As per Table 2	100	-	ns
567 to 569	D Hold after $\overline{CS}$ Rising Edge during Write	$t_{16(D)}$	As per Table 2	As per Table 2	100	-	ns
570 to 572	D Valid from Falling Edge of $\overline{CS}$ during Read	t_{17}	As per Table 2	As per Table 2	81	-	ns
573 to 575	D Valid from A Stable during Read	t_{18}	As per Table 2	As per Table 2	81	-	ns
576 to 578	$\overline{CS}$ Rising Edge to D 3-State after Read	t_{19}	As per Table 2	As per Table 2	81	-	ns

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0−5)	°C
2	Outputs - (Pins 2-3-6-7-10-11-14-15-33-40-41-43-62-63-66-67-69-70-73-74-77-78-81-82)	V_{OUT}	$V_{DD}/2$	V
3	Input - (Pin 31)	V_{IN}	V_{DD}	V
4	Input - (Pins 32-42)	V_{IN}	V_{SS}	V
5	Inputs - (Pins 4-5-8-9-12-13-16-17-18-19-20-23-24-25-26-27-28-29-34-35-36-37-38-45-46-47-48-49-50-51-52-53-54-55-56-57-58-59-60-61-68-71-72-75-76-79-80-83-84)	V_{IN}	V_{GEN1}	V
6	Input - (Pin 30)	V_{IN}	V_{GEN3}	Vac
7	Input - (Pin 44)	V_{IN}	V_{GEN2}	Vac
8	Pulse Voltage	V_{GEN}	0V to V_{DD}	Vac
9	Pulse Frequency Square Wave	f_{GEN1} f_{GEN2}	$f_{GEN2}/2$ 250k 50% Duty Cycle	Hz
10	Pulse Square Wave	GEN3	Pulse width at lower level = 3 cycles of GEN2 repeated after 1000 cycles of GEN2	-
11	Positive Supply Voltage (Pins 1-21-65)	V_{DD}	5.5(+0−0.5)	V
12	Negative Supply Voltage (Pins 22-39-64)	V_{SS}	0	V

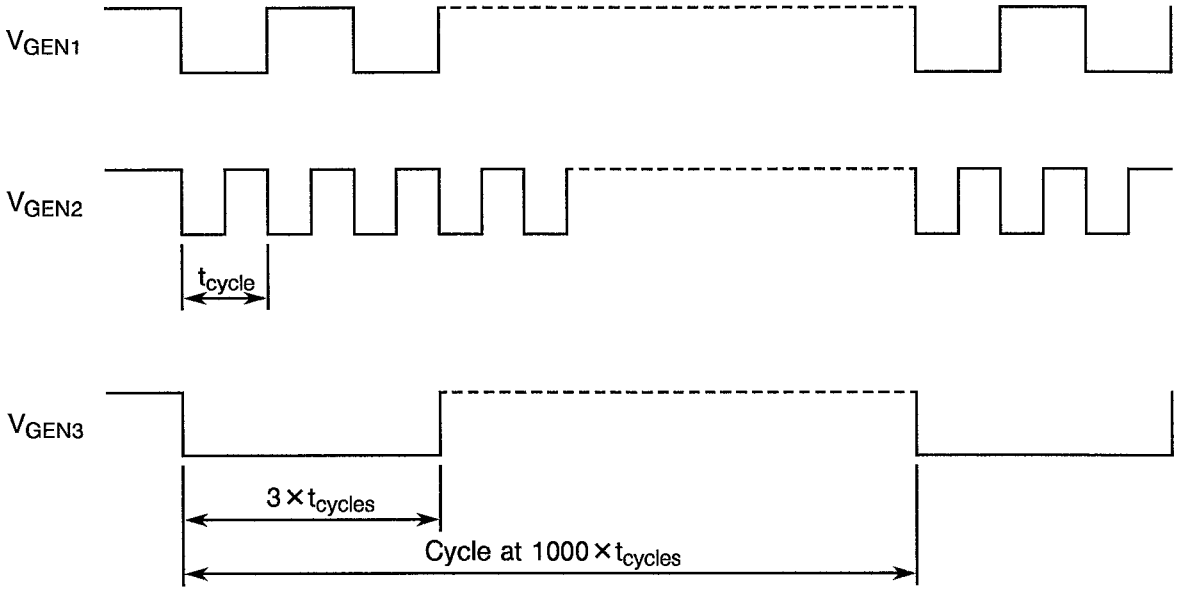
NOTES

1. Input Protection Resistor = Output Load = 10kΩ.

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING (CONT'D)

NOTES

1.



$t_{cycle} = 4.0\mu s.$

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING (CONT'D)

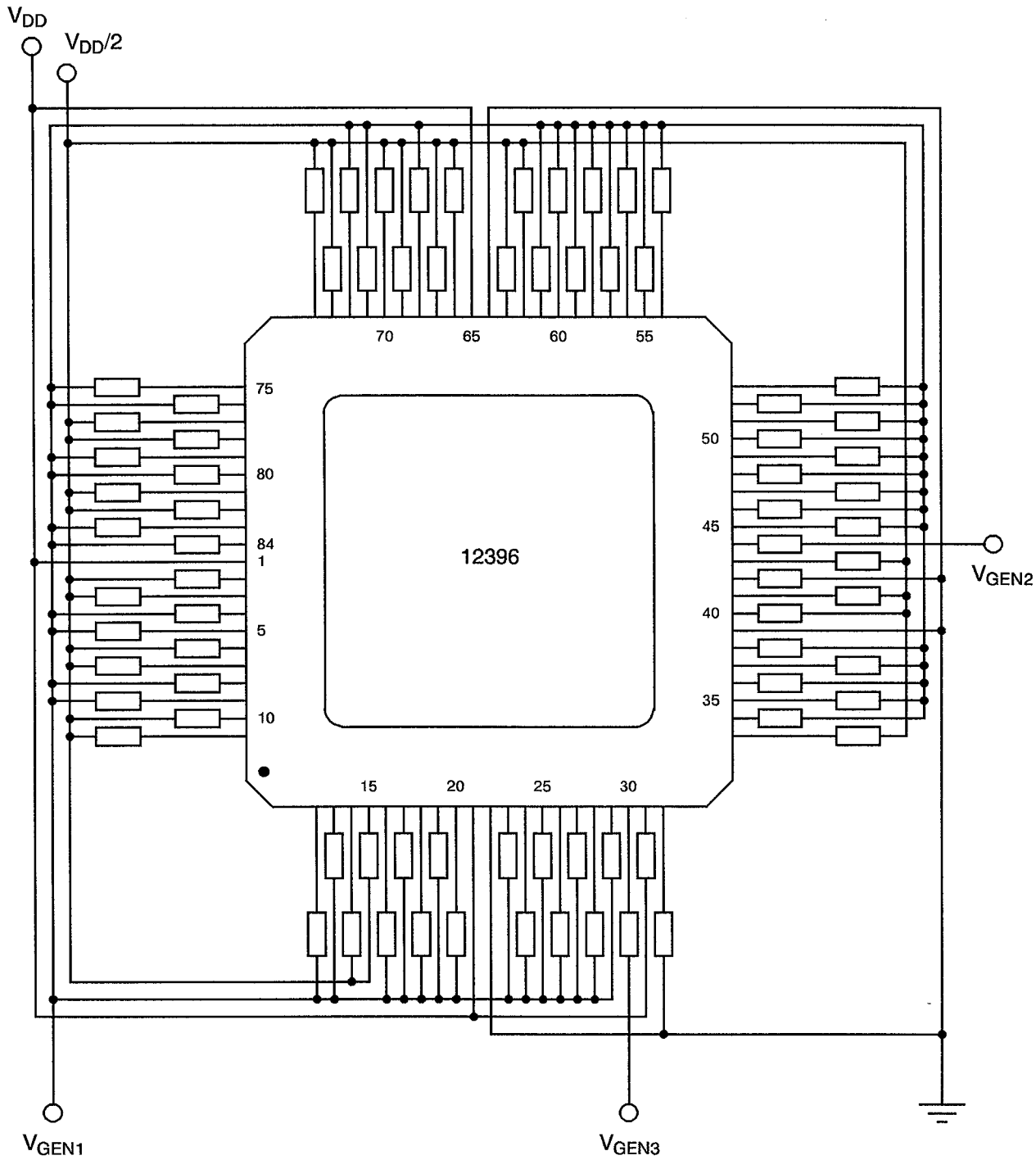


TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
5	Functional Test 1 (Basic)	-	As per Table 2	As per Table 2	-	-	-
6	Functional Test 2 (Nominal Voltage)	-	As per Table 2	As per Table 2	-	-	-
7	Functional Test 3 (High Voltage)	-	As per Table 2	As per Table 2	-	-	-
8	Functional Test 4 (Low Voltage)	-	As per Table 2	As per Table 2	-	-	-
9	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	-	3.5	mA
10 to 60	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	-	−1.0	µA
61 to 111	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	-	1.0	µA
112 to 138	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	-	0.4	V
139 to 165	Output Voltage High Level 1	V_{OH1}	As per Table 2	As per Table 2	3.9	-	V
166 to 192	Output Voltage High Level 2	V_{OH2}	As per Table 2	As per Table 2	4.2	-	V
193 to 200	Threshold Voltage Low Level 1 (TTL Inputs)	V_{THN1}	As per Table 2	As per Table 2	0.8	-	V
201 to 208	Threshold Voltage High Level 1 (TTL Inputs)	V_{THP1}	As per Table 2	As per Table 2	-	2.0	V
209	Threshold Voltage Low Level 2 (CMOS Inputs)	V_{THN2}	As per Table 2	As per Table 2	1.3	-	V
210	Threshold Voltage High Level 2 (CMOS Inputs)	V_{THP2}	As per Table 2	As per Table 2	-	3.2	V
211 to 215	Threshold Voltage Low Level 3 (SCHMITT Trigger Inputs)	V_{THN3}	As per Table 2	As per Table 2	1.0	2.8	V

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
216 to 220	Threshold Voltage High Level 3 (SCHMITT Trigger Inputs)	V_{THP3}	As per Table 2	As per Table 2	1.5	3.3	V
221 to 225	Hysteresis Voltage	V_H	As per Table 2	As per Table 2	0.5	-	V
226 to 233	Threshold Voltage Low Level 4 (TTL Inputs)	V_{THN4}	As per Table 2	As per Table 2	0.8	-	V
234 to 241	Threshold Voltage High Level 4 (TTL Inputs)	V_{THP4}	As per Table 2	As per Table 2	-	2.0	V
242	Threshold Voltage Low Level 5 (CMOS Inputs)	V_{THN5}	As per Table 2	As per Table 2	1.7	-	V
243	Threshold Voltage High Level 5 (CMOS Inputs)	V_{THP5}	As per Table 2	As per Table 2	-	3.9	V
244 to 248	Threshold Voltage Low Level 6 (SCHMITT Trigger Inputs)	V_{THN6}	As per Table 2	As per Table 2	1.2	3.8	V
249 to 253	Threshold Voltage High Level 6 (SCHMITT Trigger Inputs)	V_{THP6}	As per Table 2	As per Table 2	1.7	4.3	V
254 to 331	Input/Output Clamp Voltage (to V_{SS})	V_{IC1}	As per Table 2	As per Table 2	-	−2.0	V
332 to 409	Input/Output Clamp Voltage (to V_{DD})	V_{IC2}	As per Table 2	As per Table 2	-	2.0	V
410 to 412	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	-	−20	µA
413 to 415	Output Leakage Current Third State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	-	20	µA
416	Supply Current 1 (During BIST)	I_{DDS1}	As per Table 2	As per Table 2	-	60	mA

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
417	Supply Current 2 (During Normal Operation)	I_{DDS2}	As per Table 2	As per Table 2	-	15	mA
486 to 488	RESET Activated	t_{RES}	As per Table 2	As per Table 2	$3t_{BCK}$	-	-
489 to 491	PVCF Setup to Falling Edge of BITCLK	$t_{1(PVCF)}$	As per Table 2	As per Table 2	3.0	-	ns
492 to 494	PVCF Hold after Falling Edge of BITCLK	$t_{2(PVCF)}$	As per Table 2	As per Table 2	97	-	ns
495 to 497	RTS Setup to Falling Edge of BITCLK	$t_{1(RTS)}$	As per Table 2	As per Table 2	3.0	-	ns
498 to 500	RTS Hold after Falling Edge of BITCLK	$t_{2(RTS)}$	As per Table 2	As per Table 2	97	-	ns
501 to 503	RTS Setup to Rising Edge of SYNCMARK (Ext. Selection)	t_3	As per Table 2	As per Table 2	$2t_{BCK}$	-	-
504 to 506	RTS Hold after Rising Edge of SYNCMARK (Ext. Selection)	t_4	As per Table 2	As per Table 2	$2t_{BCK}$	-	-
507 to 509	POLL Valid from Falling Edge of BITCLK	$t_{5(POLL)}$	As per Table 2	As per Table 2	-	53	ns
510 to 512	CTS Valid from Falling Edge of BITCLK	$t_{5(CTS)}$	As per Table 2	As per Table 2	-	53	ns
513 to 515	SOUT Valid from Falling Edge of BITCLK	$t_{5(SOUT)}$	As per Table 2	As per Table 2	-	53	ns
516 to 518	FRAME Valid from Falling Edge of BITCLK	$t_{5(FRAME)}$	As per Table 2	As per Table 2	-	54	ns
519 to 521	ODDFRAME Valid from Falling Edge of BITCLK	$t_{5(ODD-FRAME)}$	As per Table 2	As per Table 2	-	54	ns

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
522 to 524	ALTSOUT Valid from Falling Edge of BITCLK	$t_{6(ALT-SOUT)}$	As per Table 2	As per Table 2	-	56	ns
525 to 527	SYNCMARK Valid from Falling Edge of BITCLK	$t_{6(SYNC-MARK)}$	As per Table 2	As per Table 2	-	57	ns
528 to 530	D0TTC, D1TTC Setup to CLKTTC Low	t_7	As per Table 2	As per Table 2	60	-	ns
531 to 533	D0TTC, D1TTC Hold after CLKTTC Low	t_8	As per Table 2	As per Table 2	0	-	ns
534 to 536	SELCLCW Setup to SAMPLE Low	$t_{9(SEL-CLCW)}$	As per Table 2	As per Table 2	$2t_{BCK}$	-	-
537 to 539	TCID Setup to SAMPLE Low	$t_{9(TCID)}$	As per Table 2	As per Table 2	$2t_{BCK}$	-	-
540 to 542	SELCLCW Hold after SAMPLE Low	$t_{10(SEL-CLCW)}$	As per Table 2	As per Table 2	$2t_{BCK}$	-	-
543 to 545	TCID Hold after SAMPLE Low	$t_{10(TCID)}$	As per Table 2	As per Table 2	$2t_{BCK}$	-	-
546 to 548	R/$\overline{W}$ Low to $\overline{CS}$ Low	t_{11}	As per Table 2	As per Table 2	100	-	ns
549 to 551	$\overline{CS}$ High to R/$\overline{W}$ High	t_{12}	As per Table 2	As per Table 2	100	-	ns
552 to 554	$\overline{CS}$ Width	t_{13}	As per Table 2	As per Table 2	100	-	ns
555 to 557	$\overline{CS}$ Width De-activated after Write	t_{14}	As per Table 2	As per Table 2	$4t_{BCK}$	-	-
558 to 560	A to $\overline{CS}$ Rising Edge during Write	$t_{15(A)}$	As per Table 2	As per Table 2	200	-	ns

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
561 to 563	D to $\overline{CS}$ Rising Edge during Write	$t_{15(D)}$	As per Table 2	As per Table 2	200	-	ns
564 to 566	A Hold after $\overline{CS}$ Rising Edge during Write	$t_{16(A)}$	As per Table 2	As per Table 2	100	-	ns
567 to 569	D Hold after $\overline{CS}$ Rising Edge during Write	$t_{16(D)}$	As per Table 2	As per Table 2	100	-	ns
570 to 572	D Valid from Falling Edge of $\overline{CS}$ during Read	t_{17}	As per Table 2	As per Table 2	81	-	ns
573 to 575	D Valid from A Stable during Read	t_{18}	As per Table 2	As per Table 2	81	-	ns
576 to 578	$\overline{CS}$ Rising Edge to D 3-State after Read	t_{19}	As per Table 2	As per Table 2	81	-	ns

APPENDIX 'A'

AGREED DEVIATIONS FOR MITEL (S)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.2	Paragraph 4.4 - Marking (plus Serialisation for Level B): May be performed to follow Paragraph 9.3 (Encapsulation). Paragraph 9.1 - Visual Inspection MIL-STD-883C, Method 2010.10, Paragraph 3.1.3: Scribing and die defects, "high magnification": Clauses c and d shall not be applicable for the device. Instead, the following criteria shall be used: - No device shall be acceptable if it exhibits cracks that:- (a) Come closer than 0.25mil to any operating metallisation or other functional circuit element. (b) Exceed 3.0mil in length pointing toward any operating metallisation or other functional circuit element. - For areas which are metallised, MIL-STD-883C, Method 2010.10, Paragraph 3.1.3 d is applicable without exception.
Para. 4.2.3	Paragraph 9.12 - Radiographic Inspection (a) ESA/SCC Basic Specification No. 20990, Paragraph 4.1: Inspection for foreign particles, voids and seal defects only may be performed. (b) Para. 9.9.2, Electrical Measurements at High and Low Temperatures: May be performed after Paras. 9.8.1 and 9.8.2, Seal Test.
Para's 4.2.4 and 4.2.5	Paragraph 9.18 - Solderability (a) A manually controlled dipping device may be used.

The following test patterns may be used:-

1. TEST PATTERN M1

Test Vectors

@ 0
- TEST1 = "0" (Enable BIST)
- TEST2 = "0" (Disables outputs during BIST)

@ 50
- TEST2 = "1" (Enable outputs during BIST test)

@ 4500 cycles the input conditions are:
- VCA7 selected
- LEN0 = "0", LEN1 = "0" (Frame length of 223 octets)
- RSSPACE = "0" (No space for RSSPACE)
- FECW = "1" (FECW to be output)
- OPCF = "1" (OPCF to be output)
- RTS = "00000010" (VCA6 ready to output PVCF data)
- The update of the CLCW data is to be delayed until OPCF output
- CLCWCLK enabled

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@ 4999
- TEST2 = "0" (De-activate test pin for normal operation)

@ 5500
- CLCWCLK disabled

@ 6000
- CLCWCLK enabled

@ 6100
- SELCLCW and TCID3, TCID4 changed while SAMPLE activated high

@ 6816
- VCA6 selected
- LEN0 = "0", LEN1 = "1" (Frame length of 446 octets)
- RSSPACE = "1" ('0's to be output for RSSPACE)
- OPCF = "1" (OPCF to be output)
- FECW = "0" (No FECW to be output)
- RTS = "00111100" (VCAs 2 to 5 ready to output PVCF data)
- The CLCW delayed to the next frame, previous value output

@ 7000
- SELCLCW, TCID3, TCID4 changed while SAMPLE activated high

@ 7200
- CLCWCLK disabled

@ 10700
- CLCWCLK enabled

@ 10928
- VCA2 selected
- LEN0 = "1", LEN1 = "0" (Frame length of 892 octets)
- RSSPACE = "0" (No space for RSSPACE)
- OPCF = "0" (No OPCF to be output)
- FECW = "1" (FECW to be output)
- RTS = "00001000" (VCA4 ready to output PVCF data)

@ 10929
- EXTSEL = "1" (EXTSEL = SYNCMARK)

@ 10961
- EXTSEL = "0" (EXTSEL = SYNCMARK)

@ 18096
- VCA4 selected
- LEN0 = "1", LEN1 = "1" (Frame length of 1115 octets)
- RSSPACE = "1" ('0's to be output for RSSPACE)
- OPCF = "1" (OPCF to be output)
- FECW = "1" (FECW to be output)
- RTS = "00000000" (No VCAs ready to output PVCF data)

@ 27010
- SELCLCW, TCID3, TCID4 changes after SAMPLE activated but while OPCF output

A number of repeated resets are generated to check the CTS signals. External selection of VCA4, VCA3, VCA0, VCA1 and VCA5 requested. The CLCW data is delayed to change while OPCF output

@ 28300
- EXTSEL = "1"
- TEST1 = "1"
- RTS = "10011111"

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@ 28328
- LEN0 = "0", LEN1 = "1"
- RSSPACE = "1"
- OPCF = "0"
- FECW = "0"

@ 28495
- RESET $\overline{N}$ = "0"
- RTS = "01110101"

@ 28500
- RESET $\overline{N}$ = "1"

@ 28595
- RESET $\overline{N}$ = "0"

@ 28600
- RESET $\overline{N}$ = "1"
- RTS = "00000010"

@ 28695
- RESET $\overline{N}$ = "0"
- RTS = "00111001"

@ 28700
- RESET $\overline{N}$ = "1"

@ 28795
- RESET $\overline{N}$ = "0"
- RTS = "10101010"

@ 28800
- RESET $\overline{N}$ = "1"

TEST2 is driven high again at the end of the production test to multiplex data from some input buffers via the TBUSIN(23:0) and TBUSOUT(23:0) buses through to output buffers. Again a number of resets are applied to check the start-up of the VCM for different test input conditions during normal and BIST modes.

@ 29800
- TEST2 = "1"

@ 29853
- RESET $\overline{N}$ = "0"

@ 29854
- RESET $\overline{N}$ = "1"

@ 29856
- TEST2 = "0"

@ 29866
- TEST1 = "0"

@ 29867
- RESET $\overline{N}$ = "0"

@ 29870
- RESET $\overline{N}$ = "1"