INTERNAL VISUAL INSPECTION

OF MICROWAVE DEVICES

ESCC Basic Specification No. 2045010

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ESA/SCC Basic Specification No. 2045010

space components
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1. SCOPE

This specification, to be read in conjunction with ESA/SCC Basic Specification No. 20400, 'Internal Visual Inspection', contains additional requirements for microwave devices which shall be applied to each device. A microwave device is defined as being a microwave functional device fabricated on semiconductor material such as a Monolithic Microwave Integrated Circuit (MMIC) or a microwave discrete component and/or structure. A microwave device can be an integral part of a Microwave Hybrid Integrated Circuit (MHIC).

N.B.

1. This specification is not intended to cover all elements of MHICs but specific elements which are common to MHICs and MMICs are addressed.
2. This specification is not intended to cover all aspects of Manufacturer's specific features and technologies. **The in-house Manufacturer's specification is applicable if no adequate criteria can be found in this document for specific features and technologies and applies inspection criteria with a similar level of severity to the ones used in this specification.**
3. This specification contains rejection and acceptance criteria for visual defects of microwave devices. Every subsection starts with a listing of rejection criteria not particularly designated. If acceptance criteria exist for a specific subsection these criteria are listed after the rejection criteria at the end of that subsection under the header "**Acceptance Criteria**" and each single criterion contains the word "**acceptable**" given in bold.

2. GENERAL REQUIREMENTS

2.1 APPLICABILITY

The following criteria cannot be varied or modified after commencing any inspection stage. Any ambiguity or proposed minor deviation shall be referred to the Qualifying Space Agency for resolution and approval.

Any deviation from this specification applicable generally to a specific component and Manufacturer shall be defined in the Manufacturer in-house specification, if approved by the Qualifying Space Agency. That in-house specification shall be referred to in the ESA/SCC Detail Specification in the "Agreed Deviation for Manufacturers" annexe.

2.2 PROCEDURE

All components shall be submitted to examination in an area where the standard of cleanliness and ESD precautions is not less than that of the processing or assembly area, as appropriate.

All items shall be examined in such a manner that a minimum of handling and movement of the component is involved.

After blowing with nitrogen for removal of particles the devices must be re-inspected.

After the Internal Visual Inspection (IVI) during pre-cap inspection, no further assembly step (i.e. cleaning, drying, etc.) is allowed, except sealing.

2.3 MAGNIFICATION

"High magnification" inspection shall be performed perpendicular to the die surface with the device under illumination normal to the die surface.

"Low magnification" inspection shall be performed with either a monocular, binocular, or stereomicroscope with the device under sufficient illumination and within a suitable angle.

2.4 MOUNTING FIXTURES

Suitable fixtures shall be used to assist in the inspection process provided that they do not, in themselves, cause damage to the device.

3. DETAILED REQUIREMENTS

3.1 GENERAL

The device shall be examined in a suitable sequence of observations within the specified magnification range to determine compliance with the requirements of the applicable Detail Specification. The inspections and criteria in this method shall be required inspections for all devices and locations to which they are applicable. Where the criteria are intended for a specific component, structure, process or technology it has been indicated. A component shall be rejected if it exhibits one or more of the defects listed within this specification.

The lot inspected shall be homogeneous. A component shall therefore also be rejected if it exhibits a significant deviation, within the limits of this specification, from the rest of the lot. However, such components shall not be counted as a failure in any other lot definition.

If, within a lot, a large number of devices is rejected mainly because of a single criterion listed within this specification (repetitive cause of rejection), corrective actions have to be taken mutually agreed between Manufacturer and Customer.

3.2 SEQUENCE OF INSPECTION

The order in which the criteria are presented is not a required order of examination and can be varied at the discretion of the Manufacturer, or Inspector.

The backside inspection criteria that cannot be verified after mounting shall be conducted prior to attachment of the die.

3.3 DEFINITIONS

Active Circuit Area

All areas of functional circuit elements, operating metallisation or any connected combinations, excluding beam leads, ground planes, bare isolating substrates and test structures.

Active Metallisation

Any metallisation that is important for the performance of the microwave devices.

Air Bridge

A raised layer of metallisation used for interconnection that is isolated from the surface of the semiconductor and/or passivation material.

Backside Pattern

The backside metallisation often has to be structured to create sawing grids which avoid metal peeling or lifting effects during sawing. In the case of a structured backside metallisation the die attach material does not cover the whole chip area and the die attach fillet will usually not be visible during vertical visual inspection.

Block Resistor

A thin film resistor which for purposes of trimming is designed to be much wider than would be dictated by power density requirements and which shall be identified in the approved Manufacturer's pre-encapsulation visual implementation document.

Chip-out

A chip-out is any section of the die whcih has broken away from the main body of the die.

Conductive Foreign Material

Any substance that cannot be clearly identified to be non-conductive.

Contact Window

An opening in the passivation, usually covered by metallisation, where electrical contact is made with an underlaying layer.

Crack

A crack is a fracture of a die that can extend through or partly through the thickness of the die or remain parallel to the surface of the die.

Crazing

The presence of numerous minute cracks in the referenced material.

Crystallographic Defect

A discontinuity of the substrate including pits, screws, mismatches and slip dislocations.

Detritus

Fragments of original or laser modified resistor material remaining in the kerf.

Dielectric Isolation

Electrical isolation of one or more elements of a monolithic semiconductor integrated circuit by surrounding the elements with an isolation barrier.

Diffusion Well

A volume (or region) formed in a semiconductor material by a diffusion process (n or p- type) and isolated from the surrounding semiconductor material by an n-p, p-n or $n-n^+$ junction, or by a dielectric material (dielectric isolation, coplanar process ..).

Down-bonding

A wire bonding operation carried out from a higher to a lower level.

FET

A field Effect Transistor consisting of the gate stripe and source and drain areas. Special FET types are MOSFET (Metal-Oxide-Semiconductor FET), MESFET (Metal-Semiconductor FET) and HFET (Heterostructure FET).

Foreign Matter

Any material that is foreign to the microcircuit or package, or any non-foreign material that is displaced from its original or intended position within the microcircuit package. Foreign material shall be considered to be attached when a gas blow of nitrogen at $140kN/m^2$ applied for a minimum of three seconds from a distance of 50mm cannot remove it. The diameter of the nozzle for the gas blow shall not be less than 1.0mm in diameter.

Functional Circuit Elements

Diodes, transistors, cross-unders, capacitors, inductors and resistors.

Gate Bus

Metallisation layer of an equal type to the gate that connects the different gate fingers to the connecting line area.

Gate Channel

The area between the drain and the source of microwave transistor structures.

Gate Finger

Single gate stripe of an FET that can consist of multiple gate stripes.

Gate Length

Smallest dimension of the gate metallisation (in the direction from source to drain).

Gate Oxide

The thin layer of oxide, or other dielectric, that separates gate metallisation (or other material used for the gate electrode) from the n- or p-type semiconductor material.

Gate Structure

The interleaved areas of source, drain and gate stripe of a field effect transistor.

Glassivation

A top layer of insulating material that covers the active circuit area including metallisation, except bonding pad areas and beam leads.

Glassivation/Passivation Cracks

Fissures in the glasivation/passivation layer resulting from stress release or poor adhesion. The cracks can form loops over metallised areas.

High Mesa Structure

Microwave devices using vertical device structures (i.e. PIN diodes, Gunn diodes, IMPATTs and HBTs) that exhibit a mesa etching in order to decrease the junction area. The height of a typical high mesa structure device is in the range of 3.0μm.

High Power Device

A microwave device with a junction area larger than $0.04mm^2$ or a temperature difference of more than 20°C between backside and junction of the die during operation. For MMICs, each junction area should be considered separately.

Implanted Resistor

Resistive part of a circuit that has been implanted into the substrate.

Inverted Mounting

A technique whereby thickened and/or extended bonding pads enable upside down mounting on a suitable substrate, such as thin or thick-film circuit.

Junction

An active junction is any p/n junction intended to conduct current during normal operation of the circuit element (i.e. collector to base).

Junction Area

The core region of transistors and diodes (i.e. FET: the gate channel; bipolar transistor: region between and/or underneath emitter finger and base/collector contact; diode: region between p and n contact).

Kerf

That portion of the component area from which material has been removed or modified by trimming or cutting.

Line of Separation

The visible distance or space between two features that are observed not to touch at the magnification in use.

Low Power Device

A microwave device with a junction area smaller than 0.04mm^2 or a temperature difference of lower than 20°C between backside and junction of the die during operation. For MMICs, each junction area should be considered separately.

Metallisation Non-adherence

Unintentional separation of material from an underlying substance, excluding air bridges and undercutting by design.

Microwave Hybrid Integrated Circuit (MHIC)

A microcircuit consisting of elements which are a combination of film microcircuit type and the semiconductor types, or a combination of one or both of the types with discrete parts.

Multilayered Metallisation (Conductors)

Two or more layers of metal or any other material used for interconnections that are isolated from each other by insulating material. The term "underlying material" shall refer to any layer below the top layer of metal.

Multilevel Metallisation (Conductors)

Two or more layers of metal or any other material used for interconnections that are isolated from each other by insulating material (also referred to as interlevel dielectric).

Narrowest Resistor Width

The narrowest portion of a given resistor prior to trimming.

Nodule

An unevenness on a, by design, plane surface area.

Operating Metallisation (Conductors)

All metal or any other material used for interconnection except metallised scribe lines, test patterns, unconnected functional circuit elements, unused bonding pads and identification markings.

Original Width

The width dimension or distance that is intended by design (e.g. original metal width, original diffusion width, original beam width, etc.).

Package Post

A generic term used to describe the bonding location on the package.

Particles

Any foreign matter (organic, dust, metallisation, part of the substrate, etc.) which is not attached to the substrate and can be removed by a gas blow of nitrogen at 140kN/m^2 at the die surface.

Passivation

A layer of insulating material that covers the active circuit area including metallisation, except bond pads.

Passivation Step

An abrupt change of level of the passivation, such as a contact window or operating metallisation cross-over.

Peripheral Metal

All metal that lies immediately adjacent to, or over, the scribe grid.

Rebond

A second bond made between two pads, or a pad and a bonding terminal, to replace the original bonded wire, which has either been removed, leaving the welded portion of the bond attached to the pad or bonding terminal, or which failed to adhere at the first bonding attempt. The meaning of rebonding excludes repair.

Recess

An etched groove into the substrate under the gate metallisation. Depending on the technology used, the recess can be larger than the gate length and then becomes visible on both sides of the gate, or the recess is hidden below the gate metallisation.

Scratch

Any tearing defect, discontinuity or tooling mark in or on the metallisation or glassivation/passivation, whether or not the bare semiconductor material and/or the oxide is exposed.

Shooting Metal

Defined as metal (e.g. aluminimum, gold) expulsion of various shapes and lengths from under the wire bond at the bonding pad.

Substrate

The supporting structual material into and/or upon which the passivation, metallisation and circuit elements are placed.

Thick-Film

A thick-film is conductive, resistive or dielectric material screen printed onto a substrate and fired at temperature to fuse into its final form.

Thin-Film

A thin-film is conductive, resistive or dielectric material, usually less than 5.0μm in thickness, that is deposited onto a substrate by vacuum evaporation, sputtering, or other means.

Up-bonding

A wire bonding operation carried out from the die up to a higher level.

Via Hole

A hole formed through the wafer and metallised, causing electrical connection to be made from the front side of the wafer on which the circuitry is formed, to the back face of the wafer.

Via Metallisation

Feature which allows the interconnection between two or more metallisation levels. Not to be confused with via-hole metallisation.

Void

For metallisation, any region in the metallisation not caused by a scratch, where bare semiconductor material or pasivation is visible within the design areas of the metallisation.

In the case of die mounting, a void is the absence of die attach material in the defined areas.

In the case of glassivation/passivation, a void is the absence of glassivation/passivation over any active circuit area of the die.

4. TEST CRITERIA

The internal visual examination shall be conducted on each microwave device and each component therein. Devices shall be inspected to all of the applicable criteria.

TABLE I - MAGNIFICATION CHECKLIST

N.B.
The following magnifications are given as aguideline only. **For small features, or where additional verification is required, increased magnification shall be used, if considered necessary.**

DEFECT	MAGNIFICATION	PARAGRAPH
Die Defects	100X - 200X	4.1
Metallisation Defects	100X - 400X	4.2
Diffusion and Passivation	100X - 400X	4.3
Glassivation	100X - 200X	4.4
Resistors	100X - 200X	4.5
Die Mounting Defects	30X - 60X	4.6
Header Defects	As required	4.7
Bond Defects	30X - 60X	4.8
Foreign Matter	100X - 400X	4.9

4.1 DIE DEFECTS

For conventional and flip-chip mounting no device shall be acceptable that exhibits the following die defects (except where **"acceptable"** is explicitly designated):-

(a) Less than 5.0um of passivation visible between active metallisation or between isolation/diffusion channel or bond periphery and the edge of the die.

N.B.
This criterion can be excluded for beam leads and peripheral metallisation including bonding pads where the metallisation is at the same potential as the die.

(b) Die having attached portions of the glassivation/pasivation or metallisation of another die.

(c) A chip-out or crack in the active circuit area. A chip-out into, or underneath, the functional metallisation or any cracks in the substrate, which propagate through, or underneath metallisation patterns of the device, i.e. bond pads, capacitors, peripheral metallisation, but excluding test structures of the device.

N.B.
An annular ring of 50µm from the edge of the mesa of a diode has to be kept defect free.

(d) Chip-out or offset scribe lines/breaks into the non-active circuit area. The minimum acceptable distance between any metallised area involved in the electrical operation of the device and the edge of the fault shall be 2.5µm.

(e) Chip-outs meeting the annular channel stopper, isolation or guard ring.

(f) Any cracks in the substrate outside of, but pointing toward, the active circuit area of the device.

(g) A crack or crystallographic defect whose length exceeds 100µm or 1/3 of the dimension of the die (whichever is smaller) or comes closer than 2.5µm to any operating metallisation (except for substrate potential peripheral metal) or functional circuit element.

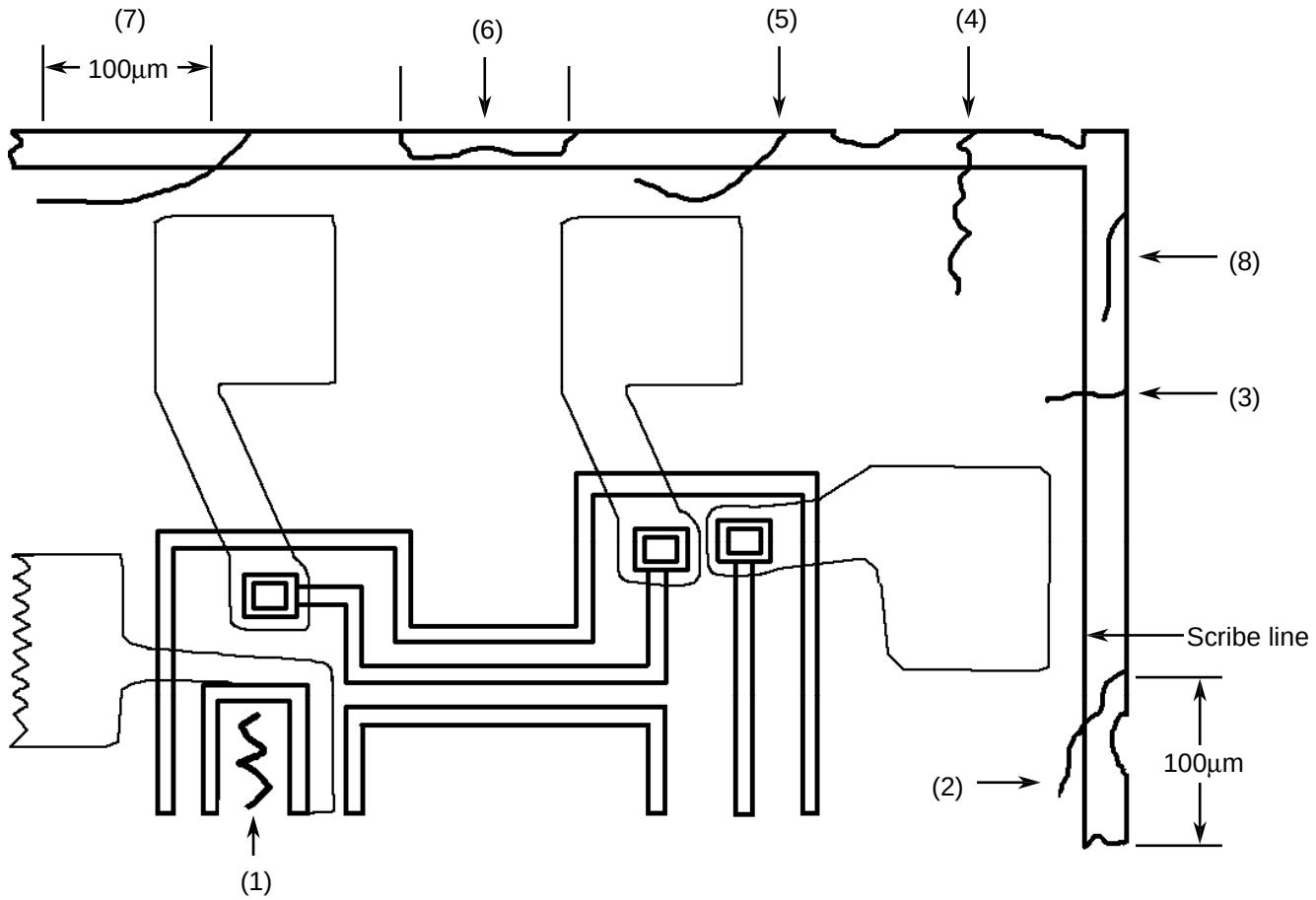
(h) Semicircular crack(s) terminating at the edge, whose chord is long enough to bridge the narrowest spacing between unglassivated operating material in the case of detachment (e.g. metallisation, bare semiconductor material, mounting material, bonding wire, etc.).

N.B.
Not applicable for isolating material (e.g. GaAs).

General Notes

1. In all cases, a variation of the die size could not be accepted if the limits fixed in the product specification are not respected.
2. The number of chip-outs is not limited.

FIGURE I - DIE DEFECTS



FAULT	DEFECT	PARA.
1. REJECT	Substrate crack in active area	4.1 (c)
2. ACCEPT	Crack<100µm in length	4.1 (g)
3. REJECT	Crack pointing toward metallisation pattern	4.1 (f)
4. REJECT	Crack pointing toward metallisation pattern	4.1 (f)
5. REJECT	Crack with <2.5µm separation to operational metallisation	4.1 (g)
6. REJECT	Semicircular crack within conductive substrate material which could bridge the narrowest spacing between unglassivated operating material in the case of detachment	4.1 (h)
7. REJECT	Crack >100µm in length	4.1 (g)
8. ACCEPT	Crack inside the scribe line	4.1 (k)

(i) Cracks in the substrate visible on the side of the die pointing in a vertical direction and tending to cross the entire thickness of the substrate.

N.B.
Not to be confused with traces of sawing which remain **acceptable**.

(j) Cracks located on the side of the die and parallel to the surface of the die (lateral, horizontal cracks) which are longer than 300µm or 1/3 of the dimension of the die (whichever is smaller).

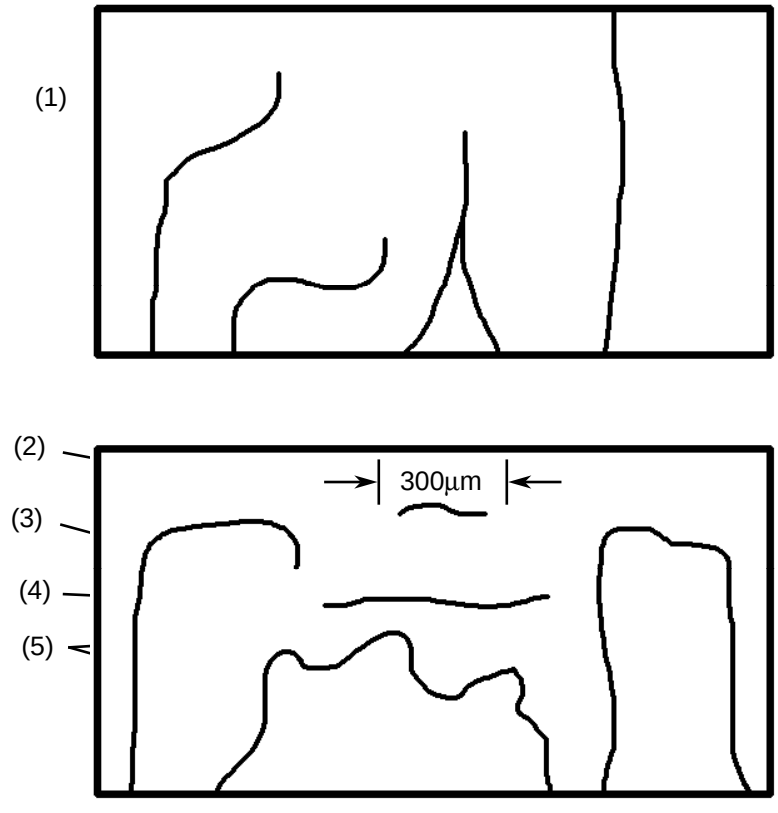
Acceptance Criteria

(k) Cracks inside the scribe line are **accepted**, except semicircular cracks because of the risk of detachment which can never be excluded.

(l) Vertical cracks located on the side of the die that do not tend to go through the entire thickness of the die are **accepted**, except for semicircular shaped cracks when there is a risk of detachment.

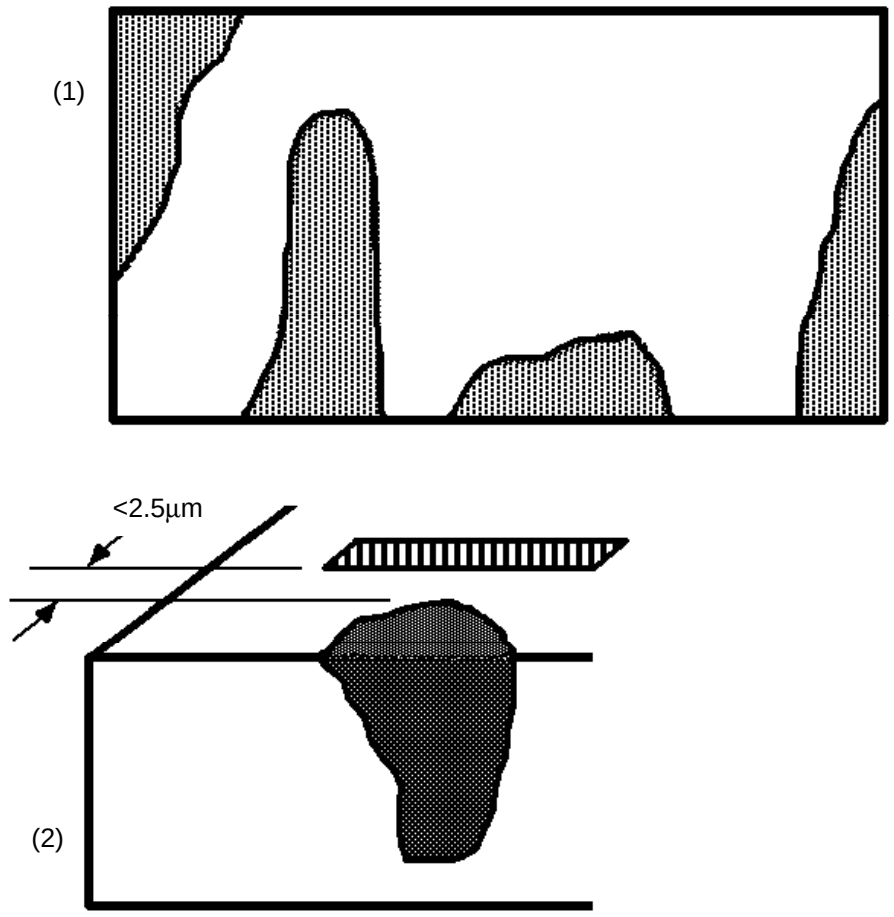
(m) Chip-outs on the side of the die are accepted regardless of their shape as long as they also verify all criteria applicable on the top of the die and the criteria listed for backside metallisation (Para. 4.2.13).

FIGURE II - CRACKS ON THE SIDE OF THE DIE



FAULT	DEFECT	PARA.
1. REJECT	Cracks pointing in vertical direction if they could expand and go all of the way through	4.1 (i)
2. ACCEPT	Crack parallel to the surface of the die<300µm	4.1 (j)
3. ACCEPT	Vertical crack that does not tend to go through the entire thickness of the die	4.1 (l)
4. REJECT	Crack parallel to the surface of the die >300µm	4.1 (j)
5. ACCEPT	Semicircular crack on the side of the die with no risk of detachment	4.1 (l)
REJECT	Semicircular crack on the side of the die with risk of detachment	

FIGURE III - CHIP-OUTS ON THE SIDE OF THE DIE



FAULT	DEFECT	PARA.
1. ACCEPT	Chip-outs on the side of the die	4.1 (m)
2. REJECT	Lateral chip-out which does not respect top-side criteria	4.1 (m) & (d)

4.2 METALLISATION CRITERIA

Rejection and Acceptance Criteria for metallisation defects are listed in the following sections. No device shall be acceptable that exhibits the following metallisation defects (except where **"acceptable"** is explicity designated).

4.2.1 General Metallisation Defects

(a) Evidence of metallisation corrosion.

(b) Metallisation having any discoloured localised area (electroplated metal lines excluded) shall be closely examined and shall be rejected unless it is demonstrated to be a harmless effect.

(c) Evidence of metallisation lifting, peeling or blistering.

4.2.2 Metallisation Scratches

(a) Scratch in the metallisation that does not expose any underlying layer, passivation or substrate and leaves less than 50% of the original metal width undisturbed.

N.B.
Specific paragraphs refer to bonding pads (see (b) + (d)), beam leads (see Para. 4.8.7 (a)) and gate structures (see Para. 4.2.8 (c)).

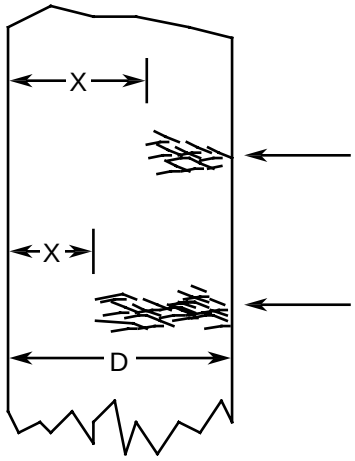
(b) Scratch in the bonding pad or fillet area that does not expose any underlying layer, passivation or substrate and reduces the metallisation path width connecting the bond to the interconnecting metallisation to less than 50% of the narrowest entering interconnect metallisation stripe width. If two or more stripes enter a bonding pad, each shall be considered separately.

(c) Scratch in single or multi-layered metallisation excluding bonding pads and beam leads that exposes underlying metal or passivation anywhere along its length and leaves less than 75% of the original metal width undisturbed.

(d) Scratch, probe marks, etc. in the bonding pad area that exposes underlying passivation or substrate and which does not allow at least 75% of the bond to be made on the undisturbed metallisation area.

(e) Scratch in the metallisation over a passivation over a passivation step that leaves less than 75% of the original metal width at the step undisturbed.

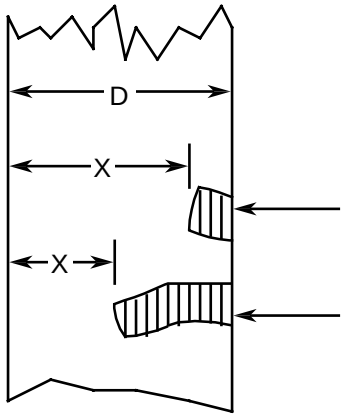
FIGURE IV - SCRATCH CRITERIA FOR METALLISATION LAYERS (Para. 4.2.2 (a))



ACCEPT: Scratch where the remaining undisturbed metal width X is greater than 50%.

REJECT: Scratch where the remaining undisturbed metal width X is less than 50%.

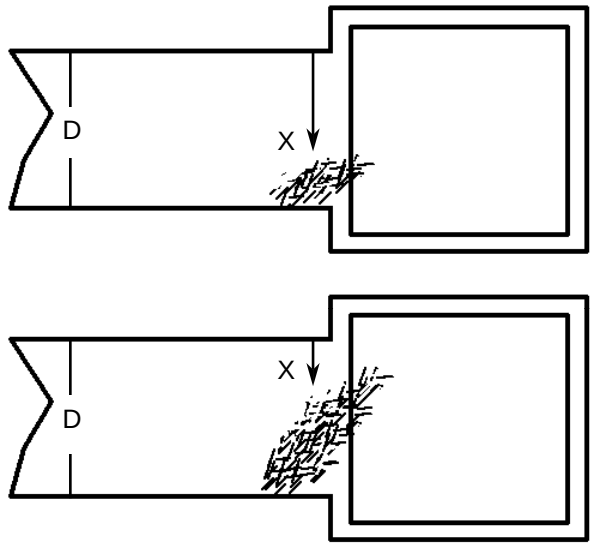
FIGURE V - SCRATCH EXPOSING UNDERLYING MATERIAL (Para. 4.2.2 (c))



ACCEPT: Scratch exposing underlying metal or passivation where the remaining undisturbed metal width X is greater than 75%

REJECT: Scratch exposing underlying metal or passivation where the remaining undisturbed metal width X is less than 75%

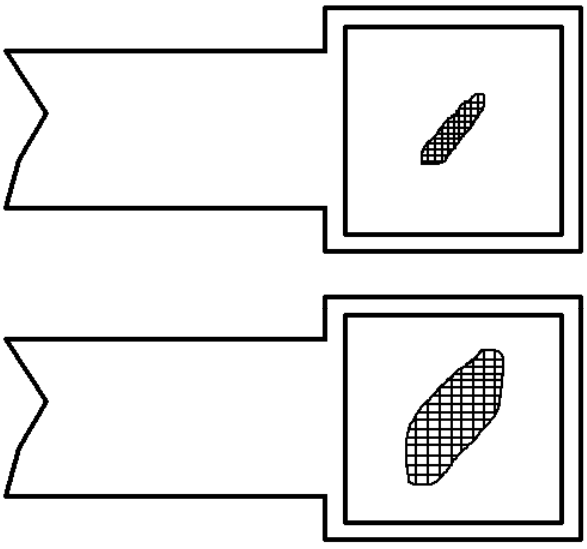
FIGURE VI - SCRATCH IN BOND PAD INTERCONNECTION AREA (Para. 4.2.2 (b))



ACCEPT: Scratch where the remaining undisturbed metal width X is greater than 50%.

REJECT: Scratch where the remaining undisturbed metal width X is less than 50%.

FIGURE VII - SCRATCH, PROBE MARKS IN THE BONDING PAD AREA (Para. 4.2.2 (d))



ACCEPT: Scratch exposing underlying passivation or substrate but which allows at least 75% of the bond to be made on the undisturbed metallisation area.

REJECT: Scratch exposing underlying passivation or substrate not allowing at least 75% of the bond to be made on the undisturbed metallisation area.

4.2.3 Metallisation Voids

N.B.
For high mesa structure devices more detailed criteria shall be applied (see Para. 4.2.11 (a)).

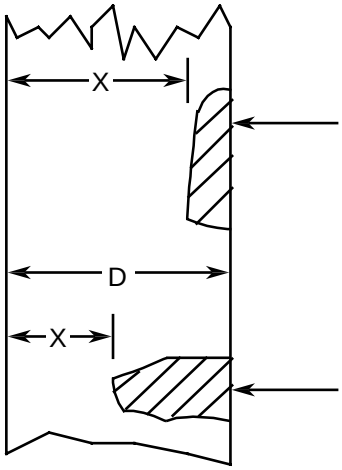
(a) Void(s) in the metallisation that leaves less than 75% of the original metal width undisturbed.

(b) Void(s) in the metallisation over a passivation step that leaves less than 75% of the original metal width, at the step, undisturbed.

(c) Void(s) in the bonding pad area not allowing at least 75% of the bond to be made on an undisturbed metallisation area.

(d) Void(s) in the bonding pad or fillet area that reduces the metallisation path width connecting the bond to the interconnecting metallisation to less than 75% of the narrowest entering metallisation stripe width. If two or more stripes enter a bonding pad, each shall be considered separately. When a fillet area exists, it is considered as a part of the entering/exiting metallisation stripe.

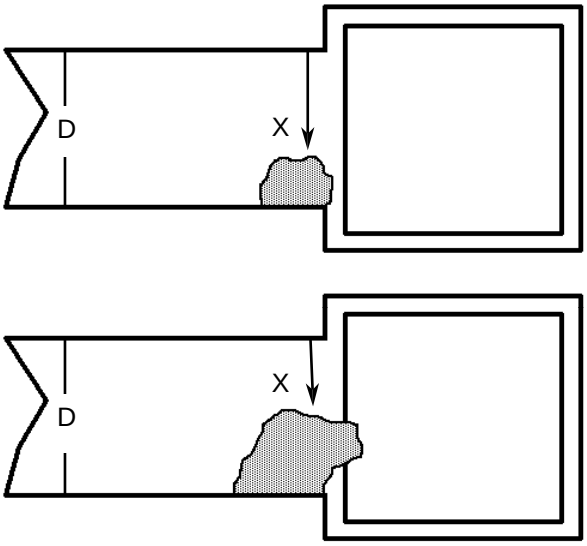
FIGURE VIII - METALLISATION VOIDS (Para. 4.2.3 (a))



ACCEPT: Void where the remaining undisturbed metal width X is greater than 75%.

REJECT: Void where the remaining undisturbed metal width X is less than 75%.

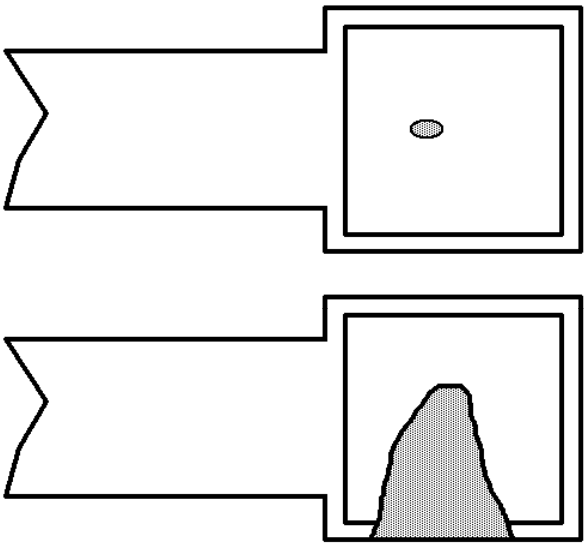
FIGURE IX - VOIDS ON BOND PAD INTERCONNECTING METALLISATION (Para. 4.2.3 (d))



ACCEPT: Void where the remaining undisturbed metal width X is greater than 75%.

REJECT: Void where the remaining undisturbed metal width X is less than 75%.

FIGURE X - VOIDS IN BONDING PAD AREA (Para. 4.2.3 (c))



ACCEPT: Void which allows at least 75% of the bond to be made on an undisturbed area.

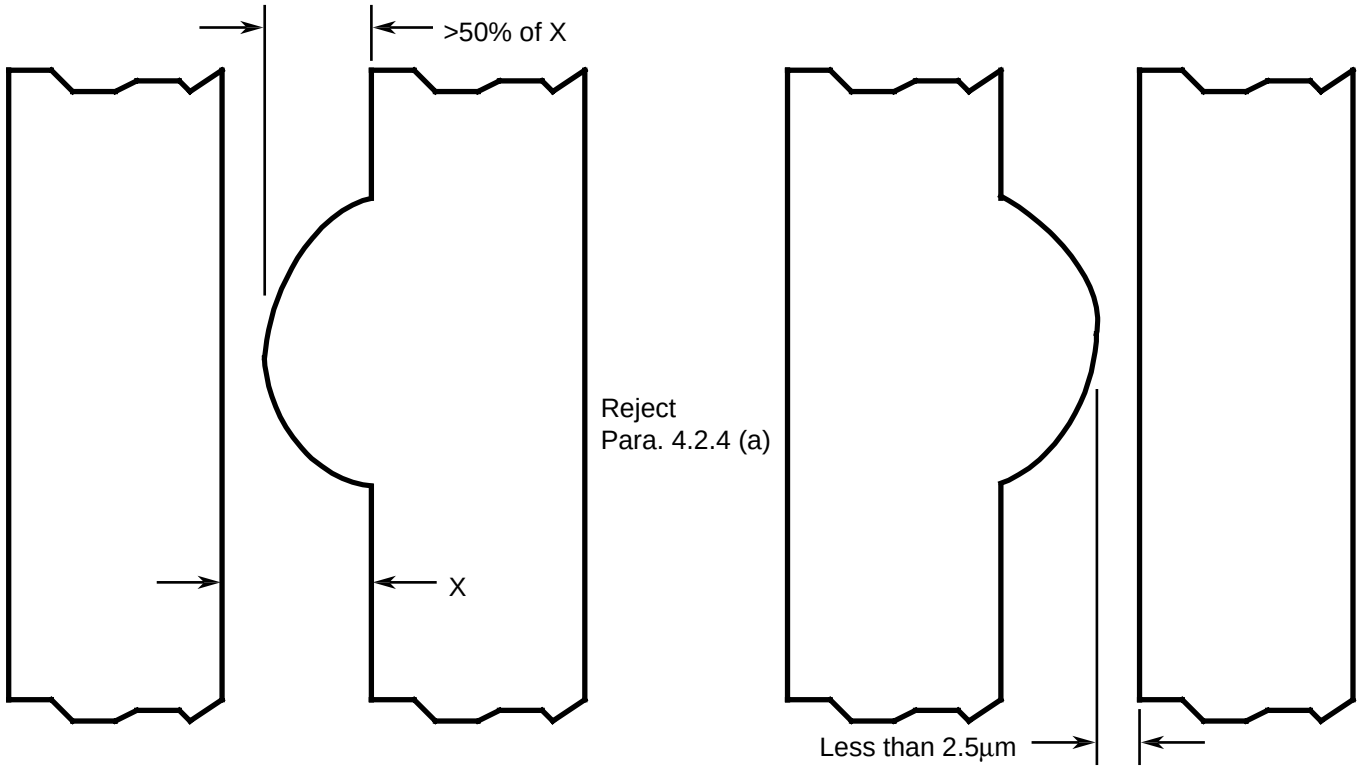
REJECT: Void which does not allow at least 75% of the bond to be made on an undisturbed area.

4.2.4 Metallisation Bridging

(a) The minimum acceptable separation between two metallisation areas shall be 50% of design width or 25µm whichever is the smaller. If 50% of design width is used, it shall not be less than 2.5µm minimum separation at any point, whether caused by smears, photo-lithographic defects or other defects. This excludes gate/source, gate/gate and gate/drain in active structures and spiral inductors.

(b) Any metal that is displaced, as a result of bonding, from its original position on the bonding pad (shooting metal) if it reduces the original separation between unglassivated operating metallisation, or scribe line and the bonding pad, to less than 2.5µm or 50% of the design separation, whichever is less.

FIGURE XI - METALLISATION BRIDGING



4.2.5 Metallisation Alignment

(a) Alignment fault such that the contact window opening through passivation is not completely covered by metallisation.

(b) Alignment fault at the gate channel where the passivation opening coincides with the plating metal edge.

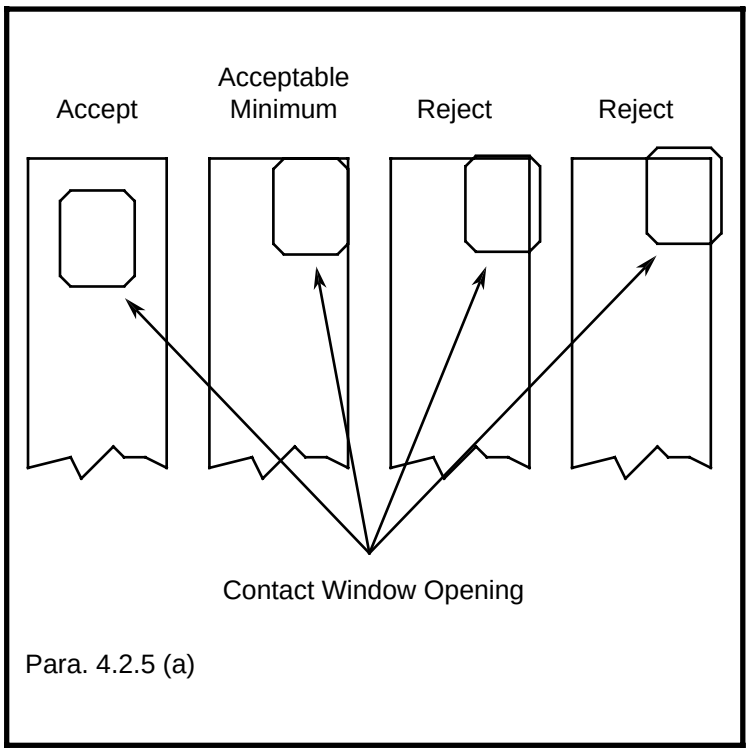
(c) Alignment fault of capacitors where the dielectric isolation layer is not visible on the whole perimeter of the top layer of the device, except connection line (air bridge).

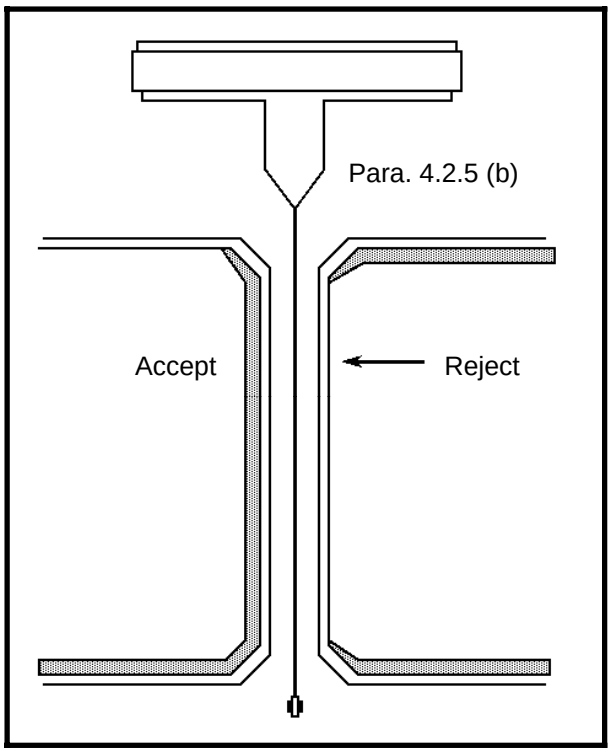
(d) Alignment fault at the gate channel where the ohmic contact layer is not visible in front of the plating layer.

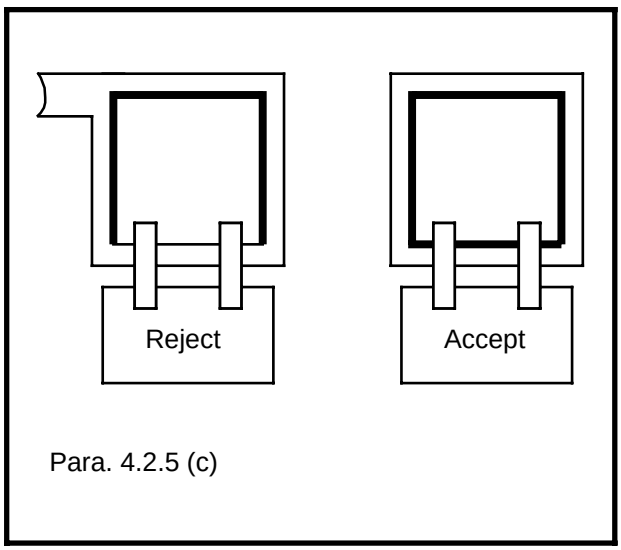
(e) Any electroplated metallisation outside the metallisation pad is rejected.

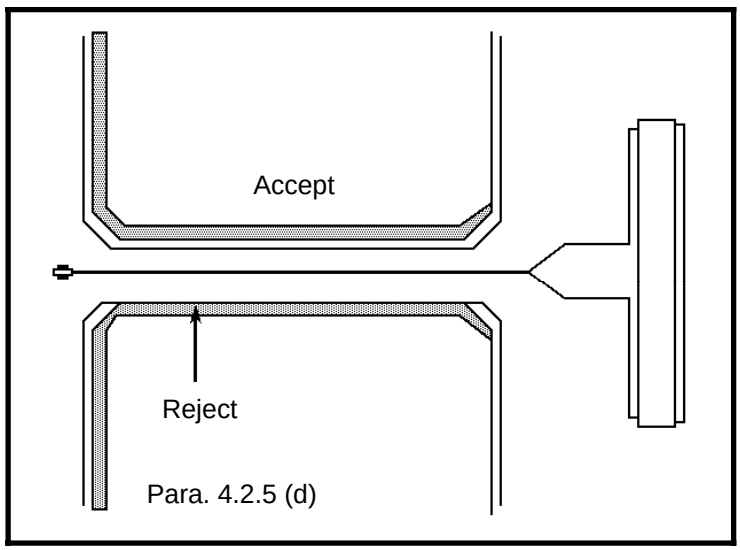
(f) A misalignment that is greater than the Manufacturer's specification for misalignment (if applicable).

FIGURE XII - METALLISATION ALIGNMENT









4.2.6 Via Hole Metallisation (Front Side)

(a) Overetched via hole or misaligned via around the pad.

(b) Poor adhesion (lifting, peeling, blistering).

(c) Any cracks in the substrate or passivation originating at the via hole.

N.B.
This criterion applies irrespective of the direction and the length of the cracks.

(d) Evidence of discolouration coming up through via hole pad, when die is mounted on a carrier. (Risk that the mounting material has migrated).

Acceptance Criteria

(e) Bulging or depressed metal of a via hole can be **accepted** if there is no evidence of holes, voids or cracks associated with these findings.

FIGURE XIII - DEPRESSED METAL OF A VIA HOLE

Colour Image is shown in Appendix A.

4.2.7 Air Bridge

N.B.
The provision of SEM data is recommended to support the inspection of sub-micron structures.

(a) A void in the air bridge metallisation that leaves less than 75% of the original metallisation width undisturbed.

(b) Nodules or bumps that reduce the separation between air bridge and underlying operational metallisation paths such that a clear separation is no longer discernible or between parallel air bridge paths such that a clear separation is less than 50% of its original value.

N.B.
Not applicable when the two operational metallisation paths are at similar potentials.

(c) No discernible separation between the air bridge and underlying operating metallisation.

N.B.
Not applicable when they are at similar potentials.

(d) Air bridge metallisation overhang over adjacent operating metallisation, not intended by design, that does not exhibit a visible separation.

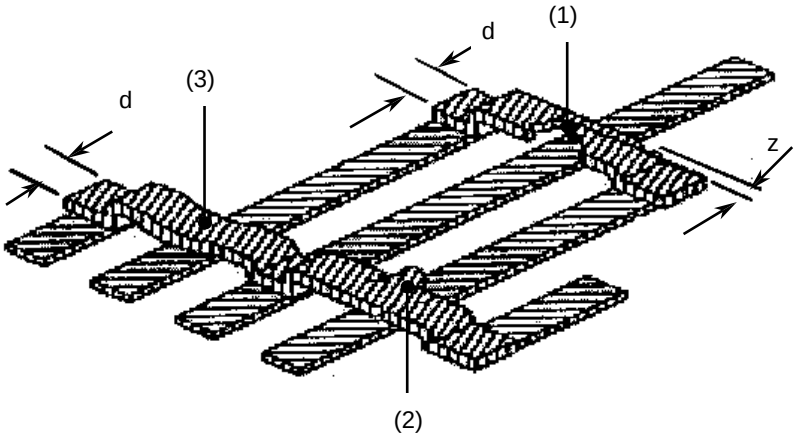
N.B.
Not applicable when they are at similar potentials.

(e) Mechanical damage (tear or scratch) to an air bridge resulting in a depression (lowering) of the air bridge arch over underlying operating metallisation that leaves a separation which is too small to be detected by the focusing/defocusing technique.

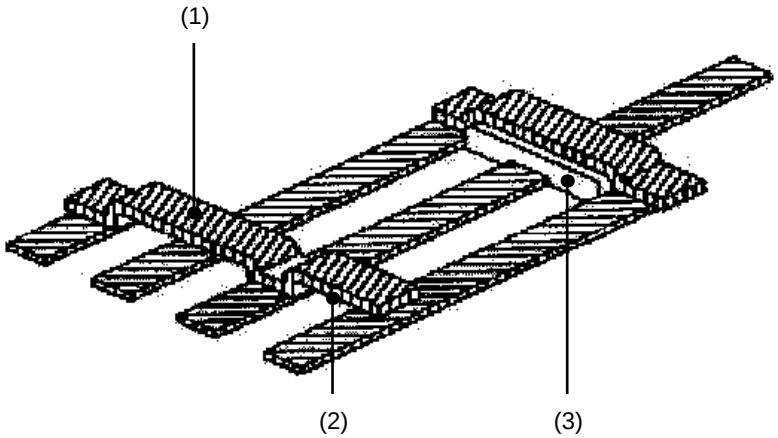
N.B.
This technique needs to be validated with a reference air bridge.

FIGURE XIV - AIR BRIDGE DEFECTS

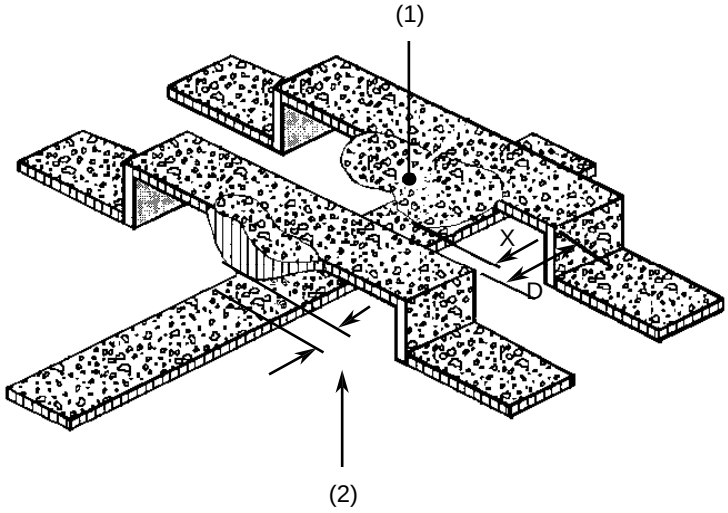
FAULT	DEFECT	PARA.
1. REJECT	Void leaving less than 75% of metal width undisturbed.	4.2.7 (a)
2. ACCEPT	Nodules/Bumps smaller than 50% of the original metallisation width on top of the metallisation.	4.2.7 (b)
3. REJECT	Depressed air bridge, no visible separation exists.	4.2.7 (c)



FAULT	DEFECT	PARA.
1. ACCEPT	Visible separation exists.	4.2.7 (c)
2. ACCEPT	Visible separation by insulting material exists.	4.2.7 (c)
3. REJECT	Air bridge overhang, no visible separation.	4.2.7 (d)



FAULT	DEFECT	PARA.
1. REJECT	Nodules/Bumps such that the remaining separation X between parallel air bridge paths at different potentials is <50% of the original value D.	4.2.7 (b)
2. REJECT	Nodules/Bumps such that a clear separation between air bridge and underlying operational metallisation at different potentials is no longer discernible.	4.2.7 (b), (c)



4.2.8 Transistor Gate Structure

N.B.

1. The provision of SEM data is recommended to support the inspection of sub-micron structures.
2. Ohmic contact and gate bus defects are covered by the general metallisation chapters.
3. **During pre-cap inspection, only criterion (a) below shall usually be evaluated except that if this criterion is not fulfilled, then all criteria shall be verified during the pre-cap.**
4. **During Construction Analysis, Destructive Physical Analysis and Failure Analysis, all criteria apply and shall be verified.**
5. If no clear line of separation between gate and ohmic contact is discernible by design or technology, then criterion (h) is not applicable.

(a) Any lack of homogeneity visible along the gate (necking, different discolouration, etc. except black spots at the gate resulting from a lift off of metallisation).

FIGURE XV - NECKING OF GATE METALLISATION

Colour Image shown in Appendix A.

(b) Excess metal on the gate shall not increase the gate length by more than 50%.

(c) Scratches in the metallisation which start at the gate channel edge or scratches on the gate metallisation, not including the pad or connecting line area.

(d) Voids in the gate stripe.

N.B.
Voids are **accepted** at the end of the gate outside of the ohmic contacts area.

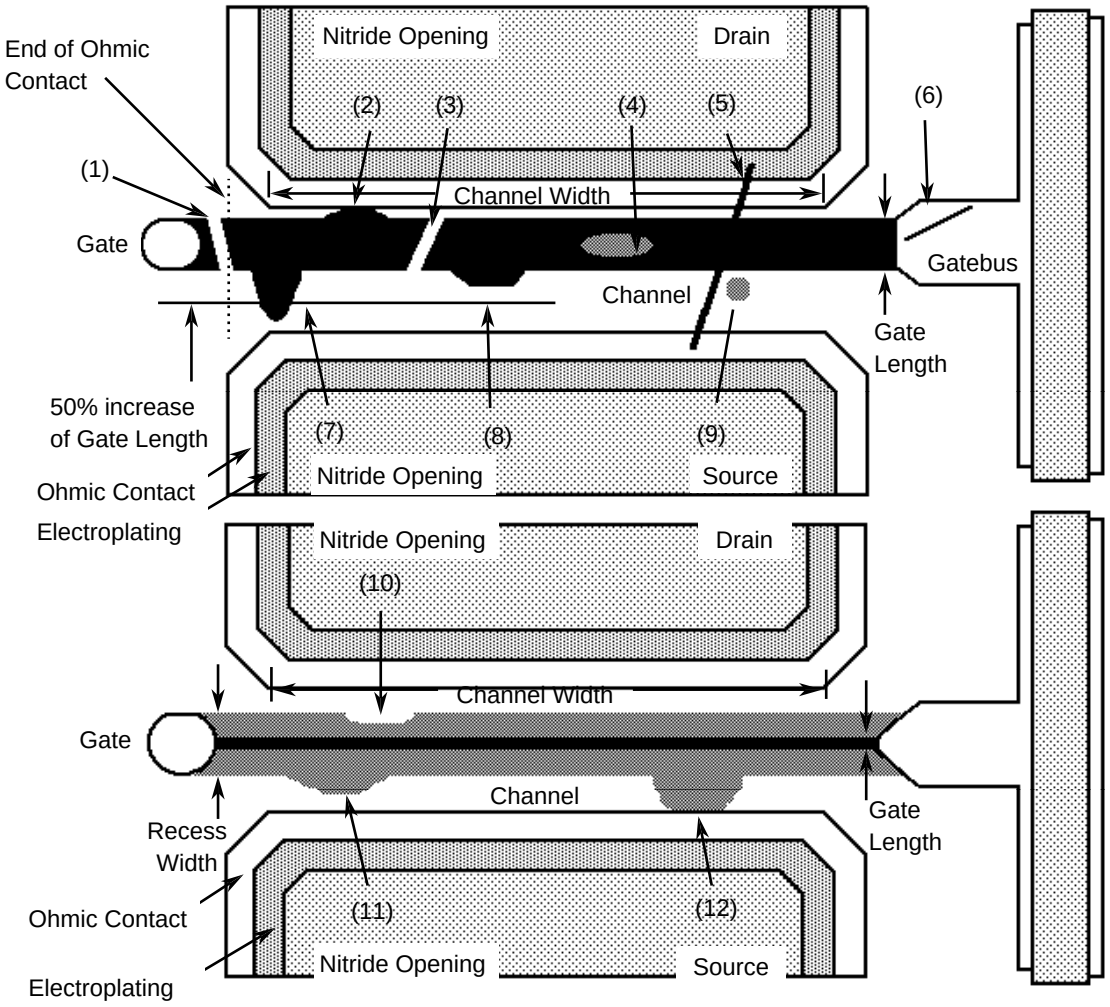
(e) If a clear line of separation between gate and ohmic contact is not discernible, device functional testing at wafer level must be demonsrated.

(f) Reduction of recess width, if applicable by design or technology.

(g) No visible space between recess and ohmic contact, if applicable by design or technology.

(h) Any metallisation bridging, gate misalignment/shift or particle under the passivation that reduces the original separation between gate and ohmic contacts to less than 50%.

FIGURE XVI - TRANSISTOR GATE STRUCTURE DEFECTS



FAULT	DEFECT	PARA.
1. ACCEPT	Void in the gate stripe at the gate outside ohmic contact area	4.2.8 (d)
2. REJECT	No line of separation between gate and ohmic contact visible (**except if** device functional testing is demonstrated)	4.2.8 (e)
3. REJECT	Void in the gate stripe	4.2.8 (d)
4. REJECT	Lack of homogeneity (i.e. discolouration) except black spots as per Para. 4.2.8 (i))	4.2.8 (a)
5. REJECT	Scratch which starts at the gate channel edge	4.2.8 (c)
6. ACCEPT	Scratch in the gate connecting line area which respects the general scratch criteria (Para. 4.2.2)	4.2.8 (c)
7. REJECT	Excess metal on the gate increases gate length by more than 50%	4.2.8 (b)
8. ACCEPT	Excess metal on the gate increases gate length by less than 50%	4.2.8 (b)
9. REJECT	Metallisation bridging or particle under the passivation reducing the original separation gate-ohmic contact to less than 50%	4.2.8 (h)
10. REJECT	Reduction of recess width	4.2.8 (f)
11. ACCEPT	Increase of recess width with visible space to ohmic contact	4.2.8 (g)
12. REJECT	Increase of recess width without visible space to ohmic contact	4.2.8 (g)

Acceptance Criteria

(i) A black spot on the edge of a lift-off of metallisation is **acceptable.**

FIGURE XVII - ACCEPTED BLACK SPOT

Colour Image shown in Appendix A.

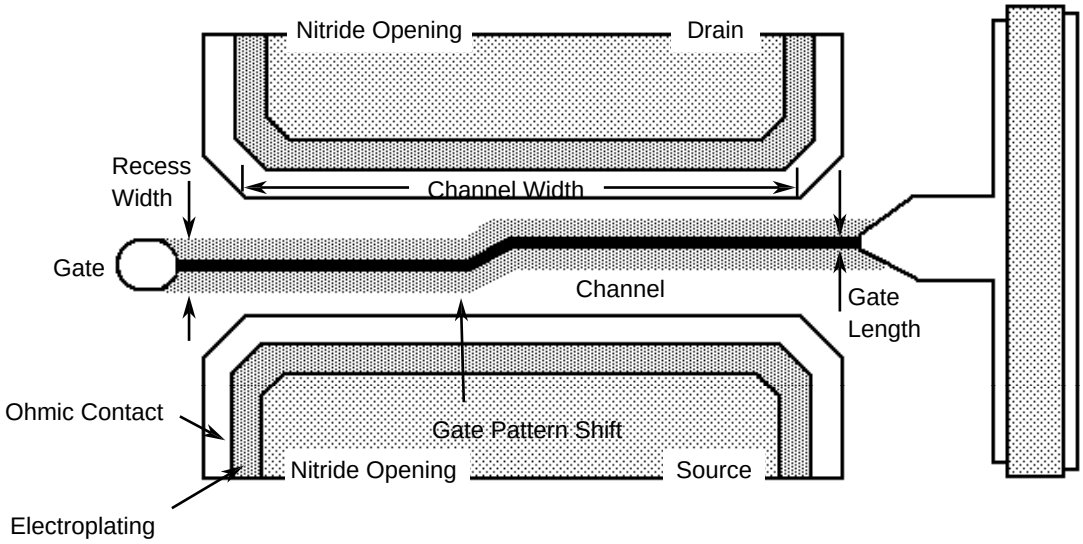
(j) Nodules on top of the gate metallisation are **acceptable.**

FIGURE XVIII - ACCEPTED NODULES ON TOP OF THE GATE

Colour Image shown in Appendix A.

(k) Misalignment of a part of the gate due to a EBEAM writing error can be **accepted** if no reduction of gate length occurs and criterion (h) is respected.

FIGURE XIX - ACCEPTED GATE PATTERN SHIFT DUE TO EBEAM WRITING ERROR



4.2.9 MIM Capacitor

(a) Scratch in the metallisation that exposes the dielectric material of a thin film capacitor or cross-over.

(b) Void(s) in the metallisation area of a thin film capacitor.

(c) Protuberances and nodules on a capacitor surface.

4.2.10 Spiral Inductor

N.B.
The provision of SEM data is recommended to support the inspection of sub-micron structures.

(a) At least a line of separation must be visible between adjacent metallisation paths.

4.2.11 High Mesa Structure

N.B.
The provision of SEM data is recommended to support the inspection of sub-micron structures.

(a) Any substrate irregularity under the metallisation.

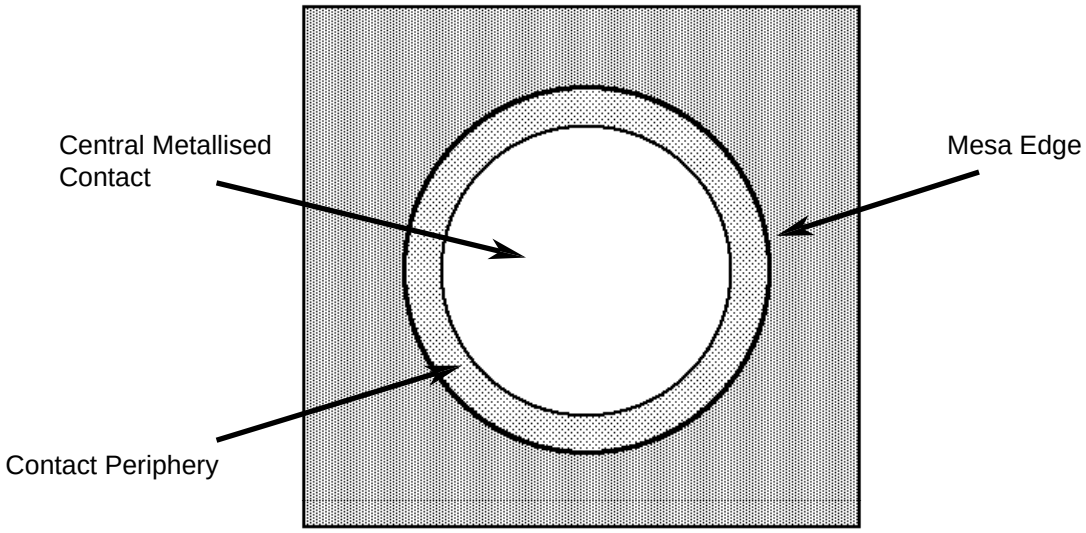
(b) If any irregularities are observed for conducting layers crossing over the mesa edge and if SEM is available, it should be applied in order to verfiy the integrity of the conducting layer.

Acceptance Criteria

(c) A certain percentage of voids, holes and lack of metallisation is **accepted** on the edge of the central metallised contact if:

- Contact area ∅<100µm, a maximum of 10% of defective contact periphery is **accepted.**
- Contact area ∅>100µm, a minimum of 25% of defective contact periphery is **accepted.**

FIGURE XX - HIGH MESA STRUCTURE DEVICES



4.2.12 Co-Planar Transmission Line

(a) Lack of homogeneity of the central line width and/or the separation of central line to ground planes.

4.2.13 Backside Metallisation

(a) Evidence of metallisation corrosion.

(b) Metallisation having any discoloured localised area shall be closely examined and shall be rejected unless it is demonstrated to be harmless effect.

(c) Any evidence of metallisation lifting, peeling or blistering.

N.B.
A saw damaged region of 25µm from the die edge needs to be excluded.

(d) If applicable, void(s), or missing metallisation on the back face metallisation (unless by design or specified by a Manufacturer in-house specification, die edge excluded), where in the case of low power devices the defective area is greater than 20%. **In the case of high power devices, any void has to be rejected.**

(e) Foreign material that is attached to the backside metallisation and might affect the die pick-up or the die attach procedure is a reason for rejection.

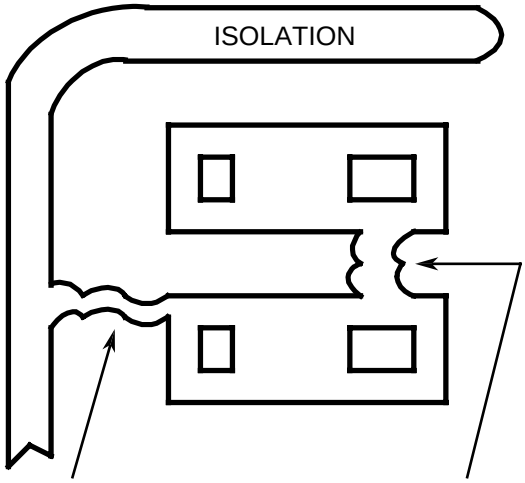
4.3 DIFFUSION AND PASSIVATION DEFECTS

No device shall be acceptable that exhibits:-

(a) A diffusion area that appears to be discontinuous.

(b) A diffusion fault that allows bridging between any two diffused areas, any two metallisation areas or any combination thereof not intended by design.

FIGURE XXI - DIFFUSION FAULT



REJECT: Diffusion Fault between Diffused Areas

(c) A contact window in a diffused area which unintentionally extends across a junction into an undiffused area or another diffused area.

(d) A passivation fault, including pinholes, that exposes bare semiconductor material and allows bridging between any two diffused areas or a combination thereof not intended by design.

(e) Pinholes on any junction or active area.

(f) Bare semiconductor material areas not covered by passivation and exposing or touching any metallisation.

(g) Unless by design, either multiple lines or a complete absence of passivation visible at the edge and continuing under the metallisation.

(h) An active junction area which is not covered by passivation (except by design) or exhibiting passivation cracking.

(i) More than two fringe undercuttings present on any junction.

(j) Areas of undercutting which exhibit other than normal passivation colour differentiation.

(k) A depression or irregularity which is not part of the design pattern and which is completely covered by metallisation.

(l) Any misalignment such that a continuous passivation colour cannot be seen.

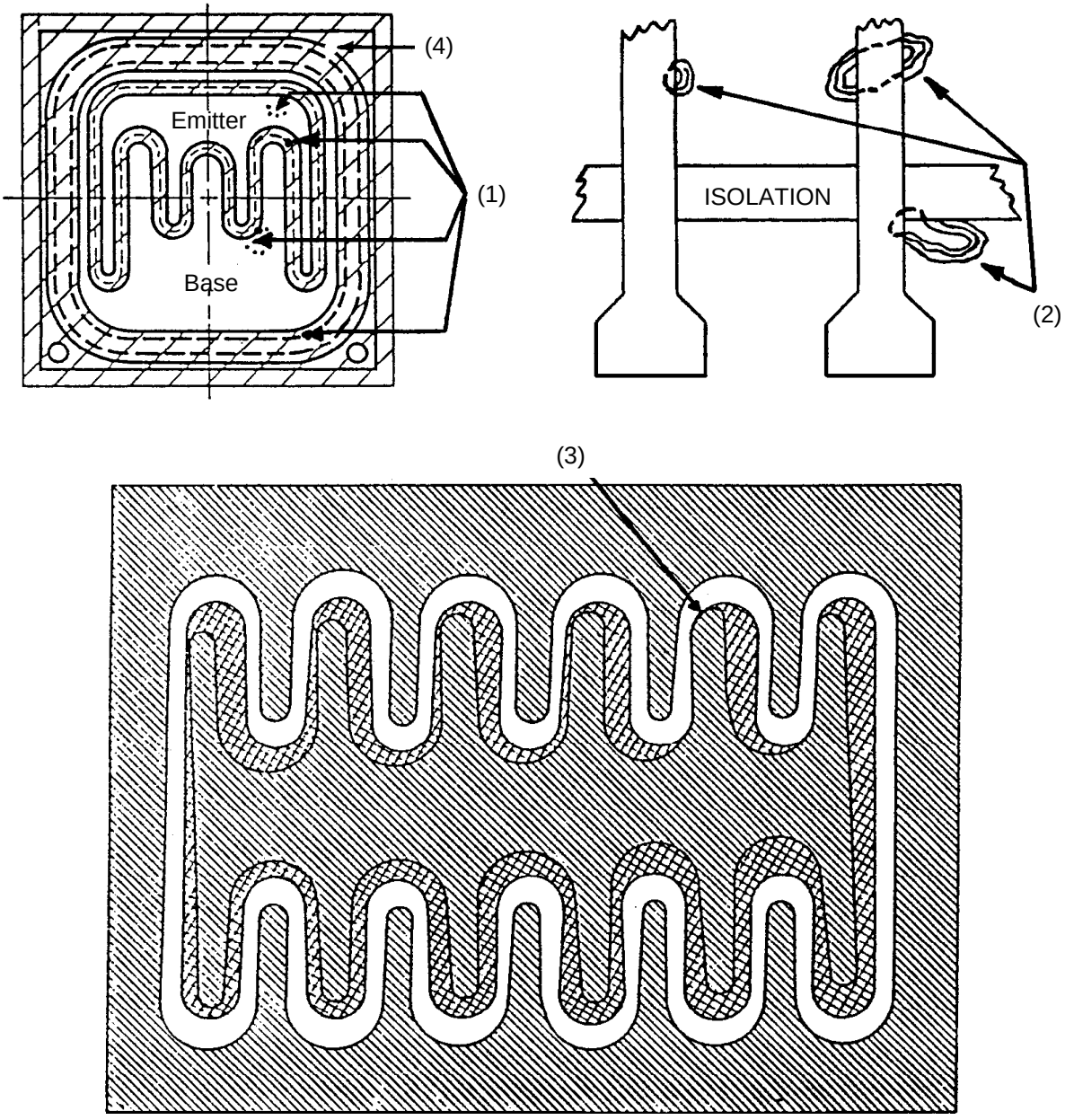
(m) A break in continuity of the annular stopper, isolation or guard ring.

(n) Evidence of over-etching.

(o) Insulation Film Defect on the gate.

(p) Passivation residue larger than 25% of bonding pad area. See also Para. 4.8.2 (v).

FIGURE XXII - PASSIVATION DEFECT



FAULT	DEFECT	PARA.
1. REJECT	Pinholes on junction/active circuit area	4.3 (e)
2. REJECT	Passivation defect under metallisation	4.3 (g)
3. REJECT	Misalignment causing non-continuous passivation colour	4.3 (l)
4. REJECT	Continuity break in annular stopper	4.3 (m)

4.4 GLASSIVATION DEFECTS

No device shall be acceptable that exhibits:-

(a) Glass crazing that prevents detection of the visual criteria contained below.

(b) Any glassivation which has delaminated. Lifting or peeling of the glassivation shall be excluded from the above when it does not extend more than 25µm from the designed periphery of the glassivation, provided that the only exposure of metal is of adjacent bond pads or of metallisation leading from those pads.

(c) Two or more adjacent active metallisation pads which are not covered by glassivation, except by design.

(d) Unglassivated areas at the edge of a bonding pad which expose semiconductor material.

(e) Glassivation which covers more than 25% of the design bonding pad area.

(f) Stains, discolouration, voids and deep scratches that extend over the active area of the device, unless by design.

(g) Scratch(es) in the glassivation that disturbs metal and which bridges metallisation areas.

(h) Voids in the glassivation which expose adjacent non-connected metal patterns of active structures.

(i) Scratches in the glassivation over adjacent non-connected metal patterns of active structures.

(j) Scratches in the glassivation over the active region of transistors, diodes, and other functional elements operating at microwave frequencies.

(k) Cracks in the glassivation which are more than 25µm inside the scribe line, or are more than 50% of the distance between the scribe line and any functional or active element (e.g. capacitor, resistor, transistor) or which point towards any functional or active element.

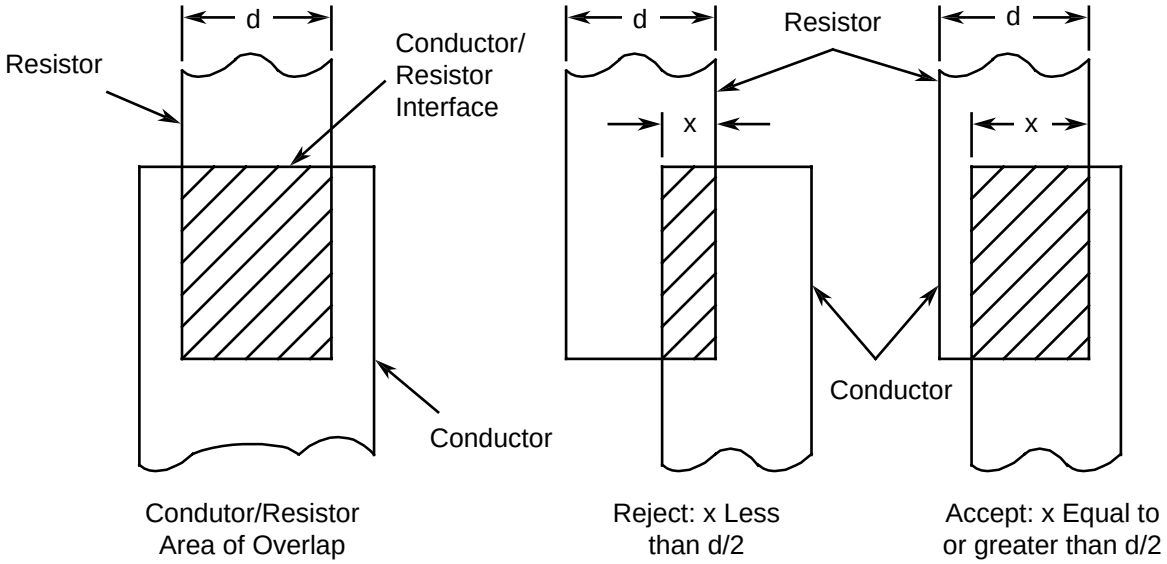
4.5 RESISTORS

4.5.1 Film Resistors

No device shall be acceptable that exhibits:-

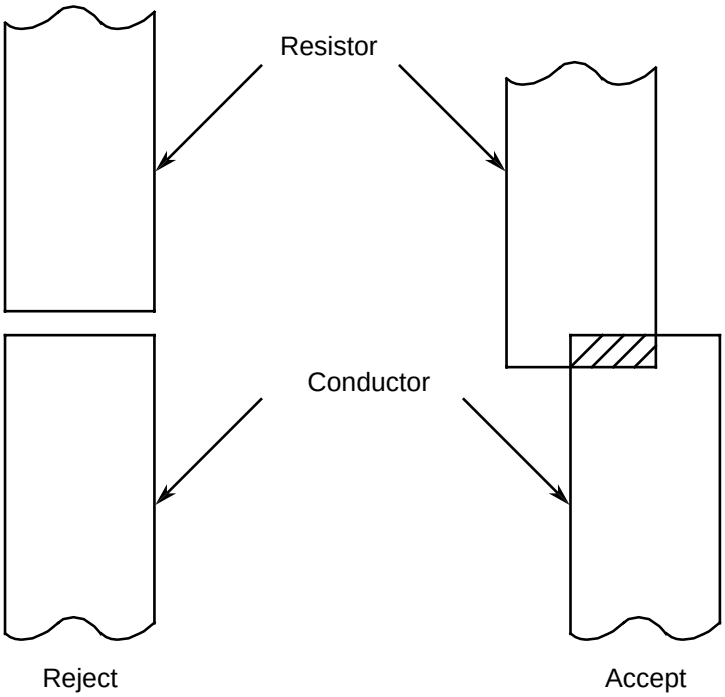
(a) Any misalignment between the conductor/resistor in which the actual width X of the overlap is less than 50% of the original resistor width.

FIGURE XXIII - LATERAL MISALIGNMENT OF FILM RESISTORS



(b) No visible line of contact overlap between the metallisation and film resistor.

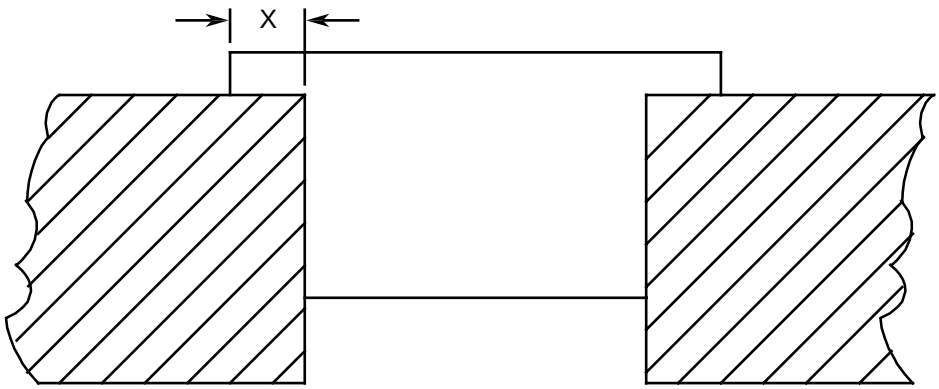
FIGURE XXIV - AXIAL MISALIGNMENT OF FILM RESISTORS



(c) For thin-film resistors, a contact overlap between metallisation and the resistor in which the length dimension X<5.0µm.

(d) For thick-film resistors, a contact overlap between metallisation and the resistor in which the length dimension x<75µm.

FIGURE XXV - CONTACT OVERLAP



REJECT WHEN X<THAN SPECIFIED

(e) Increase in resistor width greater than 25% of the original line width unless by design.

(f) Void or necking down that leaves less than 75% of the film resistor width undisturbed at a terminal.

(g) Any sharp change in colour of resistor material within 2.5µm from resistor/connector termination.

(h) Separation between any two resistors, or a resistor and a metallisation path, that is less than 2.5µm, or 50% of the design specification, whichever is less.

(i) Any substrate irregularity that leaves less than 75% of the original resistor width.

(j) Voids or scratches which reduce the resistor width to less than 75% of the narrowest resistor width.

4.5.2 Implanted Resistors

No device shall be acceptable that exhibits:-

(a) Lack of passivation on the implanted area and the contacts of an implanted resistor.

(b) Scratch within the passivation on the resistor.

(c) Scratch or void exposing underlying material that leaves less than 75% of the original area of the contact resistor undisturbed.

(d) Any substrate irregularity under the resistor.

4.6 DIE MOUNTING DEFECTS

No device shall be acceptable that exhibits:-

(a) Die mounted such that it is not flat against the bottom of the package within 10°.

(b) Die mounted such that it is not properly oriented according to the drawing.

(c) Die geometry or dimensions not in accordance with the applicable assembly drawing of the device.

(d) Die attach material at the edge of the die exceeding the height of the die, except for unprotected MESA devices where the die attach material shall not exceed the height of the lower etch limit.

(e) Die attach material on the surface of the die.

(f) Slag or crumbly die attach material visible around the die or on the header.

(g) Voids in the fillet greater than 1/3 on any side of the die (see Fig. XXVI), not applicable for thin AuGe backside metallisation or backside patterned devices, as no fillet will be visible.

(h) For low power devices, die mounting material (eutectic wetting or solder) not visible around at least one complete side, or 25%, of the perimeter, except for transparent die or dies with backside patterned.

(i) Die mounting material (eutectic wetting or solder) not visible around at least two complete sides, or 60%, of the die perimeter, except for transparent die or dies with backside patterned.

(j) Flaking of the die mounting material.

(k) Balling or build-up of the die mounting material that does not exhibit a minimum of a 50% peripheral fillet, when viewed from above, or the accumulation of bonding material is such that the height of the accumulation is greater than the longest base dimension or the accumulation necks down at any point.

(l) Where top metallisation of the die extends to the die edge or to the edge of a MESA etching, the maximum height of conductive material allowable is 50% up the side of the die.

FIGURE XXVI - DIE MOUNTING DEFECTS

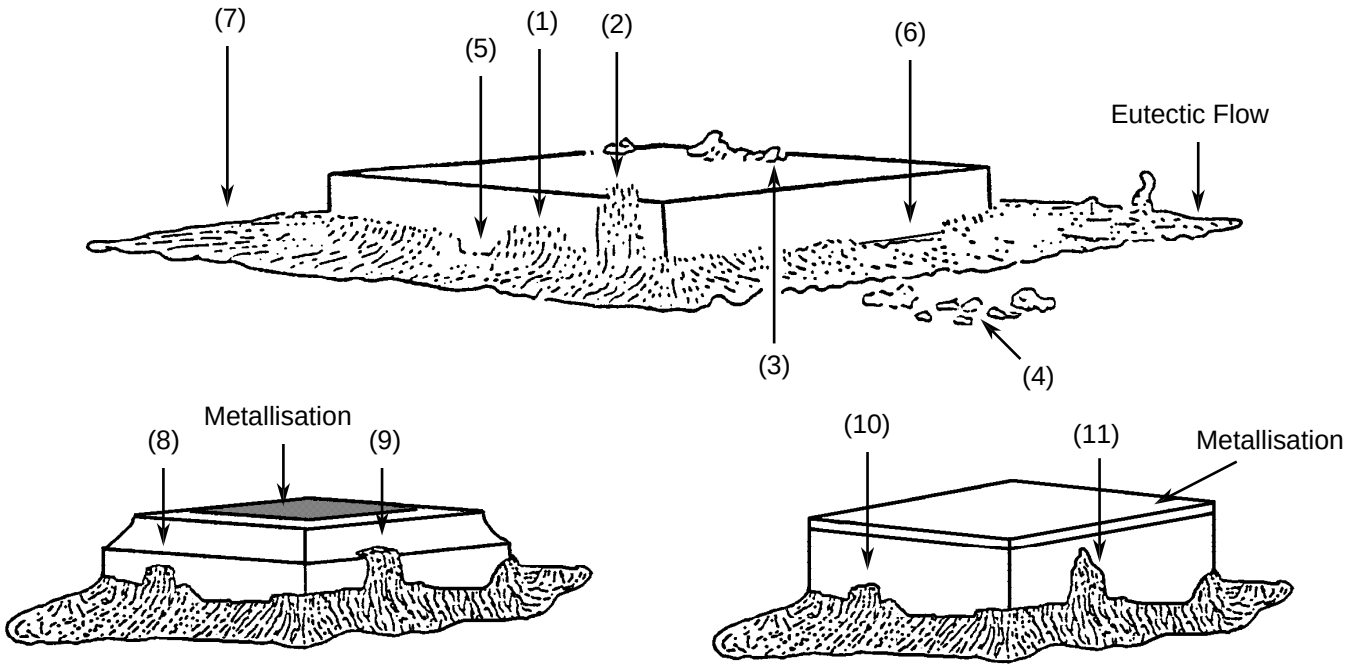


TABLE TO FIGURE XXVI

FAULT	DEFECT	PARA.
1. ACCEPT	Not exceeding die height	4.6 (d)
2. REJECT	Exceeding die height	4.6 (d)
3. REJECT	Die attach material on the surface of the die	4.6 (e)
4. REJECT	Crumbly die attach material	4.6 (f)
5. ACCEPT	Void less than 1/3 of a side	4.6 (g)
6. REJECT	Void larger than 1/3 of a side	4.6 (g)
7. REJECT	Flaking of the die mounting material	4.6 (i)
8. ACCEPT	Die attach material not exceeding the lower etch limit	4.6 (d)
9. REJECT	Die attach material exceeding the lower etch limit	4.6 (d)
10. ACCEPT	Die attach material not exceeding 50% of die height	4.6 (k)
11. REJECT	Die attach material exceeding 50% of die height	4.6 (k)

(m) Any eutectic material on the glass to metal seal which reduces the exposed glass surface distance from header to post by more than 25%.

FIGURE XXVII - EUTECTIC MATERIAL ON GLASS TO METAL SEAL

Colour Image is shown in Appendix A.

(n) Any flaking, peeling, or lifting of the adhesive material.

(o) Separation, cracks or fissures whose width is larger than 100µm in the adhesive at the cavity wall or cavity floor.

(p) Crazing in the adhesive. Cracks are fractures in the adhesive that have sharp broken edges. Crazing is the presence of numerous minute interconnected surface cracks.

(q) Any adhesive material that is connected to the fillet or conductive cavity (e.g. metal package base or metallised floor of ceramic package) and extends up the cavity wall to within 25µm of the package post.

(r) Die mounting material (other than non-conductive glasses) build up that touches the conductive top surface of the insulating island.

(s) Die mounting material (other than non-conductive glasses) that extends vertically above the top surface of the insulating island.

(t) Unmelted preform.

(u) Preform that overlaps onto any insulation material.

(v) Preforms that are not firmly attached to the package.

(w) Foreign material or rough surface holding the die off the header.

(x) Die which overlap onto insulation material.

4.7 HEADER DEFECTS

No device shall be acceptable that exhibits:-

(a) Blistering, flaking or cracking of gold or nickel plating.

(b) Die or part of a die on the flange or on the side of the header.

(c) Grease, varnish, ink or similar stain on the flange or the side of the header.

(d) Plating or die attach material overlapping the seals.

(e) Excess metallisation which reduces the insulation separation by more than 50%.

(f) Corrosion of the package, header or can.

(g) Cracks in the ceramic body.

(h) Mechanical damage.

(i) Radial cracks that extend in excess of a third of the distance from the pin to the outer perimeter of the seal.

(j) Cracks in the circumference, except the meniscus, that extend more than 90° about the seal centre.

(k) Contamination on the flange, rim or other cap sealing area with any dimension greater than half the width of the sealing/welding area.

(l) Bubbles in the glass to metal seal with dimensions greater than 0.8mm or any cluster of bubbles with a combined dimension greater than two adjacent pins.

(m) Bubbles, or an area of adjacent or interconnecting bubbles, in the seal area larger than 12.5% of the seal area or which are more than half of the distance between the pin and body or pin and pin.

(n) Foreign particles enclosed in the glass seal.

(o) Cracked or chipped glass seals. Meniscus chip-outs must not exceed 0.2mm in any dimension.

4.8 BOND DEFECTS

No device shall be acceptable that exhibits the following bond defects.

4.8.1 General Part 1

N.B.

1. All criteria defined for wire bonds shall also be valid for tape bonding, if applicable. For Tape Automated Bonding Techniques, the same integrity as for bond wires shall be kept, but due to the large variety of different forms no specific criteria can be given for this technique. Cross-shaped bonds can be inspected according to existing single bond criteria (See e.g. Paras. 4.8.4 (d) and (e) and the exceptions given in Paras. 4.8.1 (i), 4.8.2 (d), (e), (g) and (r)).

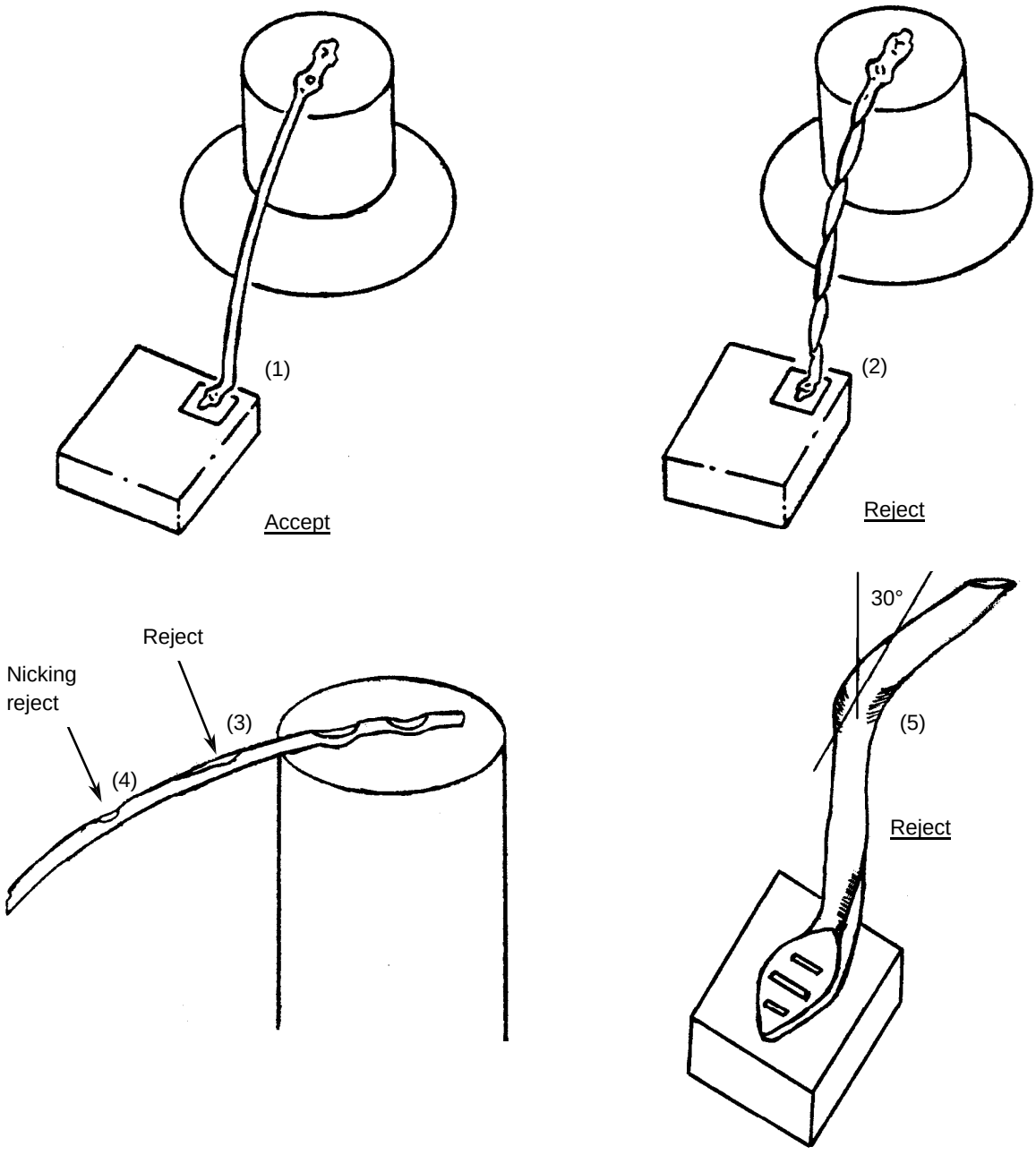
2. Some of the criteria listed below can be omitted if package dimensions are too small to respect these criteria.

(a) Wire twisted more than 360° from pad bond to pillar bond.

(b) Any nicks, crimps, twisting, scratching, scoring or other deformity which reduces the wire diameter by more than 25%.

(c) Any wire exhibiting a kink of exterior angle greater than 30°.

FIGURE XXVIII - GENERAL BOND DEFECTS



FAULT	DEFECT	PARA.
1. ACCEPT	No twist	4.8.1 (a)
2. REJECT	360° twist	4.8.1 (a)
3. REJECT	Scratch reduces wire diameter by >25%	4.8.1 (b)
4. REJECT	Nick reduces wire diameter by >25%	4.8.1 (b)
5. REJECT	Kink with exterior angle >30°	4.8.1 (c)

(d) Black or purple plague or other corrosion around the bond perimeter or on the metallisation.

(e) Bonds on the package post which are not completely within the boundaries of the package post.

(f) Missing or broken bonds/wires.

(g) Tearing at the junction of the wire and the bond.

(h) Wire or wires not in accordance with the device bonding diagram.

(i) A bond placed on top of an existing bond, unless defined in the design document.

(j) Any evidence of repair of metallisation by bridging with a bond or the addition of a bonding wire or ribbon.

(k) Bond or wire bond tails that extend over and make contact with any metallisation not covered by glassivation other than bonding pad metallisation.

(l) For bonds on the die bonding pad, the minimum percentage of bond within the unglassivated bonding pad area shall be:

- Where the bond area is smaller than the bonding wire, 50%. However, the bond must cover the entire area of the bond pad.
- Where the bond pad is larger than the bond, 75%.

(m) Any evidence of bond wires having attached portions of die mounting material.

4.8.2 General Part 2

(a) Lifted bonds.

(b) Excessive loops, bows or sags in any wires such that they could short to another wire, to another pad or any other package post, to the die or could touch any portion of the package.

(c) Bond wire fragments or bond pad metal detached from the bond or pad.

(d) Bonds placed such that the wire exiting from the bond crosses over another bond unless by design.

(e) Separation of bonds and/or bond wires from adjacent bonds, exposed semiconductor material or active unglassivated metallisation not connected to the bond shall not be less than a wire diameter, unless by design.

(f) For bonds made to an area on the package containing die mounting material, the maximum acceptable area of bond located in this area shall be 25%.

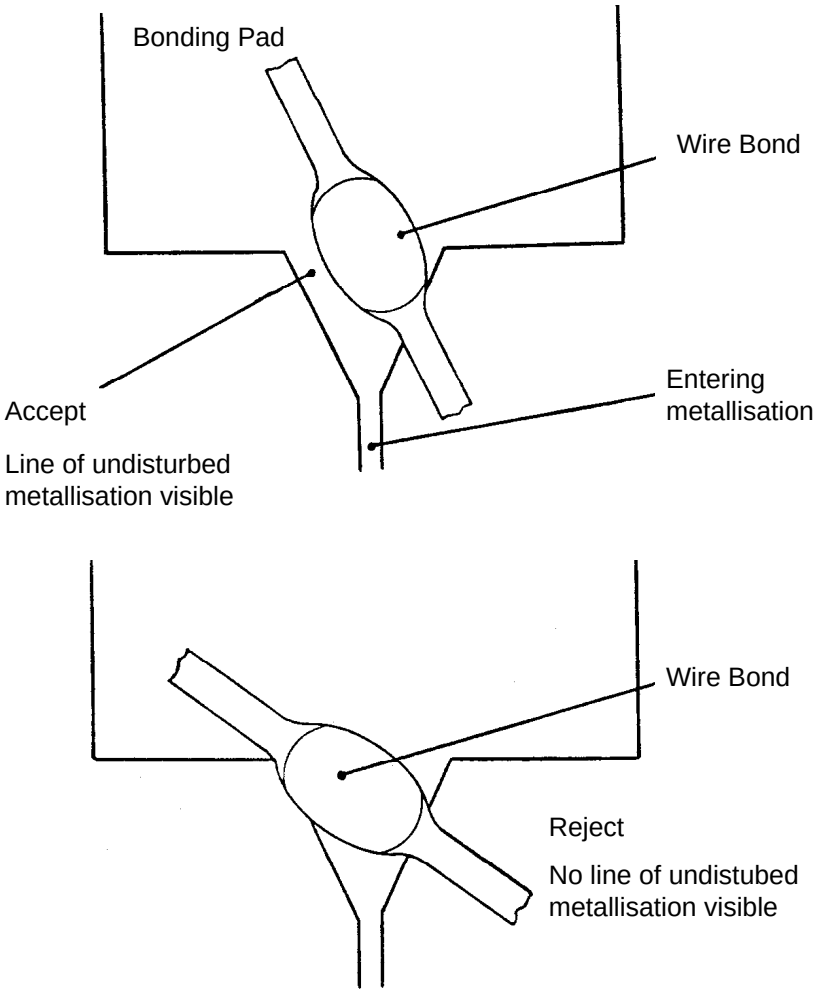
(g) A bond overlapping another bond, bond wire or residual segment of lead wires, unless by design.

(h) Bonds that at the point where metallisation exits from the bonding pad, do not exhibit a line of undisturbed metallisation visible between the periphery of the bond and at least one side of the entering metallisation (see Figure XXIX).

N.B.
When bond tails prevent visibility of the connecting path and the metallisation immediately adjacent to the bond tail is disturbed, the device shall be unacceptable.

When a fillet area exists, it is considered as part of the entering/exiting metallisation stripe.

FIGURE XXIX - BONDS AT THE METALLISATION EXIT



(i) Metallic protrusions around the bond wires in the form of scuffed bonding pad material or wire bond whiskers. This excludes lateral metal disturbance up to 5.0µm around the side of the wire bond or 1 x wire diameter in front of the wire bond.

(j) The minimum acceptable distance of heel of wedge or tailless bond from edge of post/lead shall be 1 x wire.

(k) A bow or a loop between double bonds at package rim greater than 2 x wire diameter.

(l) Wire bond tails exceeding 2 x wire diameters in length at the pad or 4 x wire diameters at package post/lead.

(m) Bond tails extending over glassivated metallisation where the glass exhibits evidence of crazing or cracking that extends under the tail, excluding common conductors.

(n) Intermetallic formation extending radially in excess of 2.5µm completely around the periphery of that portion of the gold bond located on metal.

(o) Bonds on foreign material.

(p) Bond touching metallisation other than bond pad metallisation.

(q) Side welds having less than an estimated 50% of the package-post weld situated on the specified bonding area.

(r) No visible gap between the bonds of a multiple bonding, unless specified by design.

(s) Bond lifting or tearing at the interface of the pad and wire. This criterion is applicable to single bonds and any part of a double bond.

(t) No aluminimum whiskers accepted.

(u) Multicoloured stains in the bonding pad area. Multicoloured stains appearing along the periphery of the etch line are acceptable, provided that the unstained metallisation is not reduced to less than 75% of the bonding pad area.

4.8.3 Gold Ball Bonds

(a) Less than two thirds of the ball in contact with the pad.

(b) Wire terminating on the perimeter of the ball when viewed from above.

(c) Wire of which the diameter at the ball is reduced by more than 25%.

(d) Ball height, viewed from the side, less than one wire diameter or more than twice the wire diameter.

(e) Wire centre exit not within the boundaries of the bonding pad.

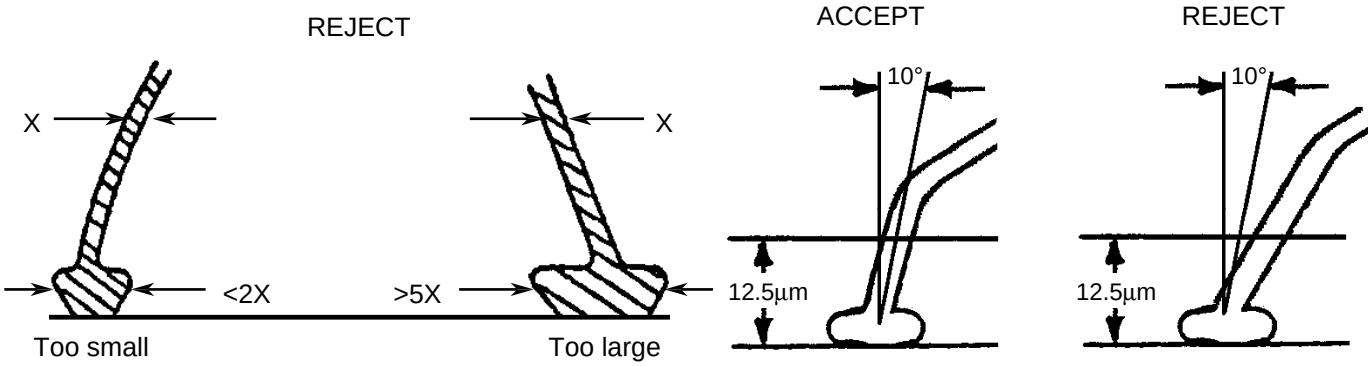
(f) Gold ball bonds on the die pad or the package post, viewed from the top, where the ball bond diameter is less than 2 x or greater than 5 x the wire diameter.

(g) Intermetallic formation extending radially more than 2.5µm completely around the periphery of any gold ball bond for that portion of the gold ball bond located on metal.

(h) The wire from the ball bond on the die rising to more than 4/3 of the post height. The requirement of the excessive loop sag must still be met.

(i) Wire not within 10° of the perpendicular to the surface of the chip for a distance of greater than 12.5µm before bending towards the package post or other terminating point.

FIGURE XXX - BALL BONDS



4.8.4 Wedge Bonds

(a) Pad bond torn in the bond area or behind the bond.

(b) Nicks in the side of the bond or holes in the centre of the bond.

(c) Needle impression area lifted more than 25%.

(d) If the bond is smaller than the pad area, at least 75% of the needle impression of the pad bond must be bonded to the metallisation, unless by design.

(e) If the bond is larger than the pad area, less than 50% of the needle impression of the pad bond appearing on the area of the pad, unless by design.

(f) Ultrasonic wedge bonds on the die or package post that are less than 1.2 x or more than 3 x the wire diameter in width, or are less than 1.5 x or more than 6 x the wire diameter in length.

(g) Thermocompression or thermosonic wedge bonds on the die or package post that are less than 1.5 x or more than 3 x the wire diameter in width, or are less than 1.5 x or more than 6 x the wire diameter in length.

(h) Wedge bonds where the tool impression does not cover the entire width of the wire or 75% of the width of the bonding ribbon.

4.8.5 Crescent Bonds

(a) Crescent bond width less than 1.2 x or more than 5 x wire diameters or length less than 0.5 x or more than 3 x wire diameters.

(b) Crescent bonds where bond impression does not cover the entire width of the wire.

4.8.6 Internal Lead Wires

(a) Nicks, bends, cuts, crimps, scoring or neck-down in any wire that reduces the wire diameter by more than 25%.

(b) Missing or extra lead wires or wires not in accordance with the internal bonding diagram.

(c) Tearing at the junction of the wire and bond or lifted bonds.

(d) Wire(s) crossing wire(s) is a reject. Excluded are common conductors, when viewed from above, and multi-tiered packages where the crossing occurs within the boundary of the lower wire bond tier(s) being crossed, or packages with down bond(s). In these situations, the wires that cross are acceptable if they maintain a minimum clearance of 2 x wire diameters.

(e) A bow or loop between double bonds at post greater than 4 x wire diameter.

4.8.7 Beam Lead Construction

(a) Voids, nicks, depressions, or scratches that leave less than 50% of the beam width undisturbed.

(b) Beam separation from the die.

(c) Missing or partially fabricated beam leads unless in accordance with with the design specification.

(d) Beam leads that are not bonded, unless by design.

(e) Bonded area closer than 2.5µm to the edge of the passivation layer.

(f) Passivation layer less than 2.5µm between the die and the beam visible at both edges of the beam.

(g) Bonds where the tool impression does not cross the beam width by at least 75%.

(h) Bonds on thin-film substrate metal where the tool impression increases the beam lead width less than 15% (10% for compliant bonds) or greater than 75% of the undeformed beam width.

(i) Bonds where the tool impression length is less than 25µm.

(j) Bonding tool impression less than 25µm from the die edge.

(k) Effective bonded area less than 50% of that which would be possible for an exactly aligned beam.

(l) Cracks or tears in the effective bonded area of the beam greater than 50% of the original beam width.

(m) Bonds placed so that the separation between bonds and between bonds and operating metallisation not connected to them, is less than 2.5µm.

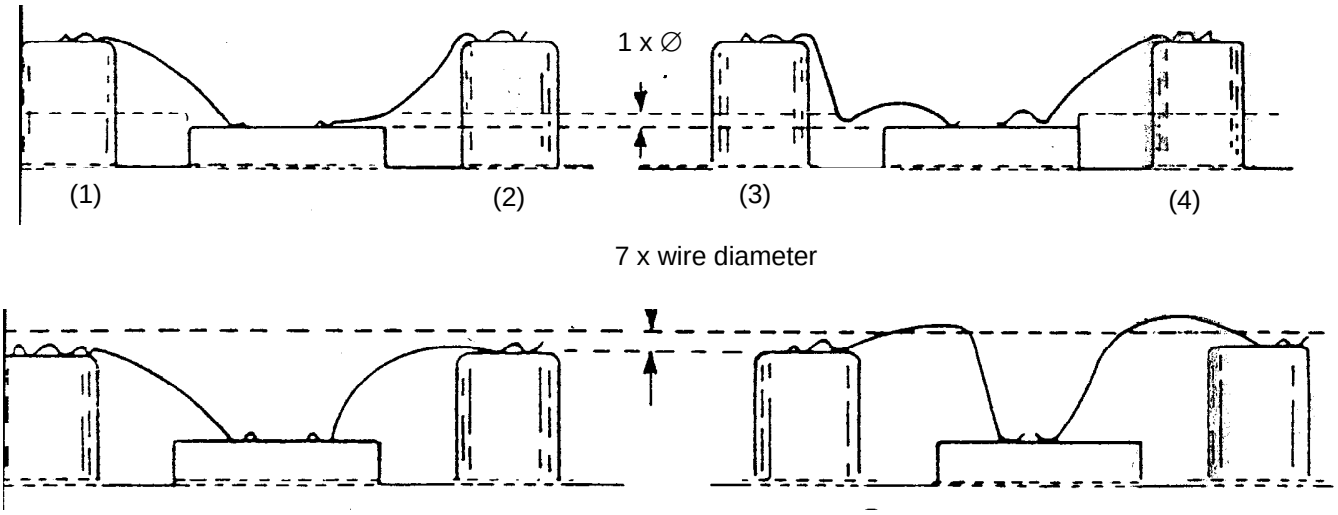
4.8.8 Up-Bonding

(a) Wire not travelling in a smooth upward arc from the pad bond to the edge of the die and clearing the edge by less than 1 x wire diameter.

(b) Wire rising more than 7 x wire diameters above the top of the pillar.

(c) Wire sagging below 1 x wire diameter above the top of the die.

FIGURE XXXI - UP-BONDING



FAULT	DEFECT	PARA.
1. ACCEPT	Proper arc and clearance	4.8.8 (a)
2. REJECT	Clearance<1 x wire diameter ∅	4.8.8 (a)
3. REJECT	Not rising in a smooth upward arc	4.8.8 (a)
4. REJECT	Sags below 1 x wire diameter ∅	4.8.8 (c)
5. ACCEPT	Rises <7 x wire diameter ∅	4.8.8 (b)
6. REJECT	Rises >7 x wire diameter ∅	4.8.8 (b)

4.8.9 Down-Bonding

(a) Wire not travelling in a smooth upward arc from the pad bond to the edge of the die and clearing the edge by less than 1 x wire diameter.

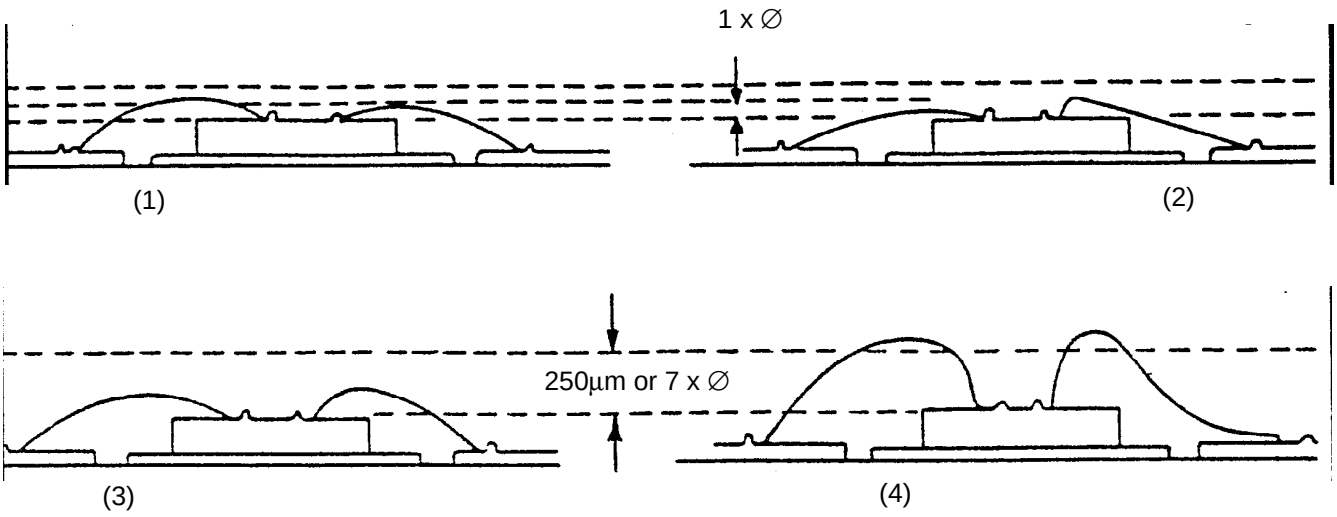
N.B.
An exception can be made for devices where short bonds are required as defined in the design document and a semi-insulating substrate material is employed.

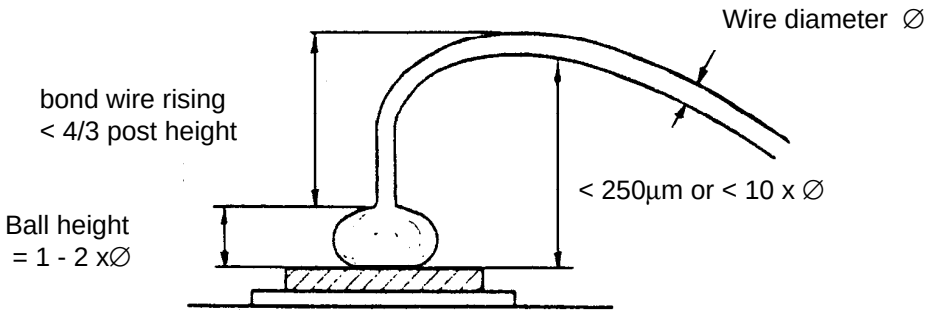
(b) Wire sagging below 1 x wire diameter above the top of the die.

(c) For ultrasonic bonding: For wires equal to or less than 75µm in diameter, rising more than 250µm or 7 x wire diameters, whichever is the less, above the top of the die. For wires greater than 75µm in diameter, rising more than 3 x wire diameters above the top of the die.

(d) For gold ball bonding, gold wire rising more than 250µm or 10 x wire diameters, whichever is the less, above the top of the die.

FIGURE XXXII - DOWN-BONDING





(5)

FAULT	DEFECTS	PARA.
1. ACCEPT	Proper arc and clearance	4.8.9 (a)
2. REJECT	Clearance<1 x wire diameter	4.8.9 (a)
3. ACCEPT	Proper arc and clearance	4.8.9 (a)
4. REJECT	>250µm or >7 x wire diameters (wire diameter <75µm) above top of the die	4.8.9 (c)
5. ACCEPT	<250µm or <10 x wire diameters above top of the die	4.8.9 (d)

4.8.10 Rebonding

N.B.
The meaning of rebonding excludes repair.

(a) Rebonding onto the die shall only be permitted where the bond pad area has been designed to accommodate a rebond (but see (b) below).

N.B.
The second bond shall be at a point near to the metallisation exit. There shall be no residual bond material between the rebond and the exiting metallisation.

(b) Rebonds are permitted only if the original bonding has not removed bond pad material.

(c) At least 50% of the attachment area of a rebond shall be placed on undisturbed metal (excluding probe marks that do not expose underlying material).

(d) The total number of rebonds shall be limited to a maximum of 10% (to the nearest whole number) of the total number of bonds on the device.

(e) A bond-off is defined as a bond with a wire tail <2 x wire diameters, made in the process of clearing the bonding tool following an unsuccessful bond attempt. Extra lead wires, other than bond-offs, anywhere on the package as a result of clearing the bonding tool are a cause for rejection.

4.9 FOREIGN MATTER

Foreign matter shall be considered to be attached when it cannot be removed with a gas blow of dry nitrogen at 140kN/m^2 gauge applied for a minimum of three seconds from a distance of 50mm. The nozzle used shall not be less than 1.0mm in diameter.

Tweezers or other instruments shall not be used to remove particles from the die surface.

4.9.1 Foreign Matter Defects

No device shall be acceptable that exhibits:-

(a) Attached foreign matter greater than 200μm in any dimension on the surface of the die out of the active area or within the package.

(b) Any attached conductive foreign matter on the surface of the die or within the package, bridging, or being capable of bridging, any two areas of metallisation, functional device elements of semiconductor junctions, package leads or any combinations thereof.

(c) Attached foreign matter which cannot be clearly identified to be non-conductive **and** which reduces the actual separation between metallisation paths, functional circuit elements or junctions, or any combination thereof by more than 50%. An appropriate magnification shall be used.

(d) Foreign matter attached to a bond pad that leaves less than 50% of the unglassivated area undisturbed.

(e) Photoresist or other extraneous chemical material that if detached could result in a short circuit.

(f) Any ink on the die surface.

APPENDIX A

FIGURE XXXIII – DEPRESSED METAL OF A VIA HOLE

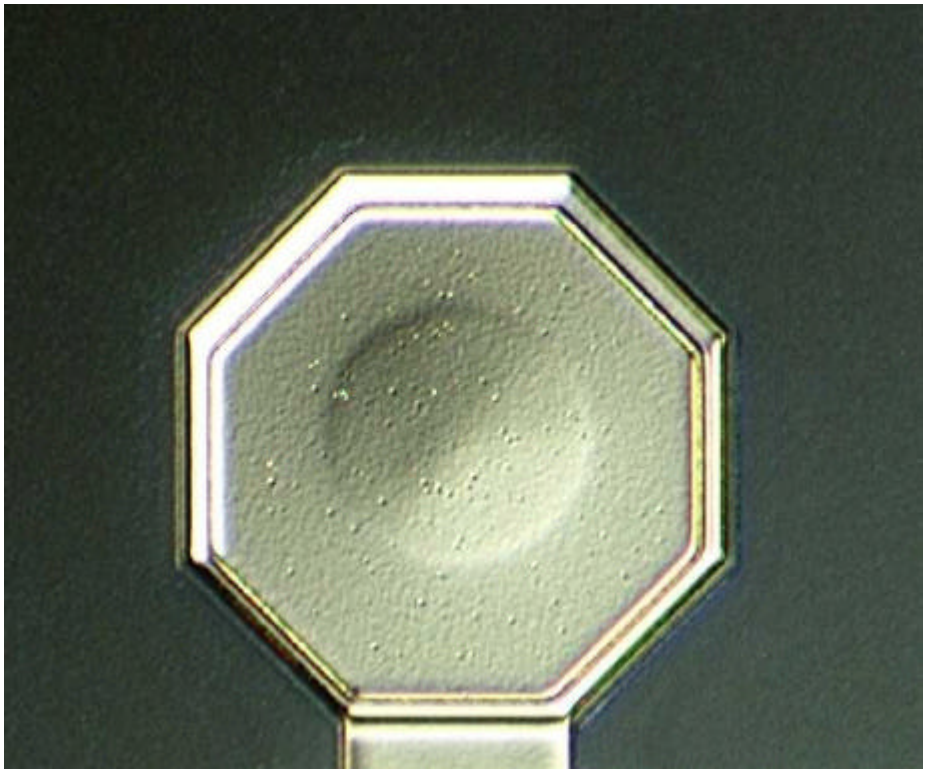


FIGURE XV – NECKING OF GATE METALLISATION

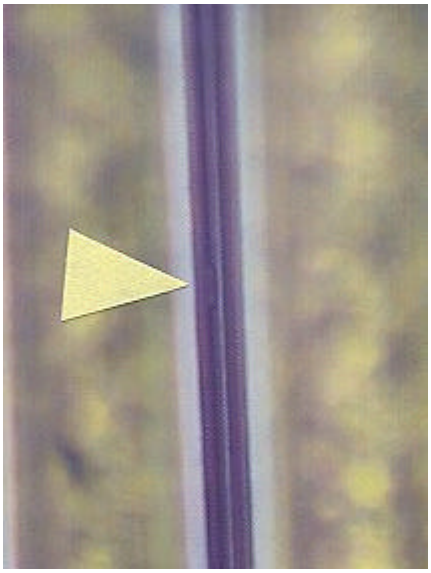


FIGURE XVII – ACCEPTED BLACK SPOT

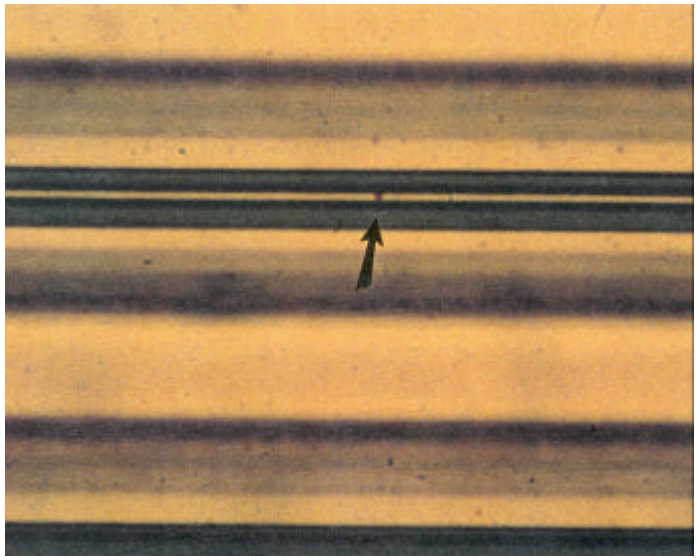


FIGURE XVIII – ACCEPTED NODULE ON TOP OF THE GATE

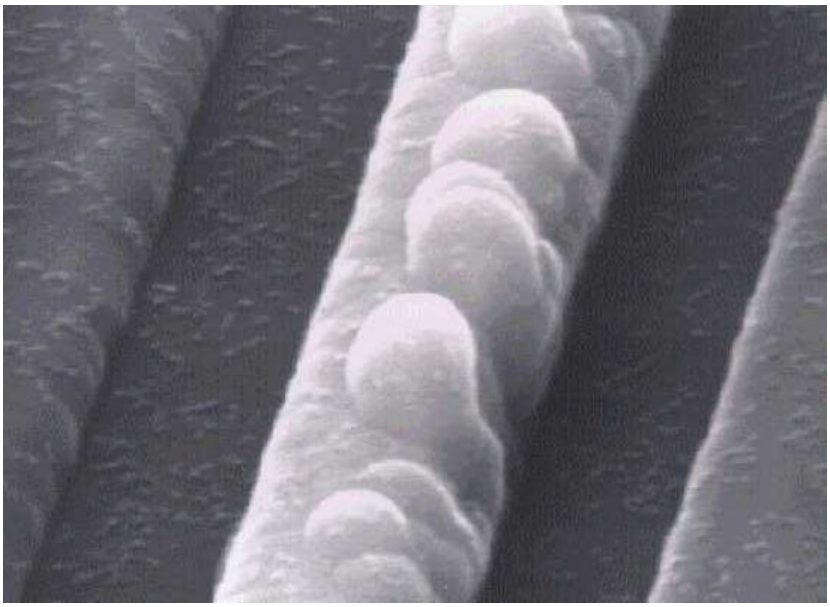


FIGURE XXVII – EUTECTIC MATERIAL ON GLASS TO METAL SEAL