INTEGRATED CIRCUITS, SILICON MONOLITHIC,

FAST SAMPLE AND HOLD

OPERATIONAL AMPLIFIER,

BASED ON TYPE HA-2420

ESCC Detail Specification No. 9101/009

ISSUE 1

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Pages 1 to 38

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ESA/SCC Detail Specification No. 9101/009

space components
coordination group

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DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.

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1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, Fast Sample and Hold Operational Amplifier, based on Type HA-2420. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The parameter derating information of the integrated circuits specified herein is shown in Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the integrated circuits specified herein are shown in Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

Not applicable.

1.8 CIRCUIT SCHEMATIC

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 with a Minimum Critical Path Failure Voltage of 1000 Volts.

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND FINISH
01	D.I.L.	2	G4

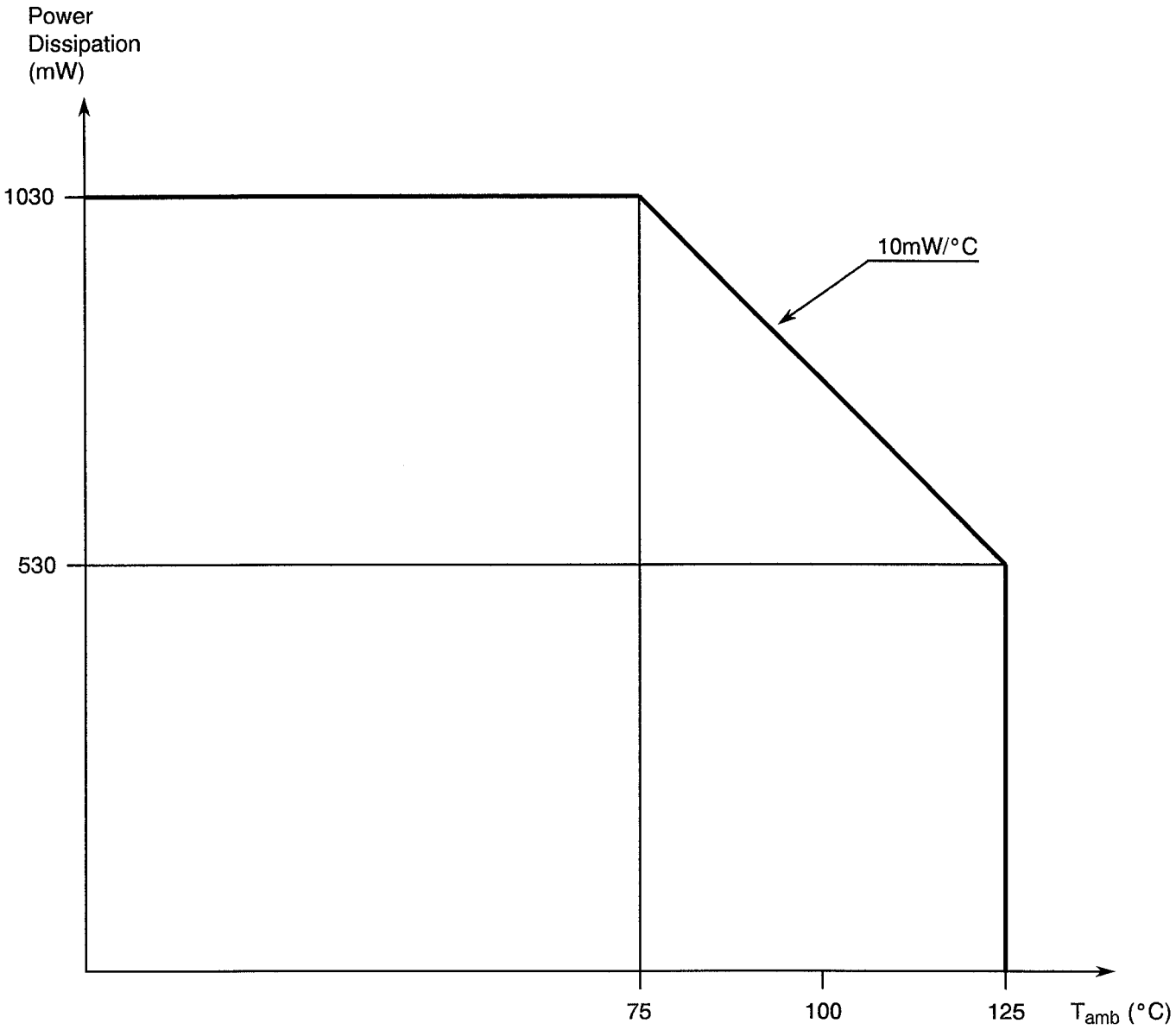
TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage Range	V_{CC}	±20	V	-
2	Differential Input Voltage Range	V_{ID}	±24	V	-
3	Digital Input Voltage Range	V_{IN}	+8.0 to −15	V	-
4	Device Power Dissipation (Continuous)	P_D	1030	mW	Note 1
5	Operating Temperature Range	T_{op}	−55 to +125	°C	-
6	Storage Temperature Range	T_{stg}	−65 to +150	°C	-
7	Soldering Temperature	T_{sol}	+265	°C	Note 2
8	Junction Temperature	T_J	+175	°C	-
9	Thermal Resistance	$R_{TH(J-C)}$	24	°C/W	-

NOTES

1. At T_{amb} = +75°C. For derating at T_{amb} > +75°C, see Figure 1.
2. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

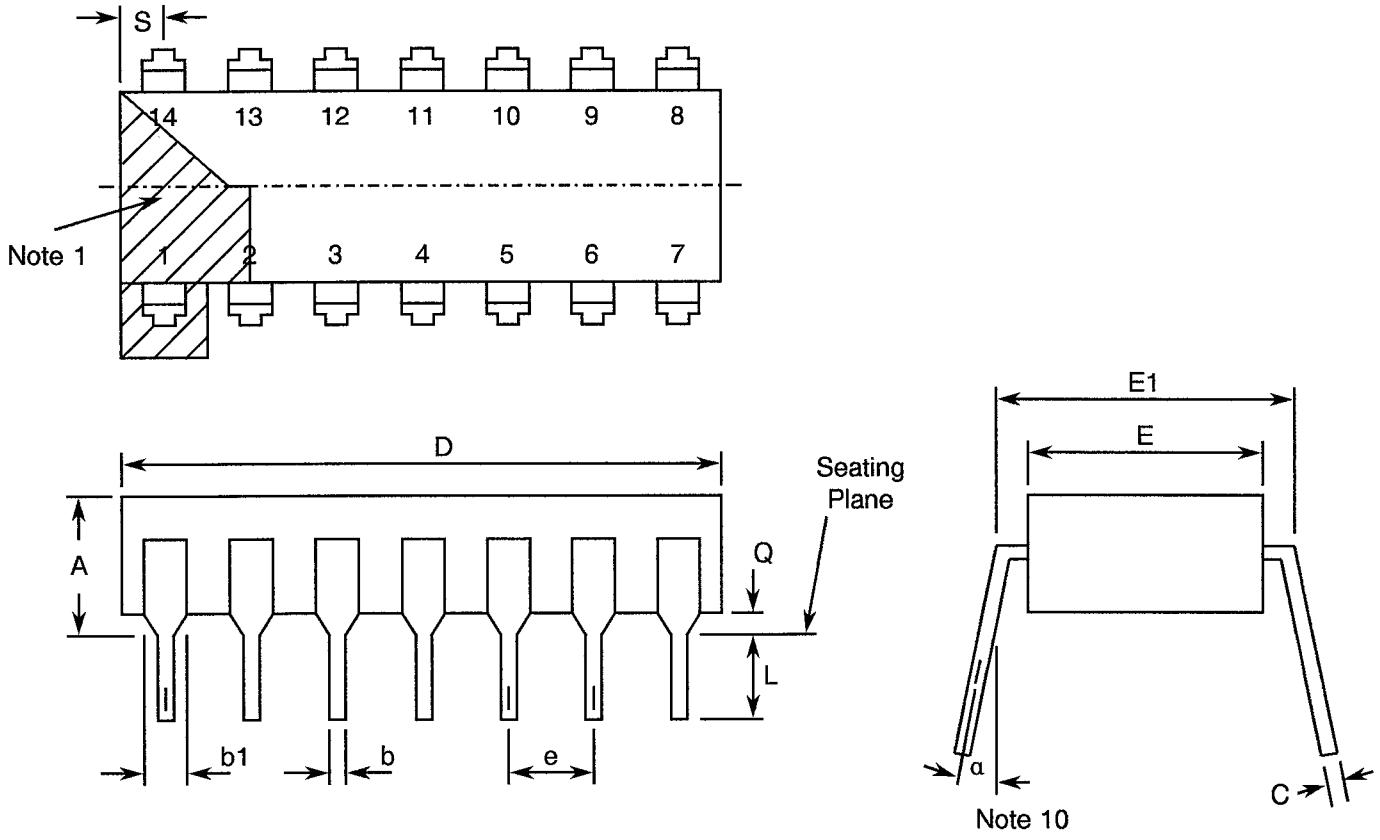
FIGURE 1 - PARAMETER DERATING INFORMATION



Power Dissipation versus Temperature

FIGURE 2 - PHYSICAL DIMENSIONS

DUAL-IN-LINE PACKAGE, 14-PIN



SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	-	5.08	
b	0.38	0.58	8, 13
b1	-	1.78	8
C	0.20	0.38	8, 13
D	-	19.94	
E	5.59	7.87	
E1	7.37	8.13	4
e	2.54 TYPICAL		6, 9
L	3.18	5.08	
Q	0.38	1.52	3
S	-	2.54	7
α	0°	15°	10

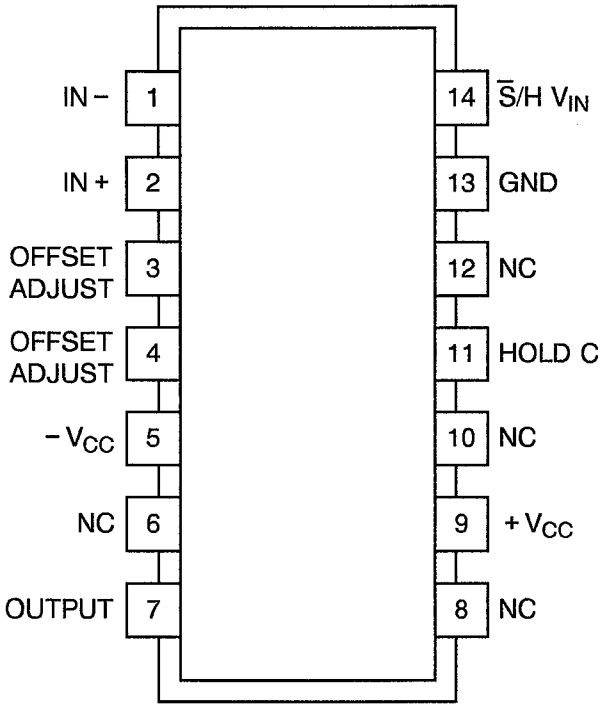
NOTES: See Page 9.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURE 2

1. Index area: a notch, letter or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown.
2. Not applicable.
3. The dimension shall be measured from the seating plane to the base plane.
4. This dimension allows for off-centre lids, meniscus and glass overrun.
5. Not applicable.
6. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ± 0.25mm of its true longitudinal position relative to Pins 1 and the highest pin number.
7. Applies to all 4 corners.
8. All leads or terminals.
9. 12 spaces.
10. Lead centre when α is 0°.
11. Not applicable.
12. Not applicable.
13. The maximum dimension may be increased by 0.077mm when hot solder dip has been applied.

FIGURE 3(a) - PIN ASSIGNMENT



(TOP VIEW)

FIGURE 3(b) - TRUTH TABLE

Not applicable.

FIGURE 3(c) - CIRCUIT SCHEMATIC

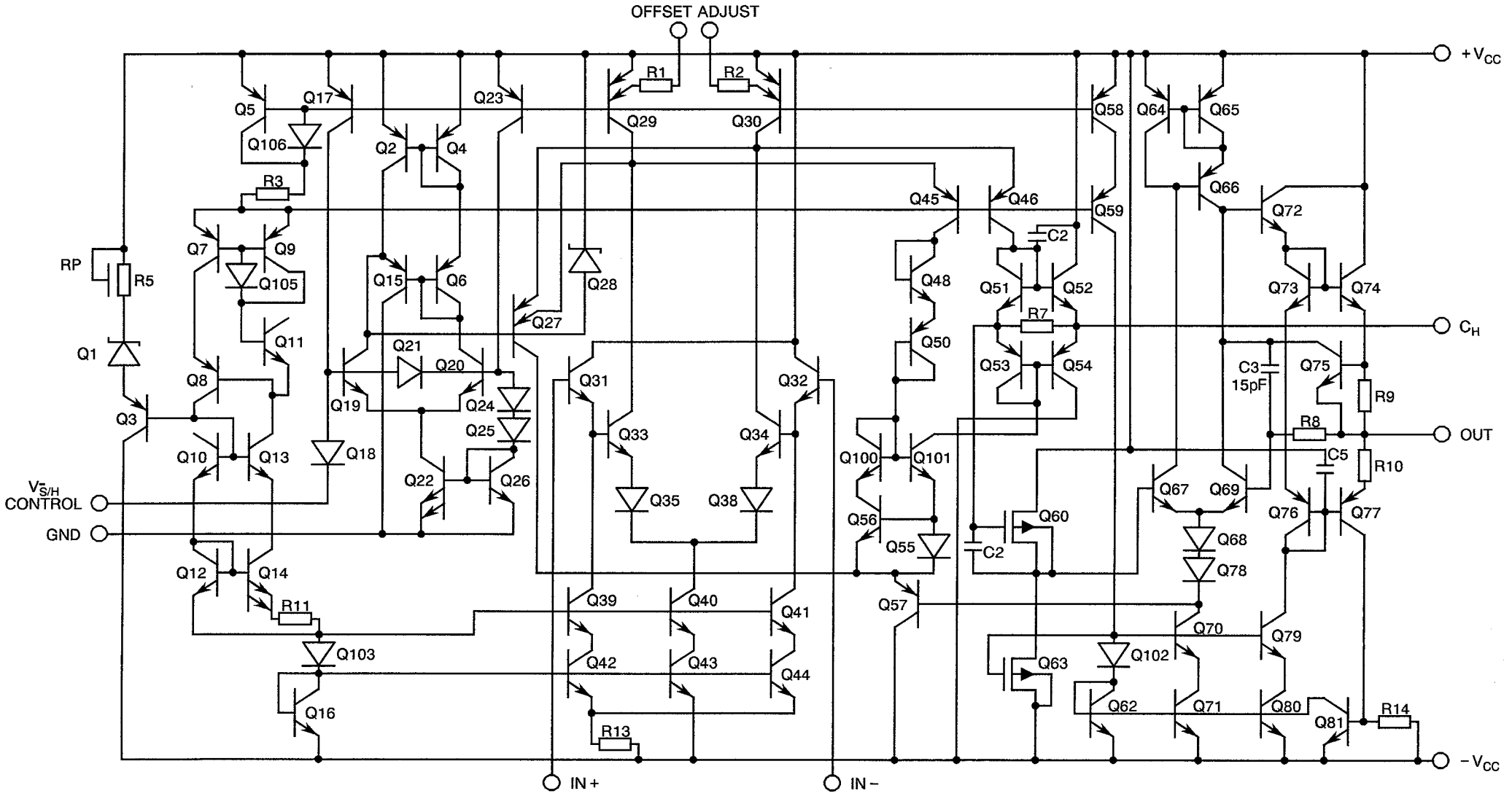
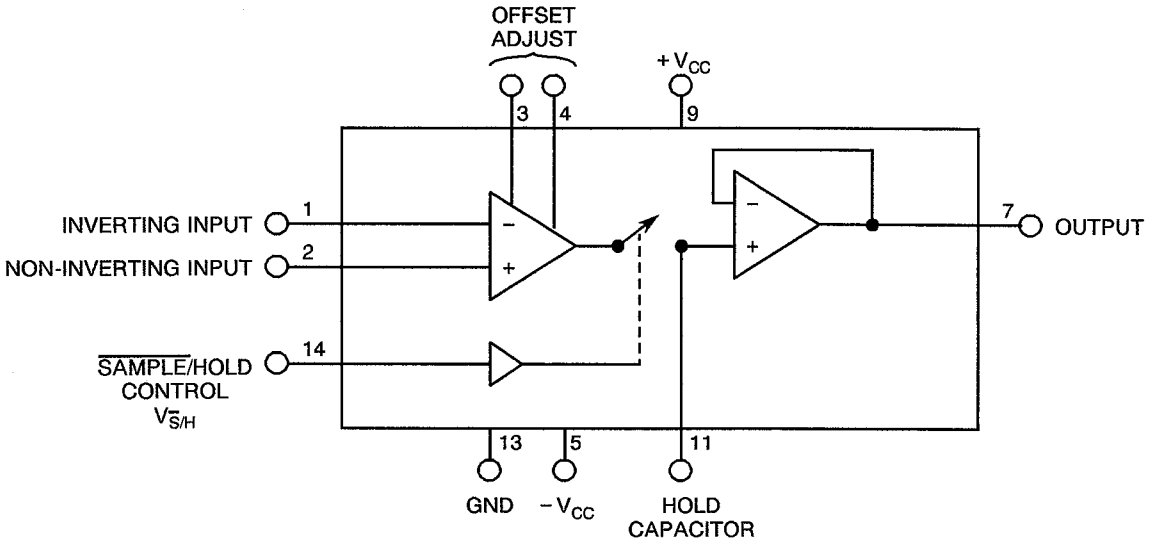


FIGURE 3(d) - FUNCTIONAL DIAGRAM



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

V_{CC} = Supply Voltage of the device under test.

AV = Gain of the device under test.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

(a) Para. 7.1.1(a), "High Temperature Reverse Bias" tests and subsequent electrical measurements related to this test shall be omitted.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 2.2 grammes.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body and the lids shall be preform-soldered or glass frit-sealed.

4.4.2 Lead Material and Finish

The lead material shall be Type 'G' with Type '4' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500.

4.5 MARKING

4.5.1 General

The marking of components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700 and the following paragraphs. When the component is too small to accommodate all of the marking as specified, as much as space permits shall be marked and the marking information, in full, shall accompany the component in its primary package.

The information to be marked and the order of precedence, shall be as follows:-

(a) Lead Identification.

(b) The SCC Component Number.

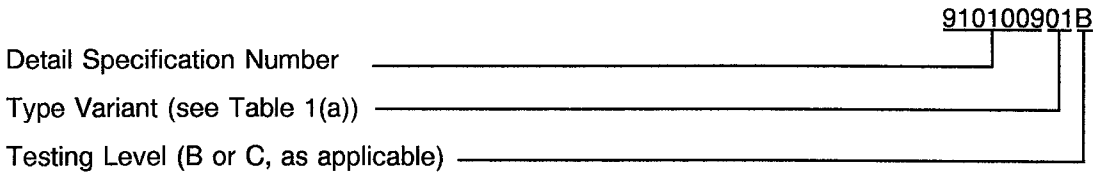
(c) Traceability Information.

4.5.2 Lead Identification

An index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits and test sequences for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +25 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-in

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for power burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for High Temperature Reverse Bias Burn-in

Not applicable.

4.7.5 Electrical Circuits for Power Burn-in

Circuits for use in performing the power burn-in tests are shown in Figure 5(b) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
1	Input Offset Voltage	V_{IO}	4001	4(a)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{DC} = 0V, $V_{\overline{S}/H}$ = +0.8V	−4.5	+4.5	mV
2	Input Offset Current	I_{IO}	4001	4(b)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{DC} = 0V, $V_{\overline{S}/H}$ = +0.8V	−50	+50	nA
3	Input Bias Current (Plus)	$+I_{IB}$	4001	4(b)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{DC} = 0V, $V_{\overline{S}/H}$ = +0.8V	−200	+200	nA
4	Input Bias Current (Minus)	$-I_{IB}$	4001	4(b)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{DC} = 0V, $V_{\overline{S}/H}$ = +0.8V	−200	+200	nA
5	Output Voltage Swing (Plus)	$+V_{OP}$	4004	4(c)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{DC} = −15V, $V_{\overline{S}/H}$ = +0.8V R_L = 2.0kΩ, C_L = 50pF	+10	-	V
6	Output Voltage Swing (Plus)	$-V_{OP}$	4004	4(c)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{DC} = +15V, $V_{\overline{S}/H}$ = +0.8V R_L = 2.0kΩ, C_L = 50pF	-	−10	V
7	Output Current High Level	I_{OH}	-	4(d)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{DC} = −13V, V_{OUT} = +10V $V_{\overline{S}/H}$ = +0.8V	+14	-	mA
8	Output Current Low Level	I_{OL}	-	4(d)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{DC} = +13V, V_{OUT} = −10V $V_{\overline{S}/H}$ = +0.8V	−14	-	mA
9	Input Current Low Level	I_{IL}	3009	4(e)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{DC} = 0V, $V_{\overline{S}/H}$ = 0V	-	800	µA
10	Input Current High Level	I_{IH}	3010	4(e)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{DC} = 0V, $V_{\overline{S}/H}$ = +5.0V	-	20	µA
11	Power Supply Current (Plus)	$+I_{CC}$	4005	4(f)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{DC} = 0V, $V_{\overline{S}/H}$ = +0.8V	-	6.0	mA
12	Power Supply Current (Minus)	$-I_{CC}$	4005	4(f)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{DC} = 0V, $V_{\overline{S}/H}$ = +0.8V	−3.5	-	mA
13	Open Loop Voltage Gain (Plus)	$+A_{VS}$	4004	4(g)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{DC} = 0V or −10V $V_{\overline{S}/H}$ = 0.8V R_L = 2.0kΩ, C_L = 50pF	25	-	V/mV
14	Open Loop Voltage Gain (Minus)	$-A_{VS}$	4004	4(g)	$+V_{CC}$ = +15V, $-V_{CC}$ = −15V V_{DC} = 0V or +10V $V_{\overline{S}/H}$ = 0.8V R_L = 2.0kΩ, C_L = 50pF	25	-	V/mV

NOTES: See Page 18.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
15	Power Supply Rejection Ratio (Plus)	+PSRR	4003	4(h)	$+V_{CC}$ = +10V or +20V $-V_{CC}$ = −15V, V_{DC} = 0V $V_{\overline{S}/H}$ = 0.8V	80	-	dB
16	Power Supply Rejection Ratio (Minus)	−PSRR	4003	4(h)	$-V_{CC}$ = −10V or −20V $+V_{CC}$ = +15V, V_{DC} = 0V $V_{\overline{S}/H}$ = 0.8V	80	-	dB
17	Common Mode Rejection Ratio (Plus)	+CMRR	4003	4(i)	$+V_{CC}$ = +25V, $-V_{CC}$ = −5.0V V_{GND} = +10V, V_{DC} = −10V $V_{\overline{S}/H}$ = 10.8V	80	-	dB
18	Common Mode Rejection Ratio (Minus)	−CMRR	4003	4(i)	$+V_{CC}$ = +5.0V, $-V_{CC}$ = −25V V_{GND} = −10V, V_{DC} = +10V $V_{\overline{S}/H}$ = −9.2V	80	-	dB

NOTES: See Page 18.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
19	Hold Step Error	V_{error}	-	4(k)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{DC} = 0V$, $V_{AC} = 0V$ $V_{\overline{S}/H} = 0V$ to 4.0V $t_r(V_{\overline{S}/H}) \leq 30ns$ $R_L = 2.0k\Omega$, $C_L = 50pF$	-20	+20	dB
20	Rise Time	t_r	4002	4(l)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $R_L = 2.0k\Omega$, $C_L = 50pF$ $t_r(V_{\overline{S}/H}) \leq 30ns$ $V_{\overline{S}/H} = 0.8V$, AV = 1.0 $V_{OUT} = 200mV$ peak-to-peak	-	100	ns
21	Fall Time	t_f	4002	4(l)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $R_L = 2.0k\Omega$, $C_L = 50pF$ $t_r(V_{\overline{S}/H}) \leq 30ns$ $V_{\overline{S}/H} = 0.8V$, AV = 1.0 $V_{OUT} = 200mV$ peak-to-peak	-	100	ns
22	Overshoot (Plus)	OS(+)	4002	4(l)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $R_L = 2.0k\Omega$, $C_L = 50pF$ $t_r(V_{\overline{S}/H}) \leq 30ns$ $V_{\overline{S}/H} = 0.8V$, AV = 1.0 $V_{OUT} = 200mV$ peak-to-peak	-	40	%
23	Overshoot (Minus)	OS(-)	4002	4(l)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $R_L = 2.0k\Omega$, $C_L = 50pF$ $t_r(V_{\overline{S}/H}) \leq 30ns$ $V_{\overline{S}/H} = 0.8V$, AV = 1.0 $V_{OUT} = 200mV$ peak-to-peak	-	40	%
24	Slew Rate (Plus)	SR(+)	4002	4(l)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $R_L = 2.0k\Omega$, $C_L = 50pF$ $t_r(V_{\overline{S}/H}) \leq 30ns$ $V_{\overline{S}/H} = 0.8V$, AV = 1.0 $V_{OUT} = \pm 10V$ step	3.5	-	V/µs
25	Slew Rate (Minus)	SR(-)	4002	4(l)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $R_L = 2.0k\Omega$, $C_L = 50pF$ $t_r(V_{\overline{S}/H}) \leq 30ns$ $V_{\overline{S}/H} = 0.8V$, AV = 1.0 $V_{OUT} = \pm 10V$ step	3.5	-	V/µs

NOTES

1. Measured at +125°C only.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
1	Input Offset Voltage	V_{IO}	4001	4(a)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{DC} = 0V$, $V_{\overline{S}/H} = +0.8V$	−6.5	+6.5	mV
2	Input Offset Current	I_{IO}	4001	4(b)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{DC} = 0V$, $V_{\overline{S}/H} = +0.8V$	−100	+100	nA
3	Input Bias Current (Plus)	$+I_{IB}$	4001	4(b)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{DC} = 0V$, $V_{\overline{S}/H} = +0.8V$	−400	+400	nA
4	Input Bias Current (Minus)	$-I_{IB}$	4001	4(b)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{DC} = 0V$, $V_{\overline{S}/H} = +0.8V$	−400	+400	nA
5	Output Voltage Swing (Plus)	$+V_{OP}$	4004	4(c)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{DC} = -15V$, $V_{\overline{S}/H} = +0.8V$ $R_L = 2.0k\Omega$, $C_L = 50pF$	+10	-	V
6	Output Voltage Swing (Minus)	$-V_{OP}$	4004	4(c)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{DC} = +15V$, $V_{\overline{S}/H} = +0.8V$ $R_L = 2.0k\Omega$, $C_L = 50pF$	-	−10	V
9	Input Current Low Level	I_{IL}	3009	4(e)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{DC} = 0V$, $V_{\overline{S}/H} = 0V$	-	0.8	mA
10	Input Current High Level	I_{IH}	3010	4(e)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{DC} = 0V$, $V_{\overline{S}/H} = +5.0V$	-	20	µA
13	Open Loop Voltage Gain (Plus)	$+A_{VS}$	4004	4(g)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{DC} = 0V$ or $-10V$ $V_{\overline{S}/H} = 0.8V$ $R_L = 2.0k\Omega$, $C_L = 50pF$	20	-	V/mV
14	Open Loop Voltage Gain (Minus)	$-A_{VS}$	4004	4(g)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{DC} = 0V$ or $+10V$ $V_{\overline{S}/H} = 0.8V$ $R_L = 2.0k\Omega$, $C_L = 50pF$	20	-	V/mV
15	Power Supply Rejection Ratio (Plus)	+PSRR	4003	4(h)	$+V_{CC} = +10V$ or $+20V$ $-V_{CC} = -15V$, $V_{DC} = 0V$ $V_{\overline{S}/H} = 0.8V$	80	-	dB
16	Power Supply Rejection Ratio (Minus)	−PSRR	4003	4(h)	$-V_{CC} = -10V$ or $-20V$ $+V_{CC} = +15V$, $V_{DC} = 0V$ $V_{\overline{S}/H} = 0.8V$	80	-	dB

NOTES: See Page 18.

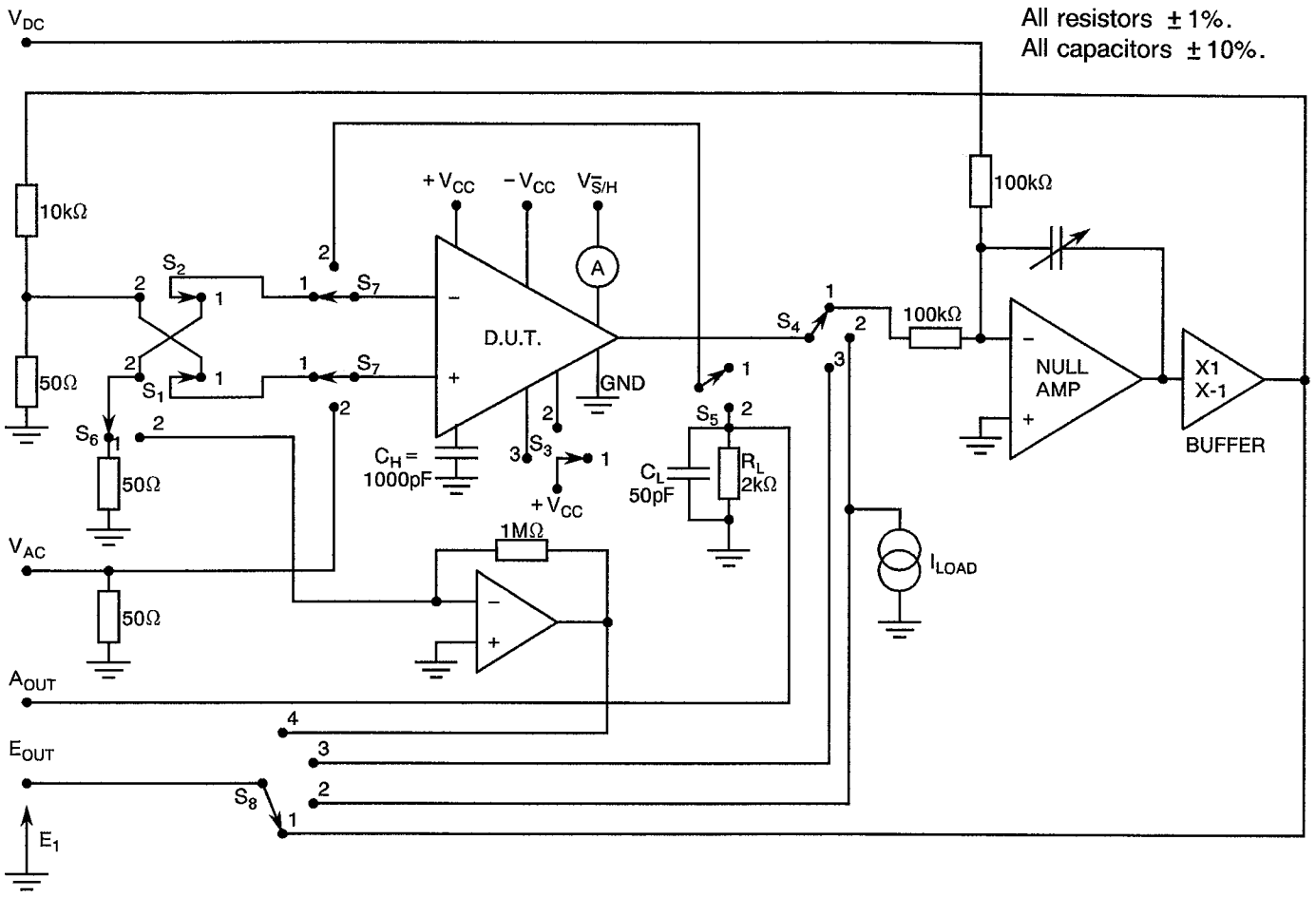
TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
17	Common Mode Rejection Ratio (Plus)	+CMRR	4003	4(i)	$+V_{CC} = +25V$, $-V_{CC} = -5.0V$ $V_{GND} = +10V$, $V_{DC} = -10V$ $V_{\overline{S}/H} = 10.8V$	80	-	dB
18	Common Mode Rejection Ratio (Minus)	-CMRR	4003	4(i)	$+V_{CC} = +5.0V$, $-V_{CC} = -25V$ $V_{GND} = -10V$, $V_{DC} = +10V$ $V_{\overline{S}/H} = -9.2V$	80	-	dB
26	Drift Current	I_D	-	4(j)	$+V_{CC} = +15V$, $-V_{CC} = -15V$ $V_{AC} = 0V$, $V_{DC} = 0V$, $V_{\overline{S}/H} = 4.0V$ $R_L = 2.0k\Omega$, $C_L = 50pF$ Note 1	-	±10	nA

NOTES: See Page 18.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - INPUT OFFSET VOLTAGE



SWITCH POSITION							
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
1	1	1	1	1	1	1	1

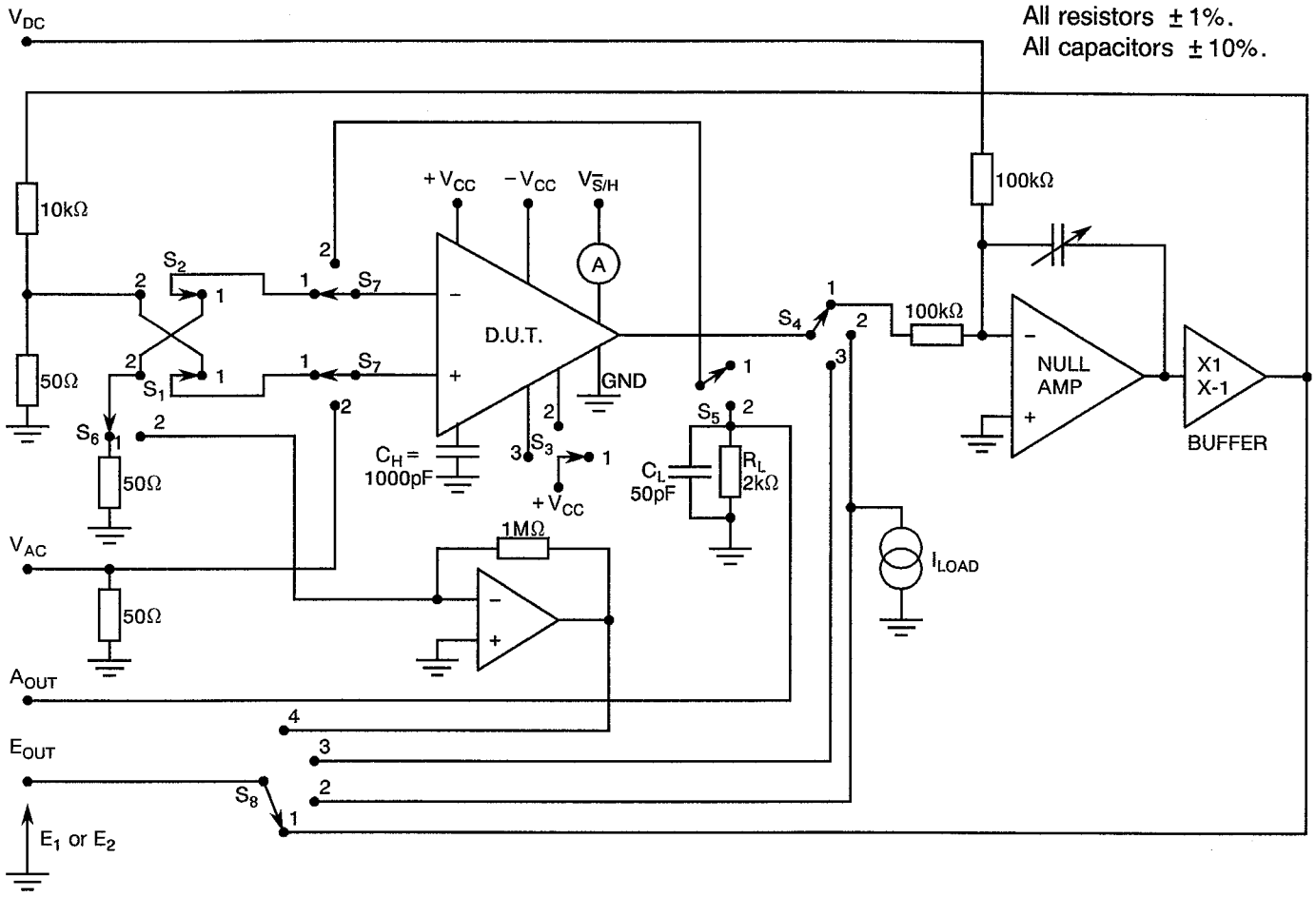
NOTES

1. Measure voltage E_1.

$$V_{IO} = \frac{E_1}{200}$$

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(b) - INPUT OFFSET AND BIAS CURRENTS



SWITCH POSITION							
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
-	-	1	1	1	2	1	4

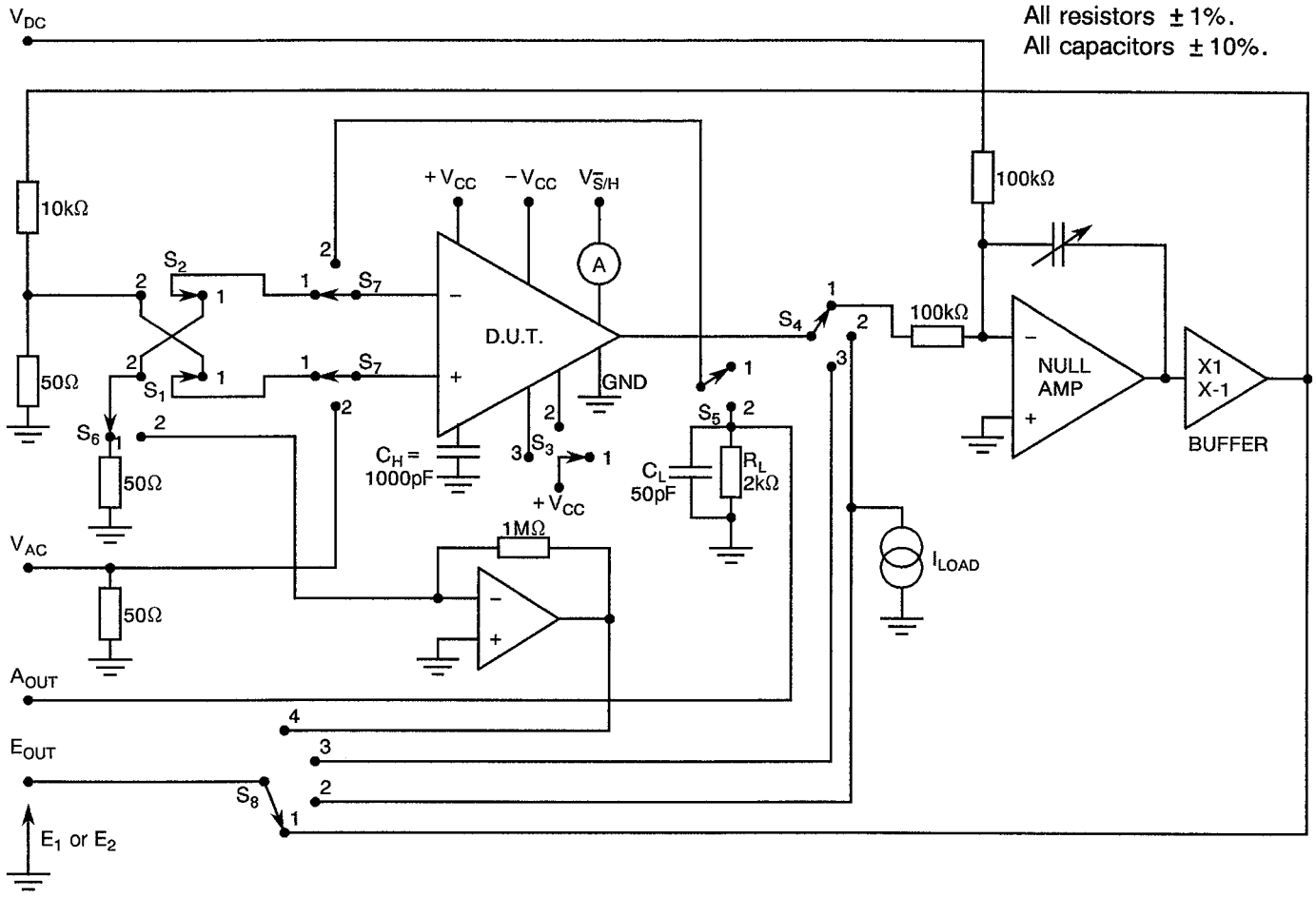
NOTES

1. Measure E_1, when S_1 and S_2 are in position 2. $+I_{IB} = \frac{E_1}{10^6}$ $I_{IO} = \frac{E_1 - E_2}{10^6}$

2. Measure E_2, when S_1 and S_2 are in position 1. $-I_{IB} = \frac{E_2}{10^6}$

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(c) - MAXIMUM OUTPUT VOLTAGE SWING



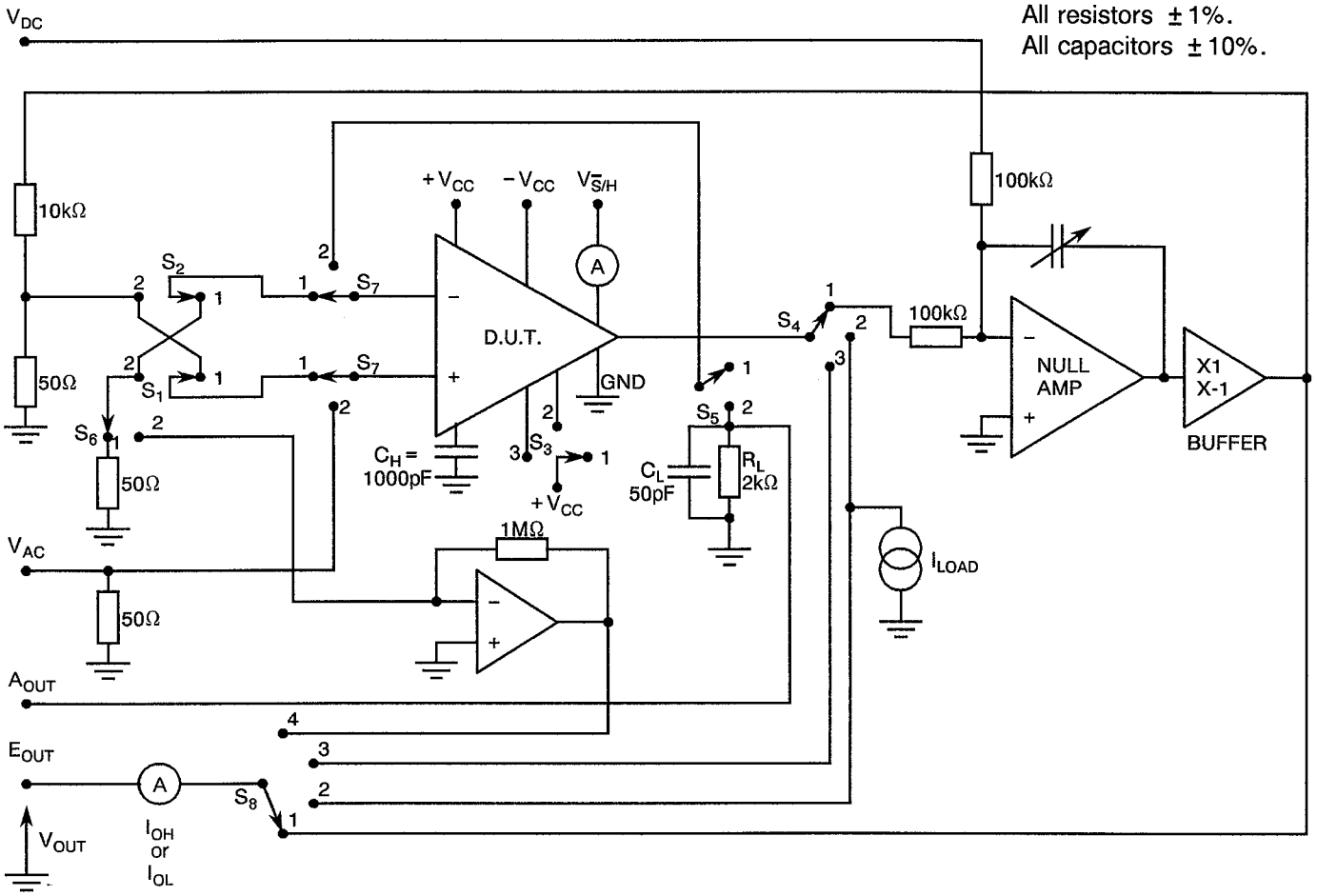
SWITCH POSITION							
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
1	1	1	3	2	1	1	3

NOTES

1. Measure E_1 when $V_{DC} = -14V$. $+V_{OP} = E_1$
2. Measure E_2 when $V_{DC} = +14V$. $-V_{OP} = E_2$

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(d) - OUTPUT CURRENT



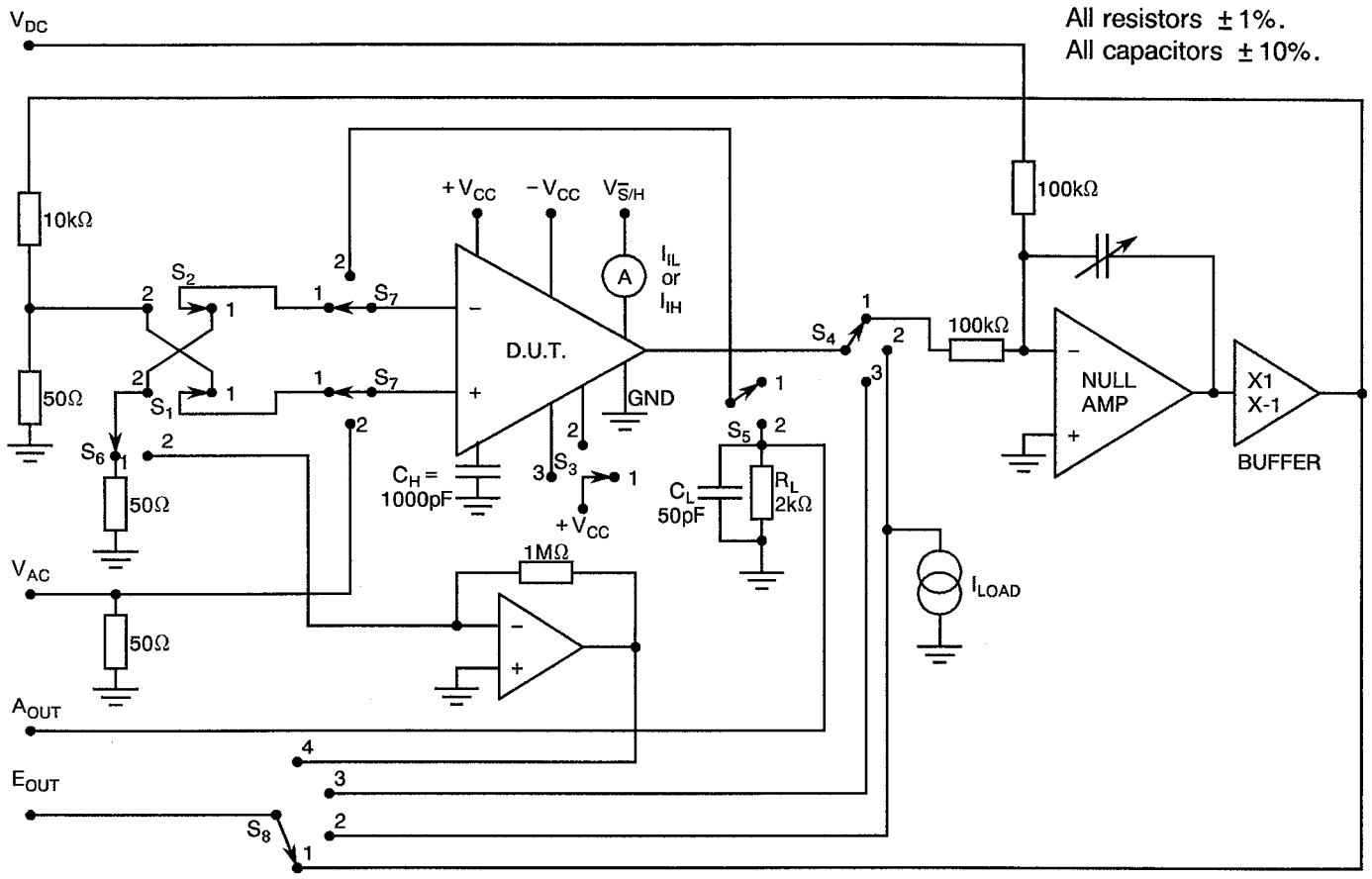
SWITCH POSITION							
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
1	1	1	3	1	1	1	3

NOTES

1. Measure I_{OH}, when $V_{DC} = -13V$ and $V_{OUT} = +10V$.
2. Measure I_{OL}, when $V_{DC} = +13V$ and $V_{OUT} = -10V$.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(e) - DIGITAL INPUT CURRENT



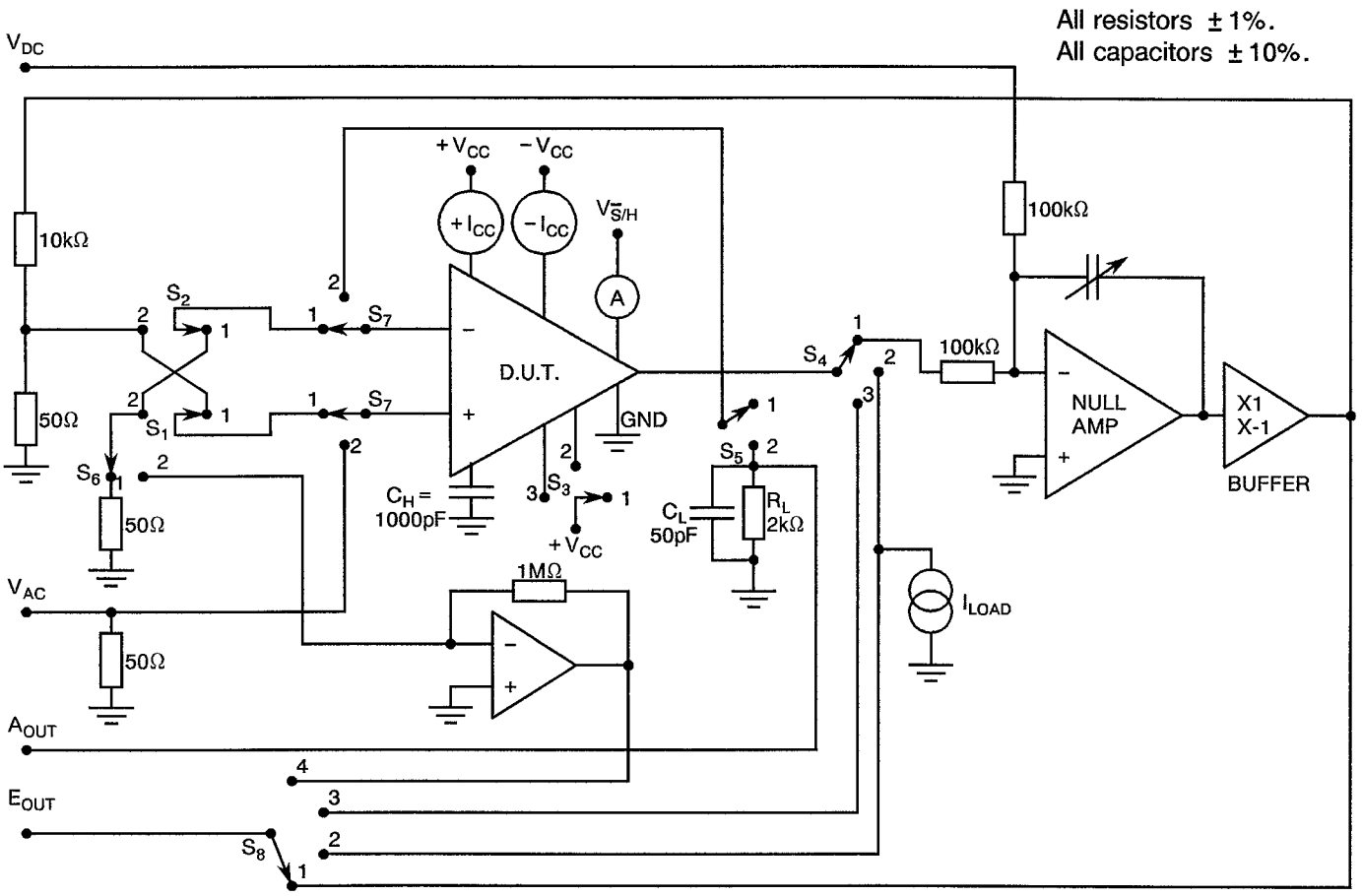
SWITCH POSITION							
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
1	1	1	1	1	1	1	1

NOTES

1. Measure I_{IL} when $V_{\overline{S}/H} = 0V$.
2. Measure I_{IH} when $V_{\overline{S}/H} = 5.0V$.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(f) - POWER SUPPLY CURRENT



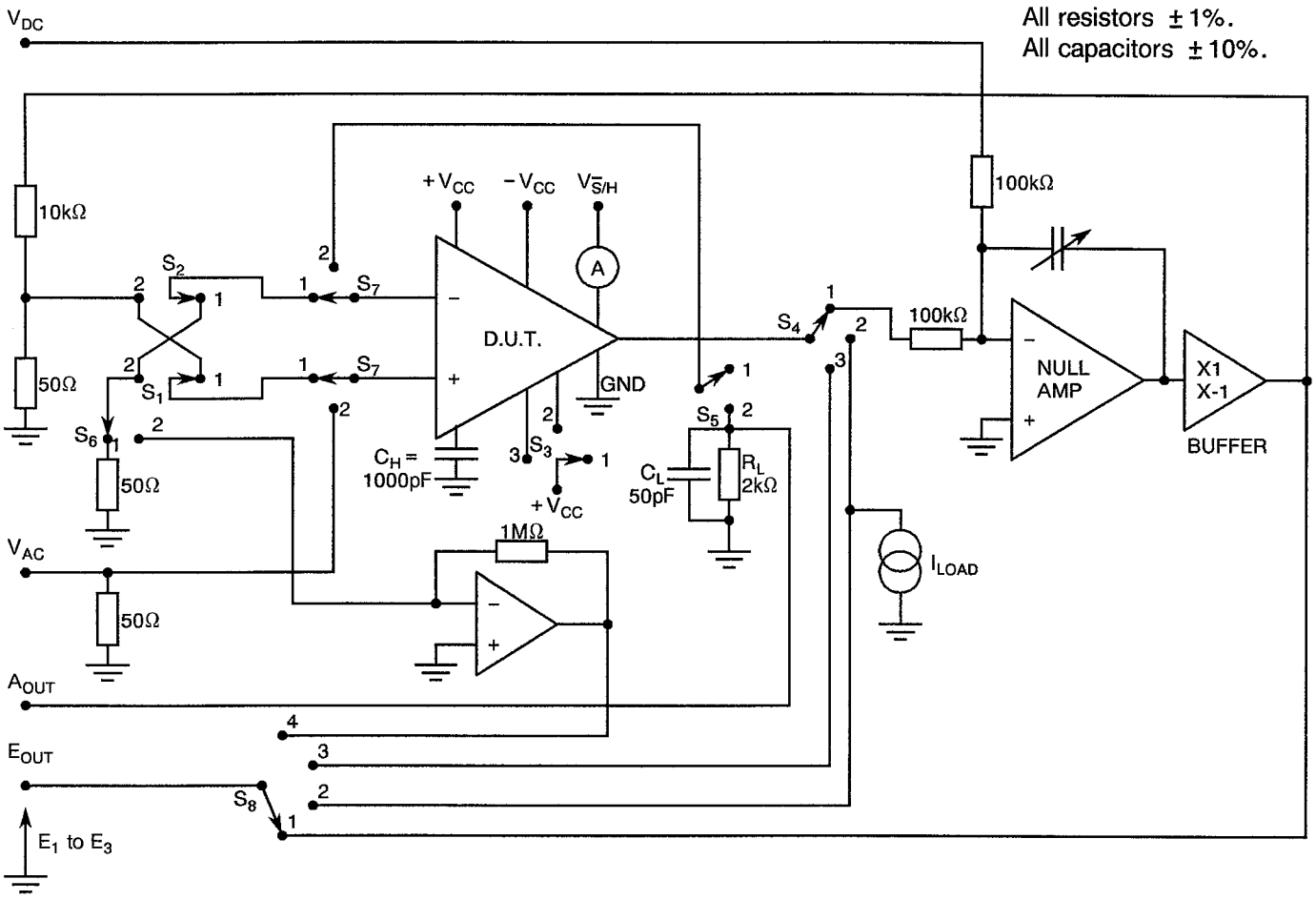
SWITCH POSITION							
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
1	1	1	1	1	1	1	1

NOTES

1. Measure $+I_{CC}$ and $-I_{CC}$.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(g) - OPEN LOOP VOLTAGE GAIN



SWITCH POSITION							
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
1	1	1	1	2	1	1	1

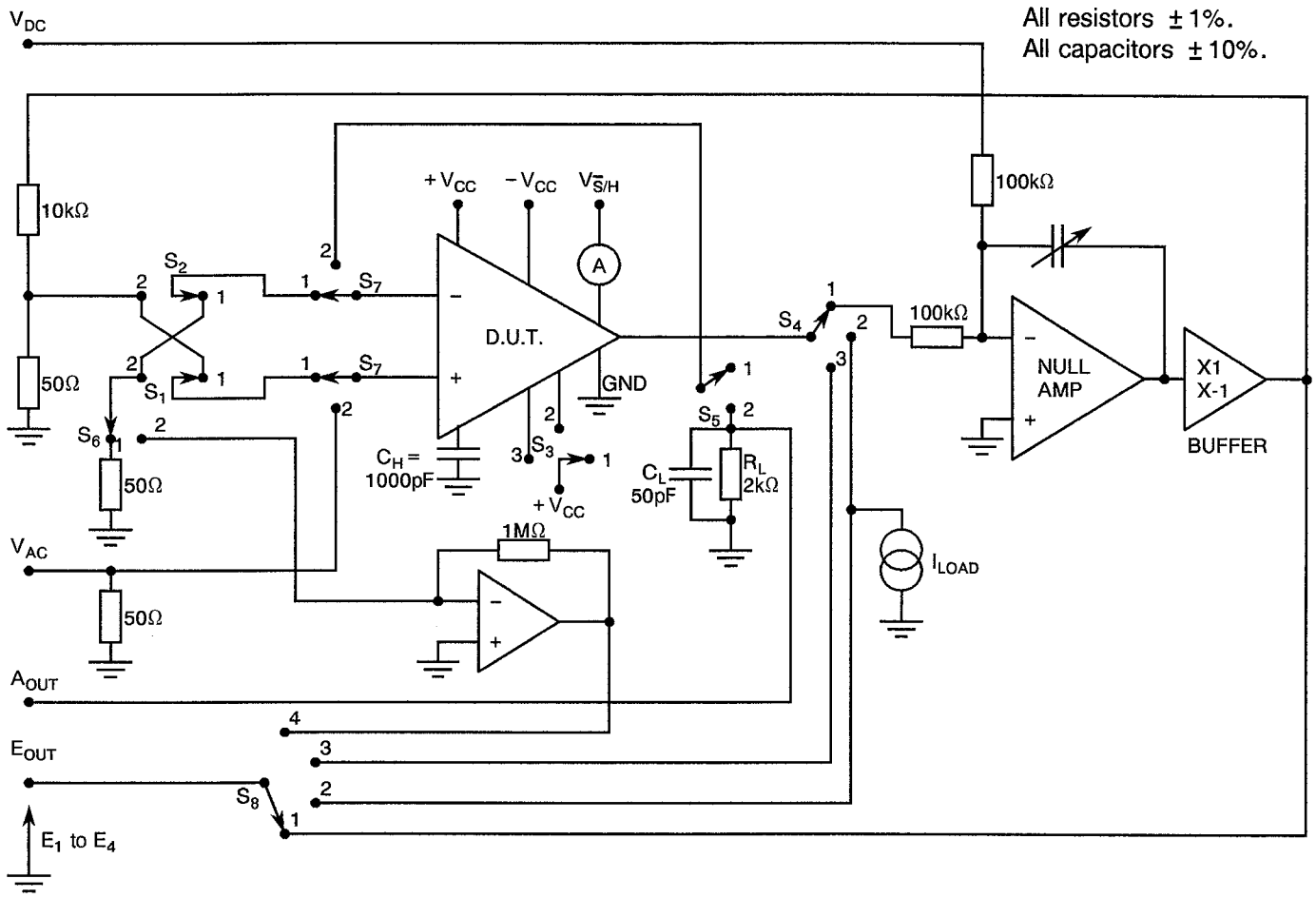
NOTES

1. Measure E_1 when $V_{DC} = 0V$.
2. Measure E_2 when $V_{DC} = -10V$.
3. Measure E_3 when $V_{DC} = +10V$.

$$+A_{VS} = 20\text{Log}_{10}\ \frac{E_1 - E_2}{200} \qquad -A_{VS} = 20\text{Log}_{10}\ \frac{E_1 - E_3}{200}$$

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(h) - POWER SUPPLY REJECTION RATIO



SWITCH POSITION							
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
1	1	1	1	1	1	1	1

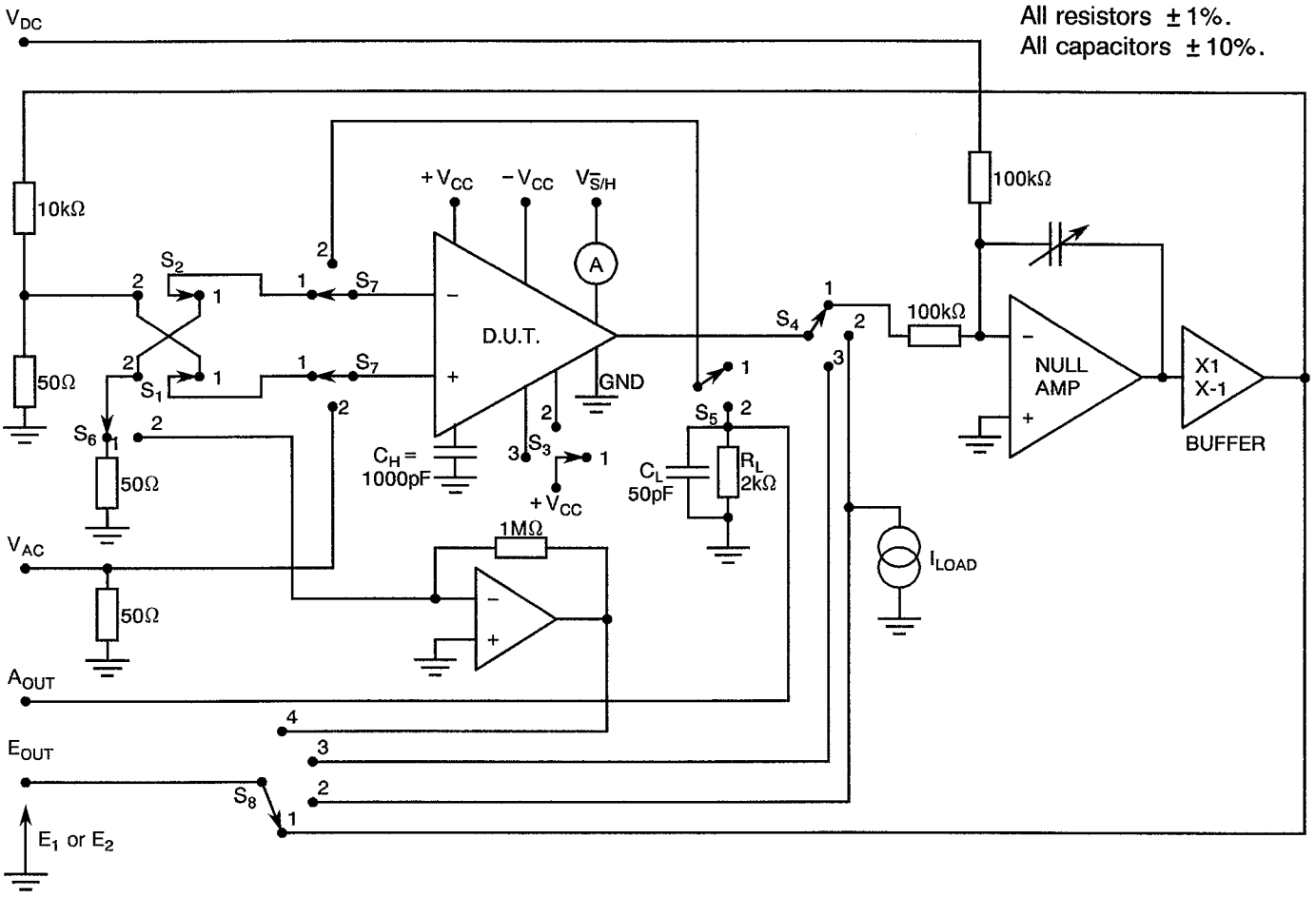
NOTES

1. Measure E_1 when $+V_{CC} = +10V$ and $-V_{CC} = -15V$.
2. Measure E_2 when $+V_{CC} = +20V$ and $-V_{CC} = -15V$.
3. Measure E_3 when $+V_{CC} = +15V$ and $-V_{CC} = -10V$.
4. Measure E_4 when $+V_{CC} = +15V$ and $-V_{CC} = -20V$.

$$+PSRR = 20Log_{10} \frac{2 \times 10^3}{E_1 - E_2} \qquad -PSRR = 20Log_{10} \frac{2 \times 10^3}{E_3 - E_4}$$

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - COMMON MODE REJECTION RATIO



SWITCH POSITION							
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
1	1	1	1	1	1	1	1

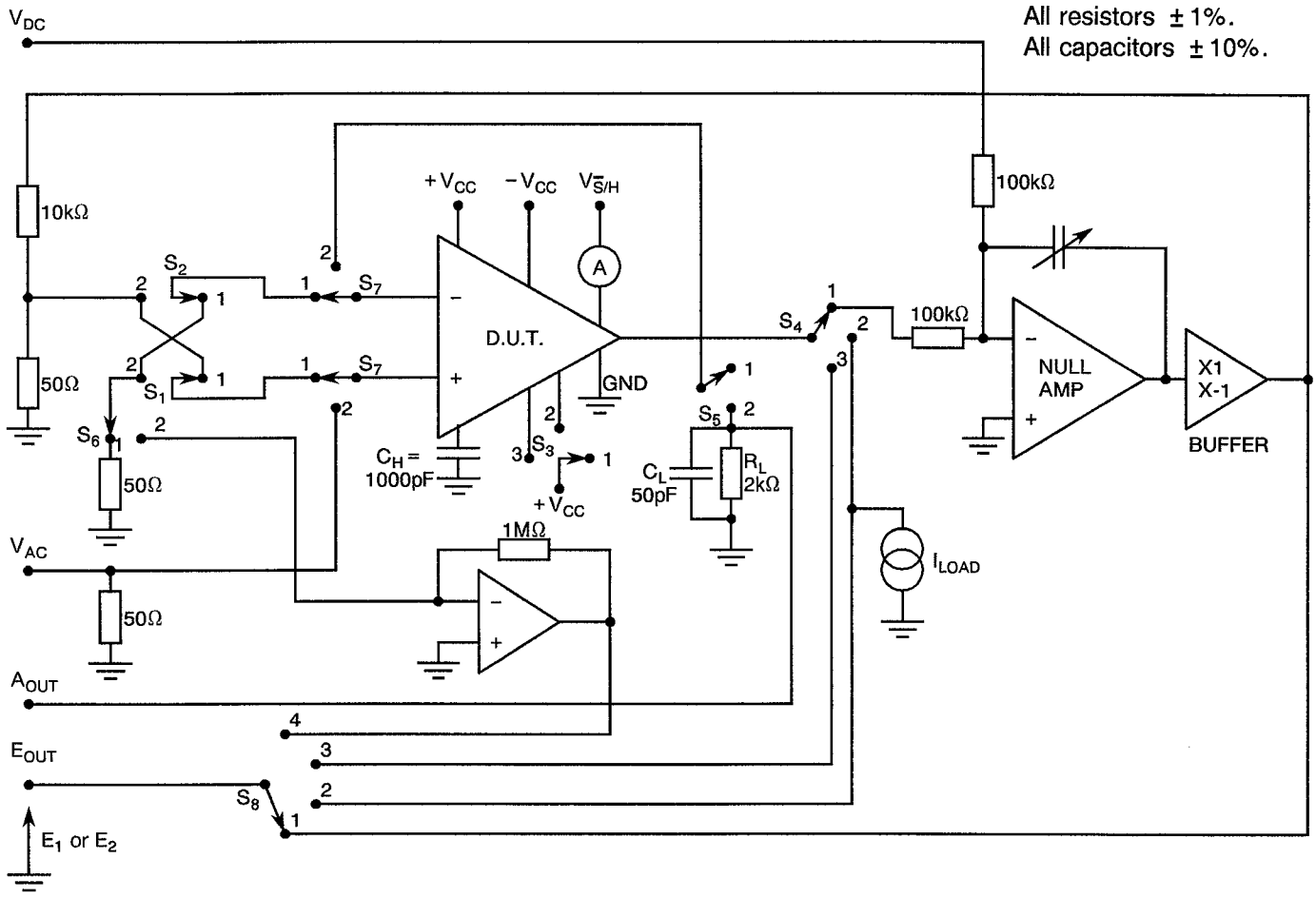
NOTES

1. Measure E_1 when $+V_{CC} = +25V$, $-V_{CC} = -5.0V$, $V_{DC} = -10V$ and $V_{\overline{S/H}} = 10.8V$.
2. Measure E_2 when $+V_{CC} = +5.0V$, $-V_{CC} = -25V$, $V_{DC} = +10V$ and $V_{\overline{S/H}} = -9.2V$.

$$+CMRR = 20\text{Log}_{10} \frac{2.10^3}{V_{IO} - E_1} \qquad -CMRR = 20\text{Log}_{10} \frac{2.10^3}{V_{IO} - E_2}$$

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(j) - DRIFT CURRENT



SWITCH POSITION							
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
1	1	1	3	2	1	2	1

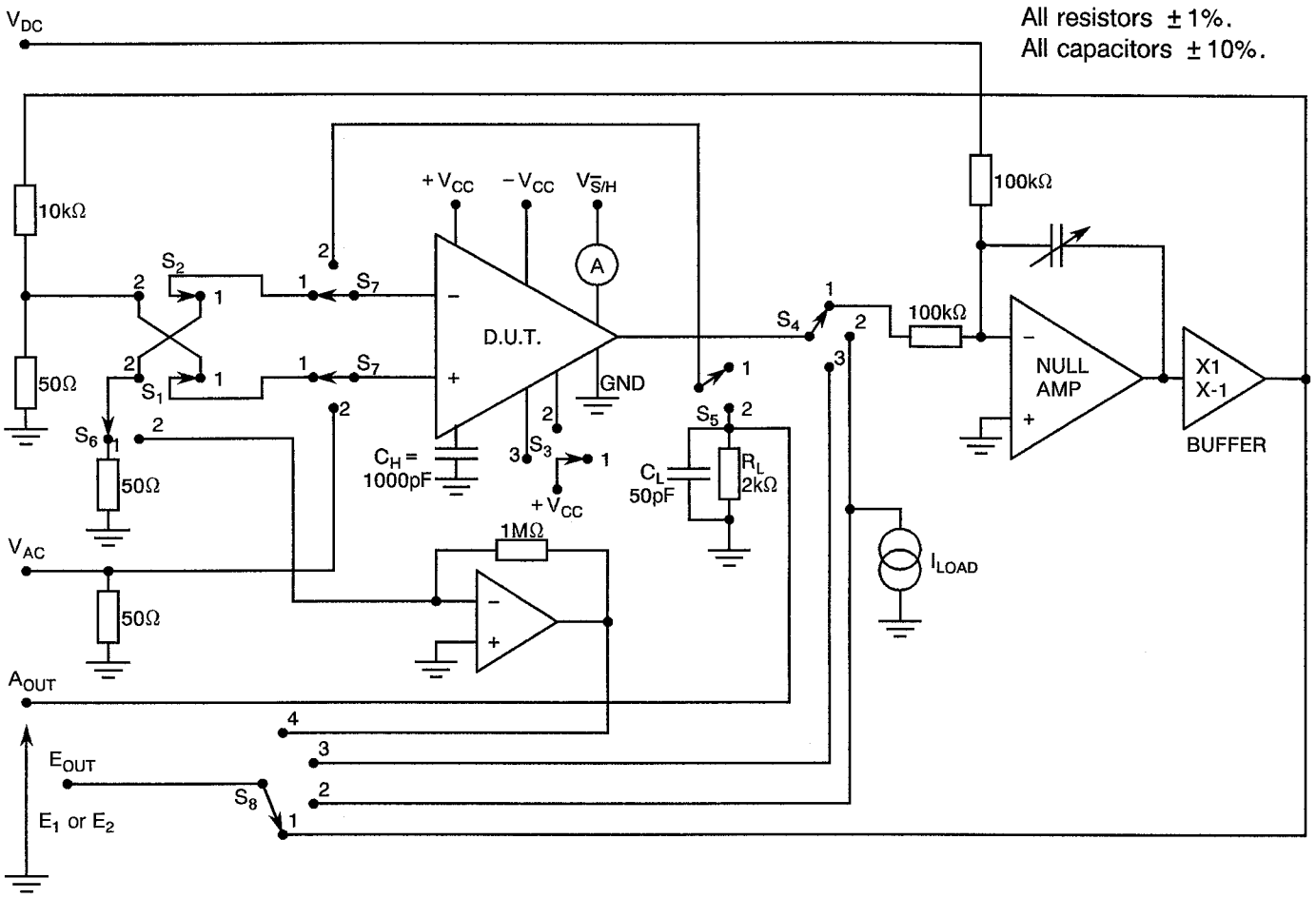
NOTES

1. $\Delta E = E_2 - E_1$, where E_1 is measured at t_1 and E_2 is measured at t_2.
2. $\Delta T = t_2 - t_1 = 0.1$ seconds.

$$I_D = C_H \times \frac{\Delta E}{\Delta T}$$

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(k) - HOLD STEP ERROR



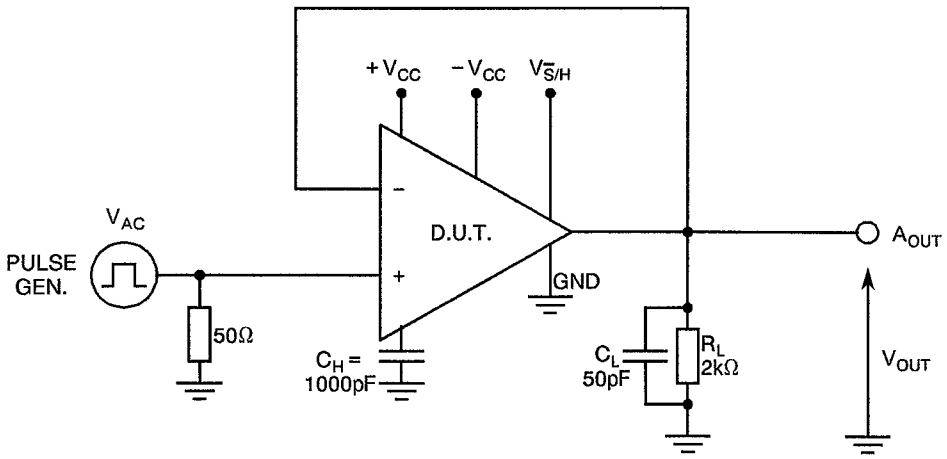
SWITCH POSITION							
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
1	1	1	3	2	1	2	1

NOTES

1. t_r ($V_{\overline{S/H}}$ = 0V to $V_{\overline{S/H}}$ = 4.0V) = 30ns.
2. Measure E_1 when $V_{\overline{S/H}}$ = 0V and measure E_2 at $V_{\overline{S/H}}$ = 4.0V. $V_{error} = |E_1 - E_2|$

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(I) - DYNAMIC TEST MEASUREMENT CIRCUIT

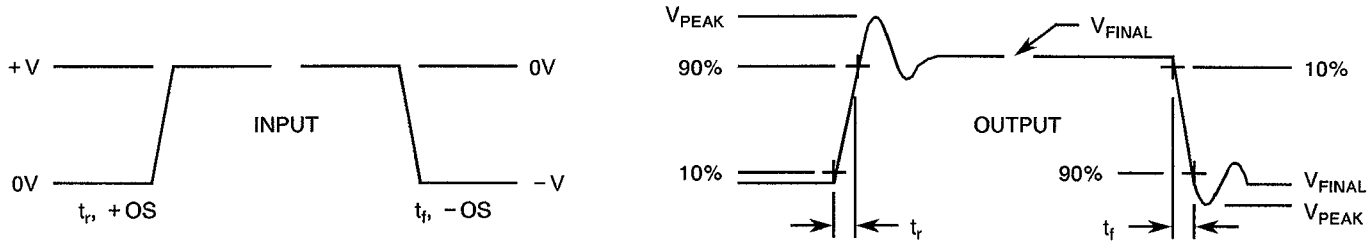


NOTES

1. Pulse Generator, rise time ≤ 10ns, repetition rate 1.0kHz (max.).
2. V_{OUT} = 200mV peak-to-peak for rise time, fall time and overshoot measurements.
3. V_{OUT} = 10V for slew rate measurements.

$$OS = \left| \frac{V_{PEAK} - V_{FINAL}}{V_{FINAL}} \right| \times 100 \qquad SR = \left| \frac{\Delta V}{\Delta t} \right|$$

OVERSHOOT, RISE AND FALL TIME WAVEFORMS



SLEW RATE WAVEFORMS

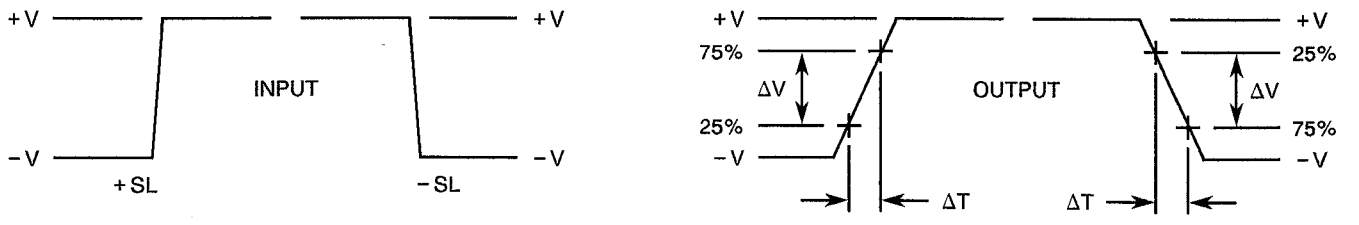


TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
1	Input Offset Voltage	V_{IO}	As per Table 2	As per Table 2	±2.0	mV
3	Input Bias Current (Plus)	$+I_{IB}$	As per Table 2	As per Table 2	±75	nA
4	Input Bias Current (Minus)	$-I_{IB}$	As per Table 2	As per Table 2	±75	nA

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

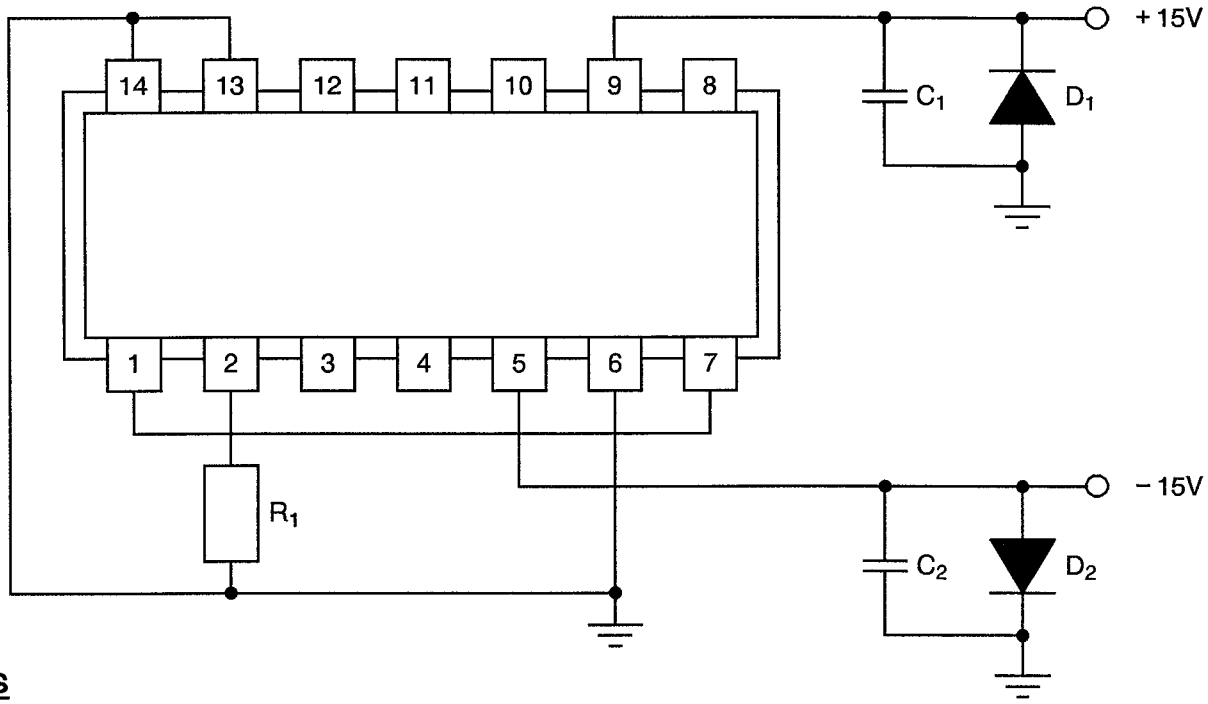
TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+10−0)	°C
2	Power Supply Voltage	V_{CC}	±15	V
3	Input Voltage	V_{IN}	0	V

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



NOTES

1. $R_1 = 100k\Omega \pm 5\%$.
2. $C_1 = C_2 = 0.01\mu F$ (one per socket) or $0.1\mu F$ (one per row).
3. $D_1 = D_2 = 1N4002$ or equivalent.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(b) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	ABSOLUTE		UNIT
					MIN.	MAX.	
1	Input Offset Voltage	V_{IO}	As per Table 2	As per Table 2	−4.5	+4.5	mV
2	Input Offset Current	I_{IO}	As per Table 2	As per Table 2	−50	+50	nA
3	Input Bias Current (Plus)	$+I_{IB}$	As per Table 2	As per Table 2	−200	+200	nA
4	Input Bias Current (Minus)	$-I_{IB}$	As per Table 2	As per Table 2	−200	+200	nA
5	Output Voltage Swing (Plus)	$+V_{OP}$	As per Table 2	As per Table 2	+10	-	V
6	Output Voltage Swing (Minus)	$-V_{OP}$	As per Table 2	As per Table 2	-	−10	V
7	Output Current High Level	I_{OH}	As per Table 2	As per Table 2	+14	-	mA
8	Output Current Low Level	I_{OL}	As per Table 2	As per Table 2	−14	-	mA
9	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	-	0.8	mA
10	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	-	20	µA
11	Power Supply Current (Plus)	$+I_{CC}$	As per Table 2	As per Table 2	-	6.0	mA
12	Power Supply Current (Minus)	$-I_{CC}$	As per Table 2	As per Table 2	−3.5	-	mA
13	Open Loop Voltage Gain (Plus)	$+A_{VS}$	As per Table 2	As per Table 2	25	-	V/mV
14	Open Loop Voltage Gain (Minus)	$-A_{VS}$	As per Table 2	As per Table 2	25	-	V/mV
15	Power Supply Rejection Ratio (Plus)	+PSRR	As per Table 2	As per Table 2	80	-	dB
16	Power Supply Rejection Ratio (Minus)	−PSRR	As per Table 2	As per Table 2	80	-	dB
17	Common Mode Rejection Ratio (Plus)	+CMRR	As per Table 2	As per Table 2	80	-	dB
18	Common Mode Rejection Ratio (Minus)	−CMRR	As per Table 2	As per Table 2	80	-	dB

APPENDIX 'A'

AGREED DEVIATIONS FOR HARRIS-SEMICONDUCTOR (USA)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.1	(a) Para. 5.2.1, ESA/SCC No. 21400 (S.E.M. Inspection) may be replaced by MIL-STD-883, Test Method 2018.
Para. 4.2.2	(a) Para. 9.1, ESA/SCC No. 20400 (Internal Visual Inspection) may be replaced by MIL-STD-883, Test Method 2010, Condition 'A'. (b) Para. 9.9.3, Electrical Measurements at Room Temperature may be performed at $T_{amb} = +25(+3-5)$ °C. (c) Para. 9.9.2, Electrical Measurements at High and Low Temperatures may be performed at $T_{amb} = +125 \pm 3$ °C and -55 ± 3 °C respectively. (d) Para. 9.4, Marking may be performed in Chart III after Electrical Measurements at High and Low Temperatures, but prior to Seal Test. Serialisation shall be performed in Chart II. (e) Para. 9.10, ESA/SCC No. 20500 (External Visual Inspection) may be replaced by MIL-STD-883, Test Method 2009. (f) Para. 9.11, Dimension Check may be performed in accordance with MIL-STD-2016.
Para. 4.2.3	(a) Para. 9.1.1, Parameter Drift Value Measurements may be performed at $T_{amb} = +25(+3-5)$ °C. (b) Para. 9.9.2, Electrical Measurements at High and Low Temperatures may be performed at $T_{amb} = +125 \pm 3$ °C and -55 ± 3 °C respectively. (c) Para. 9.9.3, Electrical Measurements at Room Temperature may be performed at $T_{amb} = +25(+3-5)$ °C. (d) Para. 9.12, ESA/SCC No. 20900 (Radiographic Inspection) may be replaced by MIL-STD-883, Test Method 2012. (e) Para. 9.10, ESA/SCC No. 20500 (External Visual Inspection) may be replaced by MIL-STD-883, Test Method 2009. (f) Visual rejects resulting from dip soldering which are not acceptable according to Para. 4.8 of ESA/SCC No. 20500 will not be included in P.D.A. calculations. These components will be kept available for final Customer inspection.
Para. 4.2.4	(a) Para. 9.9.4, Electrical Measurements during Environmental, Mechanical and Endurance Testing may be performed at $T_{amb} = +25(+3-5)$ °C. (b) Para. 9.10, ESA/SCC No. 20500 (External Visual Inspection) may be replaced by MIL-STD-883, Test Method 2009. (c) Para. 9.19, ESA/SCC No. 24800 (Permanence of Marking) may be replaced by MIL-STD-883, Test Method 2015.

APPENDIX 'A'

AGREED DEVIATIONS FOR HARRIS-SEMICONDUCTOR (USA)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.5	(a) Para. 9.9.2, Electrical Measurements at High and Low Temperatures may be performed at $T_{amb} = +125 \pm 3$ °C and -55 ± 3 °C respectively. (b) Para. 9.9.3, Electrical Measurements at Room Temperature may be performed at $T_{amb} = +25(+3-5)$ °C. (c) Para. 9.4.4, Electrical Measurements during Environmental, Mechanical and Endurance Testing may be performed at $T_{amb} = +25(+3-5)$ °C. (b) Para. 9.10, ESA/SCC No. 20500 (External Visual Inspection) may be replaced by MIL-STD-883, Test Method 2009. (c) Para. 9.19, ESA/SCC No. 24800 (Permanence of Marking) may be replaced by MIL-STD-883, Test Method 2015.