INTEGRATED CIRCUITS, SILICON MONOLITHIC,

JFET INPUT OPERATIONAL AMPLIFIER

BASED ON TYPES LF155, LF155A, LF156,

LF156A, LF157

ESCC Detail Specification No. 9101/017

ISSUE 1

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ESA/SCC Detail Specification No. 9101/017

space components
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FIGURES

APPENDICES (Applicable to specific Manufacturers only)
None.

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, JFET Input Operational Amplifier, based on Types LF155, LF155A, LF156, LF156A and LF157. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduld in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The parameter derating information of the integrated circuits specified herein is shown in Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the integrated circuits specified herein are shown in Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

Not applicable.

1.8 CIRCUIT SCHEMATIC

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as class 1 with a Minimum Critical Path Failure Voltage of 1000 Volts.

TABLE 1(a) - TYPE VARIANTS

VARIANT	TYPE	CASE	FIGURE	LEAD MATERIAL AND FINISH
01	LF155	TO99	2	D9
02	LF156	TO99	2	D9
03	LF157	TO99	2	D9
04	LF155A	TO99	2	D9
05	LF156A	TO99	2	D9

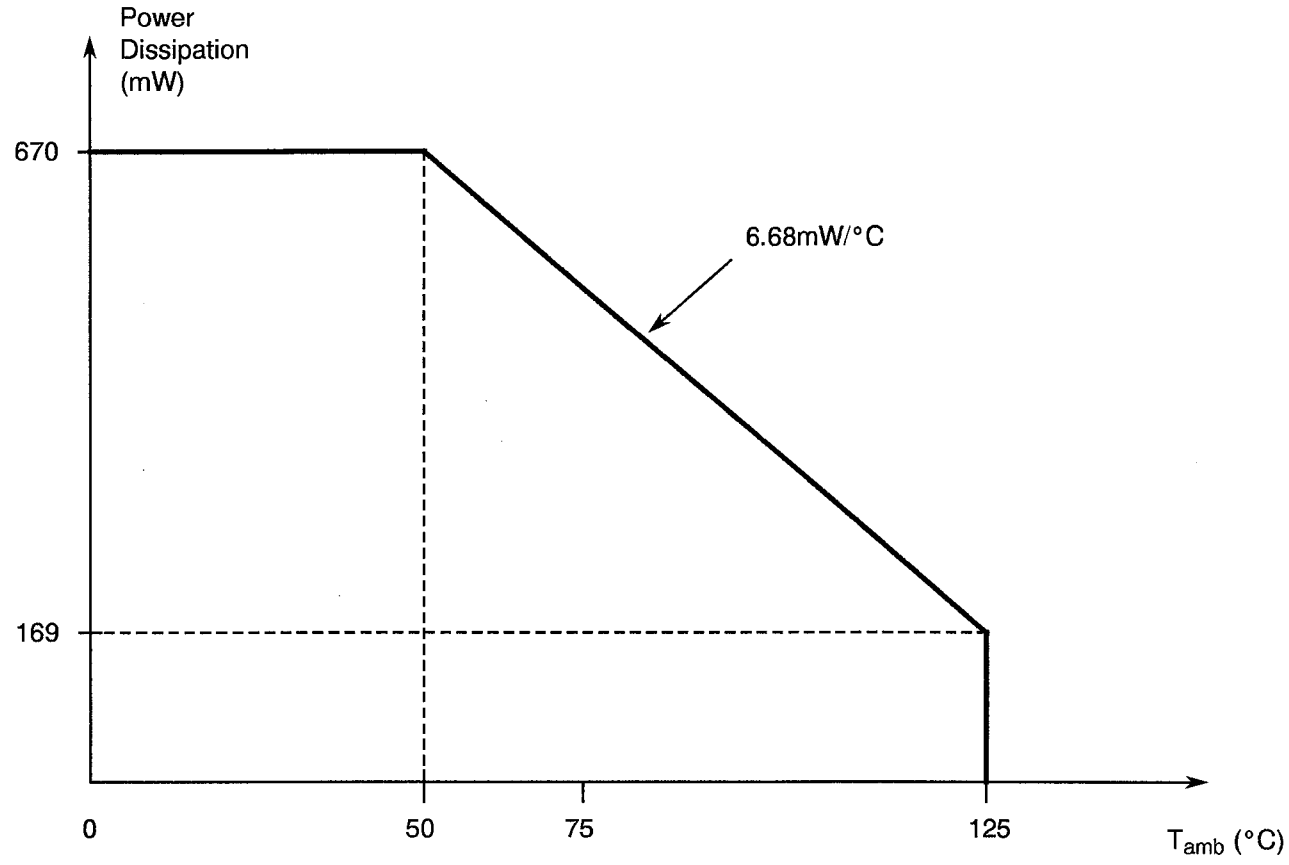
TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNITS	REMARKS
1	Supply Voltage Range	V_{CC}	±22	V	
2	Differential Input Voltage Range	V_{ID}	±40	V	Note 1
3	Input Voltage Range	V_{IN}	±20	V	Note 2
4	Device Power Dissipation (Continuous)	P_D	670	mW	Note 3
5	Operating Temperature Range	T_{op}	−55 to +125	°C	
6	Storage Temperature Range	T_{stg}	−65 to +150	°C	
7	Soldering Temperature	T_{sol}	+300	°C	Note 4
8	Junction Temperature	T_j	+150	°C	

NOTES

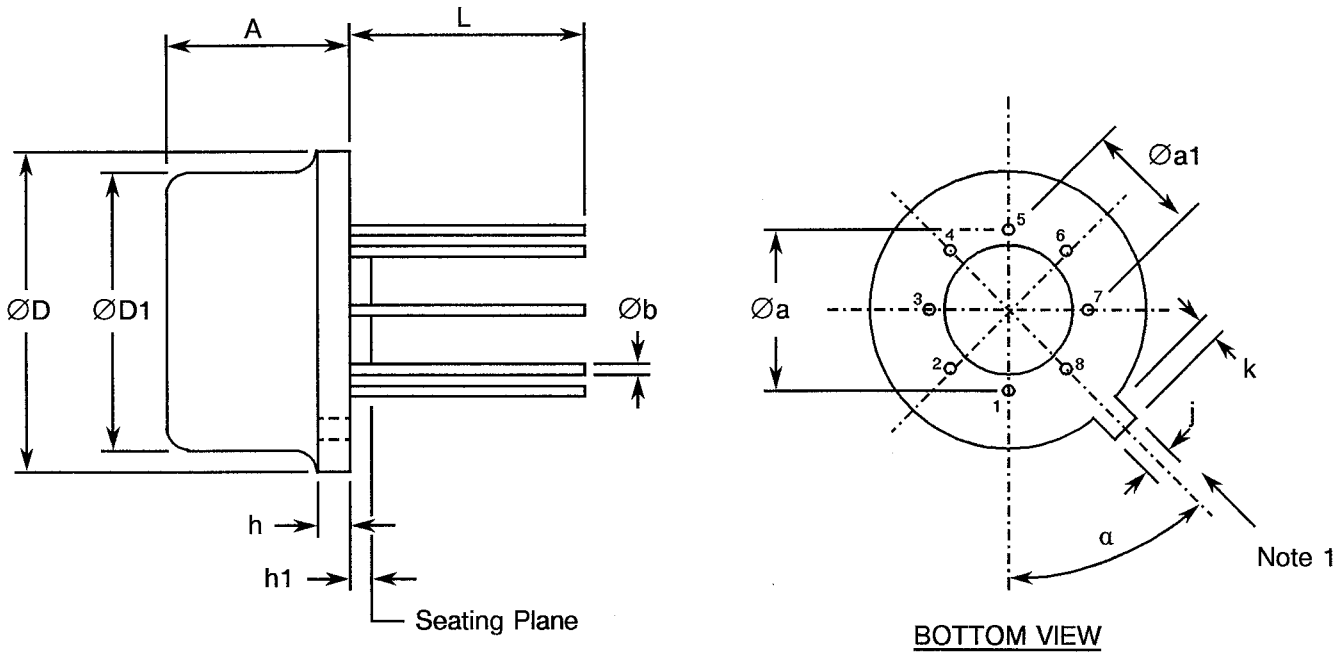
1. The inputs are shunted with back-to-back diodes for overvoltage protection.
2. If the supply voltage is less than −15V, the maximum input voltage is equal to the supply voltage.
3. At T_{amb} = +50°C. For derating at T_{amb} > +50°C, see Figure 1.
4. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION



Power Dissipation versus Temperature

FIGURE 2 - PHYSICAL DIMENSIONS - TO99 PACKAGE

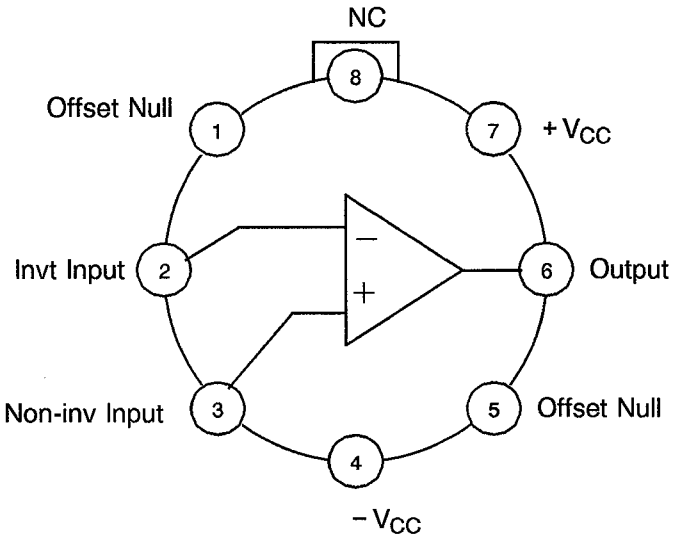


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
Øa	5.08 TYPICAL		
Øa1	3.56	4.06	
A	4.19	4.70	
Øb	0.41	0.48	2
ØD	8.51	9.40	
ØD1	7.75	8.51	
h	-	1.02	
h1	0.25	1.14	3
j	0.71	0.86	
k	0.68	1.14	
L	12.70	-	
α	45° TYPICAL		4

NOTES

1. Reference index on Pin 8.
2. All leads or terminals.
3. The dimension shall be measured from the seating plane to the base plane.
4. 8 spaces.

FIGURE 3(a) - PIN ASSIGNMENT

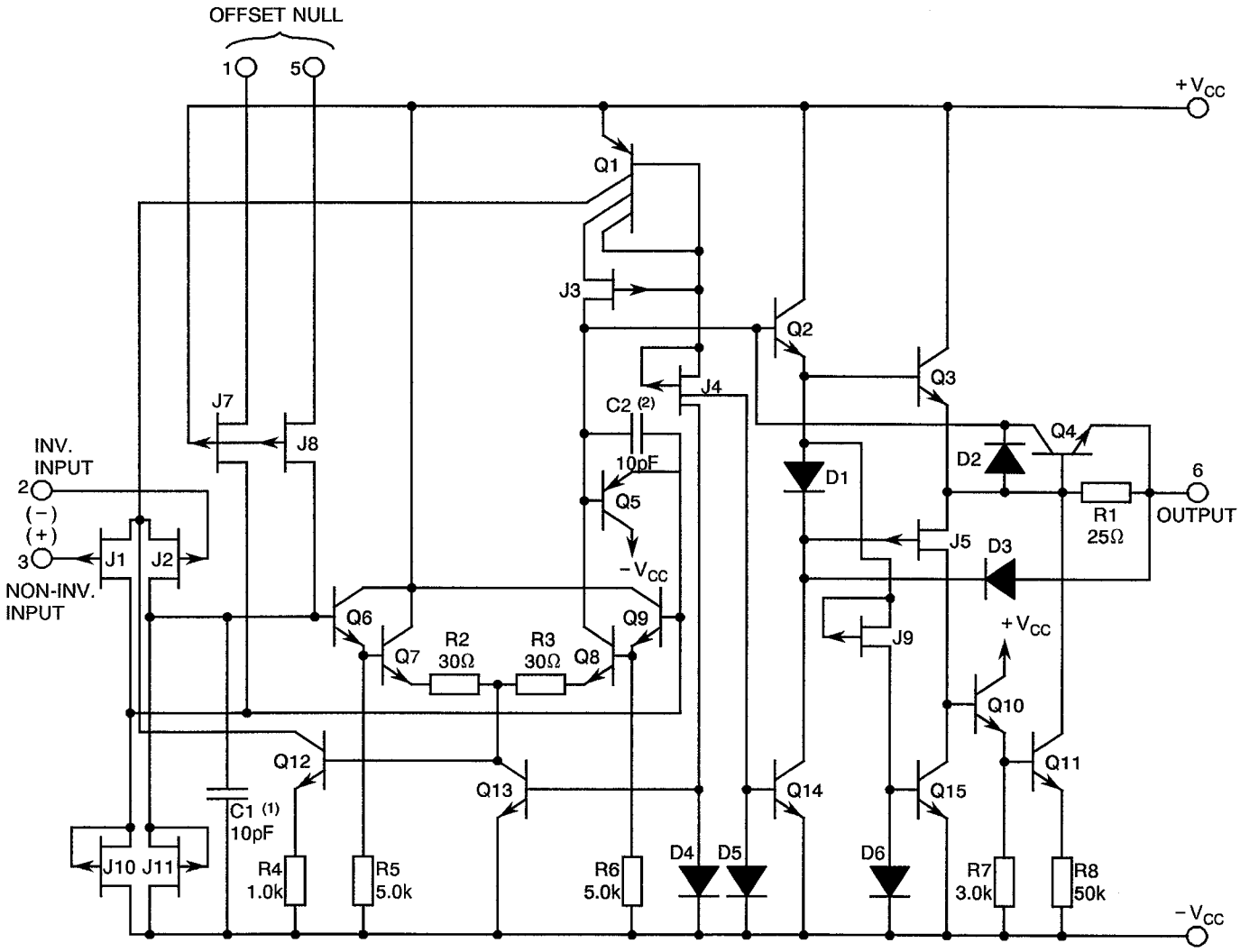


TOP VIEW

FIGURE 3 (b) - TRUTH TABLE

Not applicable.

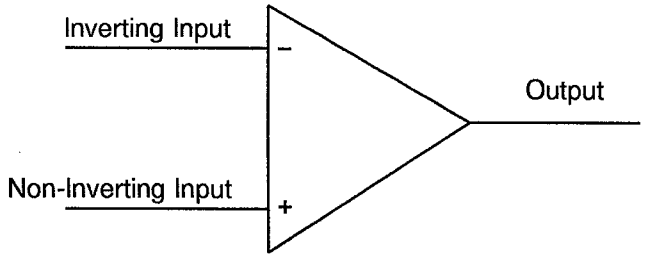
FIGURE 3(c) - CIRCUIT SCHEMATIC



NOTES

1. C1 = 5.0pF for LF157.
2. C2 = 2.0pF for LF157.

FIGURE 3(d) - FUNCTIONAL DIAGRAM



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

V_{CC} : Supply Voltage of the device under test.

AV : Gain of the device under test.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

(a) Para. 7.1.1(a), "High Temperature Reverse Bias" test and subsequent electrical measurements related to this test shall be omitted.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 1.5 grammes.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals and the lids shall be welded.

4.4.2 Lead Material and Finish

The lead material shall be Type 'D' with Type '9' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500.

4.5 MARKING

4.5.1 General

The marking of components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700 and the following paragraphs. When the component is too small to accomodate all of the marking specified, as much as space permits shall be marked and the marking information, in full, shall accompany the component in its primary package.

The information to be marked and the order of precedence, shall be as follows:

(a) Lead Identification.

(b) The SCC Component Number.

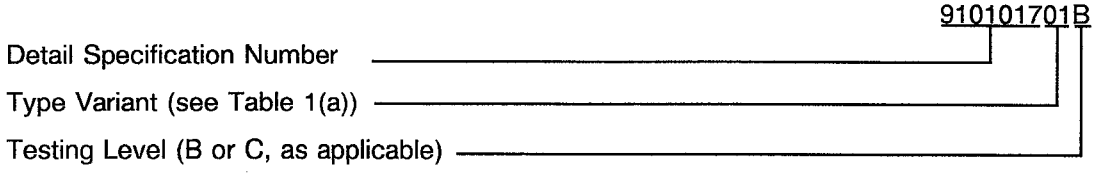
(c) Traceability Information.

4.5.2 Lead Identification

A tab shall be located at the edge of the package to identify Pin No. 8, in the position defined in Note 1 to Figure 2. The pin numbering shall be read with the tab on the left-hand side (bottom view).

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125\ (+0\ -5)$°C and $-55\ (+5\ -0)$°C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits and test sequences for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-In

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for power burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for High Temperature Reverse Bias Burn-in

Not applicable.

4.7.5 Electrical Circuits for Power Burn-in

Circuits for use in performing the power burn-in tests are shown in Figure 5(b) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
1	Input Offset Voltage	V_{IO1}	4001	4(a)	$+V_{CC} = +20V, -V_{CC} = -20V$ Variants 01, 02, 03 Variants 04, 05	 −5.0 −2.0	 +5.0 +2.0	mV
2	Input Offset Voltage	V_{IO2}	4001	4(a)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ Variants 01, 02, 03 Variants 04, 05	 −5.0 −2.0	 +5.0 +2.0	mV
3	Input Offset Current	I_{IO1}	4001	4(b)	$+V_{CC} = +20V, -V_{CC} = -20V$ Variants 01, 02, 03 Variants 04, 05	 −20 −10	 +20 +10	pA
4	Input Offset Current	I_{IO2}	4001	4(b)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ Variants 01, 02, 03 Variants 04, 05	 −20 −10	 +20 +10	pA
5	Input Bias Current (Plus)	$+I_{IB1}$	4001	4(c)	$+V_{CC} = +20V, -V_{CC} = -20V$ Variants 01, 02, 03 Variants 04, 05	 −100 −50	 +100 +50	pA
6	Input Bias Current (Plus)	$+I_{IB2}$	4001	4(c)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ Variants 01, 02, 03 Variants 04, 05	 −100 −50	 +100 +50	pA
7	Input Bias Current (Minus)	$-I_{IB1}$	4001	4(d)	$+V_{CC} = +20V, -V_{CC} = -20V$ Variants 01, 02, 03 Variants 04, 05	 −100 −50	 +100 +50	pA
8	Input Bias Current (Minus)	$-I_{IB2}$	4001	4(d)	$+V_{CC} = +5.0V$, $-V_{CC} = -5.0V$ Variants 01, 02, 03 Variants 04, 05	 −100 −50	 +100 +50	pA
9	Short Circuit Output Current (Plus)	$+I_{OS}$	3011	4(e)	$+V_{CC} = +15V, -V_{CC} = -15V$ $V_1 = -15V$ (1) Variants 01, 02, 03 Variant 04 Variant 05	 −60 −60 −60	 −20 −10 −15	mA
10	Short Circuit Output Current (Minus)	$-I_{OS}$	3011	4(e)	$+V_{CC} = +15V, -V_{CC} = -15V$ $V_1 = +15V$ (1) Variants 01, 02, 03 Variant 04 Variant 05	 +20 +10 +15	 +60 +60 +60	mA

NOTES: See Page 18.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
11	Output Voltage Swing (Plus)	$+V_{OP}$	4004	4(f)	$+V_{CC} = +15V, -V_{CC} = -15V$ $V_1 = -15V, R_L = 10k\Omega$	+12	-	V
12	Output Voltage Swing (Minus)	$-V_{OP}$	4004	4(f)	$+V_{CC} = +15V, -V_{CC} = -15V$ $V_1 = +15V, R_L = 10k\Omega$	-	−12	V
13	Power Supply Current	I_{CC}	4005	4(g)	$+V_{CC} = +20V, -V_{CC} = -20V$ Variants 01, 04 Variants 02, 03, 05	 - -	 4.0 7.0	mA
14	Open Loop Voltage Gain (Plus)	$+A_{VS}$	4004	4(h)	$+V_{CC} = +15V, -V_{CC} = -15V$ $V_1 = -10V, R_L = 2.0k\Omega$	50	-	V/mV
15	Open Loop Voltage Gain (Minus)	$-A_{VS}$	4004	4(h)	$+V_{CC} = +15V, -V_{CC} = -15V$ $V_1 = +10V, R_L = 2.0k\Omega$	50	-	V/mV
16	Power Supply Rejection Ratio (Plus)	+PSRR	4003	4(i)	$+V_{CC} = +10V, -V_{CC} = -20V$	85	-	dB
17	Power Supply Rejection Ratio (Minus)	−PSRR	4003	4(i)	$+V_{CC} = +20V, -V_{CC} = -10V$	85	-	dB
18	Common Mode Rejection Ratio (Plus)	+CMRR	4003	4(j)	$+V_{CC} = +15V, -V_{CC} = -15V$ $V_1 = -11V$	85	-	dB
19	Common Mode Rejection Ratio (Minus)	−CMRR	4003	4(j)	$+V_{CC} = +15V, -V_{CC} = -15V$ $V_1 = +11V$	85	-	dB

NOTES: See Page 18.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (NOTE 2)	LIMITS		UNIT
						MIN	MAX	
20	Slew Rate (Plus)	SR(+)	4002	4(k)	$+V_{CC} = +15V, -V_{CC} = -15V$ $V_{IN} = -2.0V$, to $+2.0V$ square AV = 5.0 Variants 01, 04 Variant 02 Variant 03 Variant 05	 3.0 7.5 30 10	 - - - -	V/µs
21	Slew Rate (Minus)	SR(−)	4002	4(k)	$+V_{CC} = +15V, -V_{CC} = -15V$ $V_{IN} = -2.0V$, to $+2.0V$ square AV = 5.0 Variants 01, 04 Variant 02 Variant 03 Variant 05	 3.0 7.5 30 10	 - - - -	V/µs
22	RiseTime	t_r	4002	4(k)	$+V_{CC} = +15V, -V_{CC} = -15V$ AV = 1.0, V_{IN} = 50 mV Variants 01, 02, 04, 05 AV = +5.0 , V_{IN} = 10 mV Variant 03	-	800	ns
23	Overshoot (Plus)	OS(+)	4002	4(k)	$+V_{CC} = +20V, -V_{CC} = -20V$ AV = 1.0, V_{IN} = 50 mV Variants 01, 02, 04, 05 AV = +5.0, V_{IN} = 10 mV Variant 03	-	20	%
24	Overshoot (Minus)	OS(−)	4002	4(k)	$+V_{CC} = +20V, -V_{CC} = -20V$ AV = 1.0, V_{IN} = 50 mV Variants 01, 02, 04, 05 AV = 5.0 , V_{IN} = 10 mV Variant 03	-	20	%
25	Gain Bandwidth	GB	-	4(k)	$+V_{CC} = +15V, -V_{CC} = -15V$ AV = 1.0 Variants 01, 04 Variants 02, 05 Variant 03	 2.0 4.0 15	 - - -	MHz

NOTES: See Page 18.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
1	Input Offset Voltage	V_{IO1}	4001	4(a)	$+V_{CC}$ = +20V, $-V_{CC}$ = −20V Variants 01, 02, 03 Variants 04, 05	 −7.0 −2.5	 +7.0 +2.5	mV
2	Input Offset Voltage	V_{IO2}	4001	4(a)	$+V_{CC}$ = +5.0V, $-V_{CC}$ = −5.0V Variants 01, 02, 03 Variants 04, 05	 −7.0 −2.5	 +7.0 +2.5	mV
3	Input Offset Current	I_{IO1}	4001	4(b)	$+V_{CC}$ = +20V, $-V_{CC}$ = −20V Variants 01, 02, 03 (3) Variants 01, 02, 03 (4) Variants 04, 05	 −10 −20 −10	 +10 +20 +10	nA
4	Input Offset Current	I_{IO2}	4001	4(b)	$+V_{CC}$ = +5.0V, $-V_{CC}$ = −5.0V Variants 01, 02, 03 (3) Variants 01, 02, 03 (4) Variants 04, 05	 −10 −20 −10	 +10 +20 +10	nA
5	Input Bias Current (Plus)	$+I_{IB1}$	4001	4(c)	$+V_{CC}$ = +20V, $-V_{CC}$ = −20V Variants 01, 02, 03, 04, 05 (3) Variants 01, 02, 03, 04, 05 (4)	 −25 −100	 +25 +100	 nA pA
6	Input Bias Current (Plus)	$+I_{IB2}$	4001	4(c)	$+V_{CC}$ = +5.0V, $-V_{CC}$ = −5.0V Variants 01, 02, 03, 04, 05 (3) Variants 01, 02, 03, 04, 05 (4)	 −25 −100	 +25 +100	 nA pA
7	Input Bias Current (Minus)	$-I_{IB1}$	4001	4(d)	$+V_{CC}$ = +20V, $-V_{CC}$ = −20V Variants 01, 02, 03, 04, 05 (3) Variants 01, 02, 03, 04, 05 (4)	 −25 −100	 +25 +100	 nA pA
8	Input Bias Current (Minus)	$-I_{IB2}$	4001	4(d)	$+V_{CC}$ = +5.0V, $-V_{CC}$ = −5.0V Variants 01, 02, 03, 04, 05 (3) Variants 01, 02, 03, 04, 05 (4)	 −25 −100	 +25 +100	 nA pA

NOTES: See Page 18.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES (CONT'D)

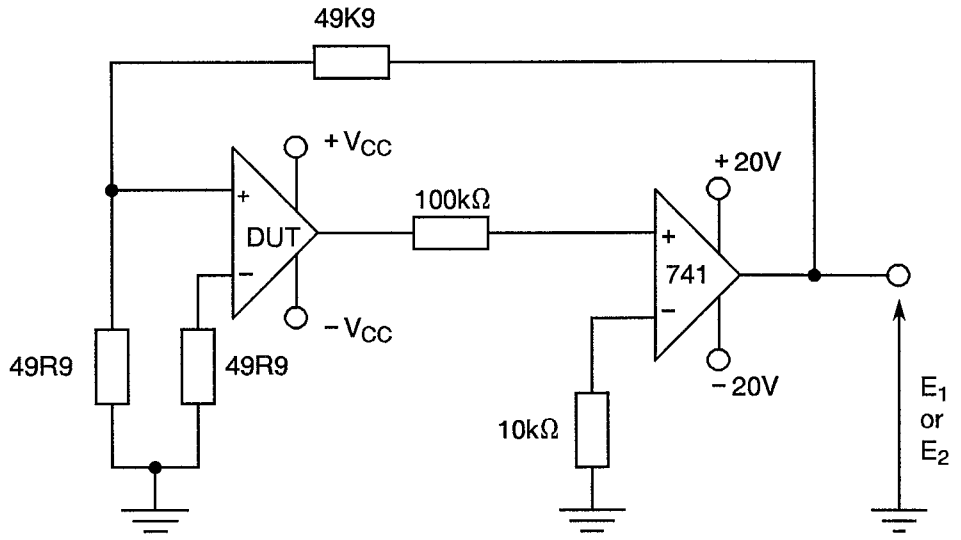
No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
11	Output Voltage Swing (Plus)	$+V_{OP}$	4004	4(f)	$+V_{CC} = +15V, -V_{CC} = -15V$ $V_I = -15V, R_L = 10k\Omega$	+12	-	V
12	Output Voltage Swing (Minus)	$-V_{OP}$	4004	4(f)	$+V_{CC} = +15V, -V_{CC} = -15V$ $V_I = +15V, R_L = 10k\Omega$	-	−12	V
14	Open Loop Voltage Gain (Plus)	$+A_{VS}$	4004	4(h)	$+V_{CC} = +15V, -V_{CC} = -15V$ $V_I = -10V, R_L = 2.0k\Omega$	25	-	V/mV
15	Open Loop Voltage Gain (Minus)	$-A_{VS}$	4004	4(h)	$+V_{CC} = +15V, -V_{CC} = -15V$ $V_I = +10V, R_L = 2.0k\Omega$	25	-	V/mV
16	Power Supply Rejection Ratio (Plus)	+PSRR	4003	4(i)	$+V_{CC} = +10V, -V_{CC} = -20V$	85	-	dB
17	Power Supply Rejection Ratio (Minus)	−PSRR	4003	4(i)	$+V_{CC} = +20V, -V_{CC} = -10V$	85	-	dB
18	Common Mode Rejection Ratio (Plus)	+CMRR	4003	4(j)	$+V_{CC} = +15V, -V_{CC} = -15V$ $V_I = -11V$	85	-	dB
19	Common Mode Rejection Ratio (Minus)	−CMRR	4003	4(j)	$+V_{CC} = +15V, -V_{CC} = -15V$ $V_I = +11V$	85	-	dB

NOTES

1. For sampling inspections and end point tests the duration of I_{OS} shall be 5ms maximum. For other tests this duration may be reduced to be consistent with automatic test procedures provided that the same limits are maintained.
2. Sample test: Inspection Level = II, AQL = 2.5%.
3. For measurements at $T_{amb} = +125°C$ only.
4. For measurements at $T_{amb} = -55°C$ only.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - INPUT OFFSET VOLTAGE

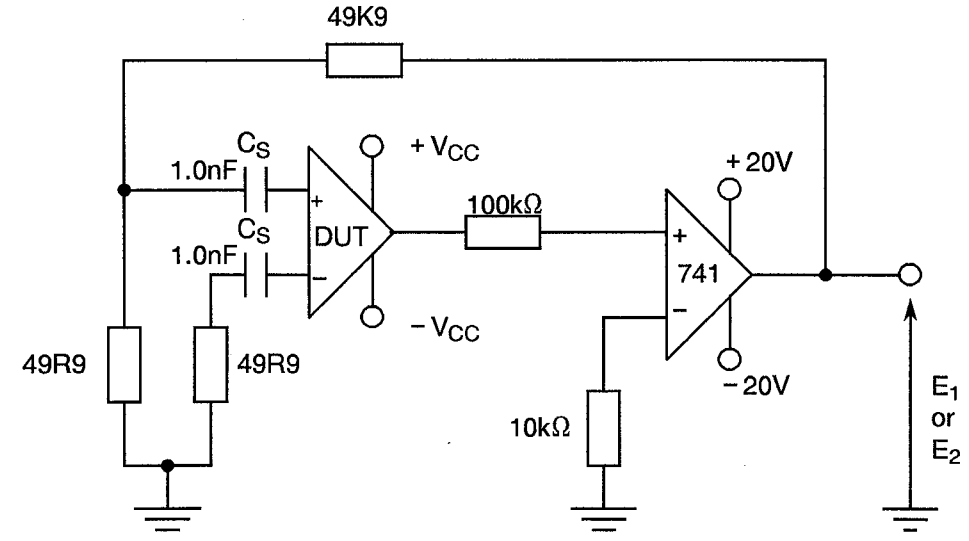


NOTES

1. Measure E_1 when $+V_{CC}$ = +20V and $-V_{CC}$ = −20V.
2. Measure E_2 when $+V_{CC}$ = +5.0V and $-V_{CC}$ = −5.0V.

$V_{IO1} = E_1$ and $V_{IO2} = E_2$

FIGURE 4(b) - INPUT OFFSET CURRENT



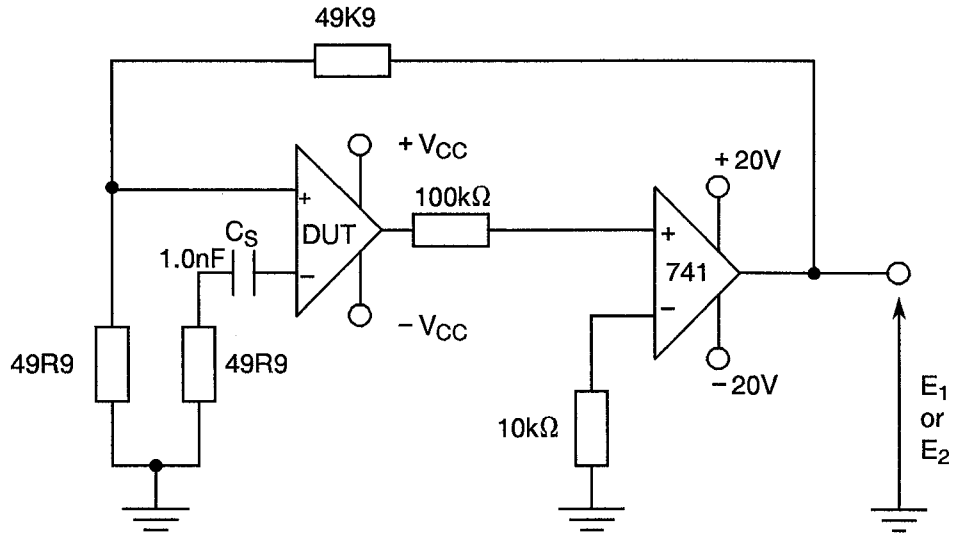
NOTES

1. Measure E_1 when $+V_{CC}$ = +20V and $-V_{CC}$ = −20V.
2. Measure E_2 when $+V_{CC}$ = +5.0V and $-V_{CC}$ = −5.0V.
3. $t_S = C_S$ capacitance charge time = 100ms.

$$I_{IO1} = \frac{(V_{IO1} - E_1) \times C_S}{t_S} \qquad I_{IO2} = \frac{(V_{IO2} - E_2) \times C_S}{t_S}$$

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(c) - POSITIVE INPUT BIAS CURRENT

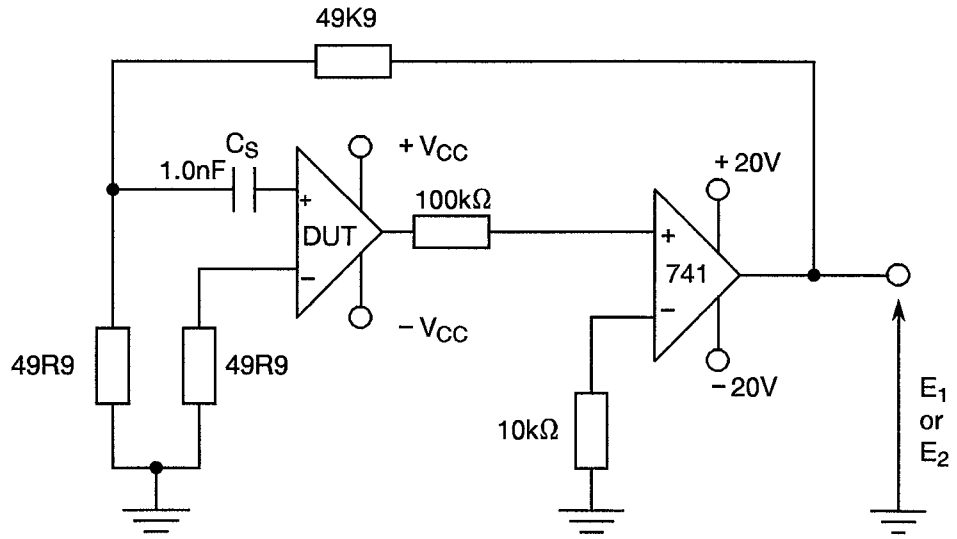


NOTES

1. Measure E_1 when $+V_{CC}$ = +20V and $-V_{CC}$ = −20V.
2. Measure E_2 when $+V_{CC}$ = +5.0V and $-V_{CC}$ = −5.0V.
3. $t_S = C_S$ capacitance charge time = 100ms.

$$+I_{IB1} = \frac{(V_{IO1} - E_1) \times C_S}{t_S} \qquad +I_{IB2} = \frac{(V_{IO2} - E_2) \times C_S}{t_S}$$

FIGURE 4(d) - NEGATIVE INPUT BIAS CURRENT



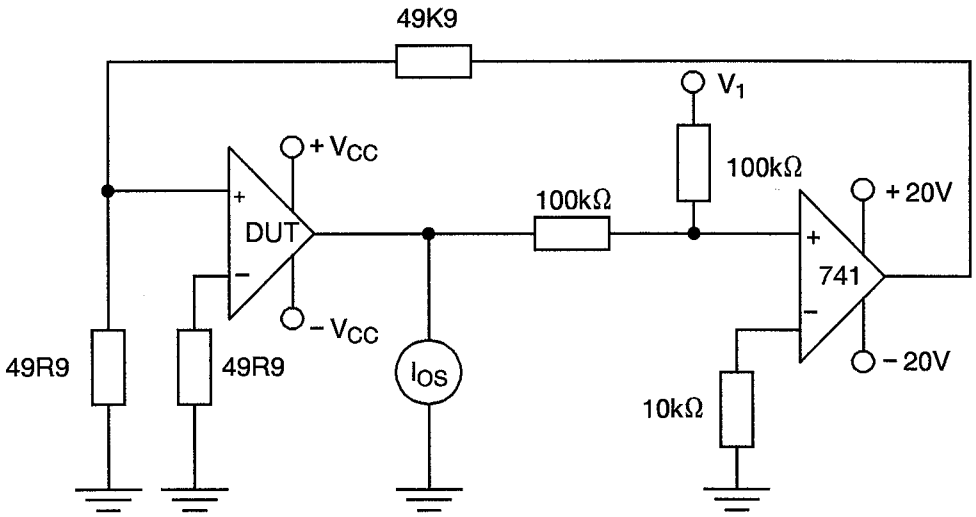
NOTES

1. Measure E_1 when $+V_{CC}$ = +20V and $-V_{CC}$ = −20V.
2. Measure E_2 when $+V_{CC}$ = +5.0V and $-V_{CC}$ = −5.0V.
3. $t_S = C_S$ capacitance charge time = 100ms.

$$-I_{IB1} = \frac{(E_1 - V_{IO1}) \times C_S}{t_S} \qquad -I_{IB2} = \frac{(E_2 - V_{IO2}) \times C_S}{t_S}$$

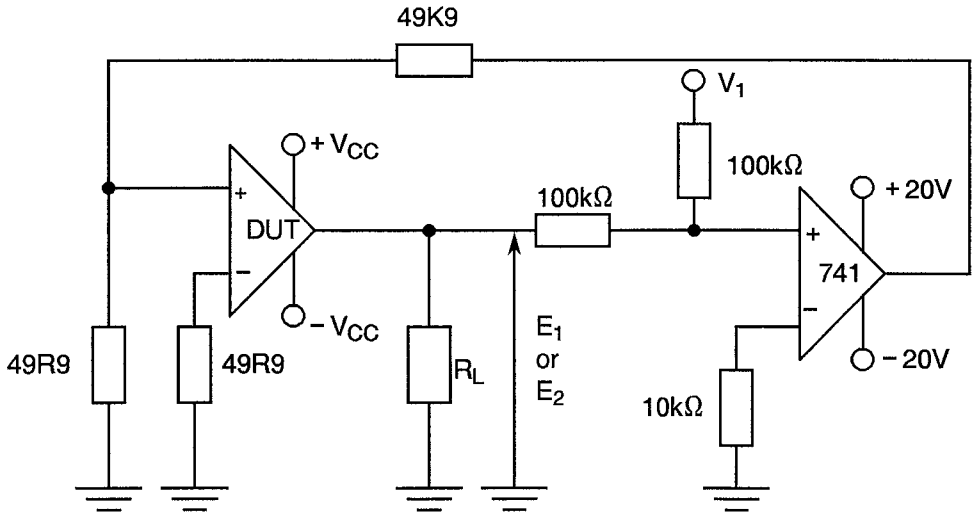
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(e) - SHORT CIRCUIT OUTPUT CURRENT



NOTES
1. Measure I_{OS}.

FIGURE 4(f) - OUTPUT VOLTAGE SWING

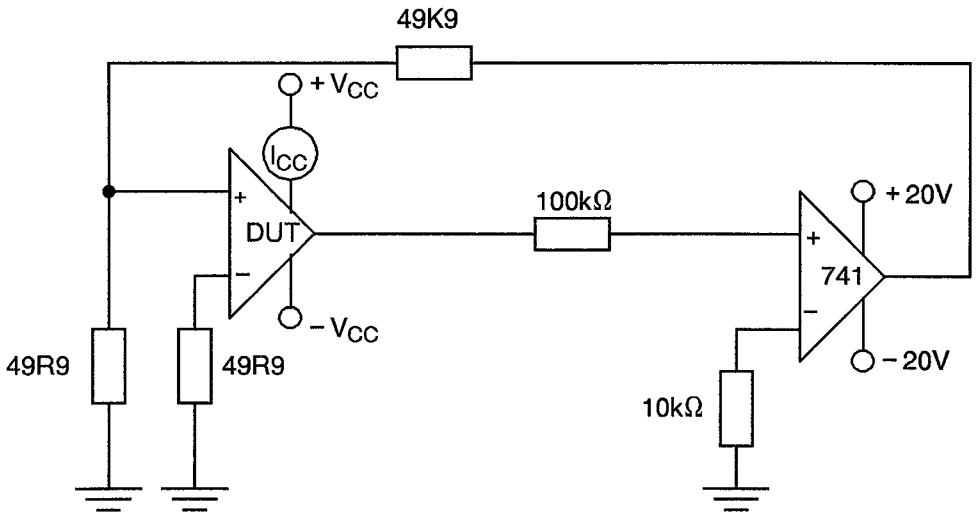


NOTES
1. Measure E_1 when $V_1 = -15V$.
2. Measure E_2 when $V_1 = +15V$.

$$+V_{OP} = E_1 \qquad -V_{OP} = E_2$$

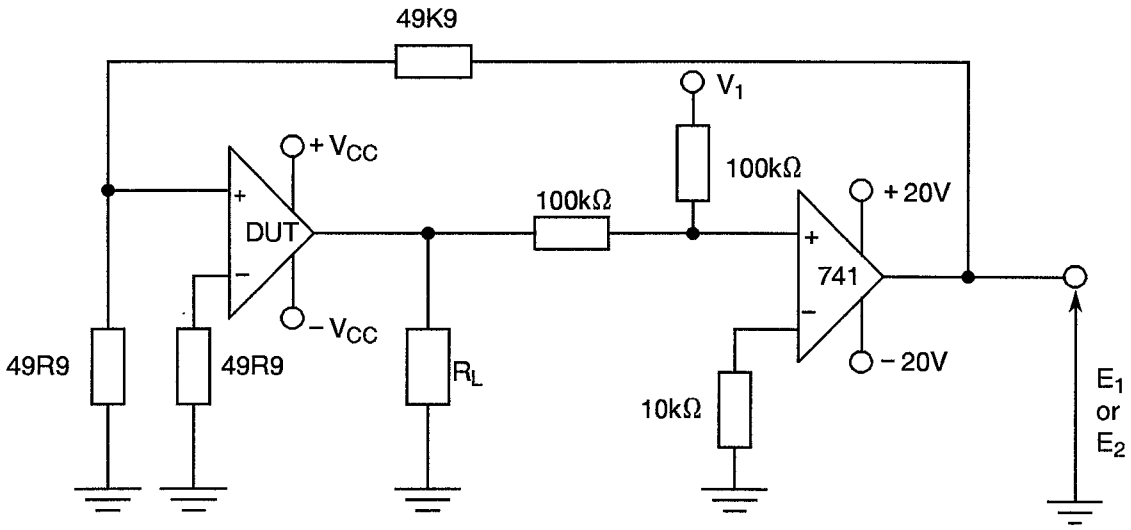
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(g) - POWER SUPPLY CURRENT



NOTES
1. Measure I_{CC}.

FIGURE 4(h) - OPEN LOOP VOLTAGE GAIN

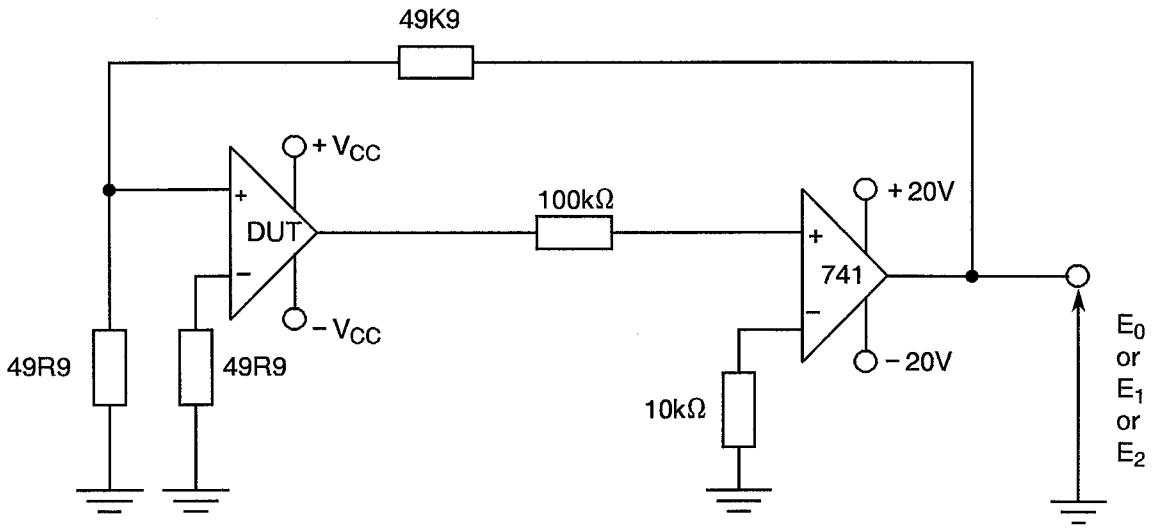


NOTES
1. Measure E_1 when $V_1 = -10V$ and E_2 when $V_1 = +10V$.

$$+A_{VS} = \frac{10}{V_{IO1} - E_1} \qquad -A_{VS} = \frac{10}{E_2 - V_{IO1}}$$

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - POWER SUPPLY REJECTION RATIO

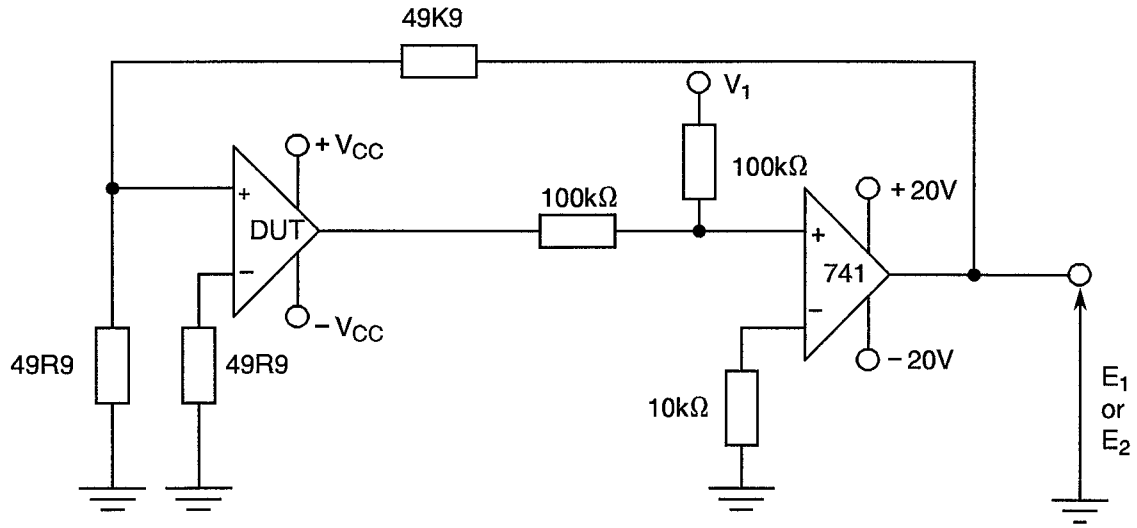


NOTES

1. Measure E_0 when $+V_{CC} = +20V$ and $-V_{CC} = -20V$.
2. Measure E_1 when $+V_{CC} = +10V$ and $-V_{CC} = -20V$.
3. Measure E_2 when $+V_{CC} = +20V$ and $-V_{CC} = -10V$.

$$+PSRR = 20 \log_{10} \frac{10^4}{E_1 - E_0} \qquad -PSRR = 20 \log_{10} \frac{10^4}{E_2 - E_0}$$

FIGURE 4(j) - COMMON MODE REJECTION RATIO



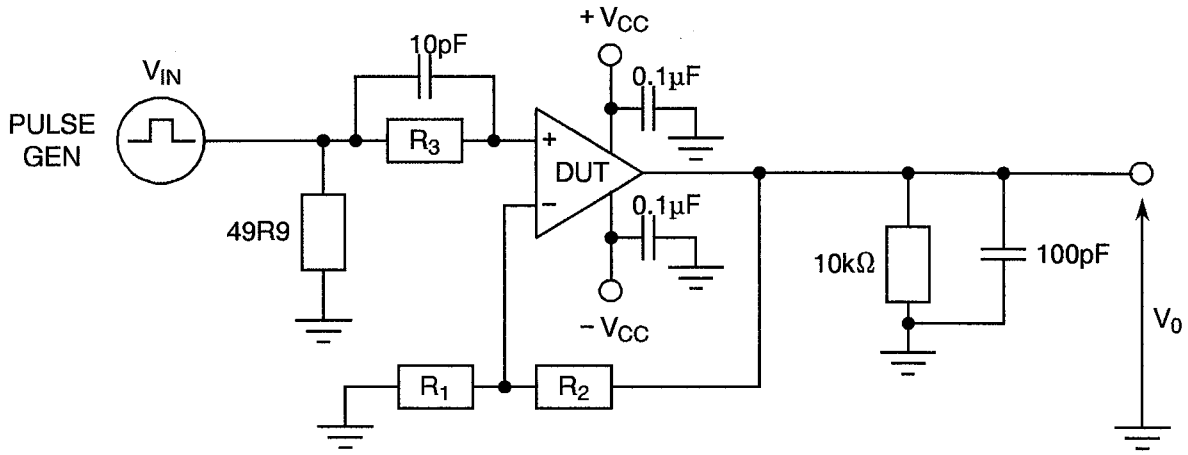
NOTES

1. Measure E_1 when $+V_{CC} = +15V$, $-V_{CC} = -15V$ and $V_1 = -11V$
2. Measure E_2 when $+V_{CC} = +15V$, $-V_{CC} = -15V$ and $V_1 = +11V$

$$+CMRR = 20 \log_{10} \frac{11 \times 10^3}{E_1 - V_{IO2}} \qquad -CMRR = 20 \log_{10} \frac{11 \times 10^3}{E_2 - V_{IO2}}$$

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

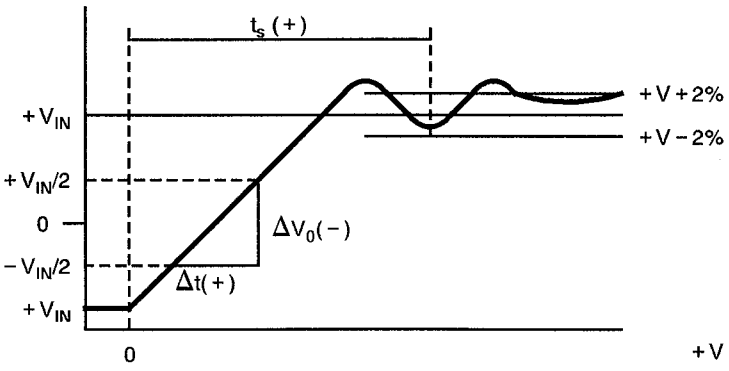
FIGURE 4(k) - DYNAMIC TEST MEASUREMENT CIRCUIT

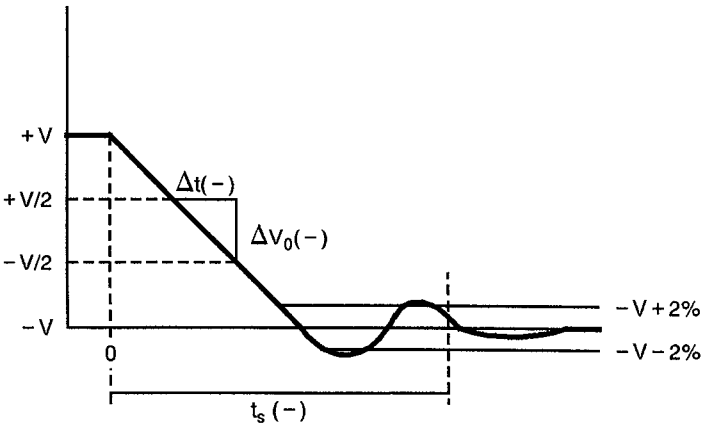


NOTES

1. Pulse Generator:
   - Rise time ≤ 10ns; Repetition rate 1.0kHz (max.)
   - Pulse voltage: −2.0V to +2.0V for slew rate measurement, AV = 5.0.
   - Pulse voltage = 50mV for rise time and overshoot measurements, AV = 1.0.
   - Pulse voltage = 10mV for rise time and overshoot measurements, AV = 5.0.
2. AV = 1.0 when R_1 is open, R_2 = 10kΩ and R_3 = 10kΩ.
3. AV = 5.0 when R_1 = 1.0kΩ, R_2 = 4.0kΩ and R_3 = 1.0kΩ.

$$SR = \left| \frac{\Delta V_0}{\Delta t} \right| \qquad OS = \frac{\Delta V}{50} \times 100 \qquad GB = \frac{0.35MHz}{t_s}$$





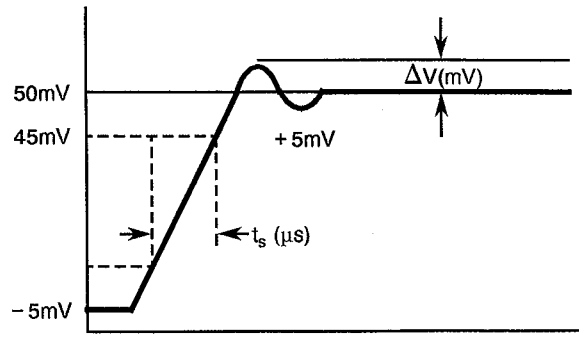


TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
1	Input Offset Voltage	V_{IO1}	As per Table 2	As per Table 2	±1.0	mV
3	Input Offset Current	I_{IO1}	As per Table 2	As per Table 2	±20	pA
5	Input Bias Current (Plus)	$+I_{IB1}$	As per Table 2	As per Table 2	±50	pA
7	Input Bias Current (Minus)	$-I_{IB1}$	As per Table 2	As per Table 2	±50	pA

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN -IN

Not applicable.

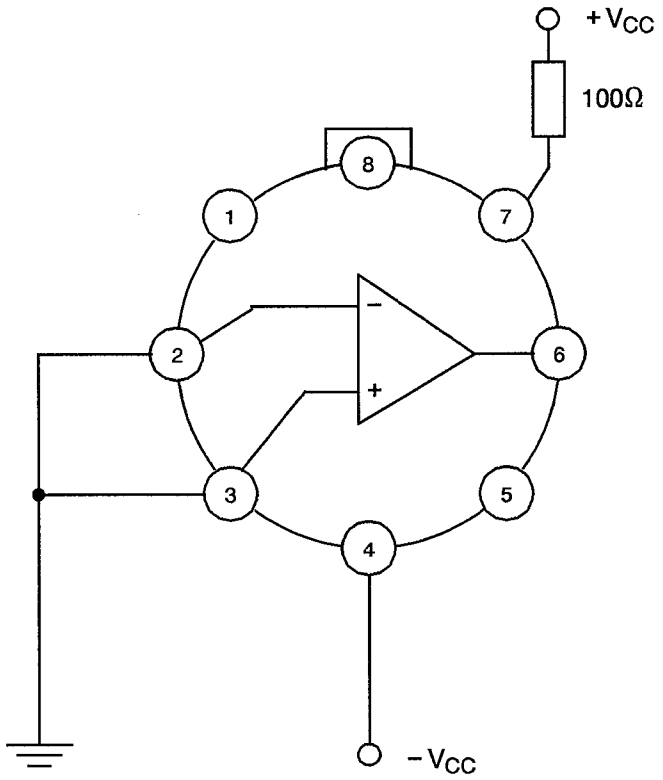
TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+5−0)	°C
2	Power Supply Voltage (±)	V_{CC}	±15	V

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(b) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)		UNIT
					MIN	MAX	
1	Input Offset Voltage	V_{IO1}	As per Table 2	As per Table 2 Variants 01, 02, 03 Variants 04, 05	 −5.0 −2.0	 +5.0 +2.0	mV
3	Input Offset Current	I_{IO1}	As per Table 2	As per Table 2 Variants 01, 02, 03 Variants 04, 05	 −20 −10	 +20 +10	pA
5	Input Bias Current (Plus)	$+I_{IB1}$	As per Table 2	As per Table 2 Variants 01, 02, 03 Variants 04, 05	 −100 −50	 +100 +50	pA
7	Input Bias Current (Minus)	$-I_{IB1}$	As per Table 2	As per Table 2 Variants 01, 02, 03 Variants 04, 05	 −100 −50	 +100 +50	pA
11	Output Voltage Swing (Plus)	$+V_{OPP}$	As per Table 2	As per Table 2	+12	-	V
12	Output Voltage Swing (Minus)	$-V_{OPP}$	As per Table 2	As per Table 2	-	+12	V
13	Power Supply Current	I_{CC}	As per Table 2	As per Table 2 Variants 01, 04 Variants 02, 03, 05	 - -	 4.0 7.0	mA
14	Open Loop Voltage Gain (Plus)	$+A_{VS}$	As per Table 2	As per Table 2	50	-	V/mV
15	Open Loop Voltage Gain (Minus)	$-A_{VS}$	As per Table 2	As per Table 2	50	-	V/mV