INTEGRATED CIRCUITS, MONOLITHIC, CMOS SILICON ON SAPPHIRE,

OBDH-REMOTE BUS INTERFACE RBI CIRCUIT,

WITH 3-STATE OUTPUTS,

BASED ON TYPE 12663

ESCC Detail Specification No. 9544/006

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Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.
'A'	June '96	P1. Cover page		None
		P2. DCN		None
		P32. Para. 4.2.3	: Deviation "(b)" added	221344
		P36. Table 2	: Nos. 124 to 186, in Conditions, V_{DD} amended to "4.5V"	221344
		P37. Table 2	: Nos. 363 to 412, Max Limit amended to "3.2"	221344
			: Nos. 413 to 462, Max Limit amended to "3.9"	221344
		P39. Table 2	: No. 713, in Conditions, "All Outputs Open" deleted	221344
			: , Max Limit amended to "4.0"	221344
		P44. Table 3	: Nos. 124 to 186, in Conditions, V_{DD} amended to "4.5V"	221344
		P45. Table 3	: Nos. 363 to 412, Max Limit amended to "3.2"	221344
			: Nos. 413 to 462, Max Limit amended to "3.9"	221344
		P57. Table 6	: New Nos. 313 to 658 added	221344
			: Nos. 830 to 837 moved to Page 58	None
		P58. Table 6	: Nos. 858 to 863 moved to Page 59	None
		P61. Table 7	: Nos. 363 to 412, Max Limit amended to "3.2"	221344
			: Nos. 413 to 462, Max Limit amended to "3.9"	221344
'B'	Jan. 97	P1. Cover page	: Part Number amended	221375
		P2. DCN		None
		P4. T of C	: Appendix 'A' entry amended	221375
		P5. Para. 1.1	: In second line, "ABB-HAFO" amended to "MITEL"	221375
			: In third line, Part Number amended	221375
		P32. Para. 4.2.3	: Item "(b)" deleted in toto.	221375
		P62. Appendix 'A'	: Title amended	221375
			: For Para. 4.2.3 entry, Item "(b)" added	221375

TABLE OF CONTENTS

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a monolithic, CMOS Silicon on Sapphire (MITEL SOS4 Process) Remote Bus Interface (RBI) Circuit, with 3-State Outputs, based on Type 12663. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

As per Figure 3(b).

1.8 CIRCUIT DESCRIPTION

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 with a Minimum Critical Path Failure Voltage of 1500Volts.

1.11 INPUT/OUTPUT PROTECTION NETWORKS

Protection networks shall be incorporated into each input, power-rail and output as shown in Figure 3(e).

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND FINISH
01	FLAT	2(a)	D2

TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage	V_{DD}	−0.5 to +7.0	V	-
2	Input Voltage	V_{IN}	−0.5 to V_{DD} +0.5	V	-
3	DC Input Current	I_{IN}	±20	mA	-
4	DC Output Current	I_{OUT}	±10	mA	Note 1
5	Device Dissipation	P_D	600	mWdc	Per package
6	Output Dissipation	P_{DSO}	50	mWdc	Note 1
7	Clock Frequency	f_{CLK}	5.0	MHz	Note 2
8	OBDH Clock Frequency	f_{OBDH}	524.288 ± 5.0	kHz	-
9	Operating Temperature Range	T_{op}	−55 to +125	°C	T_{amb}
10	Storage Temperature Range	T_{stg}	−65 to +150	°C	-
11	Soldering Temperature	T_{sol}	+260	°C	Note 3
12	Junction Temperature	T_j	+150	°C	-
13	Thermal Resistance	$R_{TH(J-A)}$	25	°C/W	-

NOTES

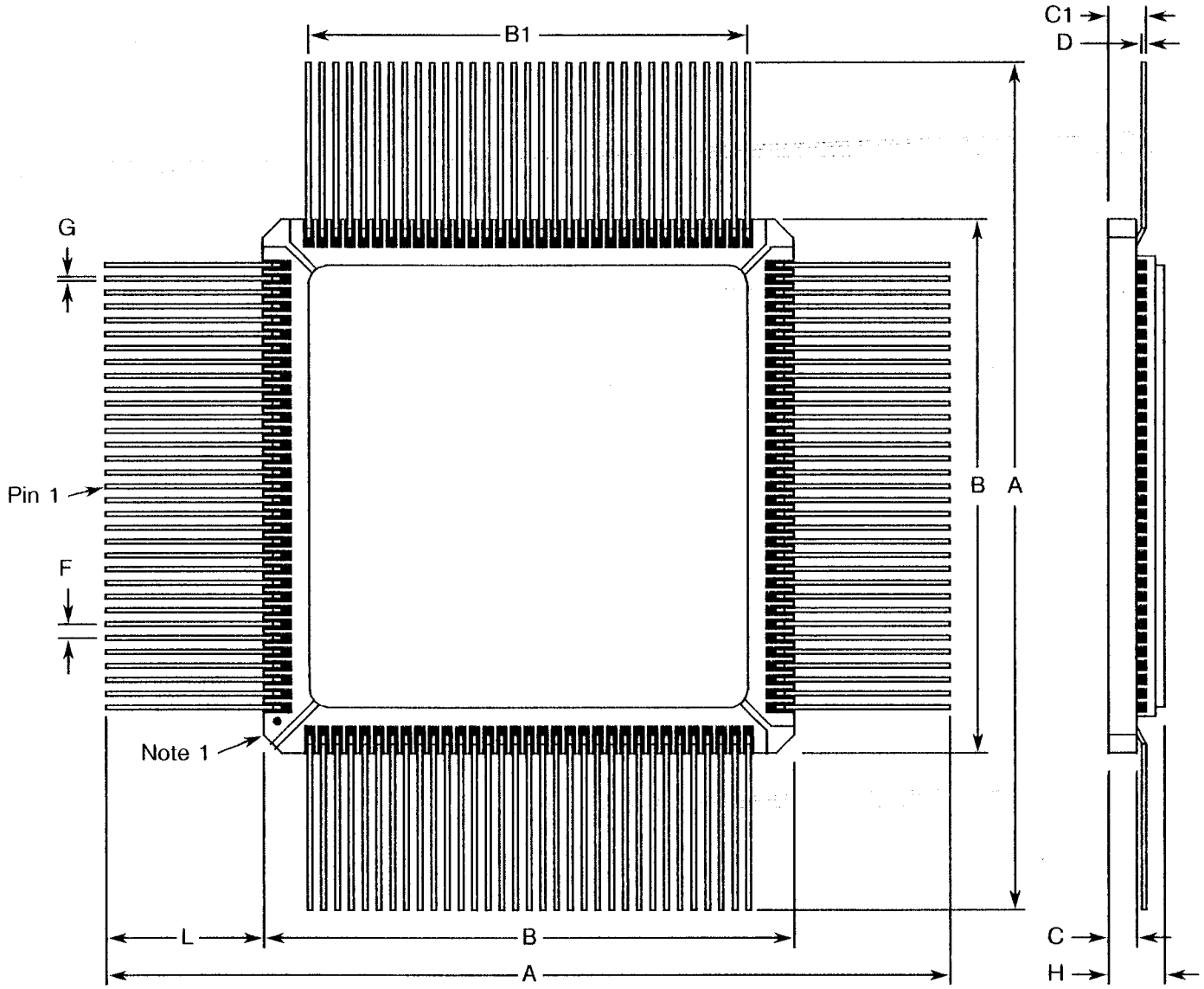
1. The maximum output current of any single output.
2. System Clock (CLK).
3. Duration 5 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION

Not applicable.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - FLAT PACKAGE, 132-PIN



SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	35.35	40.26	
B	23.88	24.26	
B1	20.32 TYPICAL		
C	1.24	1.55	
C1	1.45	1.75	2, 5
D	0.10	0.18	
F	0.635 TYPICAL		3, 4
G	0.23	0.33	2
H	1.83	2.62	
L	5.74	8.00	2

NOTES: See Page 8.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURE 2(a)

1. Index area; the index shall be as defined in Figure 2(a).
2. All leads.
3. 128 spaces for flat packages.
4. The true position pin spacing is 0.6mm between centre lines. Each pin centreline shall be located within ±0.1mm of its true longitudinal position relative to Pin 1 and the highest pin number.
5. The dimension shall be measured at the point of exit of the lead from the body.

FIGURE 3(a) - PIN ASSIGNMENT

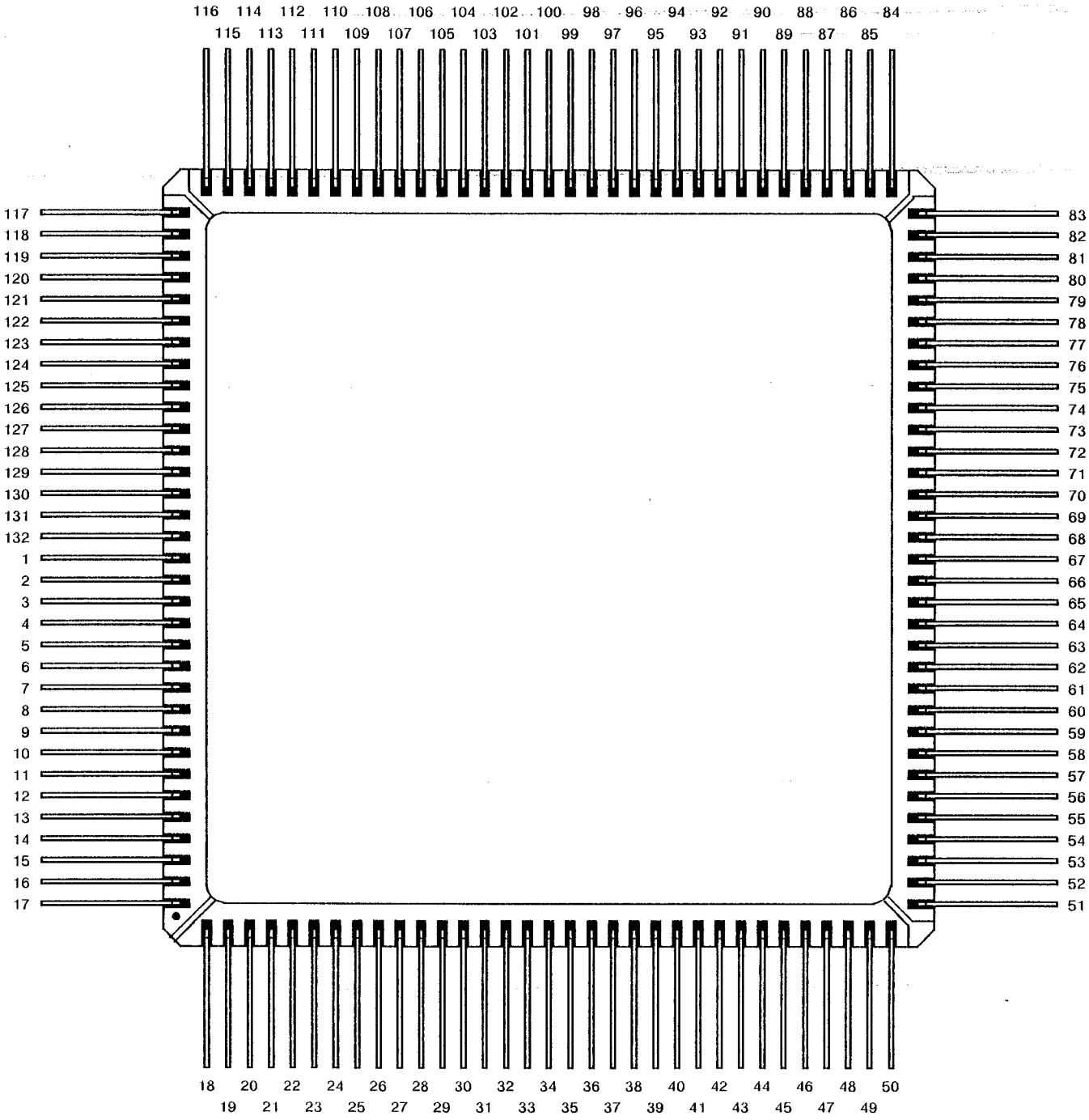


FIGURE 3(a) - PIN ASSIGNMENT (CONTINUED)

PIN DESCRIPTION

PIN NAME	FUNCTION (NOTE 1)	DESCRIPTION	PIN No.
V_{DD}	Power Supply	DC power supply.	1, 2, 14, 30, 41, 55, 69, 80, 105, 129, 132
V_{SS}	Ground	0V reference point.	15, 31, 42, 56, 65, 66, 67, 68, 79, 106, 130
CLK	System Clock (Input)	Input clock signal	100
AD<0:23>	System Address Bus (3-State Output)	Active high address bus which is High Z during bus cycles not assigned to the chip. AD0 (Pin 22) is MSB, AD23 (Pin 51) is LSB.	22 to 29, 32 to 39, 44 to 51
DATA<0:15>	System Data Bus (Input/Output)	Active high data bus which is High Z during bus cycles not assigned to the chip. DATA0 is the most significant bit.	57 to 64, 70 to 77
$\overline{\text{RESET}}$	RBI Chip Reset (Input)	Active low input to reset the RBI chip. The low to high transition will start the initialisation sequence.	104
RIR_CLK	Interrogation Data Clock (Input)	Input signal derived from the OBDH LITTON CODED interrogations (584288 Hz) used as bit clock for interrogation/response transfer.	4
RIR_VAL	Valid Interrogation Flag (Input)	Active high input to signal valid LITTON CODE and correct number of bits.	7
RIR_SYNC	Synch Pulse (Input)	Active high input to signal that a synchronisation pattern has been detected on the OBDH bus.	6
RIR_DATA	Interrogation Data (Input)	Active high input to transfer interrogations onto the chip using RIR_CLK as strobe signal.	5
RRT_DATA	Response Data Word (Output)	Active high output which transfers responses out of the chip using RIR_CLK as strobe signal.	128
RRT_EN	Response Transmission Enable (Output)	Active high output which signals that a response is being transmitted.	131
BCP1	8 Hz Signal (Output)	Active high output which reflects the BCP1 bit of the received interrogation.	8
BCP2	1 Hz Signal (Output)	Active high output which reflects the BCP2 bit of the received interrogation.	9
BCP3	Time Synchronisation (Output)	Active high output which reflects the BCP3 bit of the received interrogation.	10
BCP4	Time Verification (Output)	Active high output which reflects the BCP4 bit of the received interrogation.	11
ZEROT	Timer Reset (Output)	Active high output which signals that a BCP3-BCP2 sequence has been detected and time synchronisation is authorised.	12

NOTES: See Page 13.

FIGURE 3(a) - PIN ASSIGNMENT (CONTINUED)

PIN DESCRIPTION (CONTINUED)

PIN NAME	FUNCTION (NOTE 1)	DESCRIPTION	PIN No.
CLK256	256 Hz Clock (Output)	Clock output which carries a periodic signal derived from the OBDH bus with a nominal frequency of 256Hz. After reset or BCP3-BCP2 reception, CLK256 is set to 0.	13
USERAD<0:4>	ICU Address (Input)	Active high inputs to define the ICU address on the OBDH bus. Each of these pins must be tied to logic 0 or 1 to form an address between 1 and 31.	16 to 20
$\overline{CS}$	Chip Select (Input)	Active low input to signal that the current read or write access is addressed to the chip.	84
ADREG<0:3>	Register Address (Input)	Active high input, valid only if $\overline{CS}$ is active, to select a chip register for read or write.	112 to 115
$\overline{RD}$	Register Read Access (Input)	Falling-edge sensitive input used in conjunction with active $\overline{CS}$ to latch the contents of the chip register selected by ADREG<0:4> onto the external data bus. Internally synchronised.	82
$\overline{WR}$	Register Write Access (Input)	Active low input used in conjunction with active $\overline{CS}$ to latch the value on the data bus into the register selected by ADREG<0:4>. Internally synchronised.	83
$\overline{RDY}$	Ready Signal (Output)	Active low output to insert wait states into read or write operations performed by the processor to access the RBI chip. Signals that at the end of a register write cycle, data can be removed from the data bus.	97
$\overline{MRD}$	DMA Read from Memory (3-State Output)	Active low output to place memory contents addressed by AD<0:23> onto the external data bus to be read by the RBI chip. This output is only activated for read cycles and it is High Z when the external bus is not under control of the chip.	91
$\overline{MWR}$	DMA Write from Memory (3-State Output)	Active low output to strobe data placed on the external data bus by the RBI chip into the memory word addressed by AD<0:23>. This output is only activated for write cycles. The rising edge should be used by the memory to strobe the data from the data bus into memory. This signal is High Z when the external bus is not under control of the chip.	92
MAS	Memory Address Strobe (3-State Output)	Active high output to signal that the address bus carries a valid address. This output is High Z when the external bus is not under control of the chip.	94

NOTES: See Page 13.

FIGURE 3(a) - PIN ASSIGNMENT (CONTINUED)

PIN DESCRIPTION (CONTINUED)

PIN NAME	FUNCTION (NOTE 1)	DESCRIPTION	PIN No.
DD	Data Direction (Output)	Output to indicate the direction of the data transfer performed under RBI chip control. For write transfers the output is low, for read transfers the output is high. If no bus transfer is performed, the output is high. During read cycles performed to access RBI chip, registers the output is low.	95
$\overline{CD}$	Control Direction (Output)	Active low output to signal that the chip has control of the bus. It goes high after the chip has relinquished the bus.	96
$\overline{MRDY}$	Memory Ready (Input)	Asynchronous active low input used by the RBI chip to insert wait states into a memory read or write cycle. This signal should be used by slower devices to insert wait states into the read/write access performed by the chip.	90
$\overline{DMAR}$	DMA Request (Output)	Active low output to request bus control, remains low until the bus has been relinquished by the RBI chip.	98
$\overline{DMAK}$	DMA Acknowledge (Input)	Active low input to signal that bus control has been granted to the RBI chip.	102
$\overline{DMAREQ1}$	Bus Request 1 (Input)	Active low input to request bus control for device 1 from the on-chip arbiter. The input shall remain active until device 1 has released the bus.	126
$\overline{DMACK1}$	Bus Acknowledge 1 (Output)	Active low output to signal to device 1 that control of the bus has been granted to it.	123
$\overline{DMAREQ2}$	Bus Request 2 (Input)	Active low input to request bus control for device 2 from the on-chip arbiter. The input shall remain active until device 2 has released the bus.	125
$\overline{DMACK2}$	Bus Acknowledge 2 (Output)	Active low output to signal to device 2 that control of the bus has been granted to it.	122
$\overline{DMALOCK2}$	DMA Lock (Input)	Active low input driven by device 2 to lock bus control.	124
$\overline{IT1}$	Interrupt1 (Output)	Active low output to signal that an instruction-to-RBI has been received which carries parameter data and needs software support.	110
$\overline{IT2}$	Interrupt2 (Output)	Active low output to signal that an instruction-to-user has been received.	111
$\overline{HOLD}$	Hold Line (Output)	Active low output to suspend the microprocessor until the suspend state is removed again by OBDH instruction.	109

NOTES: See Page 13.

FIGURE 3(a) - PIN ASSIGNMENT (CONTINUED)

PIN DESCRIPTION (CONTINUED)

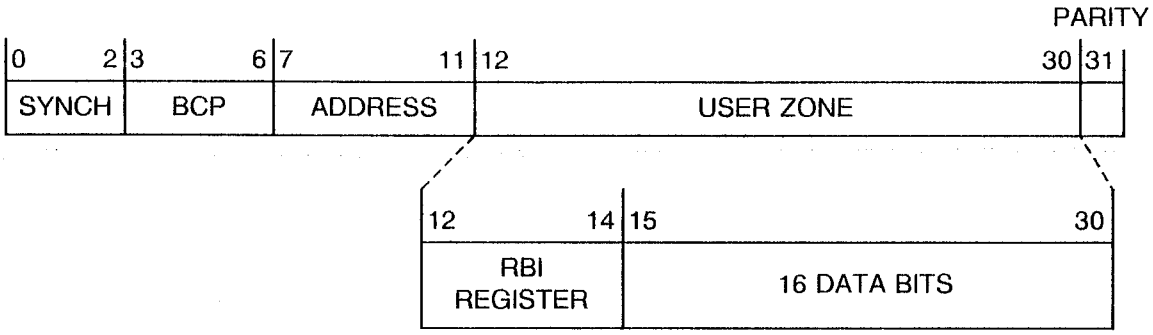
PIN NAME	FUNCTION (NOTE 1)	DESCRIPTION	PIN No.
$\overline{\text{HOLDAK}}$	Hold Acknowledge (Input)	Active low input to receive acknowledge for microprocessor suspension.	108
$\overline{\text{RESETMC}}$	ICU Reset Line (Output)	Active low output to reset the ICU microprocessor and peripherals, generated on reception of the RESET ICU instruction with zero parameter.	103
$\overline{\text{MPROTECT}}$	Memory Protection (Input)	Active low input to inhibit the write cycle (performed by the RBI chip) before $\overline{\text{WR}}$ is activated when write-access to a protected memory area has been detected.	89
$\overline{\text{FLGERR}}$	Flags Error (Input)	Falling-edge sensitive input to signal an ICU error condition. On activation, the RBI chip resets the running-bit in the RBI STATUS REGISTER.	88
$\overline{\text{Ext\_Fr1}}$	External Freeze 1 (Input)	Falling-edge sensitive input to copy the time counter value into the EXTERNAL FREEZE 1 REGISTER.	119
$\overline{\text{Ext\_Fr2}}$	External Freeze 2 (Input)	Falling-edge sensitive input to copy the time counter value into the EXTERNAL FREEZE 2 REGISTER.	120
$\overline{\text{IT\_WAT}}$	Watchdog Interrupt (Output)	Active low output to signal a time-out condition detected by the on-chip WATCHDOG function.	117
$\overline{\text{IT\_LOSS}}$	Clock Loss Interrupt (Output)	Active low output to signal OBDH clock loss for more than 16 nominal OBDH clock cycles.	118
TEST_HAFO0	Outputs Test Enable	Active high input dedicated to output buffers test.	53 (Note 2)
TEST_HAFO1	Outputs Test Input	Input dedicated to output buffers test.	54 (Note 2)
TEST_REC	Test Pin	Input dedicated to test.	3 (Note 2)
TEST_REG0	Test Pin	Input dedicated to test.	85 (Note 2)
TEST_REG1	Test Pin Input	Input dedicated to test.	86 (Note 2)
TEST_CPT	Test Pin	Input dedicated to test.	116 (Note 2)
TEST_SEG	Test Pin	Input dedicated to test.	127 (Note 2)
Not Connected	Open	Not used.	21, 40, 43, 52, 78, 81, 87, 93, 99, 101, 107, 121

NOTES

1. All inputs, outputs and input/outputs are CMOS.
2. Inputs for manufacturing test only. Pins connected to V_{SS} for normal operation.

FIGURE 3(b) - TRUTH TABLE

STRUCTURE OF INTERROGATION WORD



STRUCTURE OF RESPONSE WORD

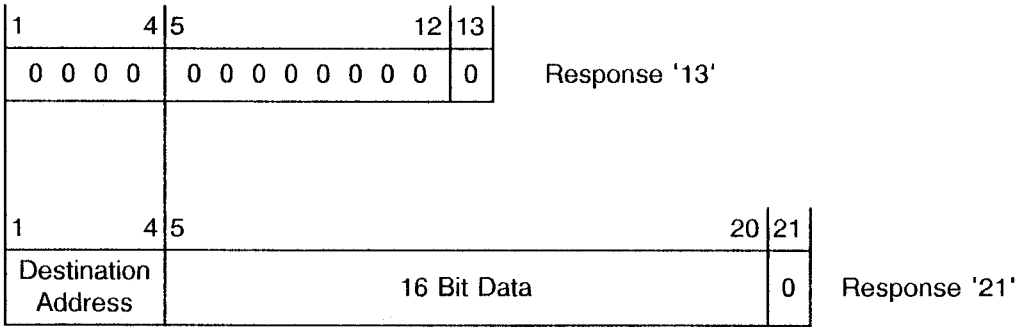


FIGURE 3(b) - TRUTH TABLE (CONTINUED)

OBDH INSTRUCTIONS

TYPE	RBI REGISTER	16 BITS DATA	RESPONSE TYPE
RESET ICU	0 0 1	0 0 0 0 0 0 0 0 <8 bit param.>	Response 13
START ICU	0 0 1	1 1 1 1 0 0 0 0 <8 bit param.>	Response 13
SUSPEND ICU	0 0 1	0 0 0 1 X X X X X X X X X X X X	Response 13
GO ICU	0 0 1	0 0 1 0 X X X X X X X X X X X X	Response 13
RESET DMA	0 0 1	0 1 0 0 X X X X X X X X X X X X	Response 13
RESET PAGE ADDRESS	0 0 1	1 0 0 0 X X X X X X X X X X X X	Response 13
INSTRUCTION TO USER	0 1 0	< 16 bits data of parameter >	Response 13
SET START ADDRESS	1 0 0	<16 bits data of Start address value>	Response 13
SET LENGTH (Write Operations)	1 0 1	0 0 0 X <12 bits Block length - 1>	Response 13
SET LENGTH (Read Operations)	1 0 1	1 0 0 X <12 bits Block length - 1>	Response 13
WRITE DATA	0 1 1	16 bits data to be written	Response 13
READ DATA	0 0 0	Dest. ad 1 0 1 0 X X X X X X X 0 (Note 1)	Response 21
IMMEDIATE READ	0 0 0	Dest. ad 1 0 1 0 <7 bits address>1 (Note 1)	Response 21
READ STATUS	0 0 0	Dest. ad 1 0 1 0 0 0 0 0 0 0 0 1 (Note 1)	Response 21
SET PAGE ADDRESS	1 1 1	<16 bits data of page address value>	Response 13

NOTES

1. Dest. ad represents the destination address (bits 1 to 4 of the response word).

MICROPROCESSOR INSTRUCTIONS

The microprocessor can command the RBI chip by writing in the configuration register.

NAME	VALUE TO BE WRITTEN IN THE CONFIGURATION REGISTER
Enter reset state	8000
Enter running state	4000
Set wrong interrogation bit	2000
Enable synchronisation	1000
Set output transfer request	800
Reset page address	400
Enter wait state	200
Enable/disable watchdog	100
Freeze OBT	80

FIGURE 3(b) - TRUTH TABLE (CONTINUED)

REGISTERS PRESENTATION

GENERAL PRESENTATION

NAME	DESCRIPTION	MICROPROCESSOR ACCESS	INTERNAL ADDRESS
RBI status	Contains current RBI state	R/W (Note 1)	0H
Instruction to RBI	Contains RESET ICU and START ICU interrogation parameters	R	1H
Instruction to USER	Contains 16 bits parameter of an INSTRUCTION TO USER	R	2H
BASE ADDRESS	Contains page address value of the CCA	R/W	3H
START ADDRESS	Contains 16 bits of the page address	R	4H
LENGTH	Contains 12 bits of the block length and the RW bit value. RW is '0' for DMA write access and '1' for DMA read access. When reading this register, only 12 bits of the block length are provided on the data bus. RW is an internal bit and is not accessible by the ICU microprocessor.	R	5H
CONFIGURATION	Microprocessor COMMAND and STATUS REGISTER	R/W	6H
PAGE ADDRESS	Contains 16 bit relative address within page	R	7H
WATCHDOG	Remaining time before a watchdog interrupt will be generated (value given in 2048 multiples of OBDH clock period)	W	8H
EXTERNAL FREEZE 1 (bits 0-15)	Number of OBDH clock cycles, OBT bits 0 to 15, until next ext-freeze 1 event occurs	R	9H
EXTERNAL FREEZE 1 (bits 16-31)	Number of OBDH clock cycles, OBT bits 16 to 31, until next ext-freeze 1 event occurs	R	0AH
EXTERNAL FREEZE 1 (bits 32-42)	Number of OBDH clock cycles, OBT bits 32 to 42, until next ext-freeze 1 event occurs	R	0BH
EXTERNAL FREEZE 2 (bits 0-15)	Number of OBDH clock cycles, OBT bits 0 to 15, until next ext-freeze 2 event occurs	R	0CH
OBT Update (bits 0-15)	16 MSB to be added to the OBT value	W	0CH
EXTERNAL FREEZE 2 (bits 16-31)	Number of OBDH clock cycles, OBT bits 16 to 31, until next ext-freeze 2 event occurs	R	0DH
OBT Update (bits 16-31)	16 LSB to be added to the OBT value	W	0DH
EXTERNAL FREEZE 2 (bits 32-42)	Number of OBDH clock cycles, OBT bits 32 to 42, until next ext-freeze 2 event occurs	R	0EH

NOTES: See Page 19.

FIGURE 3(b) - TRUTH TABLE (CONTINUED)

REGISTERS PRESENTATION (CONTINUED)

RBI STATUS REGISTER

POSITION	NAME	MEANING
0	ICU RESET	Indicates if ICU is in its RESET state (1) or not (0)
1	ICU WAIT	Indicates if ICU is in its WAIT state (1) or not (0)
2	DMA BUSY	Indicates if DMA block transfer is ongoing (1) or not (0)
3	ICU RUNNING	Indicates if ICU is in its RUNNING state (1) or not (0)
4	INTERROGATION PARITY ERROR	Indicates if a parity error has been detected in an interrogation
5	INTERROGATION VALID LITTON CODE	Indicates if a LITTON CODE or an incorrect number of bits error has been detected in an interrogation
6	Not used	
7	WRONG INTERROGATION	Indicates that a wrong interrogation has been received
8	OUTPUT TRANSFER REQUEST	Software bit
9-10	RBI INDICATION	0 0 no anomaly 0 1 illegal access to protected memory area 1 0 DMA access not granted 1 1 WATCHDOG or external error
11-15	SOFTWARE INDICATION	Directly managed by software

CONFIGURATION REGISTER (READ MODE)

POSITION	NAME	MEANING
0-7	-	Not allocated
8	IT1	Reflects level of IT1 output
9	IT2	Reflects level of IT2 output
10	Reg 4 load flag	Allows LENGTH REGISTER loading when set. Set after start address initialisation and reset after length initialisation
11	Sync-enable	Indicates if OBT reset is enabled with next BCP3-BCP2 sequence when 1
12	Error-flag	Indicates whether external error input signal has been activated
13	Bad operation	Indicates a wrong microprocessor instruction
14	HOLD bit	Reflects level of the $\overline{\text{HOLD}}$ output
15	WAT bit	Indicates whether WATCHDOG function is allowed (1) or not (0)

NOTES: See Page 19.

FIGURE 3(b) - TRUTH TABLE (CONTINUED)

DESCRIPTION OF INSTRUCTIONS

NAME	EXECUTION CONDITIONS	DESCRIPTION
RESET ICU (Note 1)	ICU RESET = 1 or ICU WAIT = 1 or ICU in RUNNING state	Stores the 16 interrogation data bits in REGISTERS 1, 2, 4 and 7, resets REGISTER 5 and enters the INIT state. If RESET ICU interrogation parameter ≠ 0: Generates an IT1 interrupt, sets IT1 = 1 in the CONFIGURATION REGISTER. If RESET ICU interrogation parameter = 0: Sets RESETMC = 0.
START ICU (Note 1)	ICU RESET = 1	Stores the 16 interrogation data bits in the INSTRUCTION TO RBI REGISTER, generates an IT1 interrupt, sets IT1 = 1 in the CONFIGURATION REGISTER.
SUSPEND ICU (Note 1)	ICU in RUNNING state	Sets HOLD = 0.
GO ICU (Note 1)	ICU WAIT = 1	Sets HOLD = 1 and sets ICU RUNNING = 1.
RESET DMA (Note 1)		Sets LENGTH REGISTER = 0, sets DMA BUSY = 0 bit and sets REG 4 LOAD FLAG = 0.
RESET PAGE ADDRESS (OBDH) (Note 1)	DMA BUSY = 0	Loads the BASE ADDRESS value into the PAGE ADDRESS REGISTER.
INSTRUCTION TO USER (Note 1)	ICU in RUNNING state	Stores the 16 interrogation data bits in the INSTRUCTION TO RBI REGISTER, generates an IT2 interrupt, sets IT2 = 0 in the CONFIGURATION REGISTER.
SET START ADDRESS (Note 1)	DMA BUSY = 0	Stores the 16 interrogation data bits in the START ADDRESS REGISTER, sets REG 4 LOAD FLAG = 1.
SET LENGTH (Write operation) (Note 1)	REG 4 LOAD FLAG = 1	Stores the 16 interrogation data bits in the LENGTH REGISTER, sets REG 4 LOAD FLAG = 0, sets DMA BUSY = 1, sets RW = 0.
SET LENGTH (Read operation) (Note 1)	REG 4 LOAD FLAG = 1	Stores the 16 interrogation data bits in the LENGTH REGISTER, sets REG 4 LOAD FLAG = 0, sets DMA BUSY = 1, sets RW = 1.
WRITE DATA (Note 1)	DMA BUSY = 1 and RW = 0	Performs DMA to write 16 interrogation data bits at the address: PAGE ADDRESS multiplied by 256 + START ADDRESS. If LENGTH = 0: Sets DMA BUSY = 0. If LENGTH ≠ 0: Increments START ADDRESS by 2 and decrements LENGTH by 1.
READ DATA (Note 1)	DMA BUSY = 1 and RW = 1	Performs DMA to read 16 data bits at the address: PAGE ADDRESS multiplied by 256 + START ADDRESS. If LENGTH = 0: Sets DMA BUSY = 0. If LENGTH > 0: Increments START ADDRESS by 2 and decrements LENGTH by 1.

NOTES: See Page 19.

FIGURE 3(b) - TRUTH TABLE (CONTINUED)

DESCRIPTION OF INSTRUCTIONS

NAME	EXECUTION CONDITIONS	DESCRIPTION
IMMEDIATE READ (Note 1)		Performs DMA to read 16 data bits at the address: BASE ADDRESS multiplied by 256 + INTERROGATION ADDRESS bits 23 to 29 and generates a response '21' with this value.
READ RBI STATUS (Note 1)		Generates a response '21' with the RBI STATUS value, resets INTERROGATION PARITY ERROR = 0, sets INTERROGATION VALID LITTON CODE = 0, sets WRONG INTERROGATION = 0.
SET PAGE ADDRESS (Note 1)	DMA BUSY = 0	Stores the 16 interrogation data bits in the PAGE ADDRESS REGISTER.
ENTER RESET STATE (Note 2)	ICU state = INIT	Enters the reset state, sets ICU RESET = 1.
ENTER RUNNING STATE (Note 2)	ICU RESET = 1	Enters the running state, sets ICU RUNNING = 1, sets ICU RESET = 0.
SET WRONG INTERROGATION BIT (Note 2)	ICU in RUNNING state	Sets WRONG INTERROGATION = 1.
ENABLE/DISABLE SYNCHRONISATION (Note 2)	ICU in RUNNING state	Sets SYNC-ENABLE = 1 (enabled) or = 0 (disabled).
SET OUTPUT TRANSFER REQUEST BIT (Note 2)	ICU in RUNNING state	Inverts the current logic state of OUTPUT TRANSFER REQUEST.
RESET PAGE ADDRESS (Note 2)	ICU in INIT state	Loads the BASE ADDRESS value into the PAGE ADDRESS REGISTER.
ENTER WAIT STATE (Note 2)	ICU in RUNNING state	Sets ICU RUNNING = 0, sets ICU WAIT = 1.
ENABLE/DISABLE WATCHDOG (Note 2)	ICU in RUNNING state	Sets WAT bit = 1 (enabled) or = 0 (disabled) in the CONFIGURATION REGISTER.
FREEZE ON-BOARD TIME (Note 2)		Loads the OBT register value into the EXTERNAL FREEZE 2 REGISTER.

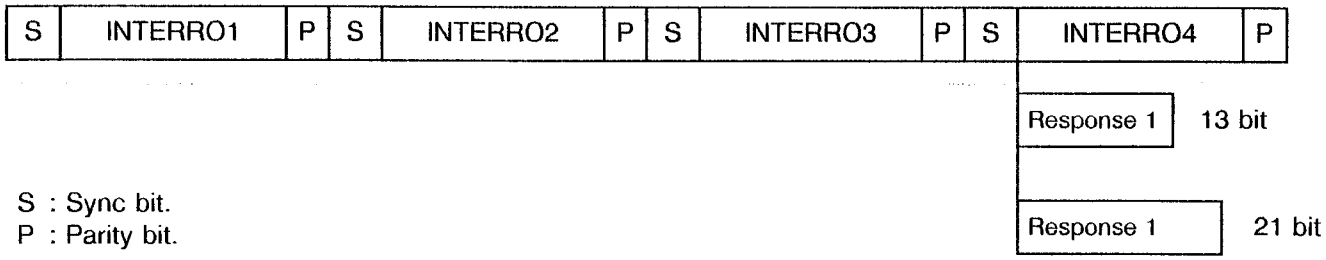
NOTES

1. OBDH instructions. If execution conditions are not met, RBI sets the WRONG INTERROGATION bit.
2. Microprocessor instructions. If execution conditions are not met, RBI sets BAD OPERATION bit.

FIGURE 3(b) - TRUTH TABLE (CONTINUED)

TIMING WAVEFORMS

TIMING-RELATIONSHIP BETWEEN INTERROGATIONS AND RESPONSES



S : Sync bit.
P : Parity bit.

OBDH INTERFACE TIMING

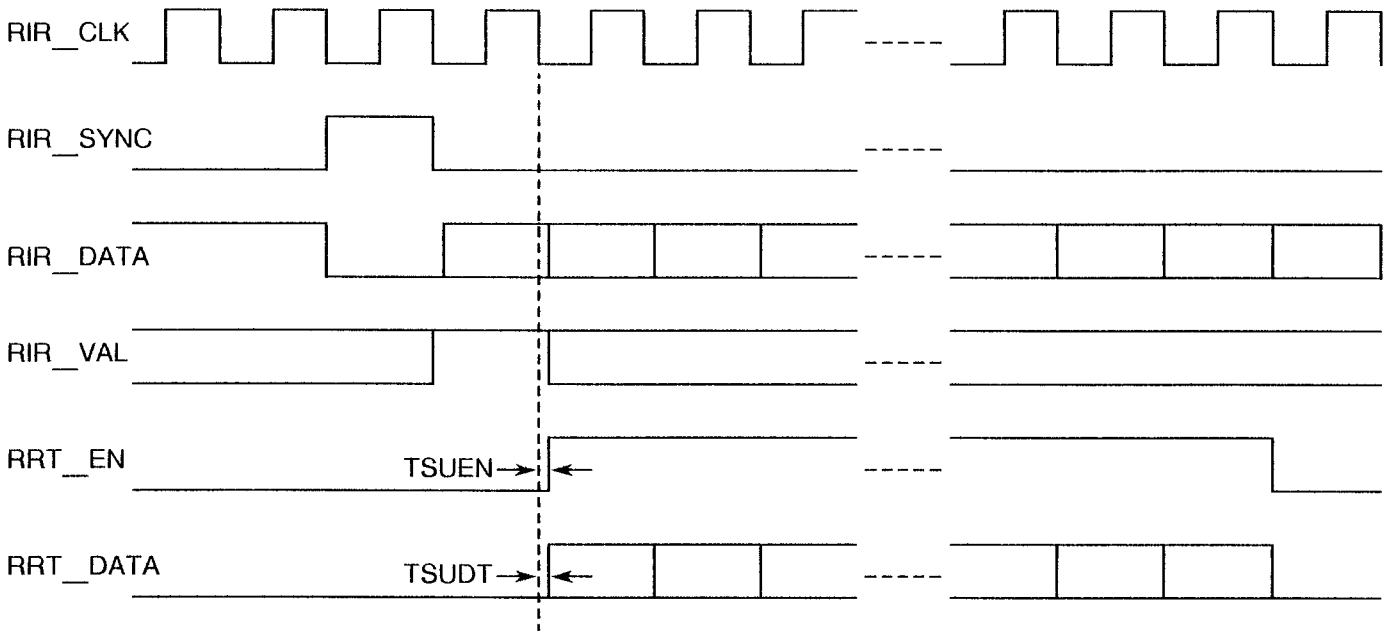
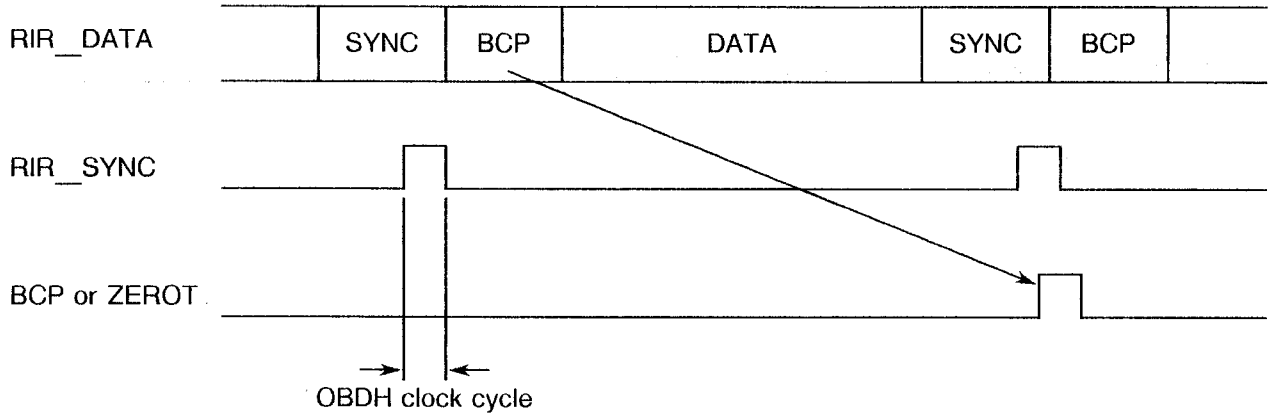


FIGURE 3(b) - TRUTH TABLE (CONTINUED)

TIMING WAVEFORMS (CONTINUED)

BROADCAST PULSES TIMING



PROCESSOR TO STANDARD RBI CHIP WRITE CYCLE

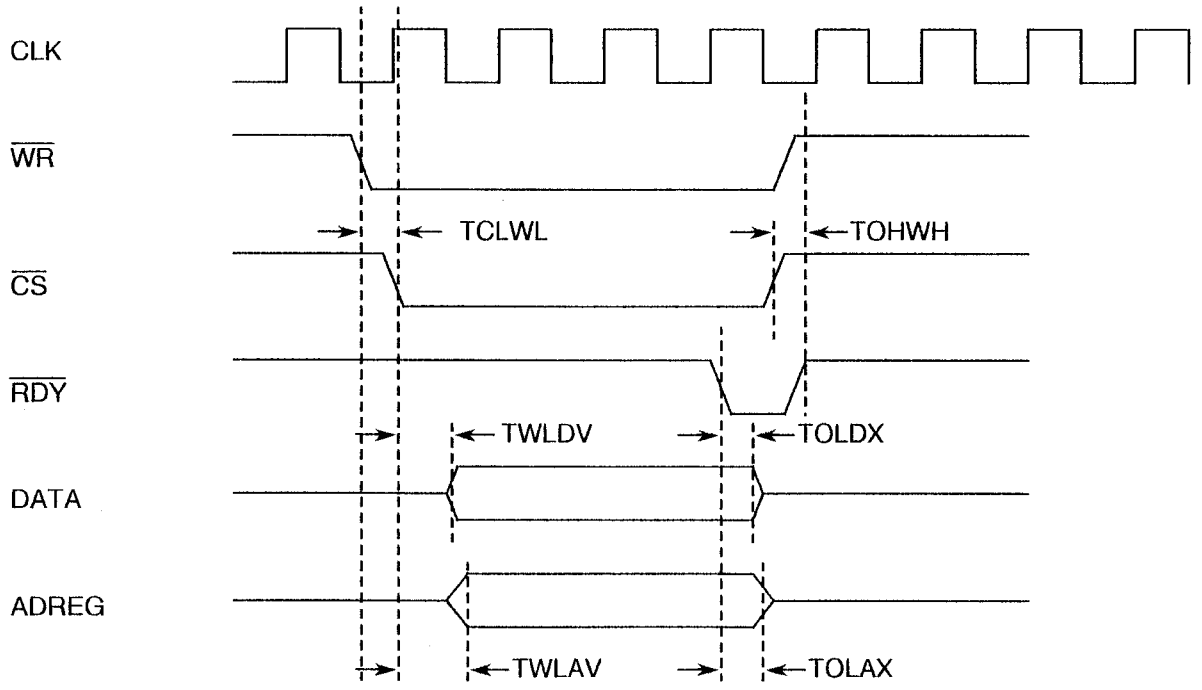


FIGURE 3(b) - TRUTH TABLE (CONTINUED)

TIMING WAVEFORMS (CONTINUED)

PROCESSOR TO STANDARD RBI CHIP READ CYCLE

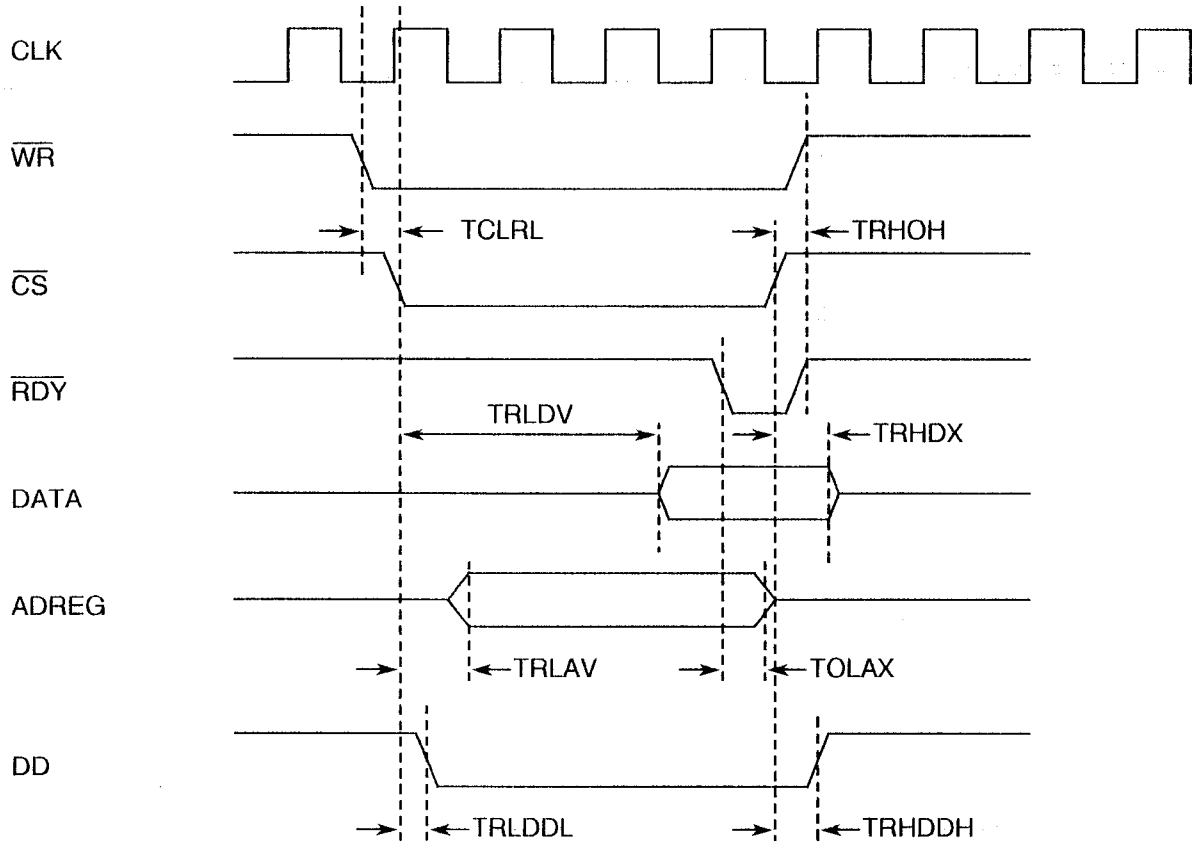
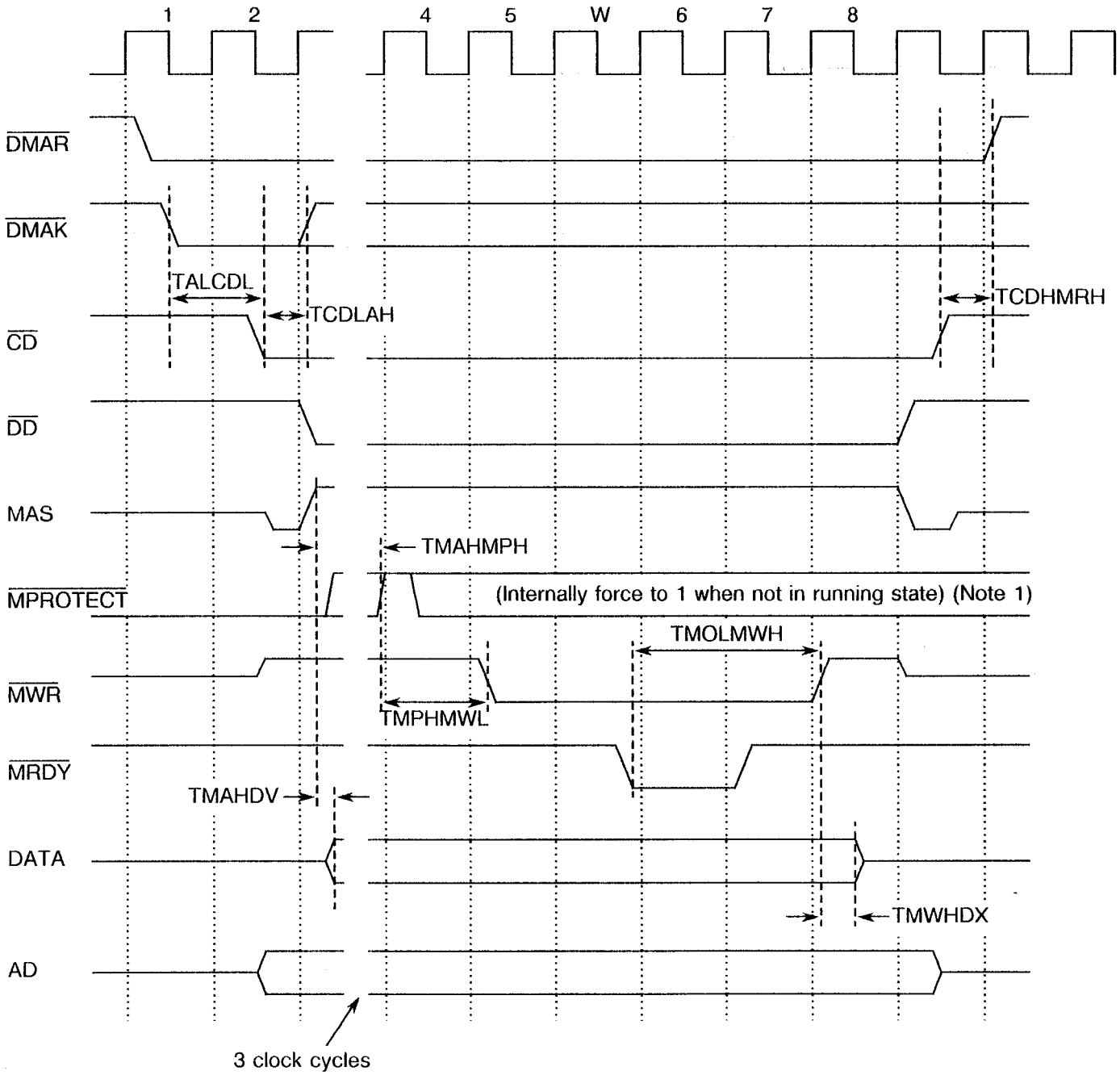


FIGURE 3(b) - TRUTH TABLE (CONTINUED)

TIMING WAVEFORMS (CONTINUED)

RBI CHIP TO MEMORY WRITE CYCLE



NOTES

1. TMAHMPH is fixed to 3 clock cycles, even if MPROTECTn is pulled to V_{DD} or if the component is not in a "running state".

FIGURE 3(b) - TRUTH TABLE (CONTINUED)

TIMING WAVEFORMS (CONTINUED)

RBI CHIP TO MEMORY READ CYCLE

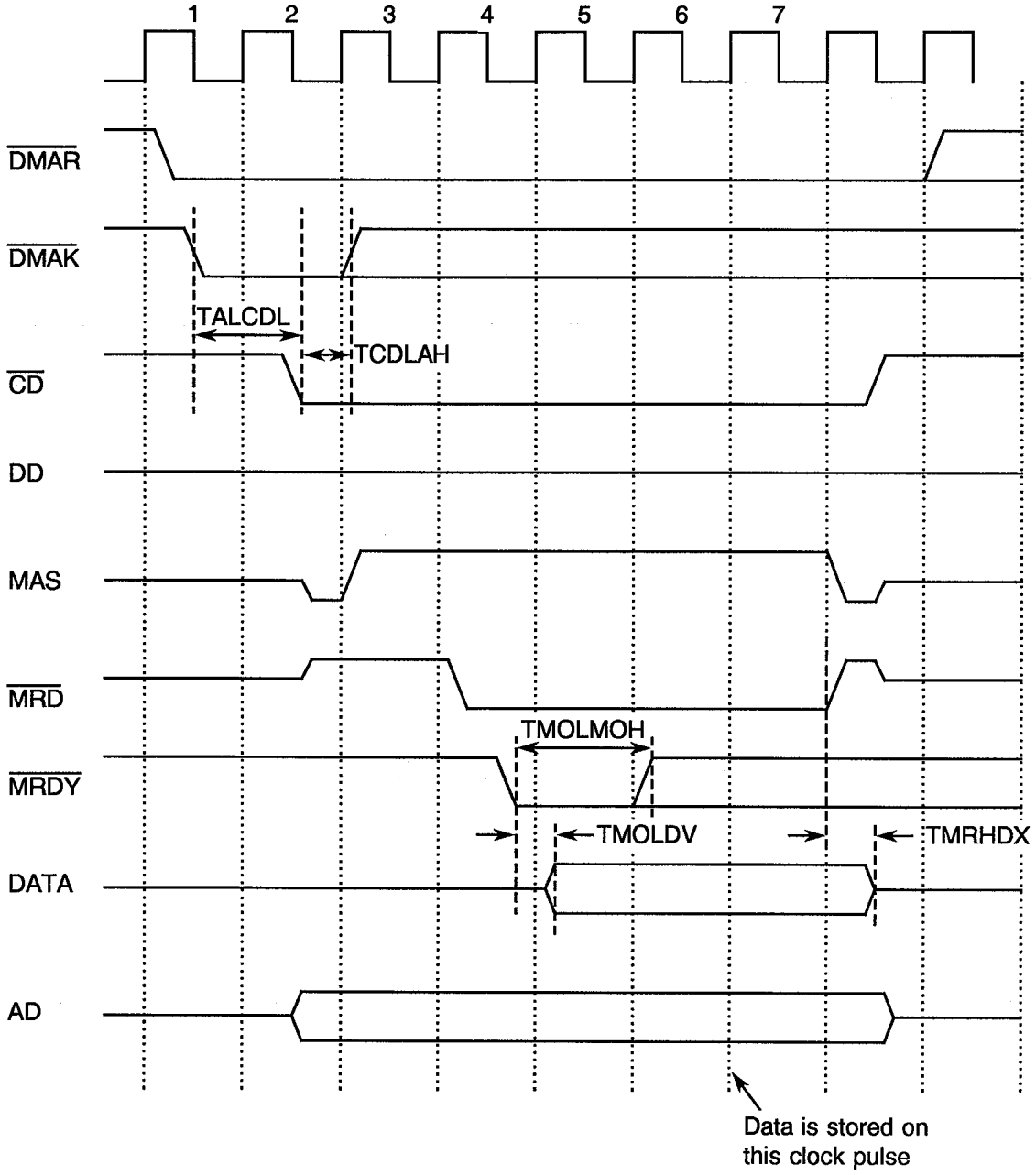


FIGURE 3(c) - CIRCUIT DESCRIPTION

Low Level Protocol Management Functions

The standard RBI chip is fully compliant with the OBDH low-level and RBI-level protocol and handles the 6 signals provided at the Digital Bus Interface to receive interrogations and transmit responses.

The receiver function acquires serial data from the RIR-DATA line. Each interrogation is checked for valid LITTON CODE and correct number of bits (both performed by the DBU) and correct parity (performed by the RBI chip). If the destination address carried by the interrogation matches the ICU address and the interrogation is valid, it is passed to the decoder for further processing.

The BCP management function extracts the active BCP pulses from each valid interrogation and activates the corresponding BCP signal lines on the BCP output interface. The BCP management function is also in charge of detecting the BCP3-BCP2 sequence to be used for on-board time synchronisation.

The emitter function is in charge of response generation. It ensures that for each interrogation addressed to the ICU, a response is generated with correct type and timing.

RBI Protocol Management Functions

All interrogations defined by the RBI-level protocol are recognised by the standard RBI chip. If these interrogations do not need software support, they are completely handled by the standard RBI chip, which is the case for most of the interrogations.

The interrogation decoder function is in charge of interrogation decoding and semantic verification, e.g. whether the interrogation is authorised in the present ICU state.

The state transition function handles all state transitions commanded by the OBDH bus master.

The high-level interface function manages the interface between the RBI-level and high level of the OBDH protocol.

The memory transfer function handles the access to the ICU MEMORY. This includes loading of START ADDRESS, PAGE ADDRESS and LENGTH REGISTERS as well as the processing of the instructions to reset the PAGE ADDRESS and DMA.

The microprocessor interface establishes and controls the communication with the ICU microprocessor.

The memory interface establishes and controls the communication with the ICU MEMORY.

Timer Functions

The standard RBI Chip provides a timer function compatible with the specification for instrument on-board time handling. The timer is a 43 bit counter incremented with the OBDH clock signal which has a nominal frequency of 524288 Hz.

For time synchronisation, the timer is reset on a BCP3-BCP2 sequence reception if previously authorised by the ICU software.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

The addition of the offset loaded by the processor into the OBT UPDATE REGISTER (usually derived from the synchronisation macrocommand) to the current on-board time value is performed internally by the standard RBI chip when bits 16 to 31 of the OBT UPDATE REGISTER are loaded.

The standard RBI chip provides 2 separate time registers (43 bits each) for datation of asynchronous events. One of these registers is also used for time readout by the microprocessor and for synchronisation. The maximum error introduced by the datation function is 1 LSB (1.9µs nominal).

The standard RBI chip provides a WATCHDOG function with a programmable timeout.

The WATCHDOG is based on a 12 bit down-counter, clocked by the CLK256 signal derived from the OBDH bus. The WATCHDOG timeout is programmable by the microprocessor. If the counter reaches zero, and if enabled by the ICU software, an interrupt to the microprocessor is generated. At the same time the RUNNING bit of the RBI status word is reset independently of any microprocessor activity.

The WATCHDOG is disabled in INIT, RESET and WAIT states. It should be enabled by the ICU software when the ICU enters RUNNING state after START. When the ICU enters RUNNING state from WAIT state, the WATCHDOG status will be automatically restored to the state before the SUSPEND command was received and resume counting where it was stopped if it was enabled.

The standard RBI chip is able to detect loss of OBDH communication. A clock loss detection circuit activates an output signal if no OBDH clock has been detected for a period of 160 system clock pulses whenever the current ICU state. The actual timeout value is dependent on the chip clock frequency (5.0MHz nominal). The timeout signal can be used as an interrupt to the microprocessor to trigger transition to a contingency mode.

Registers

The OBDH protocol defines 6 different registers where the OBDH bus master has write access to initiate a particular OBDH operation. These registers are implemented on the standard RBI chip. They are all accessible in read mode by the ICU software with the exception of the DATA REGISTER involved in DMA.

The RBI STATUS REGISTER implemented and maintained by the chip takes a specific place in the OBDH protocol. It is used both to inform the OBDH bus master about the current ICU state and possible errors and to define the ICU behaviour when receiving an interrogation.

Two additional registers, BASE ADDRESS and CONFIGURATION, are implemented for application-specific RBI configuration. Both registers are accessible by the ICU software in read and write mode.

RBI STATUS REGISTER (0)

The RBI STATUS REGISTER is implemented on-chip. To achieve compatibility with the OBDH protocol, the standard RBI chip automatically maps the STATUS REGISTER into the memory when accessed by the OBDH bus master in response to interrogations reading from CCA address 0 (Immediate Read or Read Block).

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

The STATUS REGISTER is maintained by the standard RBI chip in accordance with the low-level/RBI-level specification of the OBDH protocol. STATUS REGISTER bits 0 to 8 are allocated by the OBDH protocol. These bits cannot be modified by the processor directly. Indirectly, the processor can modify those STATUS REGISTER bits by software. Details are described in the software interface section. Bits 9 and 10 are set by the RBI chip to flag errors detected by the RBI chip itself. The error codes are shown in the table below:

ERROR CODES

9 10	Definition
0 0	No anomaly
0 1	Illegal access to protected memory area flagged by MPROTECT signal
1 0	DMA access not granted
1 1	External or WATCHDOG error. If the RUNNING BIT was set then this bit has been automatically reset.

Error detection is always active and, on detection of an error, the previous error indication is overwritten. The error bits are cleared on an immediate read from the RBI STATUS REGISTER.

Bits 11 to 15 of the STATUS REGISTER are not modified by the standard RBI chip itself and should be maintained by the ICU software via write access to the STATUS REGISTER.

The RBI STATUS REGISTER can be read by the ICU software at any time.

INSTRUCTION-TO-RBI REGISTER (1)

This 16 bit register is used to store the parameters of INSTRUCTION-TO-RBI interrogations which need software support for processing. These are:

- RESET ICU
- START ICU

The parameter provided with these interrogations (bits 15 to 30 of the interrogation word) is loaded into the INSTRUCTION-TO-RBI REGISTER.

All other INSTRUCTION-TO-RBI interrogations are directly processed by the chip without modification of the INSTRUCTION-TO-RBI REGISTER contents.

INSTRUCTION-TO-USER REGISTER (2)

This 16 bits register is used to handle INSTRUCTION-TO-USER interrogations.

On reception of an INSTRUCTION-TO-USER interrogation, the RBI chip stores bits 15 to 30 of the interrogation word in the INSTRUCTION-TO-USER REGISTER.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

BASE ADDRESS REGISTER (3)

The BASE ADDRESS REGISTER (16 bit) is used to store the CCA PAGE ADDRESS value.

The BASE ADDRESS REGISTER is loaded by the ICU software and used by the RBI chip to calculate the physical memory address for IMMEDIATE READ and RESET PAGE ADDRESS interrogation processing.

START ADDRESS REGISTER (4)

The START ADDRESS REGISTER is used to calculate the address used during DMA block transfer.

The START ADDRESS REGISTER is loaded by a SET START ADDRESS interrogation and is automatically incremented by 2 after each AS16 read-block or CS16 write-block interrogation.

LENGTH REGISTER (5)

The LENGTH REGISTER is used to determine the end of a DMA block transfer.

The LENGTH REGISTER is loaded by a SET LENGTH interrogation and is automatically decremented by 1 after each AS16 read-block or CS16 write-block interrogation.

CONFIGURATION REGISTER (6)

The CONFIGURATION REGISTER allows configuration setting by the ICU microprocessor and RBI interface status retrieval.

The organisation and functionality of the CONFIGURATION REGISTER is defined in the software interface section.

PAGE ADDRESS REGISTER (7)

The PAGE ADDRESS REGISTER (16 bit) is used by the RBI chip to calculate the physical memory addresses for READ BLOCK and WRITE BLOCK interrogation handling (DMA).

The PAGE ADDRESS REGISTER is loaded by a SET PAGE ADDRESS or a RESET PAGE ADDRESS interrogation. The PAGE ADDRESS value can be modified by the OBDH bus master at any moment except when the DMA BUSY bit is set.

WATCHDOG REGISTER (8)

The WATCHDOG REGISTER contents define the timeout of the on-chip watchdog.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

EXTERNAL FREEZE REGISTERS (9 - 0 Eh)

The 2 external FREEZE REGISTERS (3 × 16-bit words each) are used to latch the time counter value on the occurrence of external trigger signals.

EXTERNAL FREEZE REGISTER 1 is loaded with the current ON-BOARD TIME value at the occurrence of an $\overline{\text{EXTFR1}}$ trigger signal.

EXTERNAL FREEZE REGISTER 2 is loaded with the current ON-BOARD TIME value at the occurrence of an $\overline{\text{EXTFR2}}$ trigger signal or by ICU software command.

The freeze operation is performed by the chip in 1 OBDH clock pulse time. After a freeze command, this delay should be respected by software before reading the register in order to acquire a stable value.

EXTERNAL FREEZE REGISTER 2 is also used for time synchronisation, to be loaded by the microprocessor for time offset addition to the timer counter.

FIGURE 3(d) - FUNCTIONAL DIAGRAM

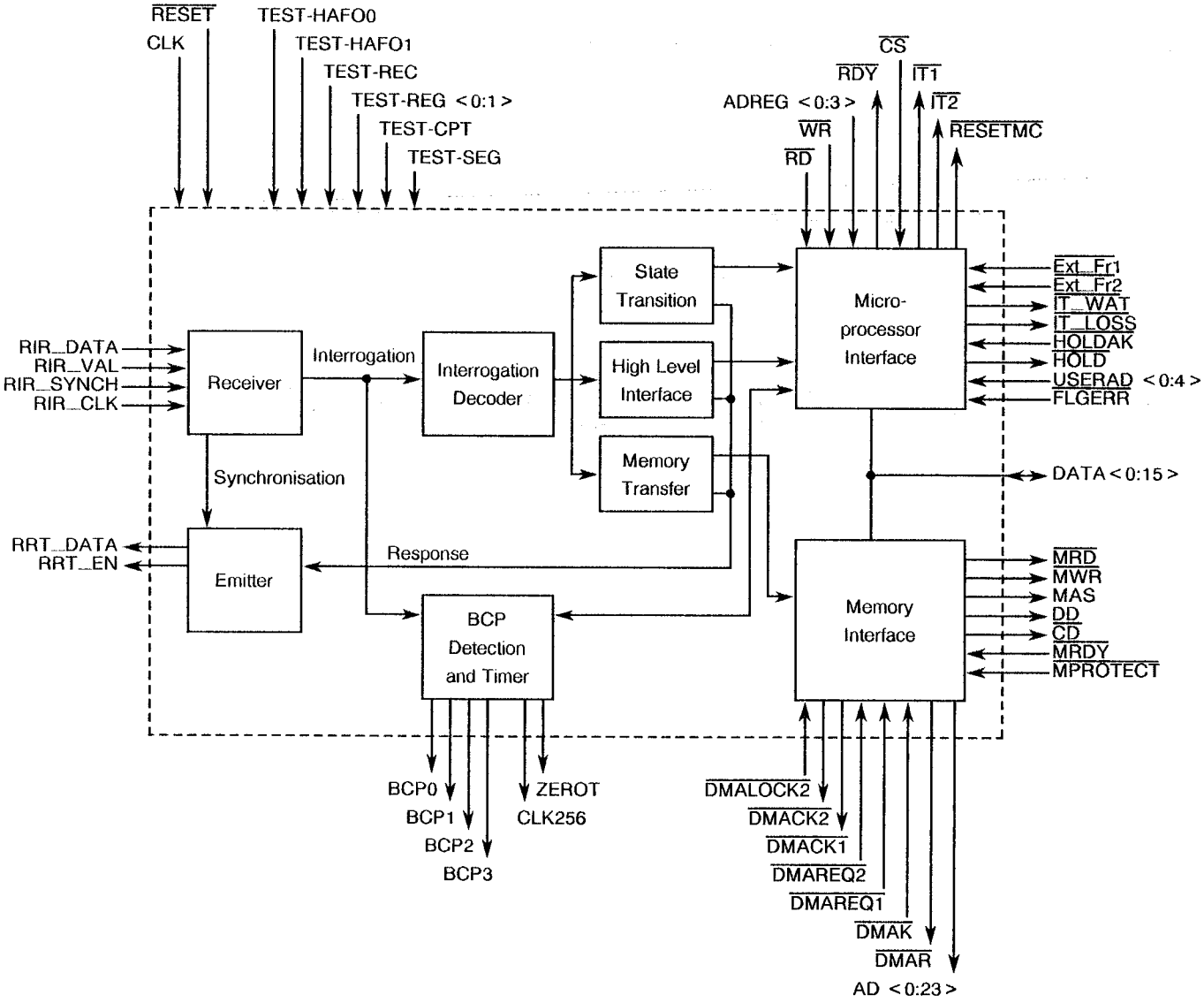
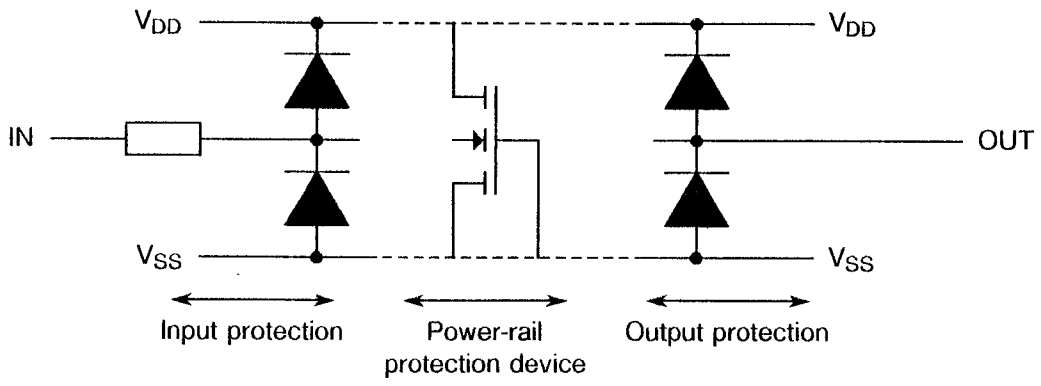


FIGURE 3(e) - INPUT/OUTPUT PROTECTION NETWORKS



NOTES

1. 1 input protection for each input, 1 output protection for each output, 4 power-rail protection devices for each die.

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

TCLWL = $\overline{WR}$ low to $\overline{CS}$ low time.
TWLDV = $\overline{WR}$ and $\overline{CS}$ low to DATA valid time.
TWLAV = $\overline{WR}$ and $\overline{CS}$ low to ADDRESS valid time.
TOLDX = $\overline{RDY}$ low to DATA undefined time.
TOLAX = $\overline{RDY}$ low to ADDRESS undefined time.
TOHWH = $\overline{WR}$ or $\overline{CS}$ high to $\overline{RDY}$ high time.
TCLRL = $\overline{CS}$ low to $\overline{RD}$ low time.
TRLDV = $\overline{CS}$ and $\overline{RD}$ low to DATA valid time.
TRLAV = $\overline{CS}$ and $\overline{RD}$ low to ADDRESS valid time.
TRHDDH = $\overline{CS}$ or $\overline{RD}$ high to DD high time.
TRHOH = $\overline{CS}$ or $\overline{RD}$ high to $\overline{RDY}$ high time.
TRHDX = $\overline{CS}$ or $\overline{RD}$ high to DATA not valid time.
TRLDDL = $\overline{RD}$ low to DD low time.
TALCDL = $\overline{DMAK}$ low to $\overline{CD}$ low time.
TCDLAH = $\overline{CD}$ low to $\overline{DMAK}$ high time.
TMAHMPH = MAS high to $\overline{MPROTECT}$ high time.
TMPHMWL = $\overline{MPROTECT}$ high to $\overline{MWR}$ low time.
TMAHDV = MAS high to DATA valid time.
TMOLMWH = $\overline{MRDY}$ low to $\overline{MWR}$ high time.
TMWHDX = $\overline{MWR}$ high to DATA undefined time.
TCDHMRH = $\overline{CD}$ high to $\overline{DMAR}$ high time.
TALCDL = $\overline{DMAK}$ low to $\overline{CD}$ low time.
TCDLAH = $\overline{CD}$ low to $\overline{DMAK}$ high time.
TMOLDV = $\overline{MRDY}$ low to DATA valid time.
TMOLMOH = $\overline{MRDY}$ pulse duration.
TMRHDX = $\overline{MRD}$ high to DATA undefined.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

(a) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during qualification and maintenance of qualification.
(b) Para. 5.2.2, Total Dose Irradiation Testing: If specified in a Purchase Order, shall be performed during procurement on a lot acceptance basis at the total dose irradiation level specified in the Purchase Order.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

(a) Para. 7.1.1(a), "High Temperature Reverse Bias" test and subsequent electrical measurements related to this test shall be omitted.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 10 grammes.

4.3.3 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESA/SCC Basic Specification No. 9000. The test conditions shall be as follows:-

Applied Force: 1.0 ± 0.1 Newtons, 3 bends at 45°.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body and the lids shall be pre-form soldered.

4.4.2 Lead Material and Finish

The lead material shall be Type 'D' with Type '2' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

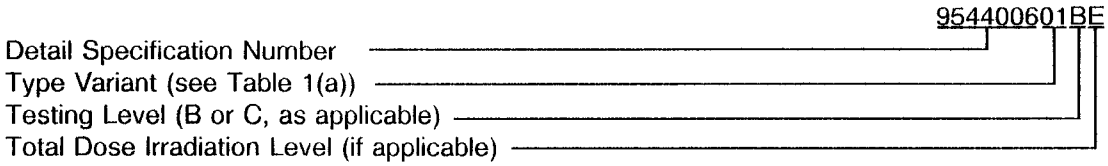
(c) Traceability Information.

4.5.2 Lead Identification

An index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



The Total Dose Irradiation Level designation shall be added for those devices for which a sample has been successfully tested to the level in question. For these devices, a code shall be added in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ °C and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for H.T.R.B. Burn-in

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for power burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for H.T.R.B. Burn-in

Not applicable.

4.7.5 Electrical Circuits for Power Burn-in

A circuit for use in performing the power burn-in test is shown in Figure 5(b) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
1 to 20	V_{SS} and V_{DD} Continuity	-	-	4(a)	I_{OUT} = 10µA V_{DD} = V_{SS} = 0V (Pins 1-2-14-15-30-31-41-42-55-56-65-66-67-79-80-105-106-129-130-132 to 68 + 69)	-	100	mV
21	Functional Test 1 (Min. V_{DD} Voltage)	-	-	-	Verify Device Operation with Load V_{IL} = 0.5V, V_{IH} = 4.0V V_{OL} = 1.0V, V_{OH} = 3.5V f = 5.0MHz I_{OUT} = ± 1.0mA C_L = 100pF(+ 0 − 20%) V_{DD} = 4.5V, V_{SS} = 0V Note 1	-	-	-
22	Functional Test 2 (Max. V_{DD} Voltage)	-	-	-	Verify Device Operation with Load V_{IL} = 0.5V, V_{IH} = 4.5V V_{OL} = 1.0V, V_{OH} = 4.5V f = 5.0MHz I_{OUT} = ± 1.0mA C_L = 100pF(+ 0 − 20%) V_{DD} = 5.5V, V_{SS} = 0V Note 1	-	-	-
23	Quiescent Current	I_{DD}	3005	4(b)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V All Outputs Open Note 2	-	800	µA
24 to 73	Input Current Low Level	I_{IL}	3009	4(c)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 3-4-5-6-7-16-17-18-19-20-53-54-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-82-83-84-85-86-88-89-90-100-102-104-108-112-113-114-115-116-119-120-124-125-126-127)	-	− 1.0	µA

NOTES: See Page 39.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
74 to 123	Input Current High Level	I_{IH}	3010	4(d)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 3-4-5-6-7-16-17-18-19-20-53-54-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-82-83-84-85-86-88-89-90-100-102-104-108-112-113-114-115-116-119-120-124-125-126-127)	-	1.0	µA
124 to 186	Output Voltage Low Level	V_{OL}	3007	4(e)	V_{IL} = 0.5V, V_{IH} = 5.0V I_{OL} (Under Test) = −4.0mA All Other Outputs Open V_{DD} = 4.5V, V_{SS} = 0V (Pins 8-9-10-11-12-13-22-23-24-25-26-27-28-29-32-33-34-35-36-37-38-39-44-45-46-47-48-49-50-51-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-91-92-94-95-96-97-98-103-109-110-111-117-118-122-123-128-131) (Note 3)	-	400	mV
187 to 249	Output Voltage High Level 1	V_{OH1}	3006	4(f)	V_{IL} = 0.5V, V_{IH} = 4.0V I_{OH} (Under Test) = 4.0mA All Other Outputs Open V_{DD} = 4.5V, V_{SS} = 0V (Pins 8-9-10-11-12-13-22-23-24-25-26-27-28-29-32-33-34-35-36-37-38-39-44-45-46-47-48-49-50-51-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-91-92-94-95-96-97-98-103-109-110-111-117-118-122-123-128-131) (Note 3)	3.9	-	V

NOTES: See Page 39.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
250 to 312	Output Voltage High Level 2	V_{OH2}	3006	4(f)	V_{IL} = 0.5V, V_{IH} = 4.0V I_{OH} (Under Test) = 500µA All Other Outputs Open V_{DD} = 4.5V, V_{SS} = 0V (Pins 8-9-10-11-12-13-22-23-24-25-26-27-28-29-32-33-34-35-36-37-38-39-44-45-46-47-48-49-50-51-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-91-92-94-95-96-97-98-103-109-110-111-117-118-122-123-128-131) (Note 3)	4.2	-	V
313 to 362	Threshold Voltage Low Level	V_{THN}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V V_{OL} = 1.0V, V_{OH} = 3.5V I_{OUT} = ±1.0mA C_L = 100pF(+ 0 − 20%) (Pins 3-4-5-6-7-16-17-18-19-20-53-54-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-82-83-84-85-86-88-89-90-100-102-104-108-112-113-114-115-119-120-124-125-126-127, Note 4)	1.35	-	V
363 to 412	Threshold Voltage High Level 1	V_{THP1}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V V_{OL} = 1.0V, V_{OH} = 3.5V I_{OUT} = ±1.0mA C_L = 100pF(+ 0 − 20%) (Pins 3-4-5-6-7-16-17-18-19-20-53-54-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-82-83-84-85-86-88-89-90-100-102-104-108-112-113-114-115-119-120-124-125-126-127, Note 5)	-	3.2	V
413 to 462	Threshold Voltage High Level 2	V_{THP2}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V V_{OL} = 1.0V, V_{OH} = 4.5V I_{OUT} = ±1.0mA C_L = 100pF(+ 0 − 20%) (Pins 3-4-5-6-7-16-17-18-19-20-53-54-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-82-83-84-85-86-88-89-90-100-102-104-108-112-113-114-115-119-120-124-125-126-127, Note 5)	-	3.2	V

NOTES: See Page 39.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
463 to 560	Input/Output Clamp Voltage (to V_{SS})	V_{IC1}	3022	4(h)	I_{IN} = − 100uA V_{DD} = V_{SS} = 0V (Pins 3-4-5-6-7-8-9-10-11-12-13-16-17-18-19-20-22-23-24-25-26-27-28-29-32-33-34-35-36-37-38-39-44-45-46-47-48-49-50-51-53-54-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-82-83-84-85-86-88-89-90-91-92-94-95-96-97-98-100-102-103-104-108-109-110-111-112-113-114-115-116-117-118-119-120-122-123-124-125-126-127-128-131)	-	− 2.0	V
561 to 658	Input/Output Clamp Voltage (to V_{DD})	V_{IC2}	3022	4(h)	I_{IN} = 100uA V_{DD} = V_{SS} = 0V (Pins 3-4-5-6-7-8-9-10-11-12-13-16-17-18-19-20-22-23-24-25-26-27-28-29-32-33-34-35-36-37-38-39-44-45-46-47-48-49-50-51-53-54-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-82-83-84-85-86-88-89-90-91-92-94-95-96-97-98-100-102-103-104-108-109-110-111-112-113-114-115-116-117-118-119-120-122-123-124-125-126-127-128-131)	-	2.0	V
659 to 685	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	3006	4(i)	V_{IN} (3-State Control) = Note 6 V_{OUT} (Under Test) = 0V All Other Outputs Open V_{DD} = 5.5V, V_{SS} = 0V (Pins 22-23-24-25-26-27-28-29-32-33-34-35-36-37-38-39-44-45-46-47-48-49-50-51-91-92-94)	-	− 10	µA

NOTES: See Page 39.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
686 to 712	Output Leakage Current Third State (High Level Applied)	I_{OZH}	3006	4(i)	V_{IN} (3-State Control) = Note 6 V_{OUT} (Under Test) = 5.5V All Other Outputs Open V_{DD} = 5.5V, V_{SS} = 0V (Pins 22-23-24-25-26-27-28-29-32-33-34-35-36-37-38-39-44-45-46-47-48-49-50-51-91-92-94)	-	10	µA
713	Supply Current	I_{DDS}	3005	4(b)	V_{DD} = 5.5V, V_{SS} = 0V f = 1.0MHz C_L = 100pF(+ 0 − 20%) Note 7	-	4.0	mA

NOTES

1. Test files used 'tst.h', 'tst.t', 'tst.reg' and 'tst.ch' generated from the VECTORGEN source files 'tst.c' and 'tst.mt'.

   65 967 vectors providing a fault coverage of 94.66%.
2. Measurement is performed with the device being initialised for both functional tests, using a functional test pattern, stopped at Vector 7. Total combined current for all V_{DD} pins.
3. The output pin under test is configured into correct state for the measurement using a functional test pattern on the inputs which produce a low or high at the pin, as appropriate.
4. Minimum value of pin group.
5. Maximum value of pin group.
6. The device is configured using a functional test pattern stopped at Vector 9, so that the pin under test is in the Third-State condition for the measurement. The measurement includes the input currents I_{IL} and I_{IH}.
7. Average current during a functional test pattern with timing (loop from Vector 1 to Vector 922).
8. Guaranteed but not tested. Characterised after major process changes.
9. Guaranteed but not tested (simulated value without load).

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
714 to 762	Input Capacitance 1	C_{IN1}	3012	4(j)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 8 (Pins 3-4-5-6-7-16-17-18-19-20-53-54-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-82-83-84-85-86-88-89-90-102-104-108-112-113-114-115-116-119-120-124-125-126-127)	-	5.0	pF
763	Input Capacitance 2	C_{IN2}	3012	4(j)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 8 (Pin 100)	-	10	pF
764 to 790	Input/Output Capacitance	$C_{IN/OUT}$	3012	4(j)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 8 (Pins 22-23-24-25-26-27-28-29-32-33-34-35-36-37-38-39-44-45-46-47-48-49-50-51-91-92-94)	-	10	pF
791 to 827	Output Capacitance	C_{OUT}	3012	4(j)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 8 (Pins 8-9-10-11-12-13-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-95-96-97-98-103-109-110-111-117-118-122-123-128-131)	-	10	pF
828 to 829	Input Rise and Fall Time	t_{r1}/t_{f1}	3004	-	Note 9	-	100	ns
830 to 831	$\overline{WR}$ and $\overline{CS}$ Low to Data Valid	TWLDV	3004	-	Note 9	-	200	ns
832 to 833	$\overline{WR}$ and $\overline{CS}$ Low to Address Valid	TWLAV	3004	-	Note 9	-	200	ns

NOTES: See Page 39.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
834 to 835	$\overline{RDY}$ Low to Data Undefined	TOLDX	3004	-	Note 9	0	-	ns
836 to 837	$\overline{RDY}$ Low to Address Undefined	TOLAX	3004	-	Note 9	0	-	ns
838 to 839	$\overline{WR}$ or $\overline{CS}$ High to RDY High	TOHWH	3004	-	Note 9	-	37	ns
840 to 841	$\overline{CS}$ and $\overline{RD}$ Low to Data Valid	TRLDV	3004	-	Note 9	-	668	ns
842 to 843	$\overline{CS}$ and $\overline{RD}$ Low to Address Valid	TRLAV	3004	-	Note 9	-	200	ns
844 to 845	$\overline{CS}$ or $\overline{RD}$ High to DD High	TRHDDH	3004	-	Note 9	-	28	ns
846 to 847	$\overline{CS}$ or $\overline{RD}$ High to $\overline{RDY}$ High	TRHOH	3004	-	Note 9	-	37	ns
848 to 849	$\overline{CS}$ or $\overline{RD}$ High to Data Not Valid	TRHDX	3004	-	Note 9	9.0	36	ns
850 to 851	$\overline{RD}$ Low to DD Low	TRLDDL	3004	-	Note 9	-	26	ns
852 to 853	$\overline{DMAK}$ Low to $\overline{CD}$ Low	TALCDL	3004	-	Note 9	-	562	ns
854 to 855	$\overline{CD}$ Low to $\overline{DMAK}$ High	TCDLAH	3004	-	Note 9	100	-	ns
856 to 857	MAS High to $\overline{MPROTECT}$ High	TMAHMPH	3004	-	Note 9	-	850	ns

NOTES: See Page 39.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
858 to 859	$\overline{\text{MPROTECT}}$ High to $\overline{\text{MWR}}$ Low	TMPHMWL	3004	-	Note 9	213	-	ns
860 to 861	MAS High to Data Valid	TMAHDV	3004	-	Note 9	-	158	ns
862 to 863	$\overline{\text{MRDY}}$ Low to $\overline{\text{MWR}}$ High	TMOLMWH	3004	-	Note 9	-	653	ns
864 to 865	$\overline{\text{MWR}}$ High to Data Undefined	TMWHDX	3004	-	Note 9	70	-	ns
866 to 867	$\overline{\text{CD}}$ High to $\overline{\text{DMAR}}$ High	TCDHMRH	3004	-	Note 9	-	136	ns
868 to 869	$\overline{\text{DMAK}}$ Low to $\overline{\text{CD}}$ Low	TALCDL	3004	-	Note 9	-	562	ns
870 to 871	$\overline{\text{CD}}$ Low to $\overline{\text{DMAK}}$ High	TCDLAH	3004	-	Note 9	100	-	ns
872 to 873	$\overline{\text{MRDY}}$ Low to Data Valid	TMOLDV	3004	-	Note 9	-	200	ns
874 to 875	$\overline{\text{MRDY}}$ Pulse Length	TMOLMOH	3004	-	Note 9	400	-	ns
876 to 877	$\overline{\text{MRDY}}$ to Data Undefined	TMRHDX	3004	-	Note 9	0	-	ns

NOTES: See Page 39.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
1 to 20	V_{SS} and V_{DD} Continuity	-	-	4(a)	I_{OUT} = 10µA V_{DD} = V_{SS} = 0V (Pins 1-2-14-15-30-31-41-42-55-56-65-66-67-79-80-105-106-129-130-132 to 68 + 69)	-	100	mV
21	Functional Test 1 (Min. V_{DD} Voltage)	-	-	-	Verify Device Operation with Load V_{IL} = 0.5V, V_{IH} = 4.0V V_{OL} = 1.0V, V_{OH} = 3.5V f = 5.0MHz I_{OUT} = ± 1.0mA C_L = 100pF(+ 0 − 20%) V_{DD} = 4.5V, V_{SS} = 0V Note 1	-	-	-
22	Functional Test 2 (Max. V_{DD} Voltage)	-	-	-	Verify Device Operation with Load V_{IL} = 0.5V, V_{IH} = 4.5V V_{OL} = 1.0V, V_{OH} = 4.5V f = 5.0MHz I_{OUT} = ± 1.0mA C_L = 100pF(+ 0 − 20%) V_{DD} = 5.5V, V_{SS} = 0V Note 1	-	-	-
23	Quiescent Current	I_{DD}	3005	4(b)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V All Outputs Open Note 2	-	5.0	mA
24 to 73	Input Current Low Level	I_{IL}	3009	4(c)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 3-4-5-6-7-16-17-18-19-20-53-54-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-82-83-84-85-86-88-89-90-100-102-104-108-112-113-114-115-116-119-120-124-125-126-127)	-	− 1.0	µA

NOTES: See Page 39.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
74 to 123	Input Current High Level	I_{IH}	3010	4(d)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 3-4-5-6-7-16-17-18-19-20-53-54-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-82-83-84-85-86-88-89-90-100-102-104-108-112-113-114-115-116-119-120-124-125-126-127)	-	1.0	µA
124 to 186	Output Voltage Low Level	V_{OL}	3007	4(e)	V_{IL} = 0.5V, V_{IH} = 5.0V I_{OL} (Under Test) = − 4.0mA All Other Outputs Open V_{DD} = 4.5V, V_{SS} = 0V (Pins 8-9-10-11-12-13-22-23-24-25-26-27-28-29-32-33-34-35-36-37-38-39-44-45-46-47-48-49-50-51-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-91-92-94-95-96-97-98-103-109-110-111-117-118-122-123-128-131) (Note 3)	-	400	mV
187 to 249	Output Voltage High Level 1	V_{OH1}	3006	4(f)	V_{IL} = 0.5V, V_{IH} = 4.0V I_{OH} (Under Test) = 4.0mA All Other Outputs Open V_{DD} = 4.5V, V_{SS} = 0V (Pins 8-9-10-11-12-13-22-23-24-25-26-27-28-29-32-33-34-35-36-37-38-39-44-45-46-47-48-49-50-51-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-91-92-94-95-96-97-98-103-109-110-111-117-118-122-123-128-131) (Note 3)	3.9	-	V

NOTES: See Page 39.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
250 to 312	Output Voltage High Level 2	V_{OH2}	3006	4(f)	V_{IL} = 0.5V, V_{IH} = 4.0V I_{OH} (Under Test) = 500µA All Other Outputs Open V_{DD} = 4.5V, V_{SS} = 0V (Pins 8-9-10-11-12-13-22-23-24-25-26-27-28-29-32-33-34-35-36-37-38-39-44-45-46-47-48-49-50-51-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-91-92-94-95-96-97-98-103-109-110-111-117-118-122-123-128-131) (Note 3)	4.2	-	V
313 to 362	Threshold Voltage Low Level	V_{THN}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V V_{OL} = 1.0V, V_{OH} = 3.5V I_{OUT} = ±1.0mA C_L = 100pF(+0−20%) (Pins 3-4-5-6-7-16-17-18-19-20-53-54-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-82-83-84-85-86-88-89-90-100-102-104-108-112-113-114-115-119-120-124-125-126-127, Note 4)	1.35	-	V
363 to 412	Threshold Voltage High Level 1	V_{THP1}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V V_{OL} = 1.0V, V_{OH} = 3.5V I_{OUT} = ±1.0mA C_L = 100pF(+0−20%) (Pins 3-4-5-6-7-16-17-18-19-20-53-54-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-82-83-84-85-86-88-89-90-100-102-104-108-112-113-114-115-119-120-124-125-126-127, Note 5)	-	3.2	V
413 to 462	Threshold Voltage High Level 2	V_{THP2}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V V_{OL} = 1.0V, V_{OH} = 4.5V I_{OUT} = ±1.0mA C_L = 100pF(+0−20%) (Pins 3-4-5-6-7-16-17-18-19-20-53-54-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-82-83-84-85-86-88-89-90-100-102-104-108-112-113-114-115-119-120-124-125-126-127, Note 5)	-	3.9	V

NOTES: See Page 39.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
463 to 560	Input/Output Clamp Voltage (to V_{SS})	V_{IC1}	3022	4(h)	I_{IN} = −100uA V_{DD} = V_{SS} = 0V (Pins 3-4-5-6-7-8-9-10-11-12-13-16-17-18-19-20-22-23-24-25-26-27-28-29-32-33-34-35-36-37-38-39-44-45-46-47-48-49-50-51-53-54-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-82-83-84-85-86-88-89-90-91-92-94-95-96-97-98-100-102-103-104-108-109-110-111-112-113-114-115-116-117-118-119-120-122-123-124-125-126-127-128-131)	-	−2.0	V
561 to 658	Input/Output Clamp Voltage (to V_{DD})	V_{IC2}	3022	4(h)	I_{IN} = 100uA V_{DD} = V_{SS} = 0V (Pins 3-4-5-6-7-8-9-10-11-12-13-16-17-18-19-20-22-23-24-25-26-27-28-29-32-33-34-35-36-37-38-39-44-45-46-47-48-49-50-51-53-54-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-82-83-84-85-86-88-89-90-91-92-94-95-96-97-98-100-102-103-104-108-109-110-111-112-113-114-115-116-117-118-119-120-122-123-124-125-126-127-128-131)	-	2.0	V
659 to 685	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	3006	4(i)	V_{IN} (3-State Control) = Note 6 V_{OUT} (Under Test) = 0V All Other Outputs Open V_{DD} = 5.5V, V_{SS} = 0V (Pins 22-23-24-25-26-27-28-29-32-33-34-35-36-37-38-39-44-45-46-47-48-49-50-51-91-92-94)	-	−10	µA

NOTES: See Page 39.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
686 to 712	Output Leakage Current Third State (High Level Applied)	I_{OZH}	3006	4(i)	V_{IN} (3-State Control) = Note 6 V_{OUT} (Under Test) = 5.5V All Other Outputs Open V_{DD} = 5.5V, V_{SS} = 0V (Pins 22-23-24-25-26-27-28-29-32-33-34-35-36-37-38-39-44-45-46-47-48-49-50-51-91-92-94)	-	10	µA
713	Supply Current	I_{DDS}	3005	4(b)	V_{DD} = 5.5V, V_{SS} = 0V f = 1.0MHz All Outputs Open C_L = 100pF(+ 0 – 20%) Note 7	-	7.0	mA

NOTES: See Page 39.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
828 to 829	Input Rise and Fall Time	t_{r1}/t_{f1}	3004	-	Note 9	-	100	ns
830 to 831	$\overline{WR}$ and $\overline{CS}$ Low to Data Valid	TWLDV	3004	-	Note 9	-	200	ns
832 to 833	$\overline{WR}$ and $\overline{CS}$ Low to Address Valid	TWLAV	3004	-	Note 9	-	200	ns
834 to 835	$\overline{RDY}$ Low to Data Undefined	TOLDX	3004	-	Note 9	0	-	ns
836 to 837	$\overline{RDY}$ Low to Address Undefined	TOLAX	3004	-	Note 9	0	-	ns
838 to 839	$\overline{WR}$ or $\overline{CS}$ High to RDY High	TOHWH	3004	-	Note 9	-	37	ns
840 to 841	$\overline{CS}$ and $\overline{RD}$ Low to Data Valid	TRLDV	3004	-	Note 9	-	668	ns
842 to 843	$\overline{CS}$ and $\overline{RD}$ Low to Address Valid	TRLAV	3004	-	Note 9	-	200	ns
844 to 845	$\overline{CS}$ or $\overline{RD}$ High to DD High	TRHDDH	3004	-	Note 9	-	28	ns
846 to 847	$\overline{CS}$ or $\overline{RD}$ High to $\overline{RDY}$ High	TRHOH	3004	-	Note 9	-	37	ns
848 to 849	$\overline{CS}$ or $\overline{RD}$ High to Data Not Valid	TRHDX	3004	-	Note 9	9.0	36	ns
850 to 851	$\overline{RD}$ Low to DD Low	TRLDDL	3004	-	Note 9	-	26	ns
852 to 853	$\overline{DMAK}$ Low to $\overline{CD}$ Low	TALCDL	3004	-	Note 9	-	562	ns

NOTES: See Page 39.

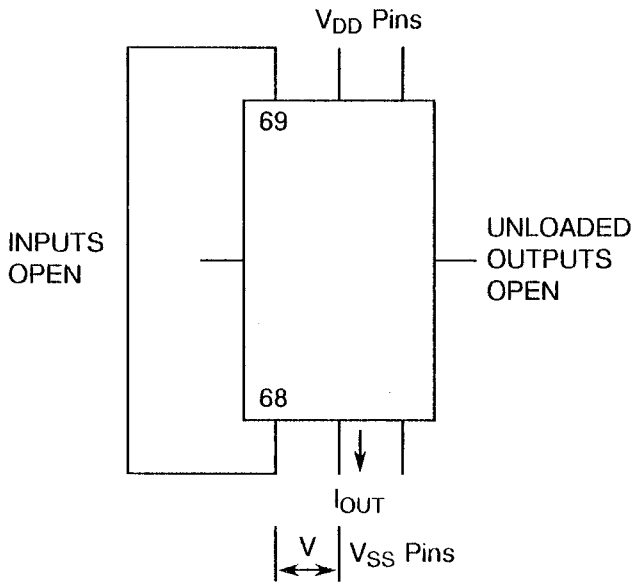
TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
854 to 855	$\overline{CD}$ Low to $\overline{DMAK}$ High	TCDLAH	3004	-	Note 9	100	-	ns
856 to 857	MAS High to $\overline{MPROTECT}$ High	TMAHMPH	3004	-	Note 9	-	850	ns
858 to 859	$\overline{MPROTECT}$ High to $\overline{MWR}$ Low	TMPHMWL	3004	-	Note 9	213	-	ns
860 to 861	MAS High to Data Valid	TMAHDV	3004	-	Note 9	-	158	ns
862 to 863	$\overline{MRDY}$ Low to $\overline{MWR}$ High	TMOLMWH	3004	-	Note 9	-	653	ns
864 to 865	$\overline{MWR}$ High to Data Undefined	TMWHDX	3004	-	Note 9	70	-	ns
866 to 867	$\overline{CD}$ High to $\overline{DMAR}$ High	TCDHMRH	3004	-	Note 9	-	136	ns
868 to 869	$\overline{DMAK}$ Low to $\overline{CD}$ Low	TALCDL	3004	-	Note 9	-	562	ns
870 to 871	$\overline{CD}$ Low to $\overline{DMAK}$ High	TCDLAH	3004	-	Note 9	100	-	ns
872 to 873	$\overline{MRDY}$ Low to Data Valid	TMOLDV	3004	-	Note 9	-	200	ns
874 to 875	$\overline{MRDY}$ Pulse Length	TMOLMOH	3004	-	Note 9	400	-	ns
876 to 877	$\overline{MRDY}$ to Data Undefined	TMRHDX	3004	-	Note 9	0	-	ns

NOTES: See Page 39.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - V_{SS}, V_{DD} CONTINUITY



NOTES
1. Each power pin tested separately.

FIGURE 4(b)(i) - QUIESCENT CURRENT

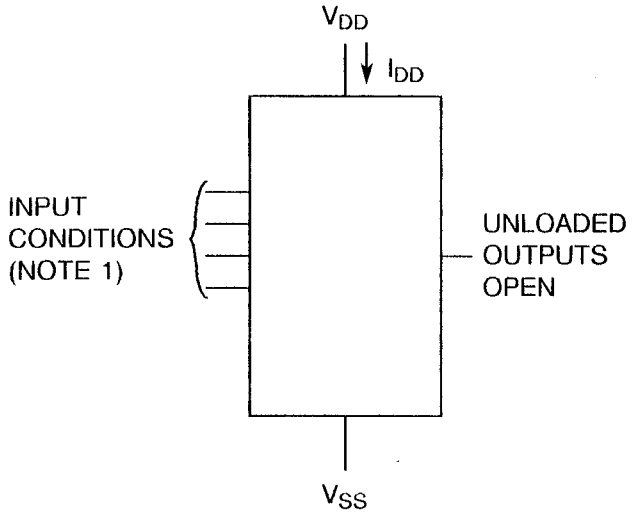
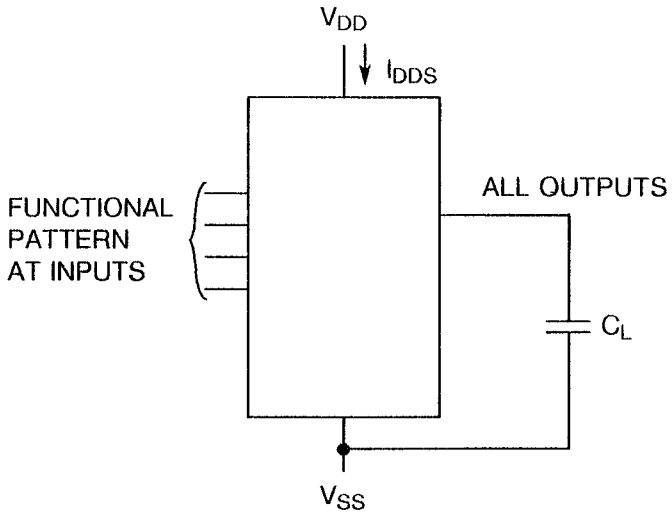


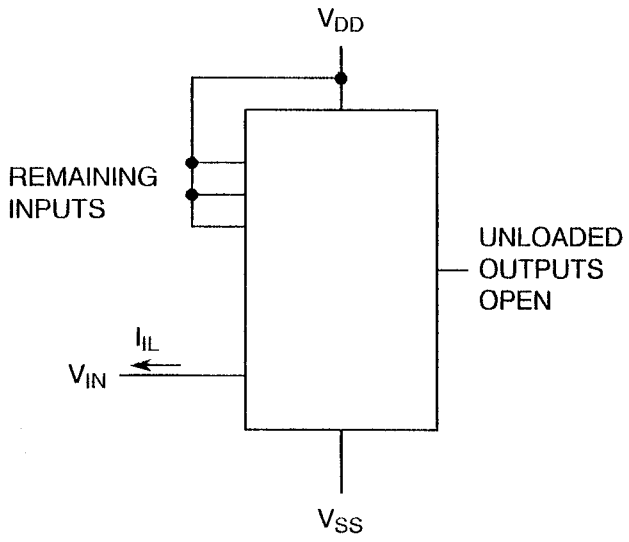
FIGURE 4(b)(ii) - SUPPLY CURRENT



NOTES
1. Input conditions as per Table 2.

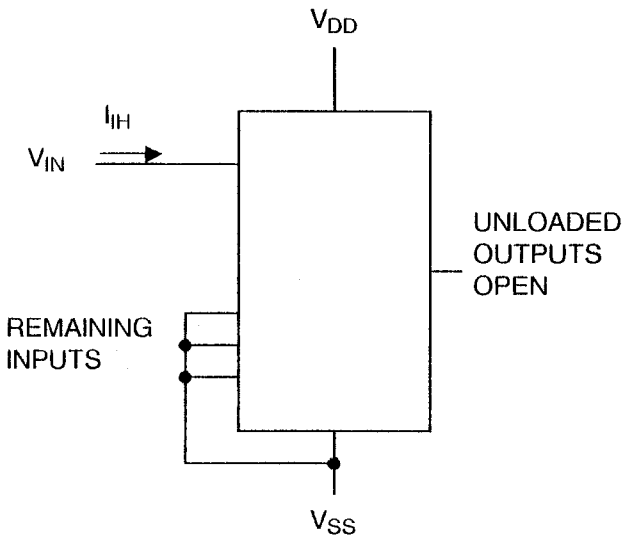
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(c) - INPUT CURRENT LOW LEVEL



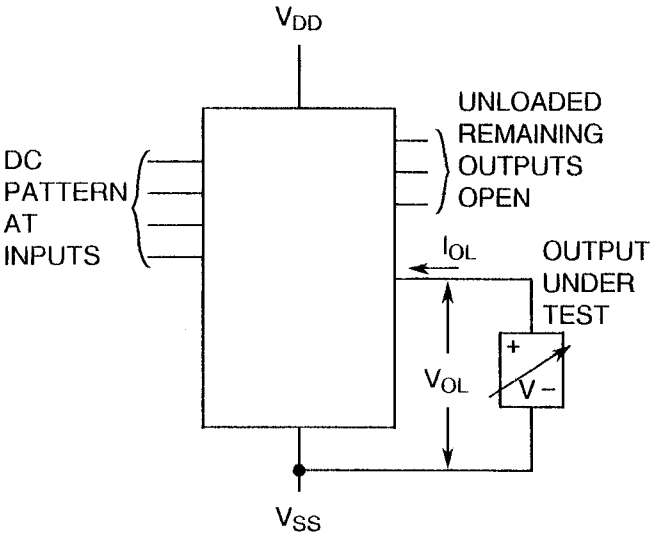
NOTES
1. Each input to be tested separately.

FIGURE 4(d) - INPUT CURRENT HIGH LEVEL



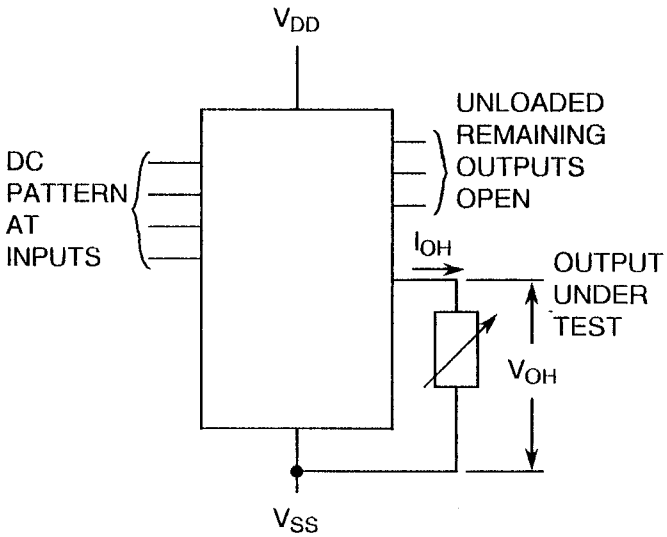
NOTES
1. Each input to be tested separately.

FIGURE 4(e) - OUTPUT VOLTAGE LOW LEVEL



NOTES
1. Each output to be tested separately.

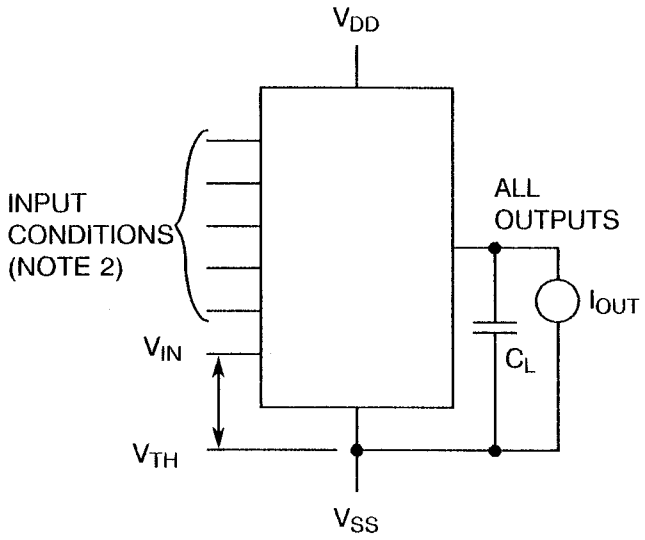
FIGURE 4(f) - OUTPUT VOLTAGE HIGH LEVEL



NOTES
1. Each output to be tested separately.

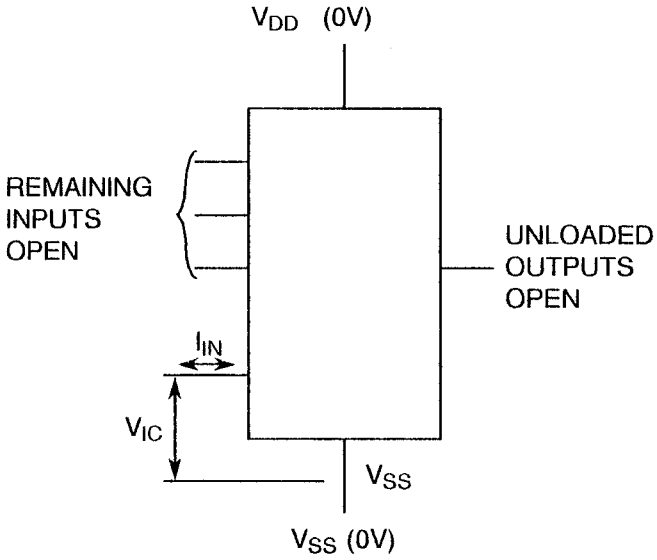
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(g) - THRESHOLD VOLTAGE



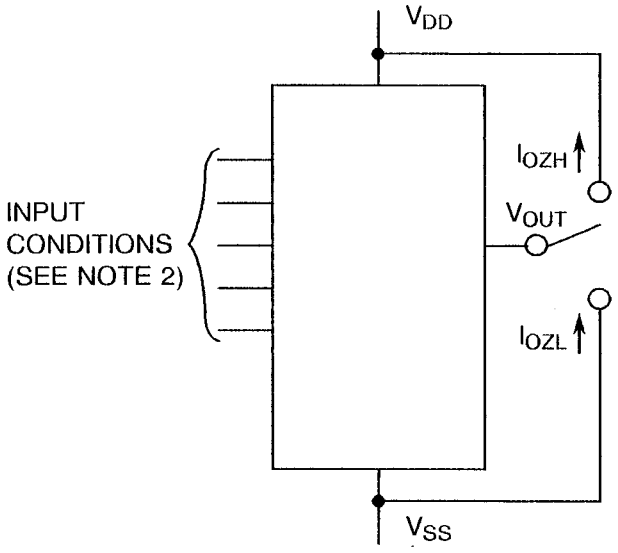
NOTES
1. Each input to be tested separately.
2. Input conditions as per Table 2.

FIGURE 4(h) - INPUT/OUTPUT CLAMP VOLTAGE



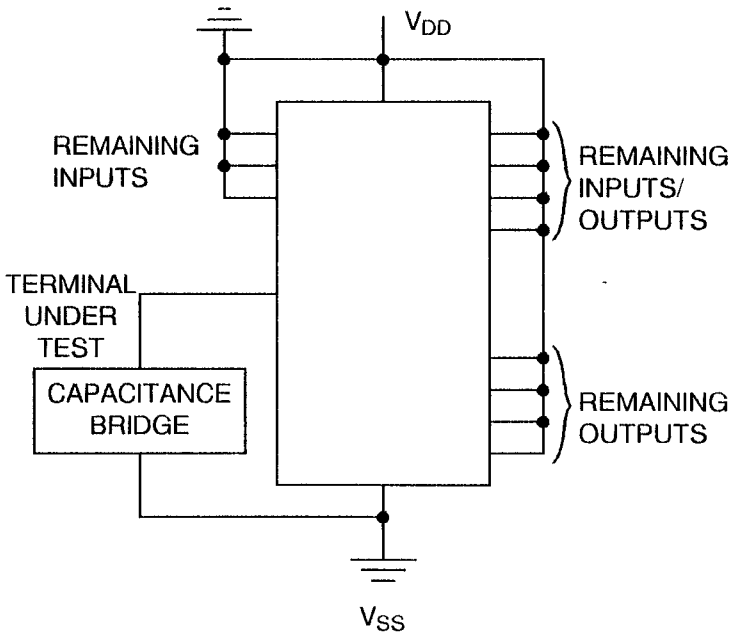
NOTES
1. Each input and output to be tested separately.

FIGURE 4(i) - OUTPUT LEAKAGE CURRENT THIRD STATE



NOTES
1. Each output to be tested separately.
2. Input conditions as per Table 2.

FIGURE 4(j) - INPUT, INPUT/OUTPUT AND OUTPUT CAPACITANCE



NOTES
1. Test frequency = 1.0MHz.
2. Each input, input/output and output to be tested separately.

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
23	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	±300	µA
24 to 73	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	±500	nA
74 to 123	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	±500	nA
124 to 186	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	±200	mV
187 to 249	Output Voltage High Level 1	V_{OH1}	As per Table 2	As per Table 2	±300	mV
250 to 312	Output Voltage High Level 2	V_{OH2}	As per Table 2	As per Table 2	±300	mV
659 to 685	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	±5.0	µA
686 to 712	Output Leakage Current Third State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	±5.0	µA

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0 – 5)	°C
2	Inputs - (Pins 4-100)	V_{IN}	V_{GEN1}	Vac
3	Inputs - (Pins 82-84)	V_{IN}	V_{GEN2}	Vac
4	Inputs - (Pins 5-6-7-16-17-18-19-20-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-83-88-89-97-102-104-108-112-113-114-115-119-120-124-125-126)	V_{IN}	V_{DD}	V
5	Pulse Voltage	V_{GEN}	0 to V_{DD}	Vac
6	Pulse Frequency Square Wave	f_{GEN1}	500 ± 50	kHz
7	Pulse Square Wave	GEN2	One 2.0s negative pulse each ms.	Vac
8	Positive Supply Voltage (Pins 1-2-14-30-41-55-69-80-105-129-132)	V_{DD}	5.5(+0 – 0.5)	V
9	Negative Supply Voltage (Pins 15-31-42-56-65-66-67-68-79-106-130)	V_{SS}	0	V

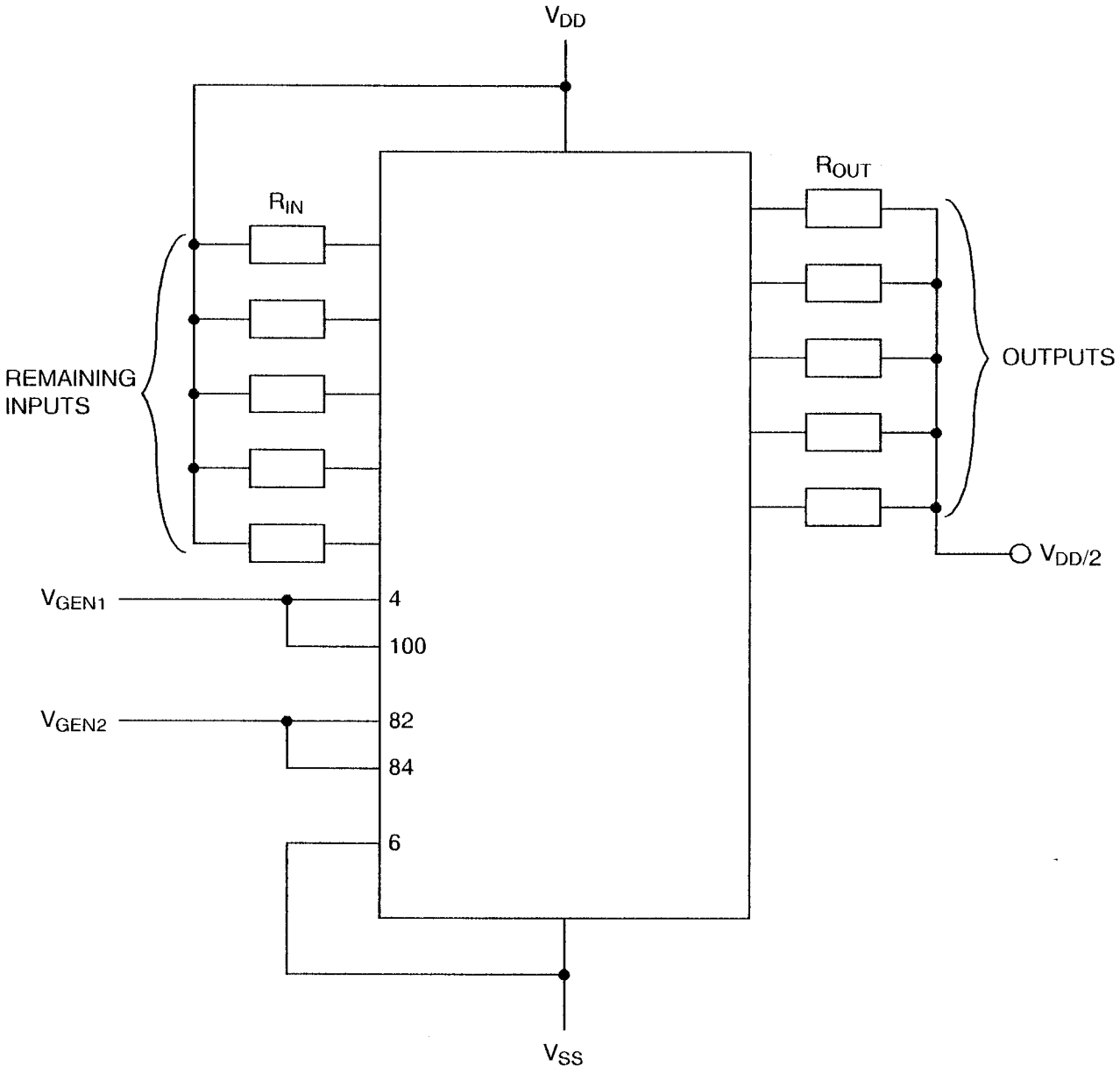
NOTES

1. Input Protection Resistor = 4.7kΩ ± 10%.
2. Output Load Resistor = 2.7kΩ ± 10%.

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(b) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

4.9 TOTAL DOSE IRRADIATION TESTING

4.9.1 Application

If specified in Para. 4.2.1 of this specification, total dose irradiation testing shall be performed in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.9.2 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6.

4.9.3 Electrical Measurements

The parameters to be measured prior to irradiation exposure are scheduled in Table 2 of this specification. Only devices which meet the requirements of Table 2 shall be scheduled in the test sample.

The parameters to be measured during and on completion of irradiation testing are scheduled in Table 7 of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
21	Functional Test (Min. V_{DD} Voltage)	-	As per Table 2	As per Table 2	-	-	-
22	Functional Test (Max. V_{DD} Voltage)	-	As per Table 2	As per Table 2	-	-	-
23	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	-	800	µA
24 to 73	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	-	−1.0	µA
74 to 123	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	-	1.0	µA
124 to 186	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	-	400	mV
187 to 249	Output Voltage High Level 1	V_{OH1}	As per Table 2	As per Table 2	3.9	-	V
250 to 312	Output Voltage High Level 2	V_{OH2}	As per Table 2	As per Table 2	4.2	-	V
313 to 362	Threshold Voltage Low Level	V_{THN}	As per Table 2	As per Table 2	1.35	-	V
363 to 412	Threshold Voltage High Level 1	V_{THP1}	As per Table 2	As per Table 2	-	3.2	V
413 to 462	Threshold Voltage High Level 2	V_{THP2}	As per Table 2	As per Table 2	-	3.9	V
463 to 560	Input/Output Clamp Voltage (to V_{SS})	V_{IC1}	As per Table 2	As per Table	-	-2.0	V
561 to 658	Input/Output Clamp Voltage (to V_{DD})	V_{IC2}	As per Table 2	As per Table	-	2.0	V
659 to 685	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	-	−10	µA
686 to 712	Output Leakage Current Third State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	-	10	µA
713	Supply Current	I_{DDS}	As per Table 2	As per Table 2	-	3.0	mA

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
830 to 831	$\overline{WR}$ and $\overline{CS}$ Low to Data Valid	TWLDV	As per Table 2	As per Table 2	-	200	ns
832 to 833	$\overline{WR}$ and $\overline{CS}$ Low to Address Valid	TWLAV	As per Table 2	As per Table 2	-	200	ns
834 to 835	$\overline{RDY}$ Low to Data Undefined	TOLDX	As per Table 2	As per Table 2	0	-	ns
836 to 837	$\overline{RDY}$ Low to Address Undefined	TOLAX	As per Table 2	As per Table 2	0	-	ns
838 to 839	$\overline{WR}$ or $\overline{CS}$ High to $\overline{RDY}$ High	TOHWH	As per Table 2	As per Table 2	-	37	ns
840 to 841	$\overline{CS}$ and $\overline{RD}$ Low to Data Valid	TRLDV	As per Table 2	As per Table 2	-	668	ns
842 to 843	$\overline{CS}$ and $\overline{RD}$ Low to Address Valid	TRLAV	As per Table 2	As per Table 2	-	200	ns
844 to 845	$\overline{CS}$ or $\overline{RD}$ High to DD High	TRHDDH	As per Table 2	As per Table 2	-	28	ns
846 to 847	$\overline{CS}$ or $\overline{RD}$ High to $\overline{RDY}$ High	TRHOH	As per Table 2	As per Table 2	-	37	ns
848 to 849	$\overline{CS}$ or $\overline{RD}$ High to Data Not Valid	TRHDX	As per Table 2	As per Table 2	9.0	36	ns
850 to 851	$\overline{RD}$ Low to DD Low	TRLDDL	As per Table 2	As per Table 2	-	26	ns
852 to 853	$\overline{DMAK}$ Low to $\overline{CD}$ Low	TALCDL	As per Table 2	As per Table 2	-	562	ns
854 to 855	$\overline{CD}$ Low to $\overline{DMAK}$ High	TCDLAH	As per Table 2	As per Table 2	100	-	ns
856 to 857	MAS High to $\overline{MPROTECT}$ High	TMAHMPH	As per Table 2	As per Table 2	-	850	ns

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
858 to 859	$\overline{\text{MPROTECT}}$ High to $\overline{\text{MWR}}$ Low	TMPHMWL	As per Table 2	As per Table 2	213	-	ns
860 to 861	MAS High to Data Valid	TMAHDV	As per Table 2	As per Table 2	-	158	ns
862 to 863	$\overline{\text{MRDY}}$ Low to $\overline{\text{MWR}}$ High	TMOLMWH	As per Table 2	As per Table 2	-	653	ns
864 to 865	$\overline{\text{MWR}}$ High to Data Undefined	TMWHDX	As per Table 2	As per Table 2	70	-	ns
866 to 867	$\overline{\text{CD}}$ High to $\overline{\text{DMAR}}$ High	TCDHMRH	As per Table 2	As per Table 2	-	136	ns
868 to 869	$\overline{\text{DMAK}}$ Low to $\overline{\text{CD}}$ Low	TALCDL	As per Table 2	As per Table 2	-	562	ns
870 to 871	$\overline{\text{CD}}$ Low to $\overline{\text{DMAK}}$ High	TCDLAH	As per Table 2	As per Table 2	100	-	ns
872 to 873	$\overline{\text{MRDY}}$ Low to Data Valid	TMOLDV	As per Table 2	As per Table 2	-	200	ns
874 to 875	$\overline{\text{MRDY}}$ Pulse Length	TMOLMOH	As per Table 2	As per Table 2	400	-	ns
876 to 877	$\overline{\text{MRDY}}$ to Data Undefined	TMRHDX	As per Table 2	As per Table 2	0	-	ns

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0−5)	°C
2	Inputs - (Pins 4-100)	V_{IN}	V_{GEN1}	Vac
3	Inputs - (Pins 82-84)	V_{IN}	V_{GEN2}	Vac
4	Inputs - (Pins 5-6-7-16-17-18-19-20-57-58-59-60-61-62-63-64-70-71-72-73-74-75-76-77-83-88-89-97-102-104-108-112-113-114-115-119-120-124-125-126)	V_{IN}	V_{DD}	V
5	Pulse Voltage	V_{GEN}	0 to V_{DD}	Vac
6	Pulse Frequency Square Wave	f_{GEN1}	500 ± 50	kHz
7	Pulse Square Wave	GEN2	One 2.0s negative pulse each ms.	Vac
8	Positive Supply Voltage (Pins 1-2-14-30-41-55-69-80-105-129-132)	V_{DD}	5.5(+0−0.5)	V
9	Negative Supply Voltage (Pins 15-31-42-56-65-66-67-68-79-106-130)	V_{SS}	0	V

NOTES

1. Input Protection Resistor = 4.7kΩ ± 10%.
2. Output Load Resistor = 2.7kΩ ± 10%.

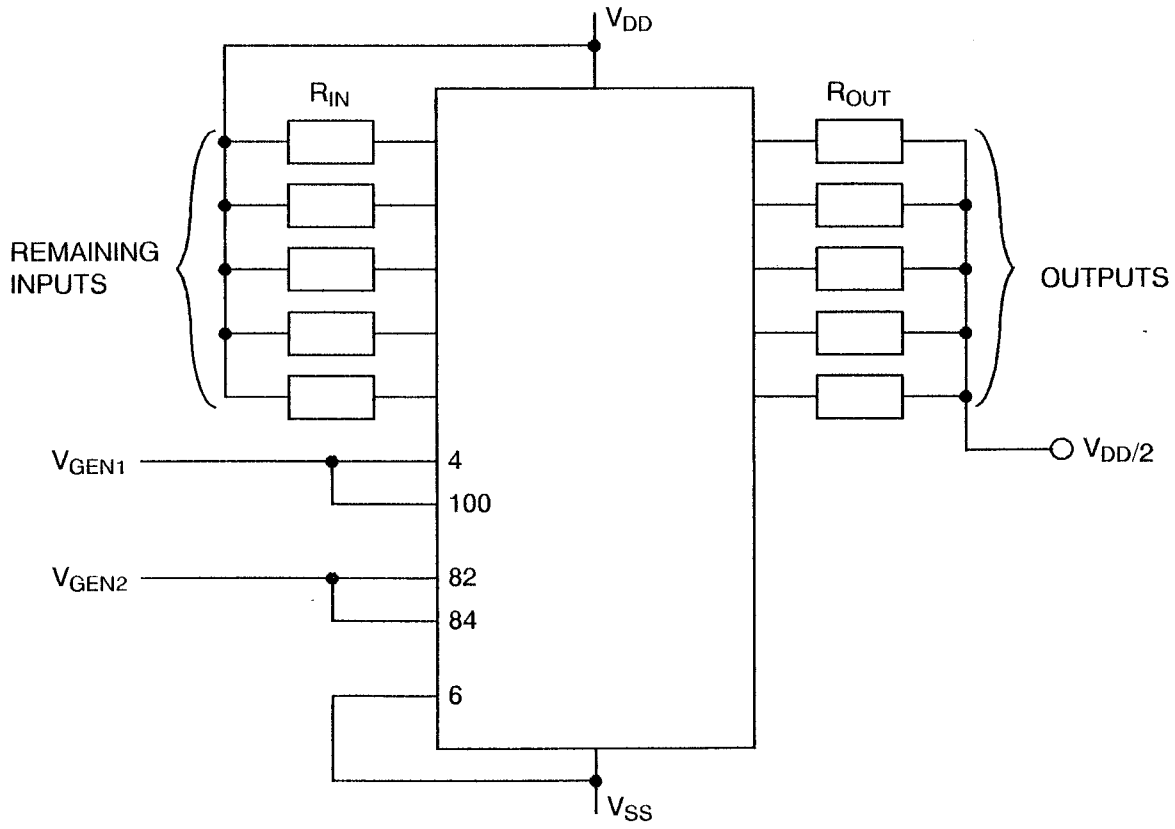


TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
21	Functional Test (Min. V_{DD} Voltage)	-	As per Table 2	As per Table 2	-	-	-
22	Functional Test (Max. V_{DD} Voltage)	-	As per Table 2	As per Table 2	-	-	-
23	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	-	5.0	mA
24 to 73	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	-	−1.0	µA
74 to 123	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	-	1.0	µA
124 to 186	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	-	400	mV
187 to 249	Output Voltage High Level 1	V_{OH1}	As per Table 2	As per Table 2	3.9	-	V
250 to 312	Output Voltage High Level 2	V_{OH2}	As per Table 2	As per Table 2	4.2	-	V
313 to 362	Threshold Voltage Low Level	V_{THN}	As per Table 2	As per Table 2	1.35	-	V
363 to 412	Threshold Voltage High Level 1	V_{THP1}	As per Table 2	As per Table 2	-	3.2	V
413 to 462	Threshold Voltage High Level 2	V_{THP2}	As per Table 2	As per Table 2	-	3.9	V
463 to 560	Input/Output Clamp Voltage (to V_{SS})	V_{IC1}	As per Table 2	As per Table 2	-	−2.0	V
561 to 658	Input/Output Clamp Voltage (to V_{DD})	V_{IC2}	As per Table 2	As per Table 2	-	2.0	V
659 to 685	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	-	−10	µA
686 to 712	Output Leakage Current Third State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	-	10	µA
713	Supply Current	I_{DDS}	As per Table 2	As per Table 2	-	7.0	mA

APPENDIX 'A'

AGREED DEVIATIONS FOR MITEL (S)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.2	Paragraph 4.4 - Marking (plus Serialisation for Level B): May be performed to follow Paragraph 9.3 (Encapsulation). Paragraph 9.1 - Visual Inspection MIL-STD-883C, Method 2010.10, Paragraph 3.1.3: Scribing and die defects, "high magnification": Clauses c and d shall not be applicable for the device. Instead, the following criteria shall be used: - No device shall be acceptable if it exhibits cracks that:- (a) Come closer than 0.25mil to any operating metallisation or other functional circuit element. (b) Exceed 3.0mil in length pointing toward any operating metallisation or other functional circuit element. - For areas which are metallised, MIL-STD-883C, Method 2010.10, Paragraph 3.1.3 d is applicable without exception.
Para. 4.2.3	Paragraph 9.12 - Radiographic Inspection (a) ESA/SCC Basic Specification No. 20990, Paragraph 4.1: Inspection for foreign particles, voids and seal defects only may be performed. (b) Para. 9.9.2, Electrical Measurements at High and Low Temperatures: May be performed after Paras. 9.8.1 and 9.8.2, Seal Test.
Para's 4.2.4 and 4.2.5	Paragraph 9.18 - Solderability (a) A manually controlled dipping device may be used.

The test programme reference is 12663P3 for all testing.