INTEGRATED CIRCUITS,

SILICON ON SAPPHIRE MONOLITHIC,

HCMOS QUAD 2-INPUT AND GATES,

BASED ON TYPES 54HSC08 AND 54HST08

ESCC Detail Specification No. 9201/144

ISSUE 1

October 2002

Document Custodian: European Space Agency - see https://escies.org

LEGAL DISCLAIMER AND COPYRIGHT

european space agency
agence spatiale européenne

Pages 1 to 34

INTEGRATED CIRCUITS,

SILICON ON SAPPHIRE MONOLITHIC,

HCMOS QUAD 2-INPUT AND GATES,

BASED ON TYPES 54HSC08 AND 54HST08

ESA/SCC Detail Specification No. 9201/144

space components
coordination group

Issue/Rev.	Date	Approved by	
		SCCG Chairman	ESA Director General or his Deputy
Issue 1	March 1995		

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.

TABLE OF CONTENTS

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a Silicon on Sapphire, monolithic, high speed CMOS and TTL Quad 2-Input AND Gate, having fully buffered outputs, based on Types 54HSC08 and 54HST08. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

As per Figure 3(b).

1.8 CIRCUIT SCHEMATIC

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 with a Minimum Critical Path Failure Voltage of 500 Volts

1.11 INPUT PROTECTION NETWORK

Protection networks shall be incorporated into each input as shown in Figure 3(e).

TABLE 1(a) - TYPE VARIANTS

VARIANT	BASED ON TYPE	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
01	54HSC08	FLAT	2(a)	G2
02	54HSC08	D.I.L.	2(b)	G2
03	54HST08	FLAT	2(a)	G2
04	54HST08	D.I.L.	2(b)	G2

TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage	V_{DD}	− 0.3 to + 7.0	V	Note 1
2	Input Voltage	V_{IN}	− 0.3 to V_{DD} + 0.3	V	Note 1
3	Output Voltage	V_{OUT}	− 0.3 to V_{DD} + 0.3	V	Notes 1, 2
4	Device Dissipation (Continuous)	P_D	137.5	mW	Note 3
5	Supply Current	I_{DDop}	25	mA	-
6	Operating Temperature Range	T_{op}	− 55 to + 125	°C	T_{amb}
7	Storage Temperature Range	T_{stg}	− 65 to + 150	°C	-
8	Soldering Temperature	T_{sol}	+ 265	°C	Note 4

NOTES

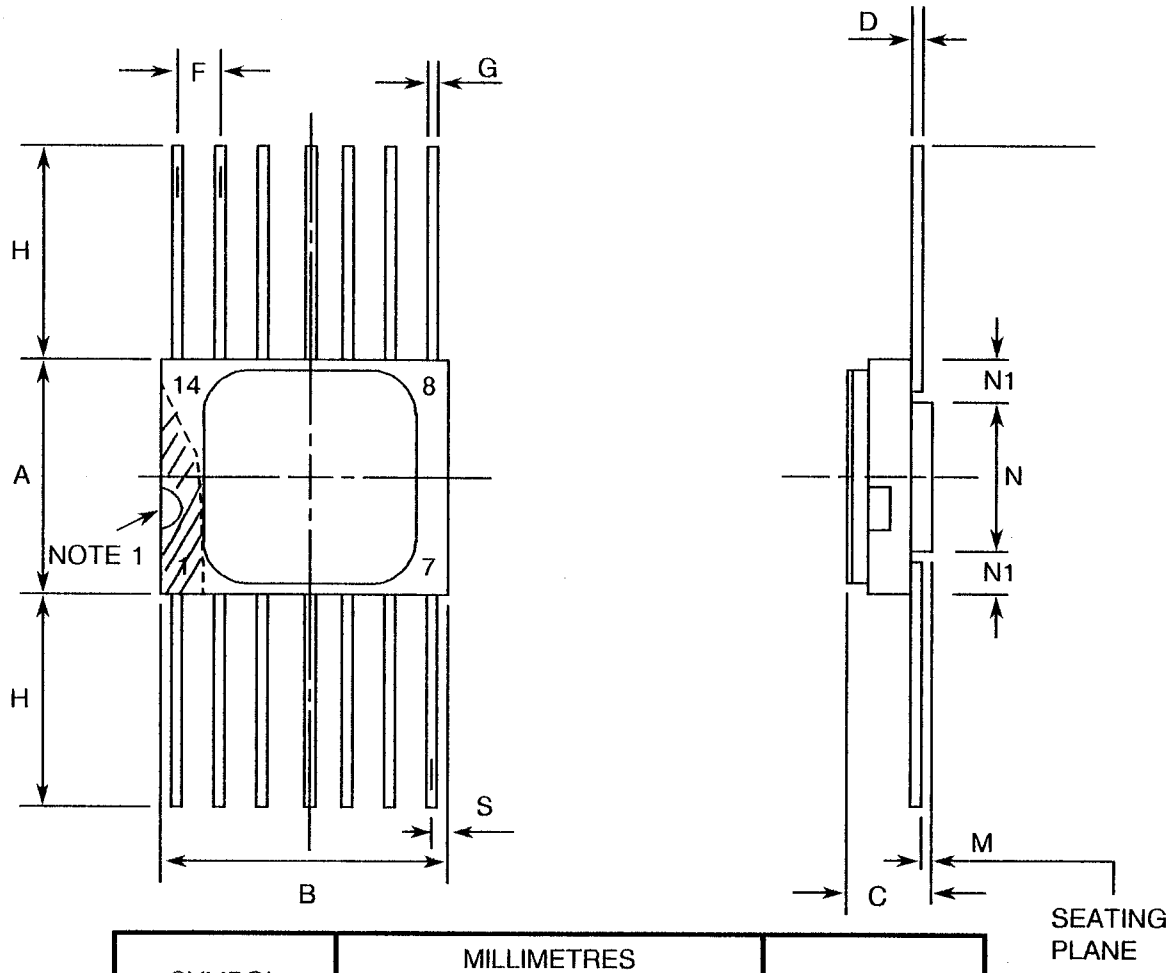
1. Device is functional for $4.5V \leq V_{DD} \leq 5.5V$.
2. Output current limited to $I_{OUT} = \pm 15mA$.
3. The device dissipation is determined by I_{DDop} max. (25mA) × 5.5V.
4. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION

Not applicable.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - FLAT PACKAGE, 14-PIN

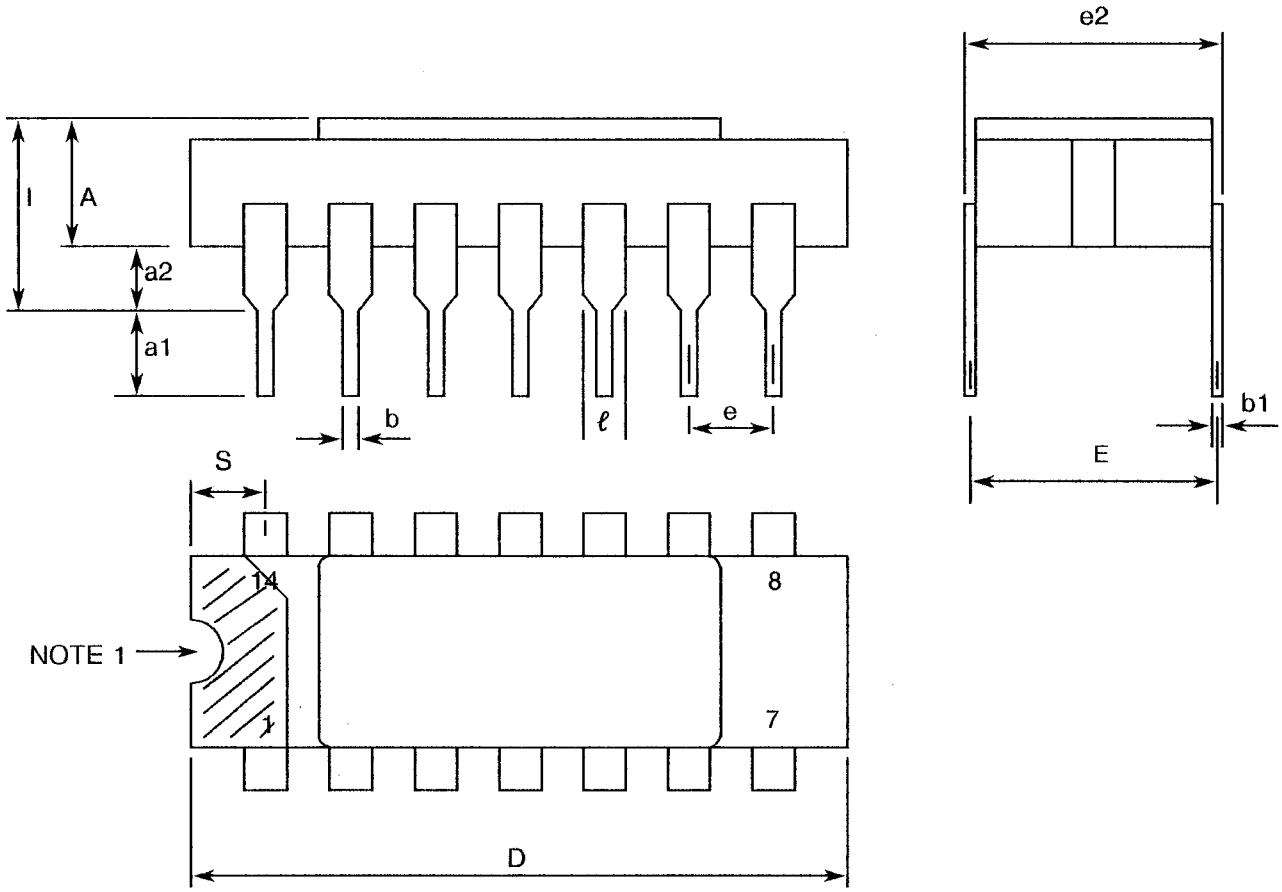


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	6.32	6.63	
B	8.46	8.81	3
C	-	4.67	
D	0.10	0.15	7
F	1.27	TYPICAL	4, 8
G	0.38	0.48	7
H	6.35	9.40	7
M	0.30	-	2
N	4.35	TYPICAL	
N1	0.76	1.45	
S	1.27	-	6

NOTES: See Page 9.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - DUAL-IN-LINE PACKAGE, 14-PIN



SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	2.10	2.74	
a1	3.30	4.75	
a2	0.38	1.53	2
b	0.35	0.59	7
b1	0.20	0.36	7
D	-	18.04	3
E	7.26 TYPICAL		
e	2.54 TYPICAL		5, 8
e2	-	8.30	
I	-	5.60	
ℓ	1.53 TYPICAL		7
S	-	1.27	6

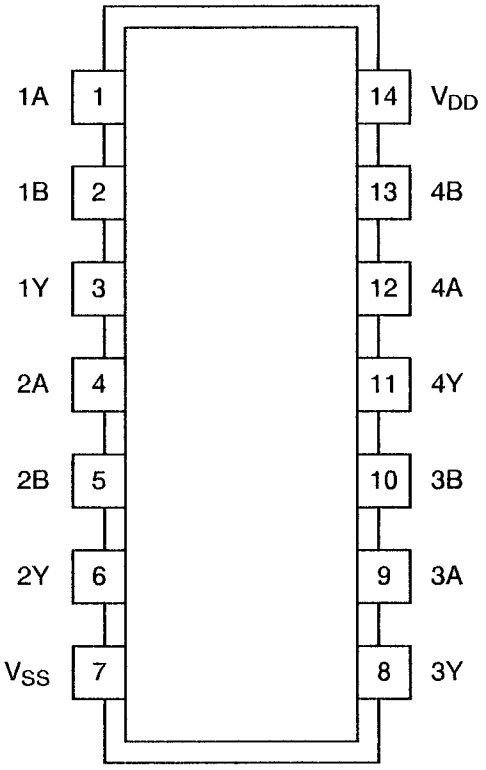
NOTES: See Page 9.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURES 2(a) AND 2(b)

1. Index area: a notch, letter or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown.
2. The dimension shall be measured from the seating plane to the base plane.
3. The dimension allows for off-centre lids, meniscus and glass overrun.
4. The true position pin spacing is 1.27mm between centrelines. Each pin centreline shall be located within ± 0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
5. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ± 0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.
6. Applies to all 4 corners.
7. All leads or terminals.
8. 12 spaces.

FIGURE 3(a) - PIN ASSIGNMENT



TOP VIEW

FIGURE 3(b) - TRUTH TABLE (EACH GATE)

INPUTS		OUTPUTS
A	B	Y = A.B
L	L	L
H	L	L
L	H	L
H	H	H

NOTES

1. Logic Level Definitions: L = Low Level, H = High Level.

FIGURE 3(c) - CIRCUIT SCHEMATIC

Not applicable.

FIGURE 3(d) - FUNCTIONAL DIAGRAM

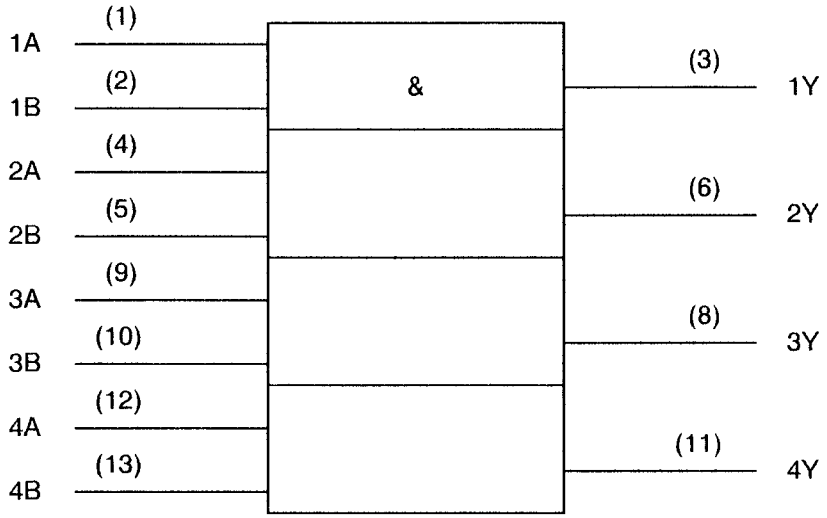
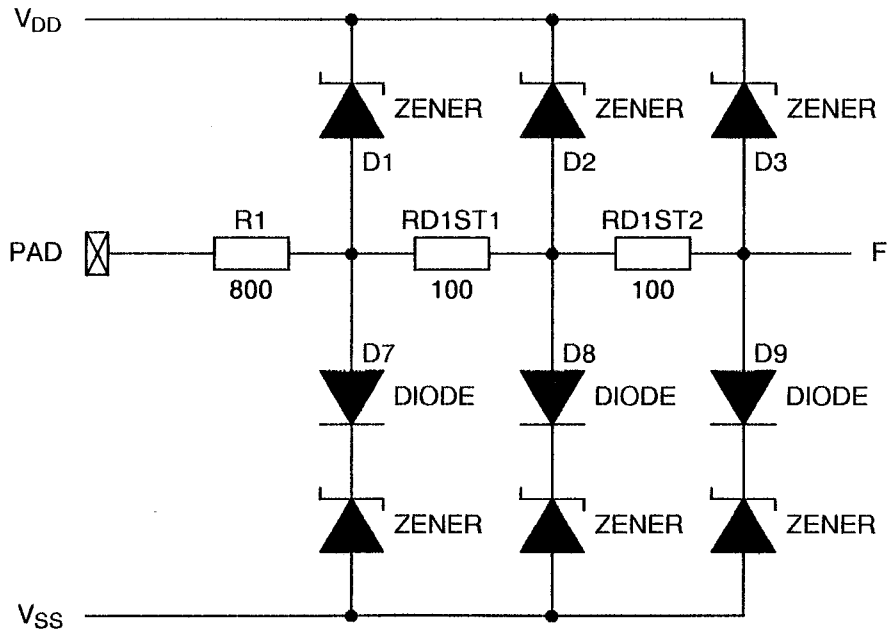


FIGURE 3(e) - INPUT PROTECTION NETWORK



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviation is used:-

V_{IC} = Input Clamp Voltage.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

(a) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during irradiation qualification and maintenance of qualification.

(b) Para. 5.2.2, Total Dose Irradiation Testing: If specified in a Purchase Order, shall be performed during procurement on an irradiation lot acceptance basis at the total dose irradiation level specified in the Purchase Order.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

(a) Para. 7.1.1(a), "High Temperature Reverse Bias" tests and subsequent electrical measurements related to this test shall be omitted.

4.2.4 Deviations from Qualification Tests (Chart IV)

(a) None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

(a) None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 2.2 grammes for the dual-in-line package and 0.7 grammes for the flat package.

4.4 MATERIALS AND FINISHES

The materials shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body and the lids shall be preform-soldered.

4.4.2 Lead Material and Finish

For dual-in-line and flat packages, the material shall be Type 'G' with Type '2' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

4.5.2 Lead Identification

For dual-in-line and flat packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:

920114401BF

Detail Specification Number
Type Variant (see Table 1(a))
Testing Level (B or C, as applicable)
Total Dose Irradiation Level (if applicable)

The Total Dose Irradiation Level designation shall be added for those devices for which a sample has been successfully tested to the level in question. For these devices, a code letter shall be added in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ °C and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits and functional test sequences for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to H.T.R.B. and Power Burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $+25 \pm 3$ °C. The parameter drift values (Δ), applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for H.T.R.B. Burn-in

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for power burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for H.T.R.B. Burn-in

Not applicable.

4.7.5 Electrical Circuits for Power Burn-in

A circuit for use in performing the power burn-in test is shown in Figure 5(b) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test 1	-	-	3(b)	Verify Truth Table without Load. V_{IL} = 0V, V_{IH} = 4.5V V_{OL} = 2.0V, V_{OH} = 3.0V V_{DD} = 4.5V, V_{SS} = 0V f = 1.0MHz	-	-	-
2	Functional Test 2	-	-	3(b)	Verify Truth Table without Load. V_{IL} = 0V, V_{IH} = 5.5V V_{OL} = 2.0V, V_{OH} = 3.0V V_{DD} = 5.5V, V_{SS} = 0V f = 1.0MHz	-	-	-
3 to 4	Quiescent Current	I_{DD}	3005	4(a)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V All Outputs Open (Pin 14)	-	10	µA
5 to 12	Input Current Low Level	I_{IL}	3009	4(b)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 1-2-4-5-9-10-12-13)	-	– 500	nA
13 to 20	Input Current High Level	I_{IH}	3010	4(c)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 1-2-4-5-9-10-12-13)	-	500	nA
21 to 24	Output Voltage Low Level 1	V_{OL1}	3007	4(d)	Gate Under Test: Variants 01 and 02 V_{IN1} = 1.5V, V_{IN2} = 3.5V Variants 03 and 04 V_{IN1} = 0.8V, V_{IN2} = 2.0V I_{OL} = 20µA All Other Gates: V_{IN} = 0V V_{DD} = 4.5V, V_{SS} = 0V Note 1 (Pins 3-6-8-11)	-	0.1	V

NOTES: See Page 18.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
25 to 28	Output Voltage Low Level 2	V_{OL2}	3007	4(d)	Gate Under Test: Variants 01 and 02 $V_{IN1} = 1.5V$, $V_{IN2} = 3.5V$ Variants 03 and 04 $V_{IN1} = 0.8V$, $V_{IN2} = 2.0V$ $I_{OL} = 6.0mA$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 1 (Pins 3-6-8-11)	-	0.2	V
29 to 32	Output Voltage Low Level 3	V_{OL3}	3007	4(d)	Gate Under Test: Variants 01 and 02 $V_{IN1} = 1.5V$, $V_{IN2} = 3.5V$ Variants 03 and 04 $V_{IN1} = 0.8V$, $V_{IN2} = 2.0V$ $I_{OL} = 9.0mA$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ (Pins 3-6-8-11)	-	0.4	V
33 to 36	Output Voltage Low Level 4	V_{OL4}	3007	4(d)	Gate Under Test: Variants 01 and 02 $V_{IN1} = 1.5V$, $V_{IN2} = 3.5V$ Variants 03 and 04 $V_{IN1} = 0.8V$, $V_{IN2} = 2.0V$ $I_{OL} = 20\mu A$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 1 (Pins 3-6-8-11)	-	0.1	V
37 to 40	Output Voltage Low Level 5	V_{OL5}	3007	4(d)	Gate Under Test: Variants 01 and 02 $V_{IN1} = 1.5V$, $V_{IN2} = 3.5V$ Variants 03 and 04 $V_{IN1} = 0.8V$, $V_{IN2} = 2.0V$ $I_{OL} = 6.0mA$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 1 (Pins 3-6-8-11)	-	0.2	V

NOTES: See Page 18.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
41 to 44	Output Voltage Low Level 6	V_{OL6}	3007	4(d)	Gate Under Test: Variants 01 and 02 $V_{IN1} = 1.5V$, $V_{IN2} = 3.5V$ Variants 03 and 04 $V_{IN1} = 0.8V$, $V_{IN2} = 2.0V$ $I_{OL} = 9.0mA$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ (Pins 3-6-8-11)	-	0.4	V
45 to 48	Output Voltage High Level 1	V_{OH1}	3006	4(e)	Gate Under Test: Variants 01 and 02 $V_{IN} = 3.5V$ Variants 03 and 04 $V_{IN} = 2.0V$ $I_{OH} = -20\mu A$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 1 (Pins 3-6-8-11)	4.4	-	V
49 to 52	Output Voltage High Level 2	V_{OH2}	3006	4(e)	Gate Under Test: Variants 01 and 02 $V_{IN} = 3.5V$ Variants 03 and 04 $V_{IN} = 2.0V$ $I_{OH} = -6.0mA$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 1 (Pins 3-6-8-11)	3.7	-	V
53 to 56	Output Voltage High Level 3	V_{OH3}	3006	4(e)	Gate Under Test: Variants 01 and 02 $V_{IN} = 3.5V$ Variants 03 and 04 $V_{IN} = 2.0V$ $I_{OH} = -11.0mA$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ (Pins 3-6-8-11)	2.5	-	V
57 to 60	Output Voltage High Level 4	V_{OH4}	3006	4(e)	Gate Under Test: Variants 01 and 02 $V_{IN} = 3.5V$ Variants 03 and 04 $V_{IN} = 2.0V$ $I_{OH} = -20\mu A$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 1 (Pins 3-6-8-11)	4.4	-	V

NOTES: See Page 18

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
61 to 64	Output Voltage High Level 5	V_{OH5}	3006	4(e)	Gate Under Test: Variants 01 and 02 V_{IN} = 3.5V Variants 03 and 04 V_{IN} = 2.0V I_{OH} = − 6.0mA All Other Gates: V_{IN} = 0V V_{DD} = 5.5V, V_{SS} = 0V Note 1 (Pins 3-6-8-11)	3.7	-	V
65 to 68	Output Voltage High Level 6	V_{OH6}	3006	4(e)	Gate Under Test: Variants 01 and 02 V_{IN} = 3.5V Variants 03 and 04 V_{IN} = 2.0V I_{OH} = − 11.0mA All Other Gates: V_{IN} = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 3-6-8-11)	2.5	-	V
69 to 76	Threshold Voltage N-Channel	V_{THN}	-	4(f)	V_{IN} = Note 2 V_{IH} = 5.0V V_{DD} = 5.0V, V_{SS} = 0V Note 3 (Pins 1-2-4-5-9-10-12-13)	1.5	-	V
77 to 84	Threshold Voltage P-Channel	V_{THP}	-	4(g)	V_{IN} = Note 2 V_{IL} = 0V V_{DD} = 5.0V, V_{SS} = 0V Note 3 (Pins 1-2-4-5-9-10-12-13)	-	3.5	V
85 to 92	Input Clamp Voltage (to V_{SS})	V_{IC1}	3022	4(h)	I_{IN} (Under Test) = − 0.1mA V_{DD} = Open, V_{SS} = 0V All Other Pins Open (Pins 1-2-4-5-9-10-12-13)	− 0.1	− 5.0	V
93 to 100	Input Clamp Voltage (to V_{DD})	V_{IC2}	3022	4(h)	I_{IN} (Under Test) = 0.1mA V_{DD} = 0V, V_{SS} = Open All Other Pins Open (Pins 1-2-4-5-9-10-12-13)	0.1	5.0	V

NOTES

1. Guaranteed, but not tested.
2. V_{IN} is applied to the pin under test and is varied until a change in the output occurs. The measured value is V_{TH}.
3. Worst case measurement only to be recorded.
4. Guaranteed, but not tested at − 55°C

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
101 to 108	Input Capacitance	C_{IN}	3012	4(i)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 1 (Pins 1-2-4-5-9-10-12-13)	-	10	pF
109	Propagation Delay Low to High (1A to 1Y)	t_{PLH}	3003	4(j)	Gate Under Test: V_{IN1} = Pulse Generator $V_{IN2} = V_{DD}$ V_{IN} (Remaining Inputs) = 0V V_{DD} = 4.5V, V_{SS} = 0V Pins 2 to 3	-	20	ns
110	Propagation Delay High to Low (1A to 1Y)	t_{PHL}	3003	4(j)	Gate Under Test: V_{IN1} = Pulse Generator $V_{IN2} = V_{DD}$ V_{IN} (Remaining Inputs) = 0V V_{DD} = 4.5V, V_{SS} = 0V Pins 2 to 3	-	20	ns
111	Transition Time Low to High	t_{TLH}	3004	4(j)	Gate Under Test: V_{IN1} = Pulse Generator $V_{IN2} = V_{DD}$ V_{IN} (Remaining Inputs) = 0V V_{DD} = 4.5V, V_{SS} = 0V Note 1 (Pin 3)	-	15	ns
112	Transition Time High to Low	t_{THL}	3004	4(j)	Gate Under Test: V_{IN1} = Pulse Generator $V_{IN2} = V_{DD}$ V_{IN} (Remaining Inputs) = 0V V_{DD} = 4.5V, V_{SS} = 0V Note 1 (Pin 3)	-	15	ns

NOTES: See Page 18.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test 1	-	-	3(b)	Verify Truth Table without Load. V_{IL} = 0V, V_{IH} = 4.5V V_{OL} = 2.0V, V_{OH} = 3.0V V_{DD} = 4.5V, V_{SS} = 0V f = 1.0MHz	-	-	-
2	Functional Test 2	-	-	3(b)	Verify Truth Table without Load. V_{IL} = 0V, V_{IH} = 5.5V V_{OL} = 2.0V, V_{OH} = 3.0V V_{DD} = 5.5V, V_{SS} = 0V f = 1.0MHz	-	-	-
3 to 4	Quiescent Current	I_{DD}	3005	4(a)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V All Outputs Open (Pin 14)	-	600	µA
5 to 12	Input Current Low Level	I_{IL}	3009	4(b)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 1-2-4-5-9-10-12-13)	-	– 5.0	µA
13 to 20	Input Current High Level	I_{IH}	3010	4(c)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 1-2-4-5-9-10-12-13)	-	5.0	µA
21 to 24	Output Voltage Low Level 1	V_{OL1}	3007	4(d)	Gate Under Test: Variants 01 and 02 V_{IN1} = 1.5V, V_{IN2} = 3.5V Variants 03 and 04 V_{IN1} = 0.8V, V_{IN2} = 2.0V I_{OL} = 20µA All Other Gates: V_{IN} = 0V V_{DD} = 4.5V, V_{SS} = 0V Note 1 (Pins 3-6-8-11)	-	0.1	V

NOTES: See Page 18.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
25 to 28	Output Voltage Low Level 2	V_{OL2}	3007	4(d)	Gate Under Test: Variants 01 and 02 $V_{IN1} = 1.5V$, $V_{IN2} = 3.5V$ Variants 03 and 04 $V_{IN1} = 0.8V$, $V_{IN2} = 2.0V$ $I_{OL} = 6.0mA$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 1 (Pins 3-6-8-11)	-	0.2	V
29 to 32	Output Voltage Low Level 3	V_{OL3}	3007	4(d)	Gate Under Test: Variants 01 and 02 $V_{IN1} = 1.5V$, $V_{IN2} = 3.5V$ Variants 03 and 04 $V_{IN1} = 0.8V$, $V_{IN2} = 2.0V$ $I_{OL} = 9.0mA$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ (Pins 3-6-8-11)	-	0.4	V
33 to 36	Output Voltage Low Level 4	V_{OL4}	3007	4(d)	Gate Under Test: Variants 01 and 02 $V_{IN1} = 1.5V$, $V_{IN2} = 3.5V$ Variants 03 and 04 $V_{IN1} = 0.8V$, $V_{IN2} = 2.0V$ $I_{OL} = 20\mu A$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 1 (Pins 3-6-8-11)	-	0.1	V
37 to 40	Output Voltage Low Level 5	V_{OL5}	3007	4(d)	Gate Under Test: Variants 01 and 02 $V_{IN1} = 1.5V$, $V_{IN2} = 3.5V$ Variants 03 and 04 $V_{IN1} = 0.8V$, $V_{IN2} = 2.0V$ $I_{OL} = 6.0mA$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 1 (Pins 3-6-8-11)	-	0.2	V

NOTES: See Page 18.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
41 to 44	Output Voltage Low Level 6	V_{OL6}	3007	4(d)	Gate Under Test: Variants 01 and 02 $V_{IN1} = 1.5V$, $V_{IN2} = 3.5V$ Variants 03 and 04 $V_{IN1} = 0.8V$, $V_{IN2} = 2.0V$ $I_{OL} = 9.0mA$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ (Pins 3-6-8-11)	-	0.4	V
45 to 48	Output Voltage High Level 1	V_{OH1}	3006	4(e)	Gate Under Test: Variants 01 and 02 $V_{IN} = 3.5V$ Variants 03 and 04 $V_{IN} = 2.0V$ $I_{OH} = -20\mu A$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 1 (Pins 3-6-8-11)	4.4	-	V
49 to 52	Output Voltage High Level 2	V_{OH2}	3006	4(e)	Gate Under Test: Variants 01 and 02 $V_{IN} = 3.5V$ Variants 03 and 04 $V_{IN} = 2.0V$ $I_{OH} = -6.0mA$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ Note 1 (Pins 3-6-8-11)	3.7	-	V
53 to 56	Output Voltage High Level 3	V_{OH3}	3006	4(e)	Gate Under Test: Variants 01 and 02 $V_{IN} = 3.5V$ Variants 03 and 04 $V_{IN} = 2.0V$ $I_{OH} = -11.0mA$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 4.5V$, $V_{SS} = 0V$ (Pins 3-6-8-11)	2.5	-	V
57 to 60	Output Voltage High Level 4	V_{OH4}	3006	4(e)	Gate Under Test: Variants 01 and 02 $V_{IN} = 3.5V$ Variants 03 and 04 $V_{IN} = 2.0V$ $I_{OH} = -20\mu A$ All Other Gates: $V_{IN} = 0V$ $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 1 (Pins 3-6-8-11)	4.4	-	V

NOTES: See Page 18

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
61 to 64	Output Voltage High Level 5	V_{OH5}	3006	4(e)	Gate Under Test: Variants 01 and 02 V_{IN} = 3.5V Variants 03 and 04 V_{IN} = 2.0V I_{OH} = − 6.0mA All Other Gates: V_{IN} = 0V V_{DD} = 5.5V, V_{SS} = 0V Note 1 (Pins 3-6-8-11)	3.7	-	V
65 to 68	Output Voltage High Level 6	V_{OH6}	3006	4(e)	Gate Under Test: Variants 01 and 02 V_{IN} = 3.5V Variants 03 and 04 V_{IN} = 2.0V I_{OH} = − 11.0mA All Other Gates: V_{IN} = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 3-6-8-11)	2.5	-	V
69 to 76	Threshold Voltage N-Channel	V_{THN}	-	4(f)	V_{IN} = Note 2 V_{IH} = 5.0V V_{DD} = 5.0V, V_{SS} = 0V Note 3 (Pins 1-2-4-5-9-10-12-13)	1.5	-	V
77 to 84	Threshold Voltage P-Channel	V_{THP}	-	4(g)	V_{IN} = Note 2 V_{IL} = 0V V_{DD} = 5.0V, V_{SS} = 0V Note 3 (Pins 1-2-4-5-9-10-12-13)	-	3.5	V
85 to 92	Input Clamp Voltage (to V_{SS})	V_{IC1}	3022	4(h)	I_{IN} (Under Test) = − 0.1mA V_{DD} = Open, V_{SS} = 0V All Other Pins Open (Pins 1-2-4-5-9-10-12-13)	− 0.1	− 5.0	V
93 to 100	Input Clamp Voltage (to V_{DD})	V_{IC2}	3022	4(h)	I_{IN} (Under Test) = 0.1mA V_{DD} = 0V, V_{SS} = Open All Other Pins Open (Pins 1-2-4-5-9-10-12-13)	0.1	5.0	V

NOTES: See Page 18.

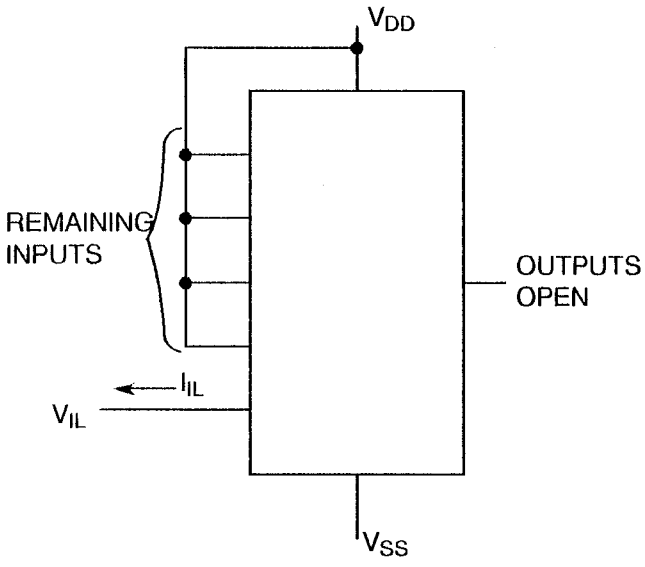
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - QUIESCENT CURRENT TEST TABLE

PATTERN No.	INPUTS								OUTPUTS				D.C. SUPPLY	
	1	2	4	5	9	10	12	13	3	6	8	11	7	14
1	1	1	1	1	1	1	1	1	OPEN				V_{SS} ↓	V_{DD} ↓
2	0	0	0	0	0	0	0	0	OPEN					

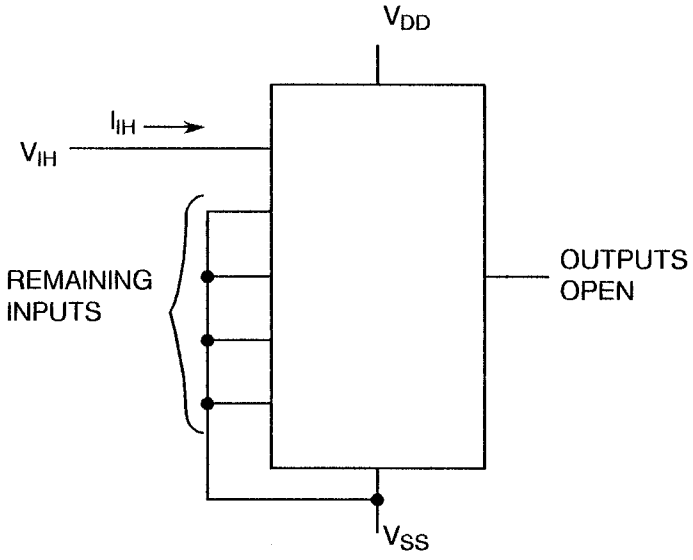
NOTES
1. Figure 4(a) illustrates one series of test patterns. Any other pattern series must be agreed with the Qualifying Space Agency and shall be included as an Appendix.
2. Logic Level Definitions: 1 = V_{IH} = V_{DD}, 0 = V_{IL} = V_{SS}.

FIGURE 4(b) - INPUT CURRENT LOW LEVEL



NOTES
1. Each input to be tested separately

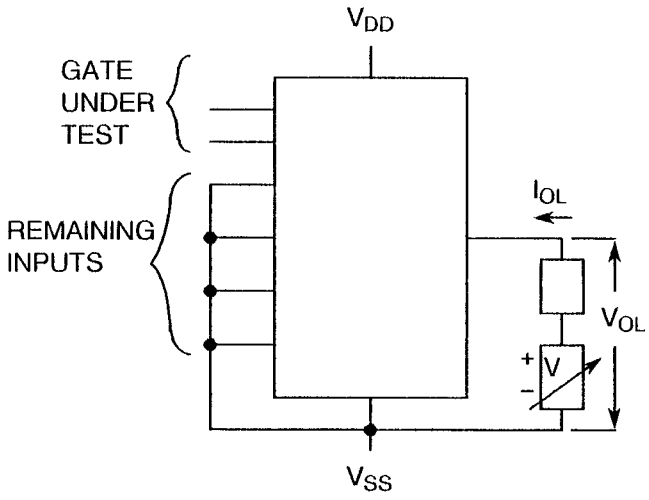
FIGURE 4(c) - INPUT CURRENT HIGH LEVEL



NOTES
1. Each input to be tested separately

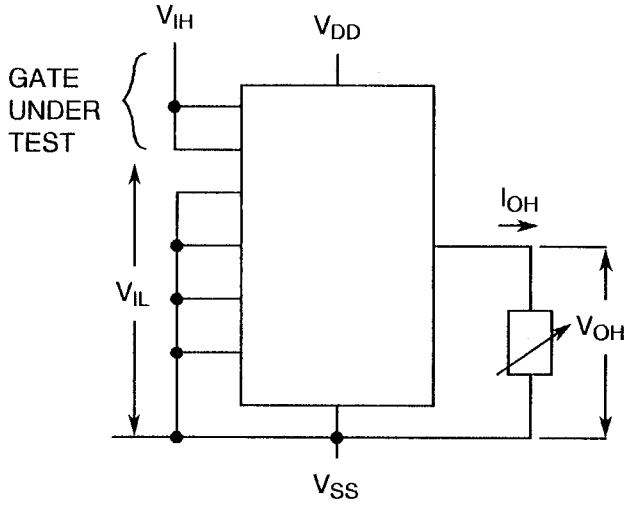
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(d) - OUTPUT VOLTAGE LOW LEVEL



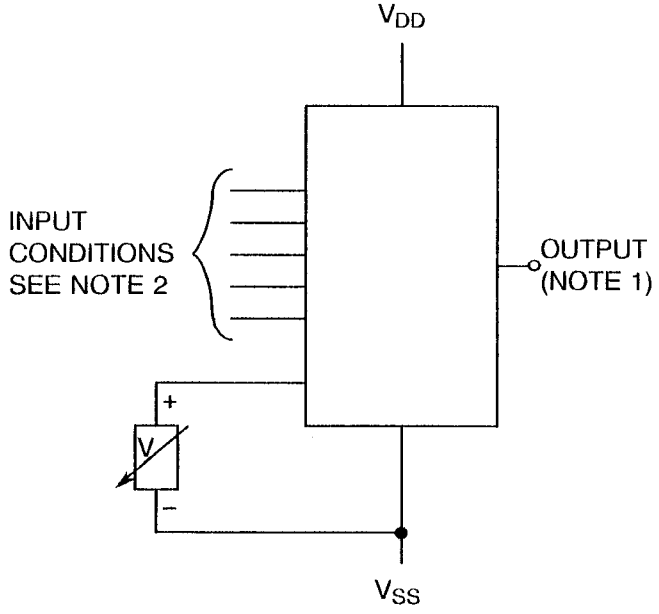
NOTES
1. Each output to be tested separately.

FIGURE 4(e) - OUTPUT VOLTAGE HIGH LEVEL



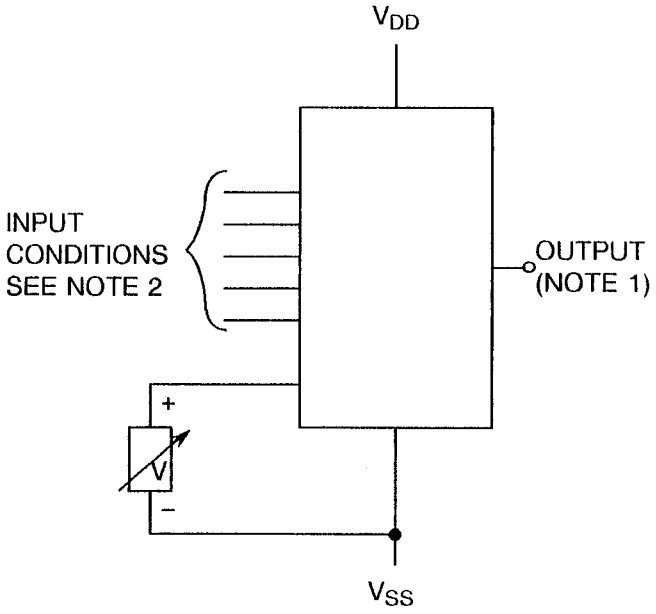
NOTES
1. Each output to be tested separately.

FIGURE 4(f) - THRESHOLD VOLTAGE N-CHANNEL



NOTES
1. Each input to be tested separately.
2. Input conditions as per Table 2.

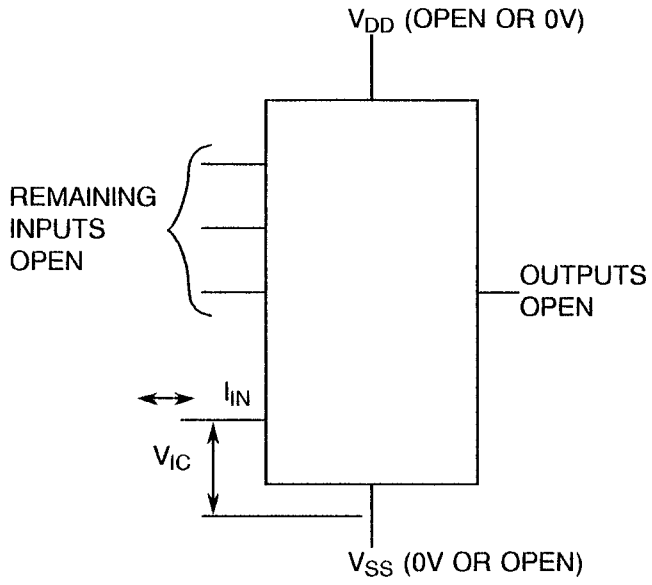
FIGURE 4(g) - THRESHOLD VOLTAGE P-CHANNEL



NOTES
1. Each input to be tested separately.
2. Input conditions as per Table 2.

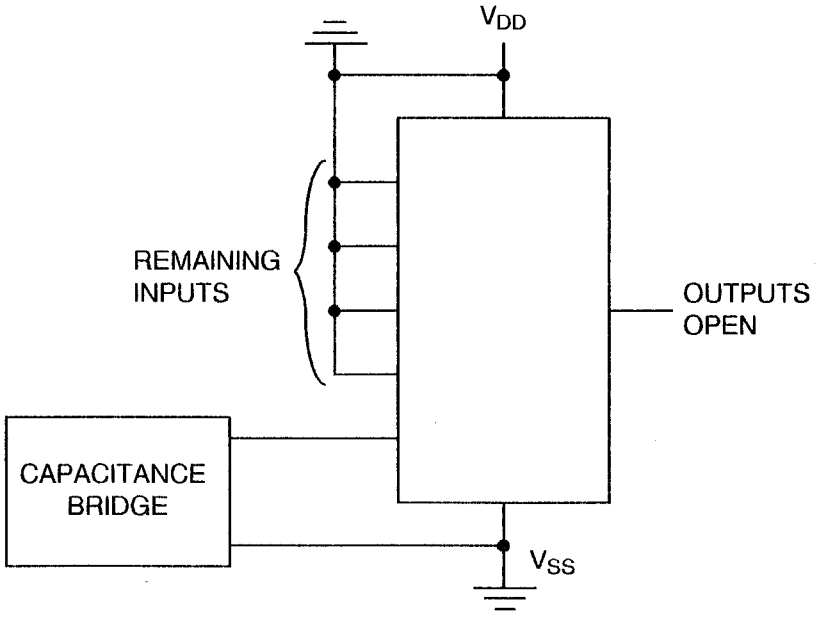
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(h) - INPUT CLAMP VOLTAGE



NOTES
1. Each input to be tested separately.

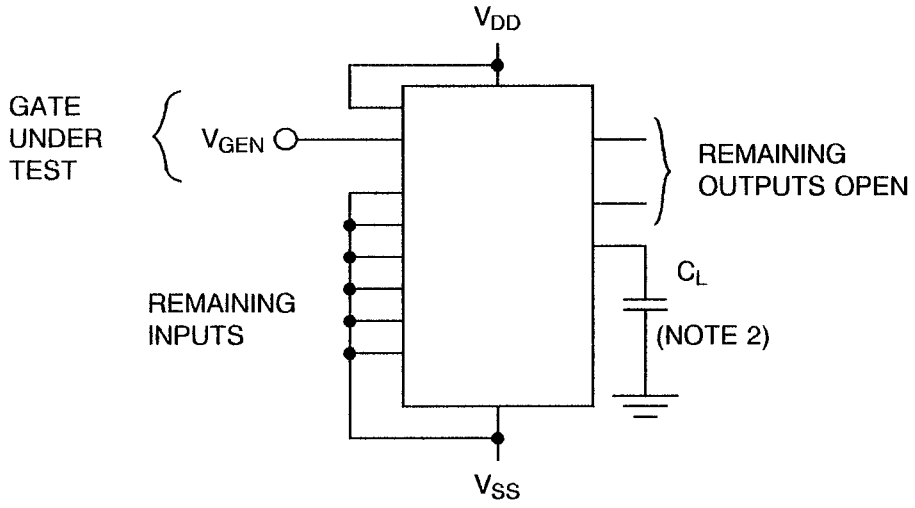
FIGURE 4(i) - INPUT CAPACITANCE



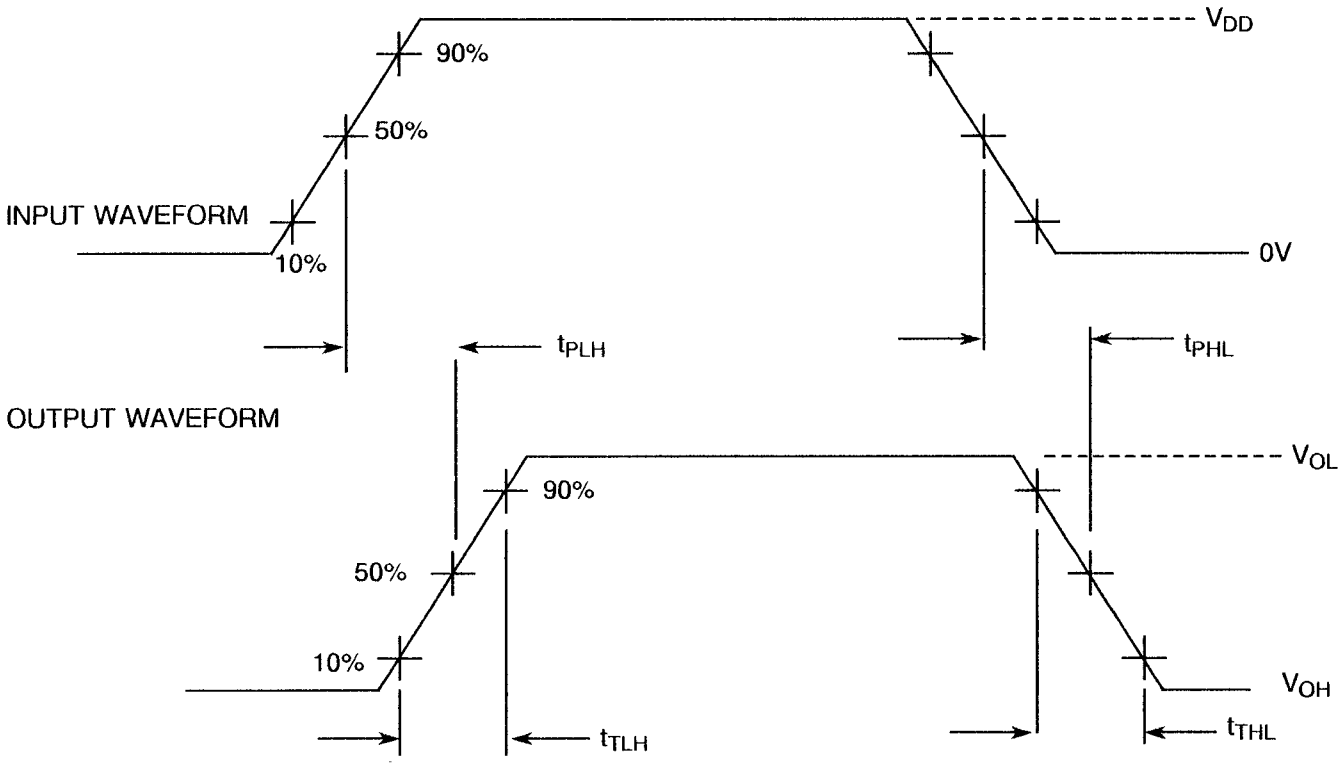
NOTES
1. Each input to be tested separately.
2. f = 100kHz to 1MHz.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(j) - PROPAGATION DELAY AND TRANSITION TIME



VOLTAGE WAVEFORMS



NOTES

1. Pulse Generator – V_P = 0V to V_{DD}, t_r and $t_f \leq 6$ns, f = 1.0MHz minimum, 50% Duty Cycle, $Z_{OUT} = 50\Omega$.
2. $C_L = 50\text{pF} \pm 5\%$ including scope, wiring and stray capacitance without package in test fixture.

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
3 to 4	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	±2.5	µA
5 to 12	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	±250	nA
13 to 20	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	±250	nA
29 to 32	Output Voltage Low Level 3	V_{OL3}	As per Table 2	As per Table 2	±0.1	V
41 to 44	Output Voltage Low Level 6	V_{OL6}	As per Table 2	As per Table 2	±0.1	V
53 to 56	Output Voltage High Level 3	V_{OH3}	As per Table 2	As per Table 2	±0.25	V
65 to 68	Output Voltage High Level 6	V_{OH6}	As per Table 2	As per Table 2	±0.25	V
69 to 76	Threshold Voltage N-Channel	V_{THN}	As per Table 2	As per Table 2	±0.4	V
77 to 84	Threshold Voltage P-Channel	V_{THP}	As per Table 2	As per Table 2	±0.4	V

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

NO.	CHARACTERISTICS	SYMBOL	CONDITIONS	UNIT
1	Ambient Temperature	T_{amb}	+ 125(+ 0-5)	°C
2	Outputs - (Pins 3-6-8-11)	V_{OUT}	$V_{DD}/2$	V
3	Inputs - (Pins 1-2-4-5-9-10-12-13)	V_{IN}	V_{GEN}	Vac
4	Pulse Voltage	V_{GEN}	0 to V_{DD}	Vac
5	Pulse Frequency Square Wave	f	150k ± 10% Duty Cycle = 50 ± 15% $t_r = t_f \leq 250$ns	Hz
6	Positive Supply Voltage (Pin 14)	V_{DD}	5.0(+ 0 − 0.5)	V
7	Negative Supply Voltage (Pin 7)	V_{SS}	0	V

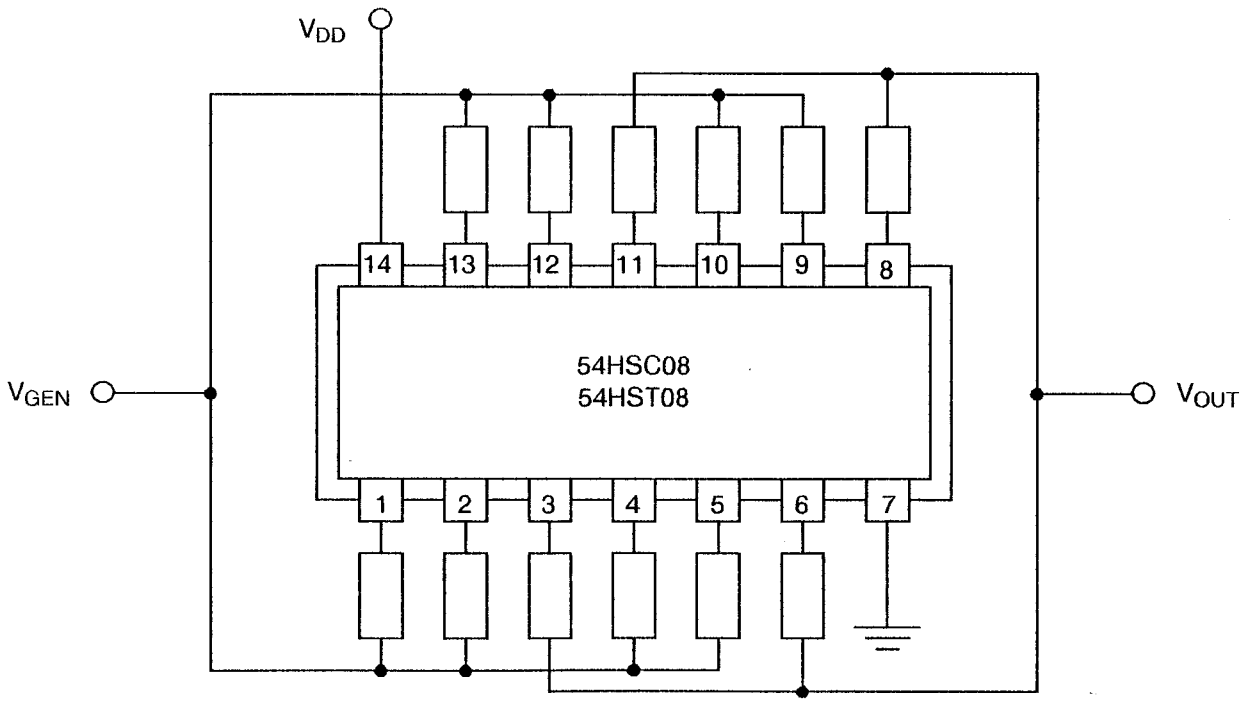
NOTES

1. Input Protection Resistor = Output Load = 1.0kΩ.

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5 of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(b) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

4.9 TOTAL DOSE IRRADIATION TESTING

4.9.1 Application

If specified in Para. 4.2.1 of this specification, total dose irradiation testing shall be performed in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.9.2 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6 of this specification.

4.9.3 Electrical Measurements

The parameters to be measured prior to irradiation exposure are scheduled in Table 2 of this specification. Only devices which meet the requirements of Table 2 shall be included in the test sample.

The parameters to be measured during and on completion of irradiation testing are scheduled in Table 7 of this specification.

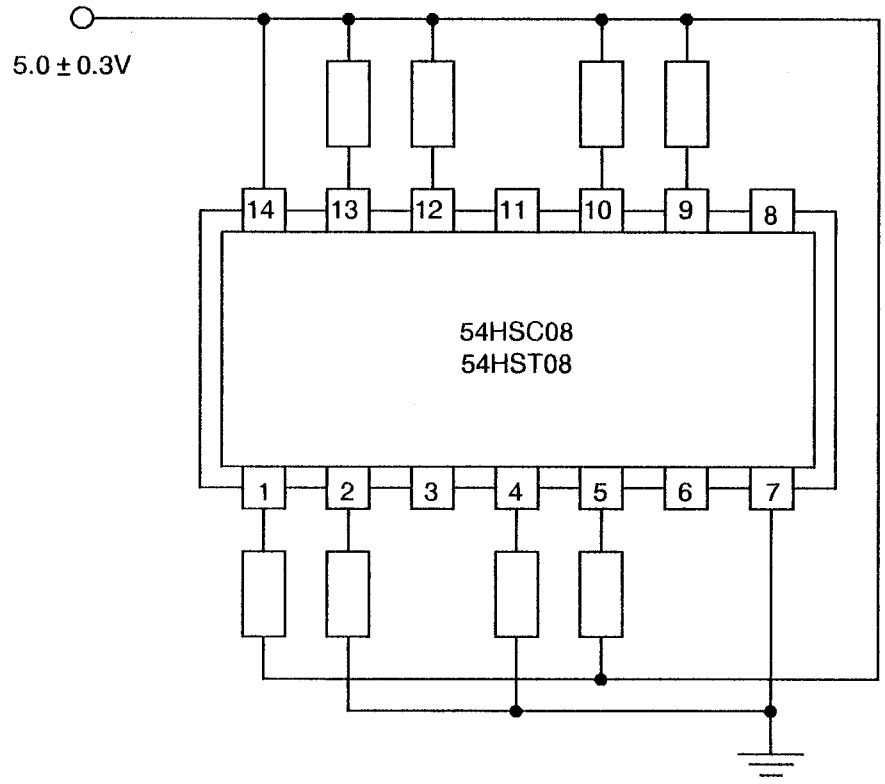
TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	ABSOLUTE		UNIT
						MIN	MAX	
1	Functional Test 1	-	As per Table 2	As per Table 2		-	-	-
2	Functional Test 2	-	As per Table 2	As per Table 2		-	-	-
3 to 4	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	±2.5	-	10	µA
5 to 12	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	±250	-	−500	nA
13 to 20	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	±250	-	500	nA
29 to 32	Output Voltage Low Level 3	V_{OL3}	As per Table 2	As per Table 2	±0.1	-	0.4	V
41 to 44	Output Voltage Low Level 6	V_{OL6}	As per Table 2	As per Table 2	±0.1	-	0.4	V
53 to 56	Output Voltage High Level 3	V_{OH3}	As per Table 2	As per Table 2	±0.25	2.5	-	V
65 to 68	Output Voltage High Level 6	V_{OH6}	As per Table 2	As per Table 2	±0.25	2.5	-	V
69 to 76	Threshold Voltage	V_{THN}	As per Table 2	As per Table 2	±0.4	1.5		V
77 to 84	Threshold Voltage	V_{THP}	As per Table 2	As per Table 2	±0.4	-	3.5	V

NOTES

1. The change limits (Δ) are applicable to the Operating Life test only. The change in parameters between initial and end point measurements shall not exceed the limits given. In addition, the absolute limits shall not be exceeded.

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING



NOTES

1. Input Protection Resistor = 10kΩ.

TABLE 7 - ELECTRICAL MEASUREMENT DURING AND ON COMPLETION OF IRRADIATION TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	ABSOLUTE		UNIT
						MIN	MAX	
3 to 4	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	-	-	600	µA
69 to 76	Threshold Voltage N-Channel	V_{THN}	As per Table 2	As per Table 2	± 0.4	1.5	-	V
77 to 84	Threshold Voltage P-Channel	V_{THP}	As per Table 2	As per Table 2	± 0.4	-	3.5	V

APPENDIX 'A'

AGREED DEVIATIONS FOR GPS (G.B.)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.2	Para's. 9.9.3 and 9.9.2, "Electrical Measurements", may be performed after Para. 9.11, "Dimension Check".
Para. 4.2.3	Para. 9.9.3, "Electrical Measurements at Room Temperature", may be performed before Para. 9.9.2, "Electrical Measurements at High and Low Temperatures". Two additional optional tests may be performed: Static Burn-ins 1 and 2, as specified below. Each burn-in shall be 24 hours and Table 4 Parameter Drift Values shall be applied at 0 and 24 hours and 24 and 48 hours. If these tests are performed, they shall be recorded and counted for PDA.

CONDITIONS FOR STATIC BURN-IN 1

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0−5)	°C
2	Outputs - (Pins 3-6-8-11)	V_{OUT}	$V_{DD}/2$	V
3	Inputs - (Pins 1-2-4-5-9-10-12-13)	V_{IN}	V_{SS}	V
4	Positive Supply Voltage (Pin 14)	V_{DD}	5.0(+0−0.5)	V
5	Negative Supply Voltage (Pin 7)	V_{SS}	0	V

NOTES

1. Input Protection Resistor = Output Load = 1.0kΩ.

CONDITIONS FOR STATIC BURN-IN 2

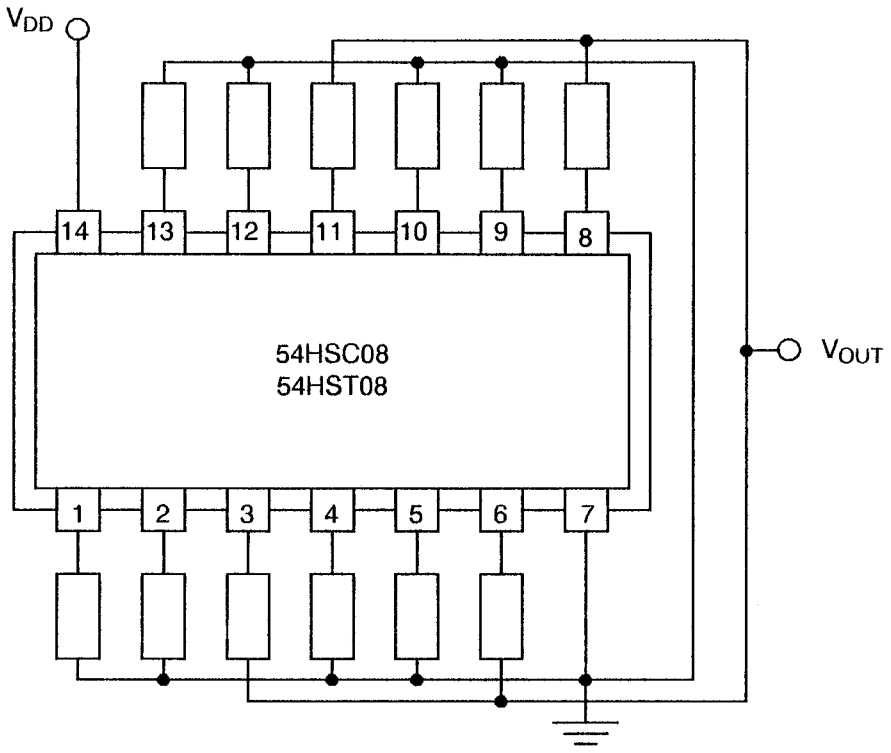
No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0−5)	°C
2	Outputs - (Pins 3-6-8-11)	V_{OUT}	$V_{DD}/2$	V
3	Inputs - (Pins 1-2-4-5-9-10-12-13)	V_{IN}	V_{DD}	V
4	Positive Supply Voltage (Pin 14)	V_{DD}	5.0(+0−0.5)	V
5	Negative Supply Voltage (Pin 7)	V_{SS}	0	V

NOTES

1. Input Protection Resistor = Output Load = 1.0kΩ.

APPENDIX 'A'

ELECTRICAL CIRCUIT FOR STATIC BURN-IN 1



ELECTRICAL CIRCUIT FOR STATIC BURN-IN 2