INTEGRATED CIRCUITS, SILICON MONOLITHIC,

CMOS SILICON GATE, STATIC 64K (4096×16 BIT)

DUAL PORT MEMORY

WITH 3-STATE OUTPUTS,

BASED ON TYPE M67024EV

ESCC Detail Specification No. 9301/034

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space components
coordination group

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1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon, monolithic, CMOS Silicon Gate, Static, 64k (4096 × 16 BIT) Dual Port Memory with 3-State Outputs, based on Type M67024EV. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

As per Figure 3(b).

1.8 CIRCUIT DESCRIPTION

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 with a Minimum Critical Path Failure Voltage of 1 000 Volts.

1.11 INPUT PROTECTION NETWORK

Double transistor protection shall be incorporated into each input as shown in Figure 3(e).

TABLE 1(a) - TYPE VARIANTS

VARIANT	BASED ON TYPE	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
01	M67024EV-45	FLAT PACK	2(a)	G2
02	M67024EV-45	CHIP CARRIER	2(b)	2
03	M67024EV-55	FLAT PACK	2(a)	G2
04	M67024EV-55	CHIP CARRIER	2(b)	2

TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage	V_{DD}	− 0.3 to + 7.0	V	Note 1
2	Input Voltage	V_{IN}	− 0.3 to V_{DD} + 0.3	V	Note 2 Power On
3	Output Current	$\pm I_{OUT}$	$V_{OUT} = V_{DD}$: + 140 $V_{OUT} = V_{SS}$: − 90	mA	Note 3
4	Device Dissipation (Continuous)	P_D	2200	mW	Per Package
5	Operating Temperature Range	T_{op}	− 55 to + 125	°C	T_{amb}
6	Storage Temperature Range	T_{stg}	− 65 to + 150	°C	
7	Soldering Temperature For FP For CCP	T_{sol}	 + 265 + 245	°C	 Note 4 Note 5
8	Thermal Resistance	$R_{TH(J-A)}$	18	°C/W	
9	Junction Temperature	T_J	+ 165	°C	

NOTES

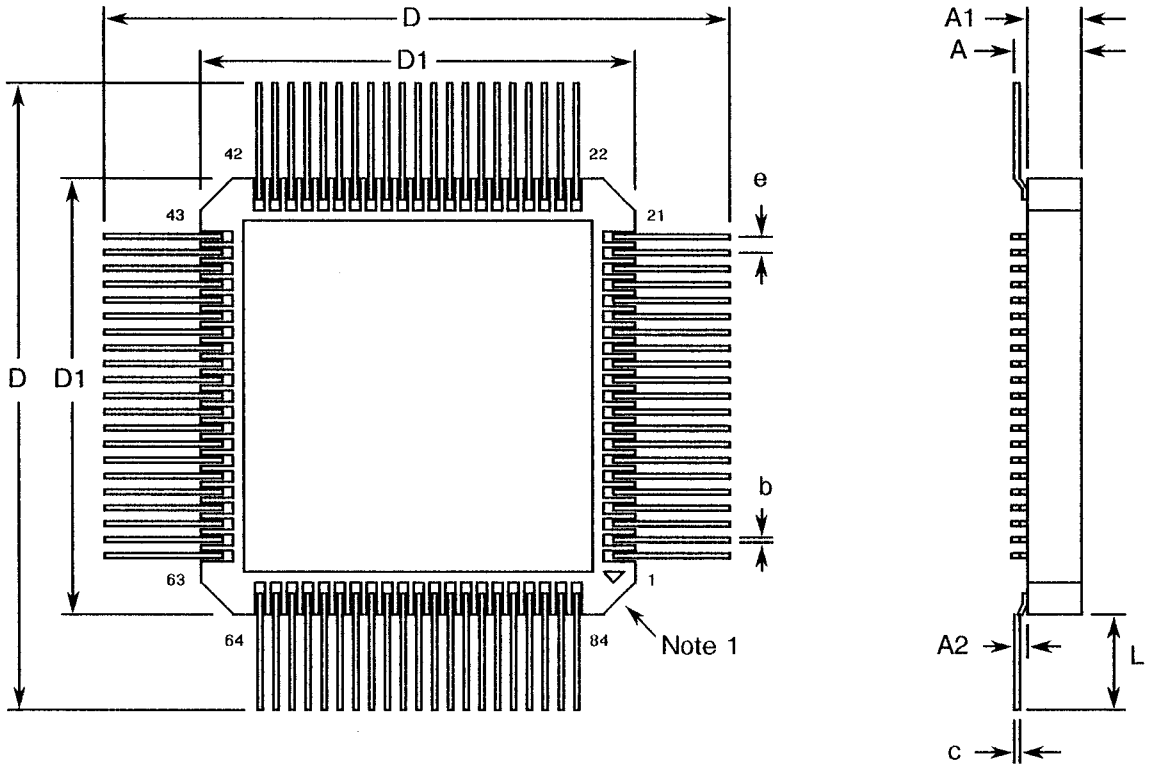
1. Device is functional from + 4.5V to + 5.5V with reference to Ground.
2. V_{DD} + 0.3V should not exceed + 7.0V.
3. The maximum output current of any single output.
4. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
5. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION

Not applicable.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - FLAT PACKAGE, 84-PIN

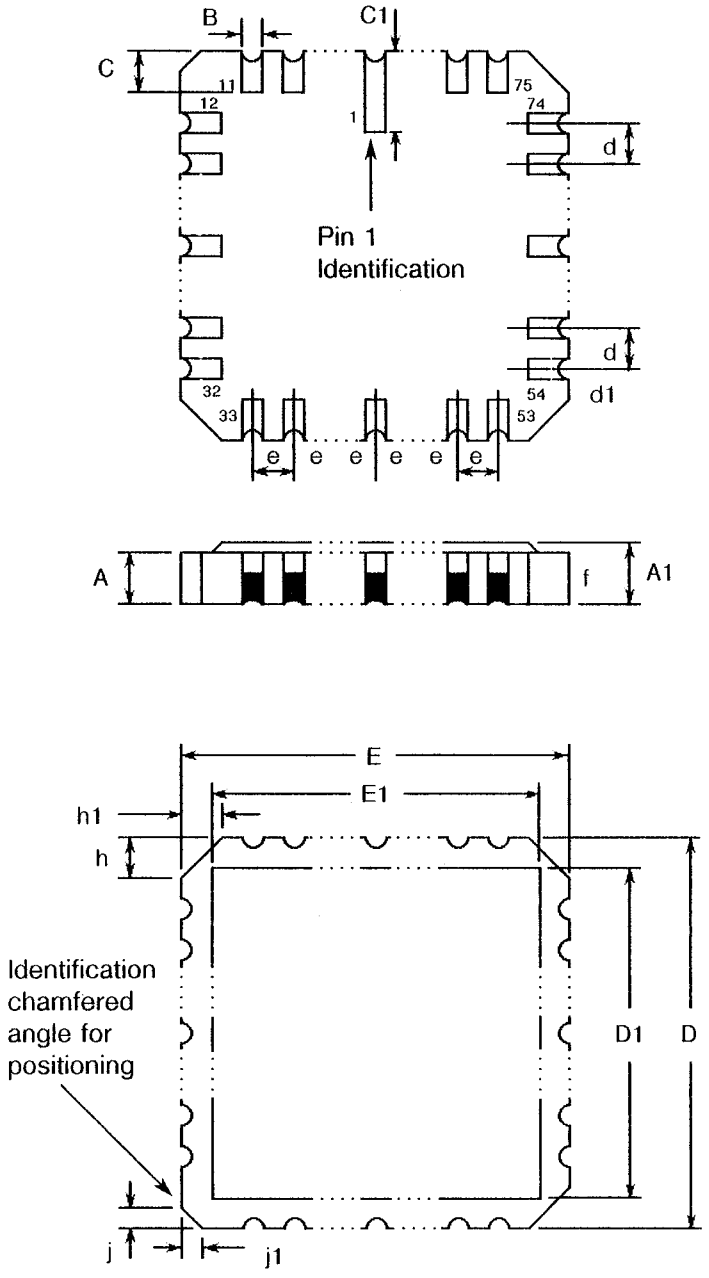


SYMBOL	MILLIMETERS		NOTES
	MIN.	MAX.	
A	2.05	2.89	
A1	1.82	2.67	
A2	-	0.356	
b	0.457 TYPICAL		3
c	0.22	0.31	
D	48.77	50.28	
D1	28.96	29.46	
e	1.27 TYPICAL		2, 4
L	8.84	11.43	

NOTES: See Page 9.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - CHIP CARRIER PACKAGE, 84-TERMINAL



SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	1.83	2.23	
A1	2.23	2.64	
B	0.91 TYPICAL		3
C	1.14	1.40	3
C1	2.20	2.72	
D	28.90	29.59	
D1	17.50 TYPICAL		
d	1.27 TYPICAL		2, 4
E	28.90	29.59	
E1	17.50 TYPICAL		
e	1.27 TYPICAL		2, 4
h, h1	1.016 TYPICAL		5
j, j1	0.51 TYPICAL		6

NOTES: See Page 9.

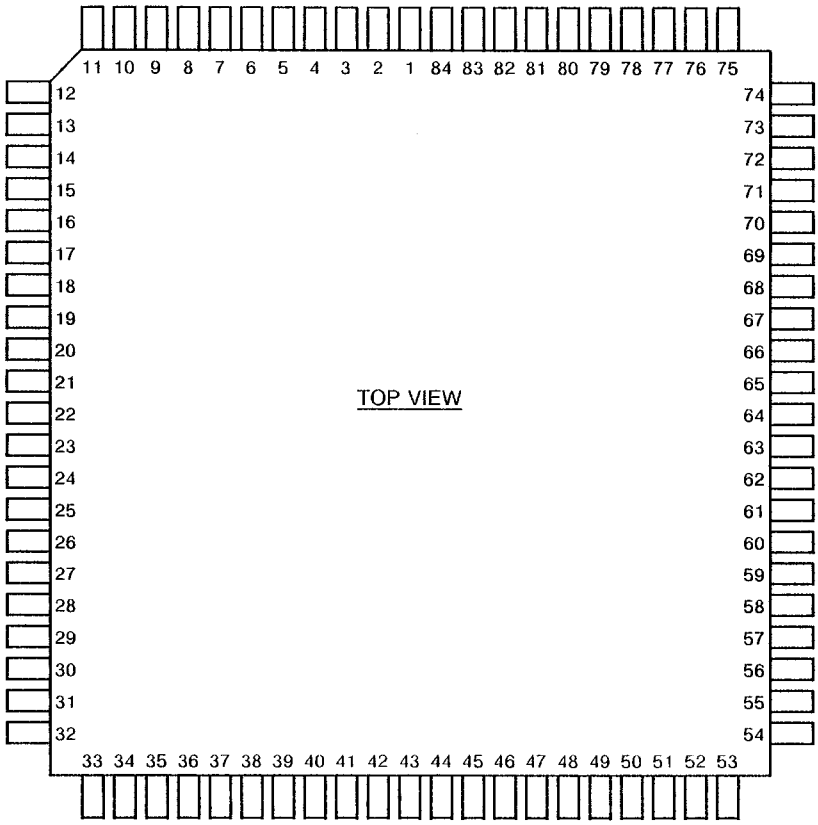
FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURES 2(a) TO 2(b) INCLUSIVE

1. Index area: a notch, letter or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages the index shall be as defined in Figure 2(b).
2. The true position pin or terminal spacing is 1.27mm between centrelines. Each pin or terminal centreline shall be located within 0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
3. All leads or terminals.
4. 76 spaces.
5. 3 non-index corners - 6 dimensions.
6. Index corner only - 2 dimensions.

FIGURE 3(a) - PIN ASSIGNMENT

FLAT AND CHIP CARRIER PACKAGES



PIN DESCRIPTION

PIN No.	FUNCTION	PIN No.	FUNCTION	PIN No.	FUNCTION	PIN No.	FUNCTION
1	V_{DD}	15	I/O_{11L}	29	I/O_{5R}	43	GND
2	$\overline{OE}_L$	16	I/O_{12L}	30	I/O_{6R}	44	$\overline{SEM}_R$
3	I/O_{0L}	17	I/O_{13L}	31	I/O_{7R}	45	$\overline{CS}_R$
4	I/O_{1L}	18	GND	32	I/O_{8R}	46	$\overline{UB}_R$
5	GND	19	I/O_{14L}	33	I/O_{9R}	47	$\overline{LB}_R$
6	I/O_{2L}	20	I/O_{15L}	34	I/O_{10R}	48	N.C.
7	I/O_{3L}	21	V_{DD}	35	I/O_{11R}	49	A_{11R}
8	I/O_{4L}	22	GND	36	I/O_{12R}	50	A_{10R}
9	I/O_{5L}	23	I/O_{0R}	37	I/O_{13R}	51	A_{9R}
10	I/O_{6L}	24	I/O_{1R}	38	I/O_{14R}	52	A_{8R}
11	I/O_{7L}	25	I/O_{2R}	39	GND	53	A_{7R}
12	I/O_{8L}	26	V_{DD}	40	I/O_{15R}	54	A_{6R}
13	I/O_{9L}	27	I/O_{3R}	41	$\overline{EO}_R$	55	A_{5R}
14	I/O_{10L}	28	I/O_{4R}	42	$R/\overline{W}_R$	56	A_{4R}

FIGURE 3(a) - PIN ASSIGNMENT (CONTINUED)

PIN DESCRIPTION (CONTINUED)

PIN No.	FUNCTION	PIN No.	FUNCTION	PIN No.	FUNCTION	PIN No.	FUNCTION
57	A_{3R}	64	GND	71	A_{4L}	78	A_{11L}
58	A_{2R}	65	$\overline{BUSY}_L$	72	A_{5L}	79	N.C.
59	A_{1R}	66	$\overline{INT}_L$	73	A_{6L}	80	$\overline{LB}_L$
60	A_{0R}	67	A_{0L}	74	A_{7L}	81	$\overline{UB}_L$
61	$\overline{INT}_R$	68	A_{1L}	75	A_{8L}	82	$\overline{CS}_L$
62	$\overline{BUSY}_R$	69	A_{2L}	76	A_{9L}	83	$\overline{SEM}_L$
63	$M/\overline{S}$	70	A_{3L}	77	A_{10L}	84	$R/\overline{W}_L$

NOTES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CS}_L$	$\overline{CS}_R$	Chip Select
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L} - A_{11L}	A_{0R} - A_{11R}	Address
I/O_{0L} - I/O_{15L}	I/O_{0R} - I/O_{15R}	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{DD}		Power
GND		Ground

FIGURE 3(b) - TRUTH TABLES

GENERAL NOTES

1. Logic level Definitions: L = Low Level, H = High Level, Z = High Impedance, ⤒ = Transition from Low to High Level, X = Irrelevant, NC = No Change.

NON-CONTENTION READ/WRITE CONTROL

INPUTS (1)						OUTPUTS		MODE
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O_8 - I/O_{15}	I/O_0 - I/O_7	
H	X	X	X	X	H	Z	Z	Deselected: Power Down
X	X	X	H	H	H	Z	Z	Deselected: Power Down
L	L	X	L	H	H	$DATA_{IN}$	Z	Write to Upper Byte Only
L	L	X	H	L	H	Z	$DATA_{IN}$	Write to Lower Byte Only
L	L	X	L	L	H	$DATA_{IN}$	$DATA_{IN}$	Write to Both Bytes
L	H	L	L	H	H	$DATA_{OUT}$	Z	Read Upper Byte Only
L	H	L	H	L	H	Z	$DATA_{OUT}$	Read Lower Byte Only
L	H	L	L	L	H	$DATA_{OUT}$	$DATA_{OUT}$	Read Both Bytes
X	X	H	X	X	X	Z	Z	Outputs Disabled
H	H	L	X	X	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Data in Semaphore Flag
X	H	L	H	H	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Data in Semaphore Flag
H	⤒	X	X	X	L	$DATA_{IN}$	$DATA_{IN}$	Write D_{IN0} into Semaphore Flag
X	⤒	X	H	H	L	$DATA_{IN}$	$DATA_{IN}$	Write D_{IN0} into Semaphore Flag
L	X	X	L	X	L	-	-	Not Allowed
L	X	X	X	L	L	-	-	Not Allowed

NOTES

1. A_{0L}-$A_{11L} \neq A_{0R}$-A_{11R}.

INTERRUPT FLAG (NOTE 1)

LEFT PORT					RIGHT PORT					FUNCTION
R/$\overline{W}_L$	$\overline{CS}_L$	$\overline{OE}_L$	A_{0L}-A_{11L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CS}_R$	$\overline{OE}_R$	A_{0R}-A_{11R}	$\overline{INT}_R$	
L	L	X	FFF	X	X	X	X	X	L (2)	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	FFF	H(3)	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L (3)	L	L	X	FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	FFE	H (2)	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES

1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then NC.
3. If $\overline{BUSY}_R$ = L, then NC.

FIGURE 3(b) - TRUTH TABLES (CONTINUED)

ARBITRATION OPTIONS

OPTIONS	INPUTS					OUTPUTS	
	$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	M/$\overline{S}$	$\overline{SEM}$	$\overline{BUSY}$	$\overline{INT}$
Busy Logic Master	L L	X L	L X	H H	H H	Output Signal	-
Busy Logic Slave	L L	X L	L X	L L	H H	Input Signal	-
Interrupt Logic	L L	X L	L X	X X	H H	-	Output Signal
Semaphore Logic (1)	H H	X X	X X	H L	L L	H Z	-

NOTES

1. Input Signals are for Semaphore Flags set and test (Write and Read) operations.

ARBITRATION

LEFT PORT		RIGHT PORT		FLAGS (1)		FUNCTION
$\overline{CS}_L$	A_{0L}-A_{11L}	$\overline{CS}_R$	A_{0R}-A_{11R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R}$-A_{11R}	L	$\neq A_{0L}$-A_{11L}	H	H	No Contention

ADDRESS ARBITRATION WITH $\overline{CS}$ LOW BEFORE ADDRESS MATCH

L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved

$\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CS}$

LL5R	$=A_{0R}$-A_{11R}	LL5R	$=A_{0L}$-A_{11L}	H	L	L-Port Wins
RL5L	$=A_{0R}$-A_{11R}	RL5L	$=A_{0L}$-A_{11L}	L	H	R-Port Wins
LW5R	$=A_{0R}$-A_{11R}	LW5R	$=A_{0L}$-A_{11L}	H	L	Arbitration Resolved
LW5R	$=A_{0R}$-A_{11R}	LW5R	$=A_{0L}$-A_{11L}	L	H	Arbitration Resolved

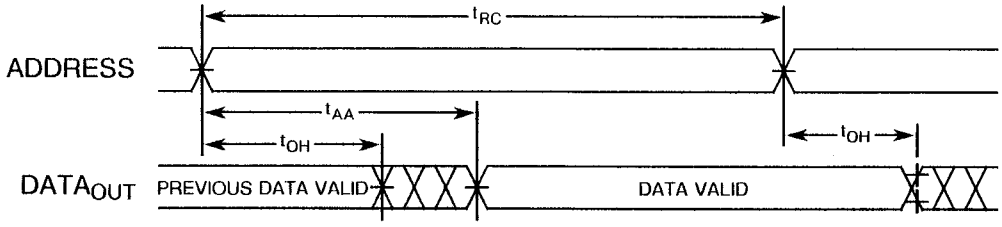
NOTES

1. $\overline{INT}$ Flags: Don't Care.
2. LV5R = Left Address Valid $\geq$5ns before right address.
   RV5L = Right Address Valid $\geq$5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CS}$ = Low $\geq$5ns before Right $\overline{CS}$.
   RL5L = Right $\overline{CS}$ = Low $\geq$5ns before Left $\overline{CS}$.
   LW5R = Left and Right $\overline{CS}$ = Low within 5ns of each other.

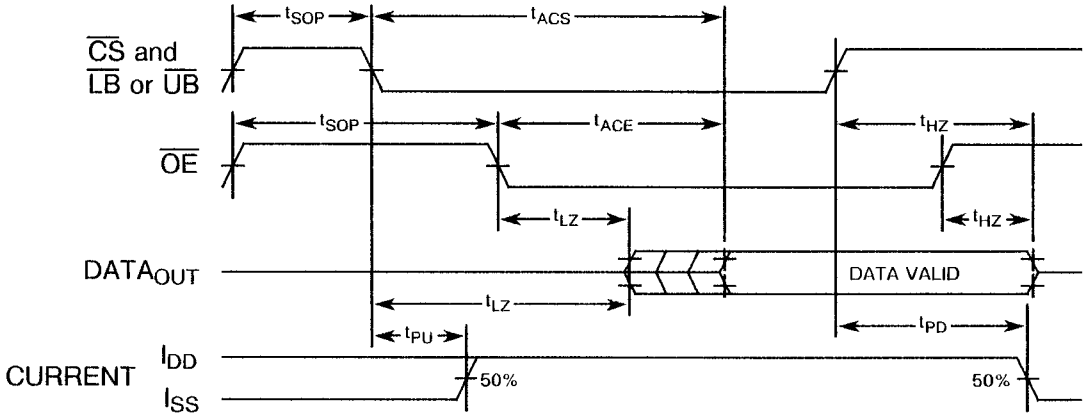
FIGURE 3(b) - TRUTH TABLE

TIMING WAVEFORMS

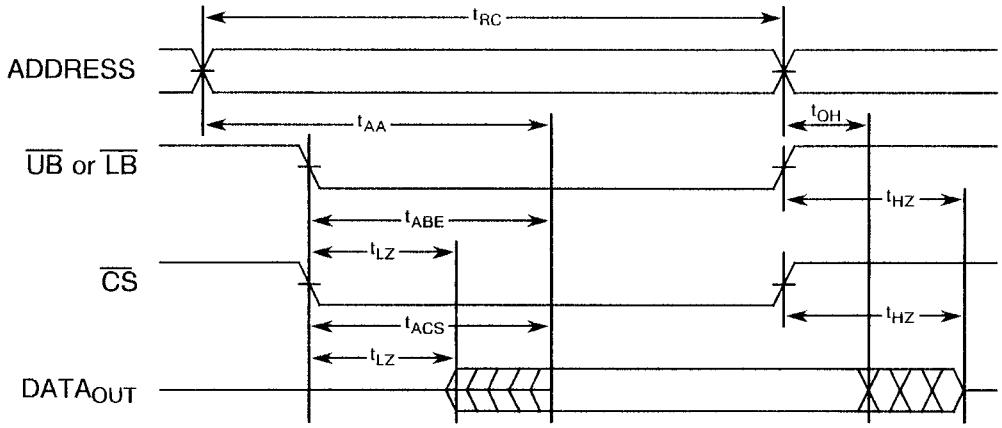
READ CYCLE 1, EITHER SIDE (NOTES 1, 2, 4)



READ CYCLE 2, EITHER SIDE (NOTES 1, 3, 5)



READ CYCLE 3, EITHER SIDE (NOTES 1, 3, 4, 5)



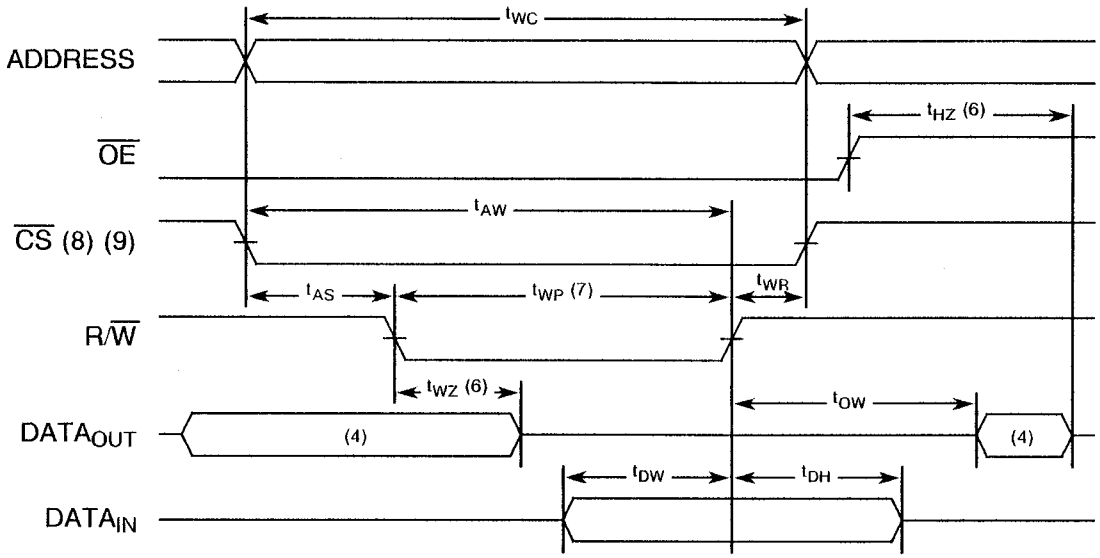
NOTES

1. R/$\overline{W}$ is high for read cycles.
2. Device is continuously enabled, $\overline{CS}$ = L, $\overline{UB}$ or $\overline{LB}$ = L. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = L.
5. To access RAM, $\overline{CS}$ = L, $\overline{UB}$ or $\overline{LB}$ = L, $\overline{SEM}$ = H. To access semaphore, $\overline{CS}$ = H, $\overline{SEM}$ = L. (See Non-contention Read/Write Control Truth Table).

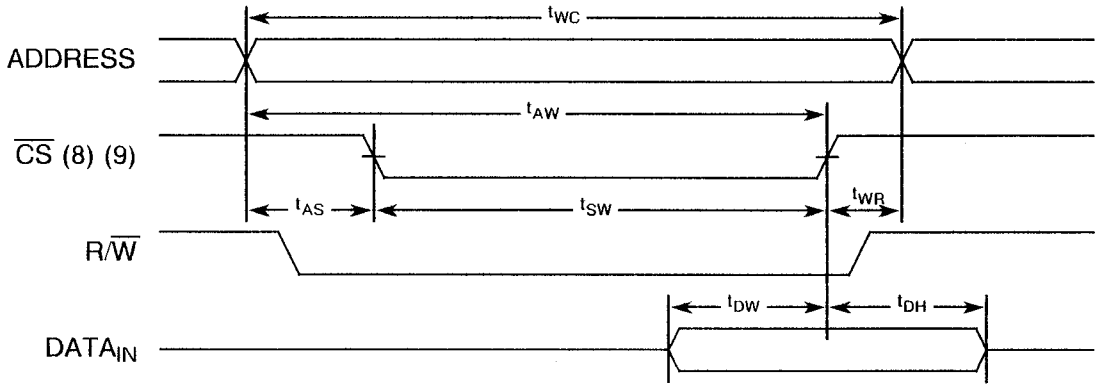
FIGURE 3(b) - TRUTH TABLE (CONTINUED)

TIMING WAVEFORMS (CONTINUED)

WRITE CYCLE 1, R/$\overline{W}$ CONTROLLED TIMING (NOTES 1, 2, 3, 7)



WRITE CYCLE 2, $\overline{CS}$ CONTROLLED TIMING (NOTES 1, 2, 3, 5)



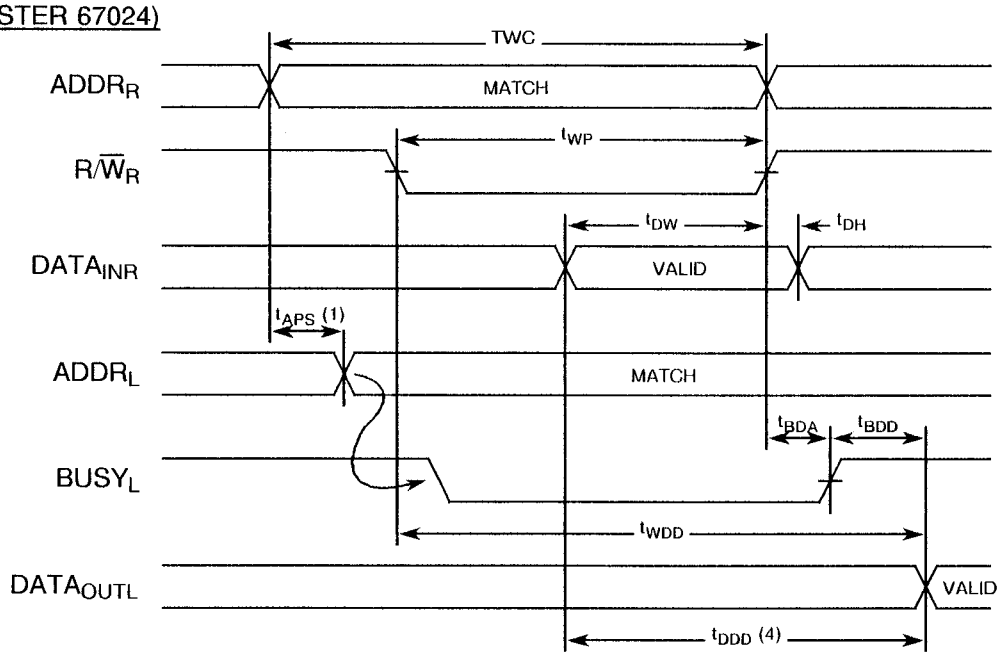
NOTES

1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{SW} or t_{WP}) of a low $\overline{CS}$ or $\overline{SEM}$ and a low R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5.0pF load (including scope and jig).
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WZ} + t_{DW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. To access RAM, $\overline{CS}$ = L, $\overline{SEM}$ = H.
9. To access upper byte, $\overline{CS}$ = L, $\overline{UB}$ = L, $\overline{SEM}$ = H.
   To access lower byte, $\overline{CS}$ = L, $\overline{LB}$ = L, $\overline{SEM}$ = H.

FIGURE 3(b) - TRUTH TABLE (CONTINUED)

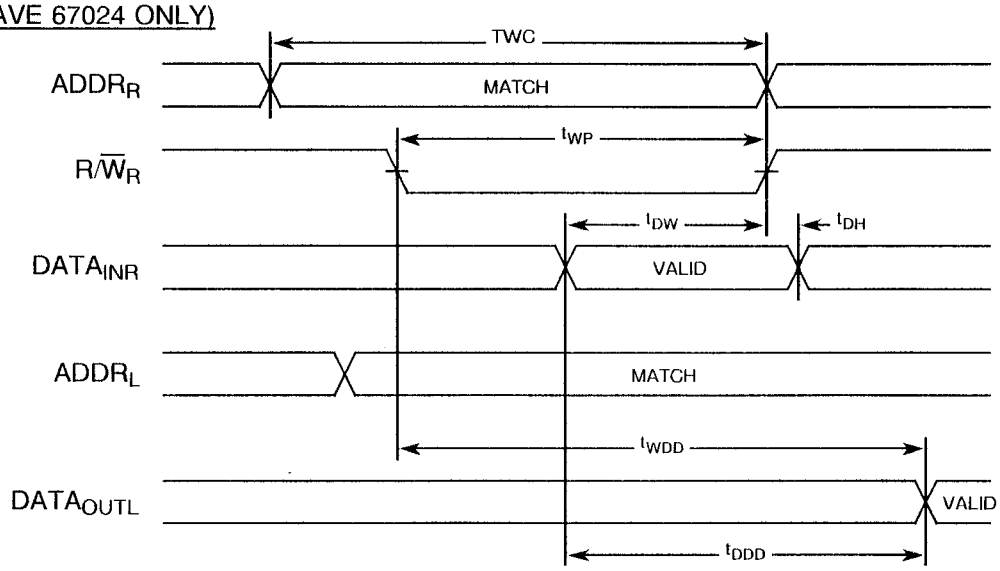
TIMING WAVEFORMS (CONTINUED)

READ WITH $\overline{BUSY}$ (NOTES 2, 3, 4)
(FOR MASTER 67024)



NOTES
1. To ensure that the earlier of the two ports wins.
2. Write cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ = L for the reading port.

WRITE WITH PORT-TO-PORT (NOTES 1, 2, 3)
(FOR SLAVE 67024 ONLY)

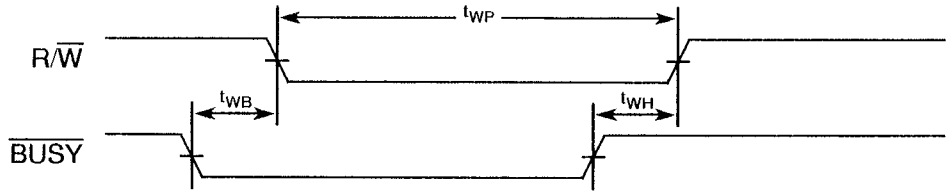


NOTES
1. Assume $\overline{BUSY}$ input = H for the writing port, and $\overline{OE}$ = L for the reading port.
2. Write cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enabled for both ports.

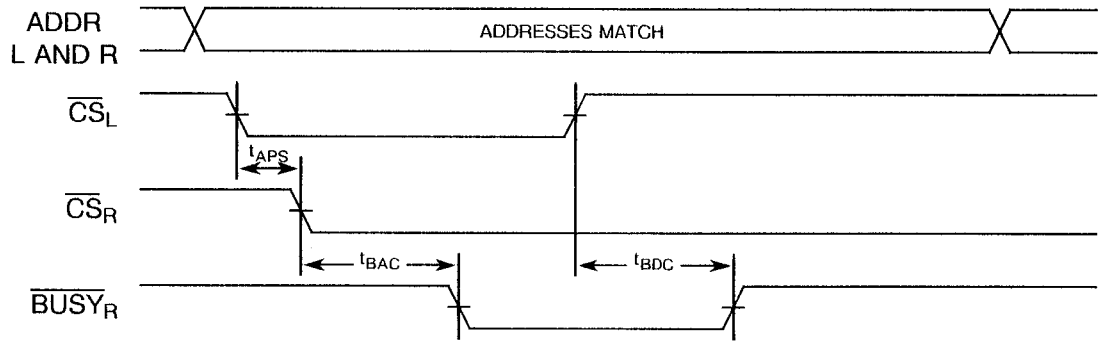
FIGURE 3(b) - TRUTH TABLE (CONTINUED)

TIMING WAVEFORMS (CONTINUED)

WRITE WITH $\overline{BUSY}$
(FOR SLAVE 67024)



CONTENTION CYCLE 1, $\overline{CS}$ ARBITRATION
(FOR MASTER 67024 ONLY)



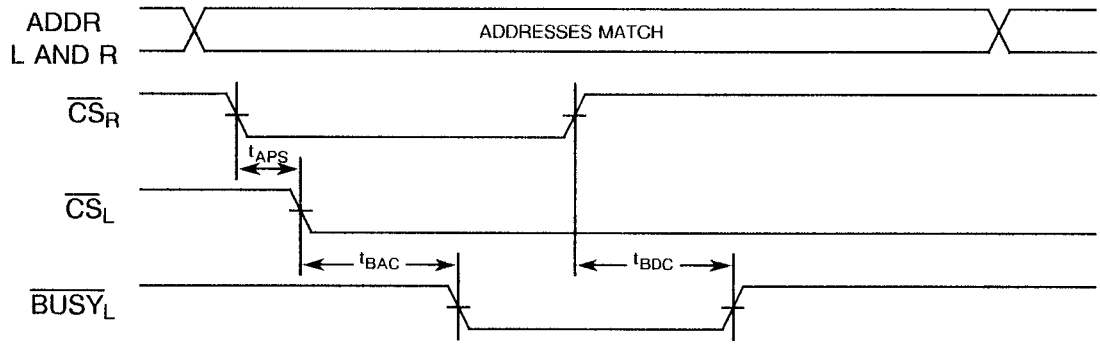
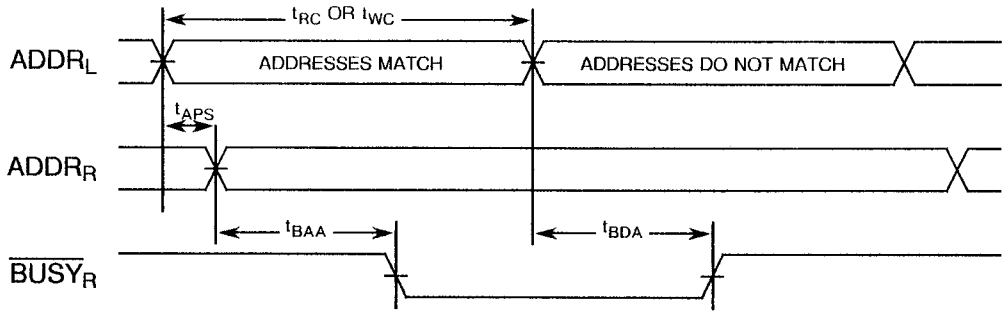


FIGURE 3(b) - TRUTH TABLE (CONTINUED)

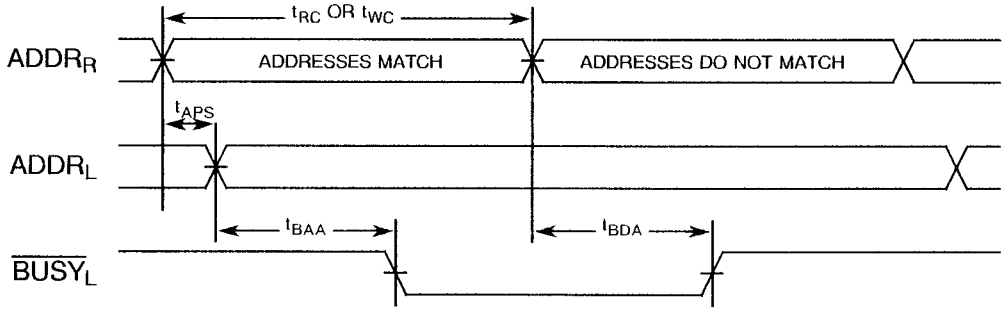
TIMING WAVEFORMS (CONTINUED)

CONTENTION CYCLE 2, ADDRESS VALID ABRITRATION (NOTE 1)
(FOR MASTER 67024 ONLY)

LEFT ADDRESS VALID FIRST



RIGHT ADDRESS VALID FIRST



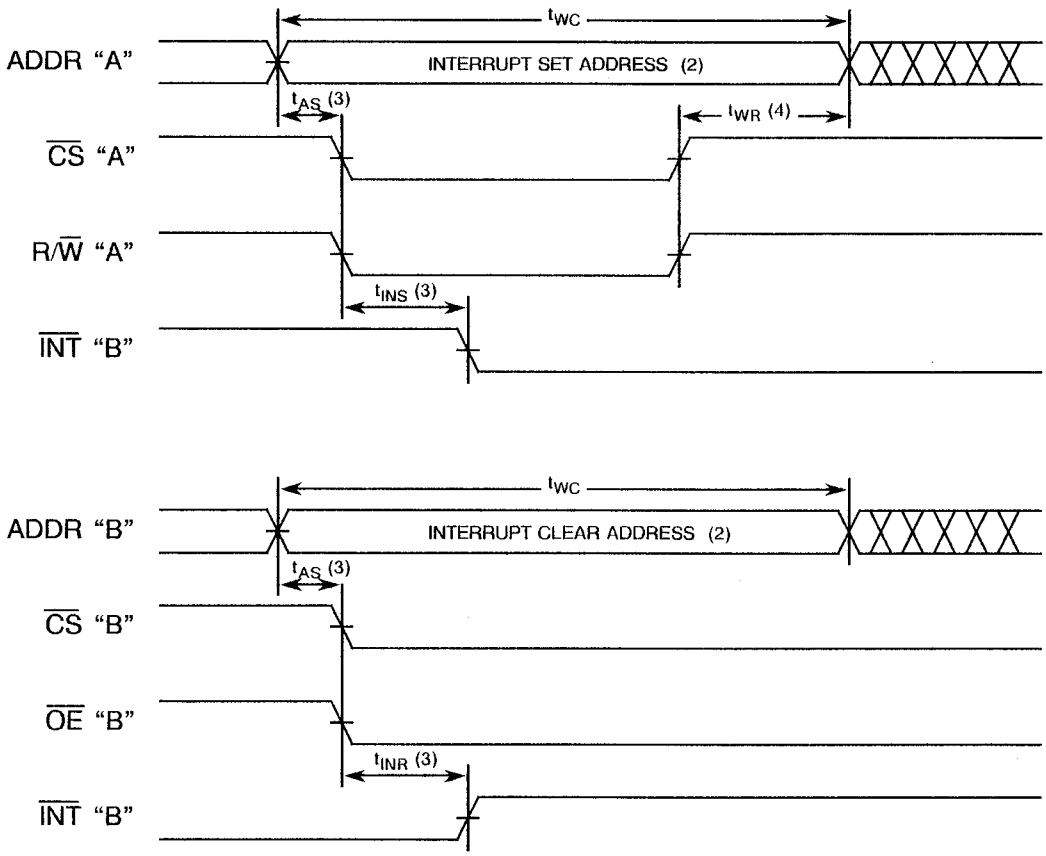
NOTES

1. $\overline{CS}_L = \overline{CS}_R = L$.

FIGURE 3(b) - TRUTH TABLE (CONTINUED)

TIMING WAVEFORMS (CONTINUED)

INTERRUPT TIMING (NOTE 1)



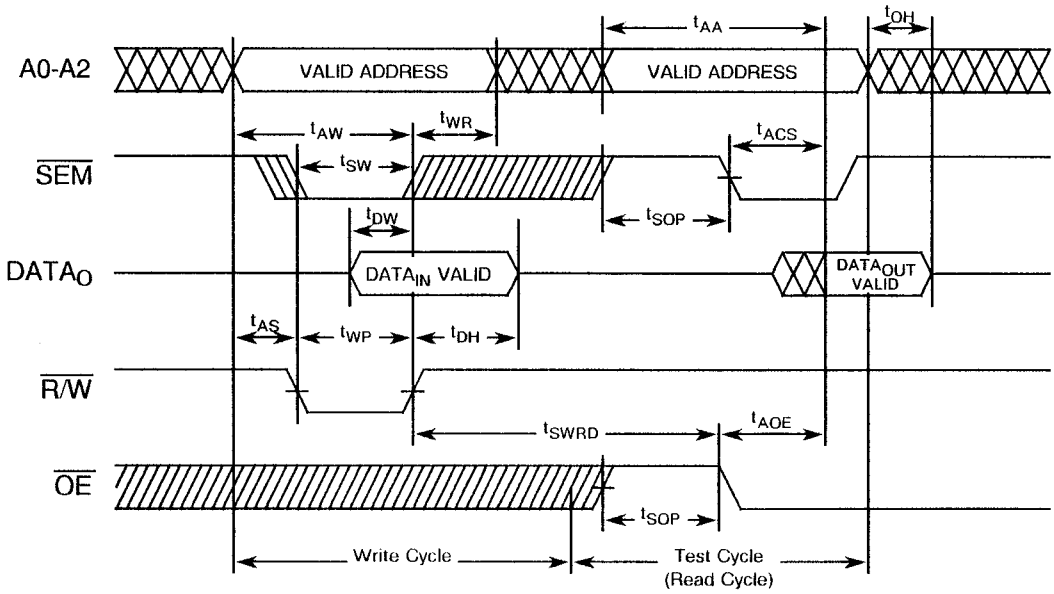
NOTES

1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt Flag Truth Table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

FIGURE 3(b) - TRUTH TABLE (CONTINUED)

TIMING WAVEFORMS (CONTINUED)

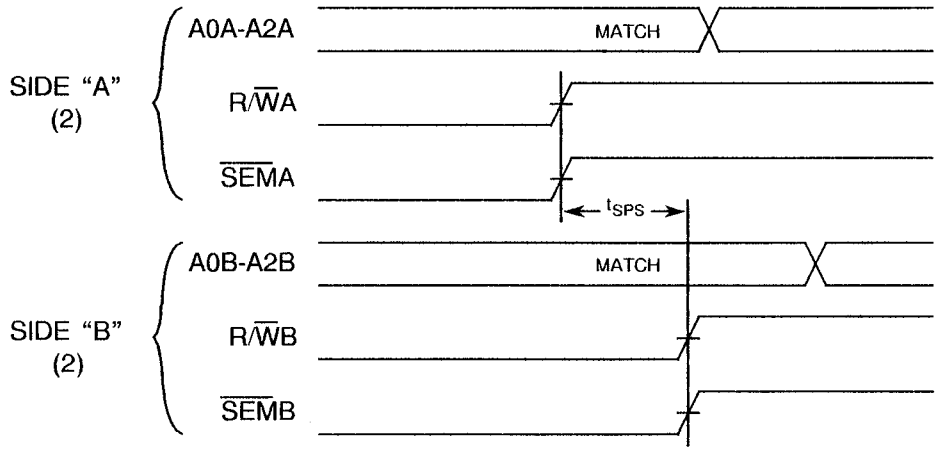
SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE (NOTE 1)



NOTES

1. $\overline{CS}$ = H for the duration of the above timing (both write and read cycle).

SEMAPHORE CONTENTION (NOTES 1, 3, 4)



NOTES

1. $D_{OR} = D_{OL}$ = L, $\overline{CS}_R = \overline{CS}_L$ = H, semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. Either side "A" = left and side "B" = right, or side "A" = right and side "B" = left.
3. This parameter is measured from the point where $R/\overline{W}_A$ or $\overline{SEM}_A$ goes high until $R/\overline{W}_B$ or $\overline{SEM}_B$ goes high.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

FIGURE 3(c) - CIRCUIT DESCRIPTION

FUNCTIONAL DESCRIPTION

The M67024 has 2 ports with separate control, address and I/O pins that permit independent read/write access to any memory location. These devices have an automatic power-down feature controlled by $\overline{CS}$. $\overline{CS}$ controls on-chip power-down circuitry which causes the port concerned to go into stand-by mode when not selected ($\overline{CS}$ high). When a port is selected, access to the full memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In read mode, the port's $\overline{OE}$ turns the Output drivers on when set Low. Non-conflicting READ/WRITE conditions are illustrated in the Truth Table.

The interrupt flag ($\overline{INT}$) allows communication between ports or systems. If the User chooses to use the interrupt function, a memory location (mail box or message centre) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location FFE (HEX). The left port clears the interrupt by reading address location FFE. Similarly, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location FFF (HEX), and the right port must read memory location FFF in order to clear the interrupt flag ($\overline{INT}_R$). The 16 bit message at FFE or FFF is user-defined. If the interrupt function is not used, address locations FFE and FFF are not reserved for mail boxes but become part of the RAM. See the Truth Table for the interrupt function.

ARBITRATION LOGIC FUNCTIONAL DESCRIPTION

The arbitration logic will resolve an address match or a chip select match down to a minimum of 5.0ns and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the inhibited port.

The $\overline{BUSY}$ flags are required when both ports attempt to access the same location simultaneously. Should this conflict arise, on-chip arbitration logic will determine which port has access and set the $\overline{BUSY}$ flag for the inhibited port. $\overline{BUSY}$ is set at speeds that allow the processor to hold the operation with its associated address and data. It should be noted that the operation is invalid for the port for which $\overline{BUSY}$ is set LOW. The inhibited port will be given access when $\overline{BUSY}$ goes inactive.

A conflict will occur when both left and right ports are active and the 2 addresses coincide. The on-chip arbitration determines access in these circumstances. 2 modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CS}$ on-chip control logic arbitrates between $\overline{CS}_L$ and $\overline{CS}_R$ for access; or (2) if the $\overline{CS}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (see the Truth Table). The inhibited port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation in both arbitration modes.

DATA BUS WIDTH EXPANSION MASTER/SLAVE DESCRIPTION

Expanding the data bus width to 32 or more bits in a dual-port RAM system means that several chips may be active simultaneously. If every chip has a hardware arbitrator, and the addresses for each chip arrive at the same time, 1 chip may activate its L $\overline{BUSY}$ signal while another activates its R $\overline{BUSY}$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To overcome this "Busy Lock-Out" problem, MHS has developed a MASTER/SLAVE system which uses a single hardware arbitrator located on the MASTER. The SLAVE has $\overline{BUSY}$ inputs which allow direct interface to the MASTER with no external components, giving a speed advantage over other systems.

When dual-port RAMs are expanded in width, the SLAVE RAMs must be prevented from writing until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a conflict situation. Conversely, the write pulse must extend a hold time beyond $\overline{BUSY}$ to ensure that a write cycle occurs once the conflict is resolved. This timing is inherent in all dual-port memory systems where more than 1 chip is active at the same time.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

The write pulse to the SLAVE must be inhibited by the MASTER's maximum arbitration time. If a conflict then occurs, the write to the SLAVE will be inhibited because of the MASTER's $\overline{BUSY}$ signal.

SEMAPHORE LOGIC FUNCTIONAL DESCRIPTION

The M67024 is an extremely fast dual-port 4k × 16 CMOS static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either of the processors on the left or right side of the dual-port RAM to claim priority over the other for functions defined by the system software. For example, the semaphore flag can be used by 1 processor to inhibit the other from accessing a portion of the dual-port RAM or any other shared resource.

The dual-port RAM has a fast access time, and the 2 ports are completely independent of one another. This means that the activity on the left port cannot slow the access time of the right port. The ports are identical in function to standard CMOS static RAMS and can be read from, or written to, at the same time with the only possible conflict arising from simultaneous writing to, or a simultaneous READ/WRITE operation on, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system programme to prevent conflicts in the non-semaphore segment of the dual-port RAM. The devices have an automatic power-down feature controlled by $\overline{CS}$, the dual-port RAM select and $\overline{SEM}$, the semaphore enable. The $\overline{CS}$ and $\overline{SEM}$ pins control on-chip power-down circuitry that permits the port concerned to go into stand-by mode when not selected. This condition is shown in the Truth Table when $\overline{CS}$ and $\overline{SEM}$ are both high.

Systems best able to exploit the M67024 are based around multiple processors or controllers and are typically very high-speed, software controlled or software-intensive systems. These systems can benefit from the performance enhancement offered by the M67024 hardware semaphores, which provide a lock-out mechanism without the need for complex programming.

Software handshaking between processors offers the maximum level of system flexibility by permitting shared resources to be allocated in varying configurations. The M67024 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more usual methods of hardware arbitration is that neither processor ever incurs wait states. This can prove a considerable advantage in very high speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of 8 latches independent of the dual-port RAM. These latches can be used to pass a flag or token from one port to the other to indicate that a shared resource is in use. The semaphores provide the hardware context for the "Token Passing Allocation" method of use assignment. This method uses the state of a semaphore latch as a token indicating that a shared resource is in use. If the left processor needs to use a resource, it requests the token by setting the latch. The processor then verifies that the latch has been set by reading it. If the latch has been set, the processor assumes control over the shared resource. If the latch has not been set, the left processor has established that the right processor had set the latch first, has the token and is using the shared resource. The left processor may then either repeatedly query the status of the semaphore, or abandon its request for the token and perform another operation whilst occasionally attempting to gain control of the token through a set and test operation. Once the right side has relinquished the token, the left side will be able to take control of the shared resource.

The semaphore flags are active low. A token is requested by writing a '0' to a semaphore latch, and is relinquished again when the same side writes a '1' to the latch.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

The 8 semaphore flags are located in a separate memory space from the dual-port RAM in the M67024. The address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$ and R/$\overline{W}$) as normally used in accessing a standard static RAM. Each of the flags has a unique address accessed by either side through address pins A0-A2. None of the other address pins has any effect when accessing the semaphores. Only data pin D_0 is used when writing to a semaphore. If a low level is written to an unused semaphore location, the flag will be set to '0' on that side and to '1' on the other side (see Semaphore Procurement Sequence Table). The semaphore can now only be modified by the side showing the '0'. Once a '1' is written to this location from the same side, the flag will be set to '1' for both sides (unless a request is pending from the other side) and the semaphore can then be written to by either side.

The effect the side writing to '0' to a semaphore location has of "locking-out" the other side is the reason for the use of semaphore logic in interprocessor communication. (A thorough discussion of the use of this feature follows below). A '0' written to the semaphore location from the locked-out side will be stored in the semaphore request latch for that side until the semaphore is relinquished by the side having control.

When a semaphore flag is read its value is distributed to all data bits so that a flag set at '1' reads as '1' in all data bits and a flag set at '0' reads as all '0'. The read value is latched into the output register of one side when its semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This prevents the semaphore changing state in the middle of a read cycle as a result of a write cycle issued by the other side. Because of this latch, a repeated read of a semaphore flag in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive, otherwise the output will never change.

The semaphore must use a WRITE/READ sequence in order to ensure that no system level conflict will occur. A processor requests access to shared resources by attempting to write a '0' to a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a '0', yet the semaphore flag will appear as a '1', and the processor will detect this status in the subsequent read (see Semaphore Procurement Sequence Table). For example, assume a processor writes a '0' to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource concerned. If a processor on the right side then attempts to write a '0' to the same semaphore flag it will fail, as will be verified by a subsequent read returning a '1' from the semaphore location on the right side.

It must be noted that a failed semaphore request needs to be followed by either repeated reads or by writing a '1' to the same location. The simple logic diagram for the semaphore flag illustrates the reason for this quite clearly. 2 semaphore request latches feed into a semaphore flag. The first latch to send a '0' to the semaphore flag will force its side of the semaphore flag low and the other side high. This status will be maintained until a '1' is written to the same semaphore request latch. Should a '0' be written to the other side's semaphore request latch in the meantime, the semaphore flag will flip over to this second side as soon as a '1' is written to the first side's request latch. The second side's flag will now stay low until its semaphore request latch is changed to a '1'. Thus, clearly, if a semaphore flag is requested and the processor requesting it no longer requires access to the resource, the entire system can hang up until a '1' is written to the semaphore request latch concerned.

Semaphore timing becomes critical when both sides request the same token by attempting to write a '0' to it at the same time. Semaphore logic is specially conceived to resolve this problem. The logic ensures that only one side will receive the token if simultaneous requests are made. The first side to make a request will receive the token where requests do not arrive at the same time. Where they do arrive at the same time, the logic will assign the token arbitrarily to one of the ports.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

It should be noted, however, that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, errors can be introduced if semaphores are misused or misinterpreted. Code integrity is of the utmost performance when semaphores are being used instead of slower, more restrictive hardware-intensive systems.

Semaphore initialisation is not automatic and must therefore be incorporated in the power-up initialisation procedures. Since any semaphore flag containing a '0' must be reset to '1', initialisation should write a '1' to all request flags from both sides to ensure that they will be available when required.

USING SEMAPHORES - Some Examples

Perhaps the simplest application of semaphores is their use as resource markers for the M67024's dual-port RAM. If it is necessary to split the 4k × 16 RAM into two 2k × 16 blocks which are to be dedicated to serving either the left or the right port at any one time. Semaphore 0 can be used to indicate which side is controlling the lower segment of memory and semaphore 1 can be defined as indicating the upper segment of memory.

To take control of a resource, in this case the lower 2k of a dual-port RAM, the left port processor would then write a '0' into semaphore flag 0 and then read it back. If successful in taking the token (reading back a '0' rather than a '1'), the left processor could then take control of the lower 2k of RAM. If the right processor attempts to perform the same function to take control of the resource after the left processor has already done so, it will read back a '1' in response to the attempted write of a '0' into semaphore 0. At this point, the software may choose to attempt to gain control of the second 2k segment of RAM by writing and then reading a '0' in semaphore 1. If successful, it will lock-out the left processor.

Once the left side has completed its task, it will write a '1' to semaphore 0 and may then attempt to access semaphore 1. If semaphore 1 is still occupied by the right side, the left side may abandon its semaphore request and perform other operations until it is able to write and then read a '0' in semaphore 1. If the right processor performs the same operation with semaphore 0, this protocol would then allow the 2 processors to swap 2k blocks of dual-port RAM between one another.

The blocks do not have to be any particular size, and may even be of variable size depending on the complexity of the software using the semaphore flags. All 8 semaphores could be used to divide the dual-port RAM or other shared resources into 8 parts. Semaphores can even be assigned different meanings on each side, rather than having a common meaning as is described in the above example.

Semaphores are a useful form of arbitration in systems such as disk interfaces where the CPU must be locked out of a segment of memory during a data transfer operation, and the I/O device cannot tolerate any wait states. If semaphores are used, both the CPU and the I/O device can access assigned memory segments, without the need for wait states, once the two devices have determined which memory area is barred to the CPU.

Semaphores are also useful in applications where no memory WAIT state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in complex data structures. Block arbitration is very important in this case, since one processor may be responsible for building and updating a data structure whilst the other processor reads and interprets it. A major error condition may be created if the interpreting processor reads an incomplete data structure. Some sort of arbitration between the two different processors is therefore necessary. The building processor requests access to the block, locks it and is then able to enter the block to update the data structure. Once the update is completed the data structure may be released. This allows the interpreting processor to return to read the complete data structure, thus ensuring a consistent data structure.

FIGURE 3 - CIRCUIT DESCRIPTION (CONTINUED)

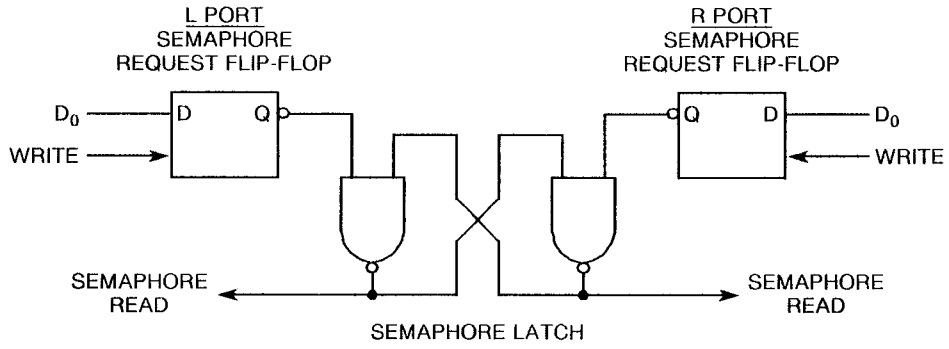
EXAMPLE SEMAPHORE PROCUREMENT SEQUENCE

FUNCTION	D_0 - D_{15} LEFT	D_0 - D_{15} RIGHT	STATUS
No Action	1	1	Semaphore free
Left Port Writes '0' to Semaphore	0	1	Left Port has semaphore token
Right Port Writes '0' to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes '1' to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes '0' to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes '1' to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes '1' to Semaphore	1	1	Semaphore free
Right Port Writes '0' to Semaphore	1	0	Right port has semaphore token
Right Port Writes '1' to Semaphore	1	1	Semaphore free
Left Port Writes '0' to Semaphore	0	1	Left port has semaphore token
Left Port Writes '1' to Semaphore	1	1	Semaphore free

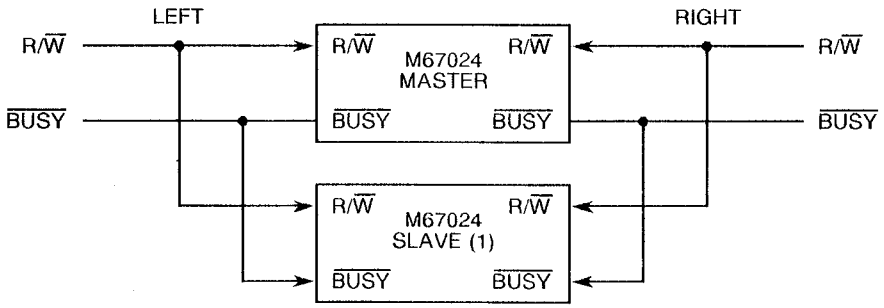
NOTES

1. This table denotes a sequence of events for only 1 of the 8 semaphores on the M67024.

SEMAPHORE LOGIC



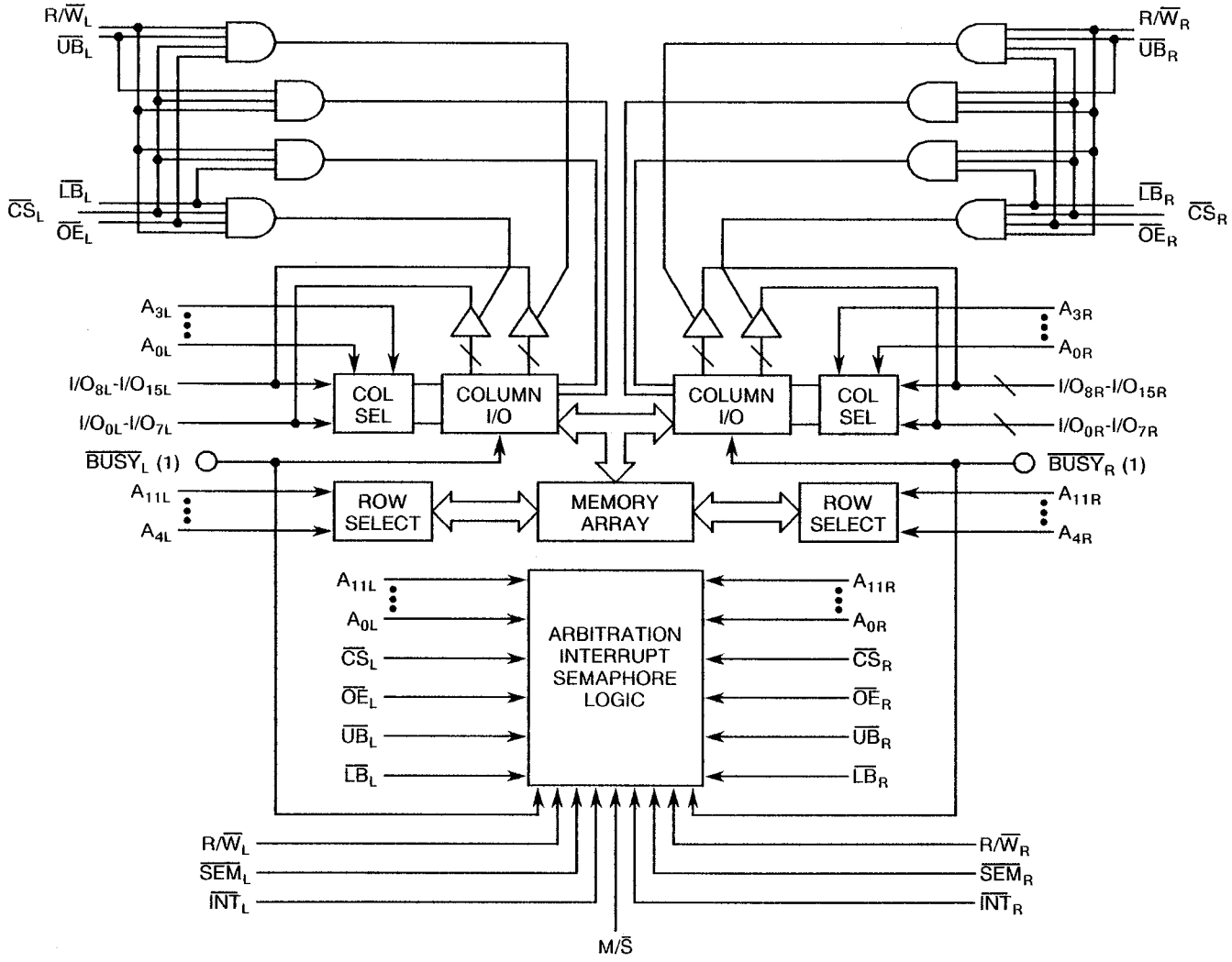
32-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



NOTES

1. No arbitration in M67024 (SLAVE). $\overline{\text{BUSY}}$-IN inhibits write in M67024 SLAVE.

FIGURE 3(d) - FUNCTIONAL DIAGRAM

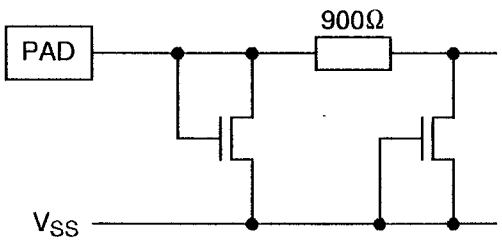


NOTES

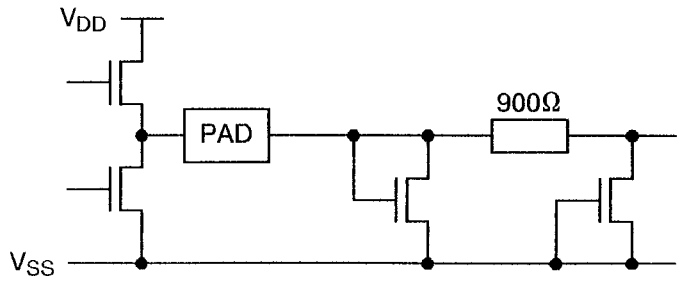
1. (MASTER): $\overline{BUSY}$ is output. (SLAVE): $\overline{BUSY}$ is input.
2. LB = Lower Byte, UB = Upper Byte.

FIGURE 3(e) - INPUT/OUTPUT PROTECTION NETWORKS

EQUIVALENT OF EACH INPUT



EQUIVALENT OF EACH OUTPUT



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:

V_{IC} = Input Clamp Voltage.
I_{DD1} = Average Power Supply Current.
I_{DD2} = Average Standby Current.
I_{DD3} = Power Down Current.
I_{OZH} = Output Leakage Current Third State (High Level Applied).
I_{OZL} = Output Leakage Current Third State (Low Level Applied).
C_{IN} = Input Capacitance.
C_{OUT} = Output Capacitance.
t_{BAA} = $\overline{BUSY}$ Access Time to Address.
t_{BDA} = $\overline{BUSY}$ Disable Time to Address.
t_{BAC} = $\overline{BUSY}$ Access Time to Chip Select.
t_{BDC} = $\overline{BUSY}$ Disable Time to Chip Select.
t_{WDDS} = Write Pulse to Data Delay (SLAVE).
t_{DDDS} = Write Data Valid to Read Data Delay (SLAVE).
t_{APS} = Arbitration Priority Set-up Time.
t_{BDD} = $\overline{BUSY}$ Disable to Valid Data.
t_{WB} = Write to $\overline{BUSY}$ Input.
t_{WH} = Write Hold After $\overline{BUSY}$.
t_{WDDM} = Write Pulse to Data Delay (MASTER).
t_{DDDM} = Write Data Valid to Read Data Delay (MASTER).
t_{AS} = Address Set-up Time.
t_{WR} = Write Recovery Time.
t_{INS} = Interrupt Set Time.
t_{INR} = Interrupt Reset Time.
t_{WC} = Write Cycle Time.
t_{SW} = Chip Select to End of Write.
t_{AW} = Address Valid to End of Write.
t_{AS} = Address Set-Up Time.
t_{WP} = Write Pulse Width.
t_{WR} = Write Recovery Time.
t_{DW} = Data Valid to End of Write.
t_{HZ} = Output High-Z Time.
t_{DH} = Data Hold Time.
t_{WZ} = Write Enable to Output in High-Z.
t_{OW} = Output Active from End of Write.
t_{SWRD} = SEM Flag Write to Read Time.
t_{SPS} = SEM Flag Contention Window.
t_{RC} = Read Cycle Time.
t_{AA} = Address Access Time.
t_{ACS} = Chip Select Access Time.
t_{ABE} = Byte Enable Access Time.
t_{AOE} = Output Enable Access Time.
t_{CH} = Output Hold from Access Change.
t_{LZ} = Output Low-Z Time.
t_{PU} = Chip Select to Power Up Time.
t_{PD} = Chip Disable to Power Down Time.
t_{SOP} = SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$).

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

(a) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during qualification and extension of qualification.

(b) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during procurement on a lot acceptance basis at the total dose irradiation level specified in the Purchase Order.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

(a) Para. 7.1.1(a), "High Temperature Reverse Bias" test and subsequent electrical measurements related to this test shall be omitted.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 10 grammes for the flat package and 8.0 grammes for the chip carrier package.

4.4 MATERIALS AND FINISHES

The materials shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body and the lids shall be welded, brazed, preform-soldered or glass-frit-sealed.

4.4.2 Lead Material and Finish

For flat packages, the material shall be Type 'G' with Type '2' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. For chip carrier packages the finish shall be Type '2' in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

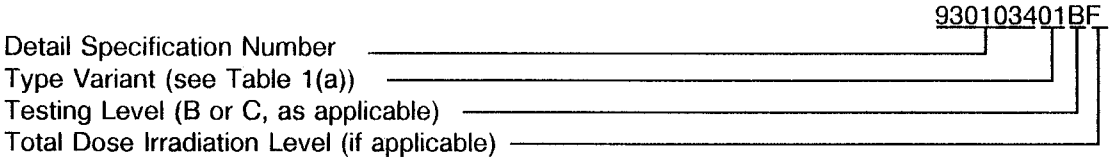
(c) Traceability Information.

4.5.2 Lead Identification

For flat packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side. For chip carrier packages, the index shall be as defined by Figure 2(b).

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



The Total Dose Irradiation Level designation shall be added for those devices for which a sample has been successfully tested to the level in question. For these devices, a code letter shall be added in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ °C and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to Power Burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ), applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-in

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for Power Burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for Power Burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for High Temperature Reverse Bias Burn-in

Not applicable.

4.7.5 Electrical Circuits for Power Burn-in

Circuits for use in performing the Power Burn-in tests are shown in Figure 5(b) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
1 to 27	Functional Test 1 (Nominal Inputs)	-	3014	3(b)	Verify Truth Table. For Input/Output Conditions and Test Patterns, see Note 1	-	-	-
28 to 35	Functional Test 2 (Worst Case Inputs)	-	3014	3(b)	Verify Truth Table. For Input/Output Conditions and Test Patterns, see Note 1	-	-	-
36 to 41	Functional Test 3 (Worst Case Outputs)	-	3014	3(b)	Verify Truth Table. For Input/Output Conditions and Test Patterns, see Note 1	-	-	-
42 to 80	Input Current Low Level	I_{IL}	3009	4(a)	V_{IN} (Under Test) = 0V, $\overline{M/S}$ = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-41-42-44-45-46-47-49-50-51-52-53-54-55-56-57-58-59-60-62-63-65-67-68-69-70-71-72-73-74-75-76-77-78-80-81-82-83-84)	-	− 1.0	µA
81 to 119	Input Current High Level	I_{IH}	3009	4(b)	V_{IN} (Under Test) = 5.5V, $\overline{M/S}$ = 0V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-41-42-44-45-46-47-49-50-51-52-53-54-55-56-57-58-59-60-62-63-65-67-68-69-70-71-72-73-74-75-76-77-78-80-81-82-83-84)	-	1.0	µA
120 to 155	Output Voltage Low Level	V_{OL}	3007	4(c)	V_{IL} = 0.8V, V_{IH} = 2.2V I_{OL} = 4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 2 (Pins 3-4-6-7-8-9-10-11-12-13-14-15-16-17-19-20-23-24-25-27-28-29-30-31-32-33-34-35-36-37-38-40-61-62-65-66)	-	0.4	V
156 to 191	Output Voltage High Level	V_{OH}	3007	4(d)	V_{IL} = 0.8V, V_{IH} = 2.2V I_{OL} = − 4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pins 3-4-6-7-8-9-10-11-12-13-14-15-16-17-19-20-23-24-25-27-28-29-30-31-32-33-34-35-36-37-38-40-61-62-65-66)	2.4	-	V

NOTES: See Page 39.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
192 to 228	Input Clamp Voltage (to V_{SS})	V_{IC}	3008	4(e)	I_{IN} (Under Test) = −200µA V_{IN} (Remaining Inputs) = 0V (Pins 2-41-42-44-45-46-47-49-50-51-52-53-54-55-56-57-58-59-60-63-67-68-69-70-71-72-73-74-75-76-77-78-80-81-82-83-84)	−0.1	−1.9	V
229 to 260	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	3007	4(f)	V_{IN} ($\overline{CS}_{L/R}$, $\overline{SEM}_{L/R}$) = 2.2V V_{OUT} = 0V V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 3-4-6-7-8-9-10-11-12-13-14-15-16-17-19-20-23-24-25-27-28-29-30-31-32-33-34-35-36-37-38-40)	-	−1.0	µA
261 to 292	Output Leakage Current Third State (High Level Applied)	I_{OZH}	3007	4(f)	V_{IN} ($\overline{CS}_{L/R}$, $\overline{SEM}_{L/R}$) = 2.2V V_{OUT} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 3-4-6-7-8-9-10-11-12-13-14-15-16-17-19-20-23-24-25-27-28-29-30-31-32-33-34-35-36-37-38-40)	-	1.0	µA
293	Supply Current (Standby)	I_{DDSB1}	3005	4(g)	V_{IN} ($\overline{CS}_{L/R}$, $\overline{SEM}_{L/R}$) = 2.2V V_{OUT} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 1 + 21 + 26)	-	10	mA
294	Supply Current (Power Down)	I_{DDSB2}	3005	4(g)	V_{IN} ($\overline{CS}_{L/R}$, $\overline{SEM}_{L/R}$) = 5.3V V_{DD} = 5.5V, V_{SS} = 0V (Pins 1 + 21 + 26)	-	400	µA
295	Supply Current (Both Ports Active)	I_{DDOP1}	3005	4(g)	V_{IN} ($\overline{OE}_{L/R}$) = 2.2V V_{IL} = 0V, V_{IH} = 3.0V Outputs Open V_{DD} = 5.5V, V_{SS} = 0V Variants 01, 02 : f = 20MHz Variants 03, 04 : f = 18MHz (Pins 1 + 21 + 26)	 - -	 250 320	mA
296	Supply Current (Left Port Active, Right Port Standby)	I_{DDOP2L}	3005	4(g)	V_{IN} ($\overline{CS}_R$, $\overline{SEM}_R$, $\overline{OE}_{R/L}$) = 3.0V V_{IN} ($\overline{CS}_L$) = 0V Outputs Open V_{DD} = 5.5V, V_{SS} = 0V Variants 01, 02 : f = 20MHz Variants 03, 04 : f = 18MHz (Pins 1 + 21 + 26)	 - -	 160 180	mA

NOTES: See Page 39.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
297	Supply Current (Right Port Active, Left Port Standby)	I_{CCOP2R}	3005	4(g)	V_{IN} ($\overline{CS}_L$, $\overline{SEM}_L$, $\overline{OE}_{R/L}$) = 3.0V V_{IN} ($\overline{CS}_R$) = 0V Outputs Open V_{DD} = 5.5V, V_{SS} = 0V Variants 01, 02 : f = 20MHz Variants 03, 04 : f = 18MHz (Pins 1 + 21 + 26)	 - -	 160 180	mA
298	Data Retention Current	I_{DDDR}	3005	4(g)	V_{IN} ($\overline{CS}_{L/R}$) = V_{DD} V_{IN} (Remaining Inputs = 0V to V_{DD} V_{DD} = 2.0V, V_{SS} = 0V (Pins 1 + 21 + 26)	-	40	µA
299	Data Retention	DR	-	-	V_{IL} = 0V, V_{IH} = 2.0V V_{IN} ($\overline{CS}_L$) = V_{DD} − 0.3V V_{DD} = 2.0V, V_{SS} = 0V Note 5	-	-	-

NOTES: See Page 39.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
300 to 336	Input Capacitance	C_{IN}	3012	4(h)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 6 (Pins 2-41-42-44-45-46-47-49-50-51-52-53-54-55-56-57-58-59-60-63-67-68-69-70-71-72-73-74-75-76-77-78-80-81-82-83-84)	-	5.0	pF
337 to 372	Output Capacitance	C_{OUT}	3012	4(i)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 6 (Pins 3-4-6-7-8-9-10-11-12-13-14-15-16-17-19-20-23-24-25-27-28-29-30-31-32-33-34-35-36-37-38-40-61-62-65-66)	-	7.0	pF
373 to 384	Functional Test 4 (Nominal Inputs)	-	3014	3(b)	Verify Truth Table. For Input and Output Conditions, see Note 7	-	-	-
385 to 386	Output Low-Z Time ($\overline{CS}$ to Output)	t_{LZ}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Note 6	5.0	-	ns
387 to 388	Output High-Z Time ($\overline{CS}$ to Output)	t_{HZ}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Note 6 Variants 01, 02 Variants 03, 04	 - -	 26 20	ns
389 to 390	Chip Select to Power Up Time	t_{PU}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Note 6	0	-	ns
391 to 392	Chip Disable to Power Down Time	t_{PD}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Note 6	-	50	ns
393 to 394	Output High-Z Time ($\overline{OE}$ to Output)	t_{HZ}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Note 6 Variants 01, 02 Variants 03, 04	 - -	 25 20	ns
395 to 396	Write Enable to Output in High-Z	t_{WZ}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Note 6 Variants 01, 02 Variants 03, 04	 - -	 26 20	ns

NOTES: See Page 39.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
397 to 398	Output Active to End of Write	t_{OW}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Note 6	0	-	ns
399 to 400	Address Access Time	t_{AA}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 - -	 55 45	ns
401 to 402	Chip Select Access Time	t_{ACS}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 - -	 55 45	ns
403 to 404	Byte Enable Access Time	t_{ABE}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 - -	 55 45	ns
405 to 406	Output Enable Access Time	t_{AOE}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 - -	 30 25	ns
407 to 408	Address Setup Time	t_{AS}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8	0	-	ns
409 to 410	Data Hold Time	t_{DH}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8	0	-	ns
411 to 412	Write Pulse Width	t_{WP}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 40 35	 - -	ns
413 to 414	$\overline{\text{BUSY}}$ Access Time to Address	t_{BAA}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 40 35	 - -	ns

NOTES: See Page 39.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
415 to 416	$\overline{BUSY}$ Disable Time to Address	t_{BDA}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 40 30	 - -	ns
417 to 418	$\overline{BUSY}$ Access Time to Chip Select	t_{BAC}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 40 30	 - -	ns
419 to 420	$\overline{BUSY}$ Disable Time to Chip Select	t_{BDC}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 35 25	 - -	ns
421 to 422	Write to $\overline{BUSY}$ Input	t_{WB}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8	0	-	ns
423 to 424	Write Hold after $\overline{BUSY}$	t_{WH}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8	30	-	ns
425 to 426	Interrupt Set Time	t_{INS}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 40 35	 - -	ns
427 to 428	Interrupt Reset Time	t_{INR}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 40 35	 - -	ns
429 to 430	Read Cycle Time	t_{RC}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9 Variants 01, 02 Variants 03, 04	 55 45	 - -	ns

NOTES: See Page 39.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
431 to 432	Write Cycle Time	t_{WC}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9 Variants 01, 02 Variants 03, 04	 55 45	 - -	ns
433 to 434	Output Hold from Address Change	t_{OH}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9	3.0	-	ns
435 to 436	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	t_{SOP}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9	15	-	ns
437 to 438	Chip Select to End of Write	t_{SW}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9 Variants 01, 02 Variants 03, 04	 45 40	 - -	ns
439 to 440	Address Valid to End of Write	t_{AW}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9 Variants 01, 02 Variants 03, 04	 45 40	 - -	ns
441 to 442	Write Recovery Time	t_{WR}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9	0	-	ns
443 to 444	Data Valid to End of Write	t_{DW}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9 Variants 01, 02 Variants 03, 04	 30 25	 - -	ns
445 to 446	$\overline{SEM}$ Flag Write to Read Time	t_{SWRD}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9	10	-	ns
447 to 448	$\overline{SEM}$ Flag Contention Window	t_{SPS}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9	10	-	ns
449 to 450	Write Pulse to Data Delay	t_{WDDS}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9 Variants 01, 02 Variants 03, 04	 80 70	 - -	ns

NOTES: See Page 39.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
451 to 452	Write Data Valid to Read Data Delay (Master Only)	t_{DDDM}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9 Variants 01, 02 Variants 03, 04	 65 55	 - -	ns
453 to 454	Arbitration Priority Setup Time	t_{APS}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9	5.0	-	ns
455 to 456	$\overline{\text{BUSY}}$ Disable to Valid Data	t_{BDD}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7, 9 and 10	-		ns
457 to 458	Write Pulse to Data Delay	t_{WDDM}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9 Variants 01, 02 Variants 03, 04	 80 70	 - -	ns
459 to 460	Write Data Valid to Read Data Delay (Slave Only)	t_{DDDS}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9 Variants 01, 02 Variants 03, 04	 65 55	 - -	ns
461 to 462	Address Setup Time (Interrupt)	TAS	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9	0	-	ns
463 to 464	Write Recovery Time (Interrupt)	TWR	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9	0	-	ns

NOTES: See Page 39.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE (CONT'D)

NOTES

1. Functional test go-no-go with the following test sequences:

FUNCTIONAL TEST 1

Pattern	RATE (ns)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	V_{OUT} (V)
CHECKERBOARD	110	4.5 / 5.0 / 5.5	0	0	3.0	4.0	−4.0	1.5
MARCH	110	4.5 / 5.0 / 5.5	0	0	3.0	4.0	−4.0	1.5
CEDES	110	5.0	0	0	3.0	4.0	−4.0	1.5
PATTERN	110	4.5 / 5.0 / 5.5	0	0	3.0	4.0	−4.0	1.5
DUAL-PORT	110	4.5 / 5.0 / 5.5	0	0	3.0	4.0	−4.0	1.5
STRESS	110	4.0 / 6.0	0	−0.5	4.5 / 6.0	4.0	−4.0	1.5
GRAY-CODE	110	4.5 / 5.5	0	0	3.0	4.0	−4.0	1.5
BUSY	110	4.5 / 5.5	0	0	3.0	4.0	−4.0	1.5
ARB-SLAVE	110	4.5 / 5.5	0	0	3.0	4.0	−4.0	1.5
ARB-MASTER	110	4.5 / 5.5	0	0	3.0	4.0	−4.0	1.5
INT	110	4.5 / 5.5	0	0	3.0	4.0	−4.0	1.5
SEM	110	4.5 / 5.5	0	0	3.0	4.0	−4.0	1.5

FUNCTIONAL TEST 2

Pattern	RATE (ns)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	V_{OUT} (V)
V_{IL}-ADD L/R	110	4.5	0	0.8	3.0	4.0	−4.0	1.5
V_{IL}-CLK L/R	110	4.5	0	0.8	3.0	4.0	−4.0	1.5
V_{IL}-DATA L/R	110	4.5	0	0.8	3.0	4.0	−4.0	1.5
V_{IL}-BUSY L/R	110	4.5	0	0.8	3.0	4.0	−4.0	1.5
V_{IH}-ADD L/R	110	5.5	0	0	2.2	4.0	−4.0	1.5
V_{IH}-CLK L/R	110	5.5	0	0	2.2	4.0	−4.0	1.5
V_{IH}-DATA L/R	110	5.5	0	0	2.2	4.0	−4.0	1.5
V_{IH}-BUSY L/R	110	5.5	0	0	2.2	4.0	−4.0	1.5

FUNCTIONAL TEST 3

Pattern	RATE (ns)	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	V_{OUT} (V)
V_{OL}-DATA L/R	110	4.5	0	0	3.0	4.0	−4.0	0.4
V_{OL}-BUSY L/R	110	4.5	0	0	3.0	4.0	−4.0	0.4
V_{OL}-INT L/R	110	4.5	0	0	3.0	4.0	−4.0	0.4
V_{OH}-DATA L/R	110	4.5	0	0	3.0	4.0	−4.0	2.4
V_{OH}-BUSY L/R	110	4.5	0	0	3.0	4.0	−4.0	2.4
V_{OH}-INT L/R	110	4.5	0	0	3.0	4.0	−4.0	2.4

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE (CONT'D)

2. Select Address inputs to produce low level output at the pin under test in accordance with Figure 3(b).
3. Select Address inputs to produce high level output at the pin under test in accordance with Figure 3(b).
4. For I/Os, the measurement includes the Input Currents I_{IL} and I_{IH}.
5. Data Retention Procedure:
   (a) Write Memory (one port) with Checkerboard pattern with timing = 110ns at the conditions given.
   (b) Power Down to V_{DD} = 2.0V for 250ms.
   (c) Restore to original conditions given, read Memory and compare with original pattern.
   (d) Repeat the procedure with $\overline{\text{Checkerboard}}$ pattern with timing = 110ns at the conditions given.
   (e) For Variants 01 and 02, t_r = 45ns.
   For Variants 03 and 04, t_r = 55ns.
6. Guaranteed but not tested. Characterised at initial design and after major process change.
7. **FUNCTIONAL TEST 4**

Pattern	RATE (ns) Variants 01, 02	RATE (ns) Variants 03, 04	V_{DD} (V)	V_{SS} (V)	V_{IL} (V)	V_{IH} (V)	I_{OL} (mA)	I_{OH} (mA)	V_{OUT} (V)
TDYN1	55	45	4.5 / 5.5	0	0	3.0	4.0	−4.0	1.5
TDYN2	55	45	4.5 / 5.5	0	0	3.0	4.0	−4.0	1.5
DUAL-PORT-TEST	55	45	4.5 / 5.5	0	0	3.0	4.0	−4.0	1.5
BUSY-R-L	55	45	4.5 / 5.5	0	0	3.0	4.0	−4.0	1.5
ARB-MASTER	55	45	4.5 / 5.5	0	0	3.0	4.0	−4.0	1.5
ARB-SLAVE	55	45	4.5 / 5.5	0	0	3.0	4.0	−4.0	1.5
INT-DYN	45	45	4.5 / 5.5	0	0	3.0	4.0	−4.0	1.5

Output load = 1 TTL gate equivalent + $C_L \leq 100$pF.
$t_r = t_f = 5.0$ns maximum.

8. Parameters measured during Functional Test 4.
9. Parameters tested go-no-go during Functional Test 4.
10 t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual) or $t_{DD} - t_{DW}$ (actual).

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
1 to 27	Functional Test 1 (Nominal Inputs)	-	3014	3(b)	Verify Truth Table. For Input/Output Conditions and Test Patterns, see Note 1	-	-	-
28 to 35	Functional Test 2 (Worst Case Inputs)	-	3014	3(b)	Verify Truth Table. For Input/Output Conditions and Test Patterns, see Note 1	-	-	-
36 to 41	Functional Test 3 (Worst Case Outputs)	-	3014	3(b)	Verify Truth Table. For Input/Output Conditions and Test Patterns, see Note 1	-	-	-
42 to 80	Input Current Low Level	I_{IL}	3009	4(a)	V_{IN} (Under Test) = 0V, $\overline{M/S}$ = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-41-42-44-45-46-47-49-50-51-52-53-54-55-56-57-58-59-60-62-63-65-67-68-69-70-71-72-73-74-75-76-77-78-80-81-82-83-84)	-	− 1.0	µA
81 to 119	Input Current High Level	I_{IH}	3009	4(b)	V_{IN} (Under Test) = 5.5V, $\overline{M/S}$ = 0V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-41-42-44-45-46-47-49-50-51-52-53-54-55-56-57-58-59-60-62-63-65-67-68-69-70-71-72-73-74-75-76-77-78-80-81-82-83-84)	-	1.0	µA
120 to 155	Output Voltage Low Level	V_{OL}	3007	4(c)	V_{IL} = 0.8V, V_{IH} = 2.2V I_{OL} = 4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 2 (Pins 3-4-6-7-8-9-10-11-12-13-14-15-16-17-19-20-23-24-25-27-28-29-30-31-32-33-34-35-36-37-38-40-61-62-65-66)	-	0.4	V
156 to 191	Output Voltage High Level	V_{OH}	3007	4(d)	V_{IL} = 0.8V, V_{IH} = 2.2V I_{OL} = − 4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pins 3-4-6-7-8-9-10-11-12-13-14-15-16-17-19-20-23-24-25-27-28-29-30-31-32-33-34-35-36-37-38-40-61-62-65-66)	2.4	-	V

NOTES: See Page 39.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
192 to 228	Input Clamp Voltage (to V_{SS})	V_{IC}	3008	4(e)	I_{IN} (Under Test) = −200µA V_{IN} (Remaining Inputs) = 0V (Pins 2-41-42-44-45-46-47-49-50-51-52-53-54-55-56-57-58-59-60-63-67-68-69-70-71-72-73-74-75-76-77-78-80-81-82-83-84)	−0.1	−1.9	V
229 to 260	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	3007	4(f)	V_{IN} ($\overline{CS}_{L/R}$, $\overline{SEM}_{L/R}$) = 2.2V V_{OUT} = 0V V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 3-4-6-7-8-9-10-11-12-13-14-15-16-17-19-20-23-24-25-27-28-29-30-31-32-33-34-35-36-37-38-40)	-	−1.0	µA
261 to 292	Output Leakage Current Third State (High Level Applied)	I_{OZH}	3007	4(f)	V_{IN} ($\overline{CS}_{L/R}$, $\overline{SEM}_{L/R}$) = 2.2V V_{OUT} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pins 3-4-6-7-8-9-10-11-12-13-14-15-16-17-19-20-23-24-25-27-28-29-30-31-32-33-34-35-36-37-38-40)	-	1.0	µA
293	Supply Current (Standby)	I_{DDSB1}	3005	4(g)	V_{IN} ($\overline{CS}_{L/R}$, $\overline{SEM}_{L/R}$) = 2.2V V_{OUT} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 1 + 21 + 26)	-	10	mA
294	Supply Current (Power Down)	I_{DDSB2}	3005	4(g)	V_{IN} ($\overline{CS}_{L/R}$, $\overline{SEM}_{L/R}$) = 5.3V V_{DD} = 5.5V, V_{SS} = 0V (Pins 1 + 21 + 26)	-	400	µA
295	Supply Current (Both Ports Active)	I_{DDOP1}	3005	4(g)	V_{IN} ($\overline{OE}_{L/R}$) = 2.2V V_{IL} = 0V, V_{IH} = 3.0V Outputs Open V_{DD} = 5.5V, V_{SS} = 0V Variants 01, 02 : f = 20MHz Variants 03, 04 : f = 18MHz (Pins 1 + 21 + 26)	 - -	 250 320	mA
296	Supply Current (Left Port Active, Right Port Standby)	I_{DDOP2L}	3005	4(g)	V_{IN} ($\overline{CS}_R$, $\overline{SEM}_R$, $\overline{OE}_{R/L}$) = 3.0V V_{IN} ($\overline{CS}_L$) = 0V Outputs Open V_{DD} = 5.5V, V_{SS} = 0V Variants 01, 02 : f = 20MHz Variants 03, 04 : f = 18MHz (Pins 1 + 21 + 26)	 - -	 160 180	mA

NOTES: See Page 39.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES
- d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
297	Supply Current (Right Port Active, Left Port Standby)	I_{CCOP2R}	3005	4(g)	V_{IN} ($\overline{CS}_L$, $\overline{SEM}_L$, $\overline{OE}_{R/L}$) = 3.0V V_{IN} ($\overline{CS}_R$) = 0V Outputs Open V_{DD} = 5.5V, V_{SS} = 0V Variants 01, 02 : f = 20MHz Variants 03, 04 : f = 18MHz (Pins 1 + 21 + 26)	 - -	 160 180	mA
298	Data Retention Current	I_{DDDR}	3005	4(g)	V_{IN} ($\overline{CS}_{L/R}$) = V_{DD} V_{IN} (Remaining Inputs = 0V to V_{DD} V_{DD} = 2.0V, V_{SS} = 0V (Pins 1 + 21 + 26)	-	40	µA
299	Data Retention	DR	-	-	V_{IL} = 0V, V_{IH} = 2.0V V_{IN} ($\overline{CS}_L$) = V_{DD} − 0.3V V_{DD} = 2.0V, V_{SS} = 0V Note 5	-	-	-

NOTES: See Page 39.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
300 to 336	Input Capacitance	C_{IN}	3012	4(h)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 6 (Pins 2-41-42-44-45-46-47-49-50-51-52-53-54-55-56-57-58-59-60-63-67-68-69-70-71-72-73-74-75-76-77-78-80-81-82-83-84)	-	5.0	pF
337 to 372	Output Capacitance	C_{OUT}	3012	4(i)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 6 (Pins 3-4-6-7-8-9-10-11-12-13-14-15-16-17-19-20-23-24-25-27-28-29-30-31-32-33-34-35-36-37-38-40-61-62-65-66)	-	7.0	pF
373 to 384	Functional Test 4 (Nominal Inputs)	-	3014	3(b)	Verify Truth Table. For Input and Output Conditions, see Note 7	-	-	-
385 to 386	Output Low-Z Time ($\overline{CS}$ to Output)	t_{LZ}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Note 6	5.0	-	ns
387 to 388	Output High-Z Time ($\overline{CS}$ to Output)	t_{HZ}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Note 6 Variants 01, 02 Variants 03, 04	 - -	 26 20	ns
389 to 390	Chip Select to Power Up Time	t_{PU}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Note 6	0	-	ns
391 to 392	Chip Disable to Power Down Time	t_{PD}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Note 6	-	50	ns
393 to 394	Output High-Z Time ($\overline{OE}$ to Output)	t_{HZ}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Note 6 Variants 01, 02 Variants 03, 04	 - -	 25 20	ns
395 to 396	Write Enable to Output in High-Z	t_{WZ}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Note 6 Variants 01, 02 Variants 03, 04	 - -	 26 20	ns

NOTES: See Page 39.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES
- a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
397 to 398	Output Active to End of Write	t_{OW}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Note 6	0	-	ns
399 to 400	Address Access Time	t_{AA}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 -	 55	ns
						-	45	
401 to 402	Chip Select Access Time	t_{ACS}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 -	 55	ns
						-	45	
403 to 404	Byte Enable Access Time	t_{ABE}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 -	 55	ns
						-	45	
405 to 406	Output Enable Access Time	t_{AOE}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 -	 30	ns
						-	25	
407 to 408	Address Setup Time	t_{AS}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8	0	-	ns
409 to 410	Data Hold Time	t_{DH}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8	0	-	ns
411 to 412	Write Pulse Width	t_{WP}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 40	 -	ns
						35	-	
413 to 414	$\overline{\text{BUSY}}$ Access Time to Address	t_{BAA}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 40	 -	ns
						35	-	

NOTES: See Page 39.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
415 to 416	$\overline{BUSY}$ Disable Time to Address	t_{BDA}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 40 30	 - -	ns
417 to 418	$\overline{BUSY}$ Access Time to Chip Select	t_{BAC}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 40 30	 - -	ns
419 to 420	$\overline{BUSY}$ Disable Time to Chip Select	t_{BDC}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 35 25	 - -	ns
421 to 422	Write to $\overline{BUSY}$ Input	t_{WB}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8	0	-	ns
423 to 424	Write Hold after $\overline{BUSY}$	t_{WH}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8	30	-	ns
425 to 426	Interrupt Set Time	t_{INS}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 40 35	 - -	ns
427 to 428	Interrupt Reset Time	t_{INR}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 8 Variants 01, 02 Variants 03, 04	 40 35	 - -	ns
429 to 430	Read Cycle Time	t_{RC}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9 Variants 01, 02 Variants 03, 04	 55 45	 - -	ns

NOTES: See Page 39.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
431 to 432	Write Cycle Time	t_{WC}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9 Variants 01, 02 Variants 03, 04	 55 45	 - -	ns
433 to 434	Output Hold from Address Change	t_{OH}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9	3.0	-	ns
435 to 436	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	t_{SOP}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9	15	-	ns
437 to 438	Chip Select to End of Write	t_{SW}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9 Variants 01, 02 Variants 03, 04	 45 40	 - -	ns
439 to 440	Address Valid to End of Write	t_{AW}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9 Variants 01, 02 Variants 03, 04	 45 40	 - -	ns
441 to 442	Write Recovery Time	t_{WR}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9	0	-	ns
443 to 444	Data Valid to End of Write	t_{DW}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9 Variants 01, 02 Variants 03, 04	 30 25	 - -	ns
445 to 446	$\overline{SEM}$ Flag Write to Read Time	t_{SWRD}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9	10	-	ns
447 to 448	$\overline{SEM}$ Flag Contention Window	t_{SPS}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9	10	-	ns
449 to 450	Write Pulse to Data Delay	t_{WDDS}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9 Variants 01, 02 Variants 03, 04	 80 70	 - -	ns

NOTES: See Page 39.

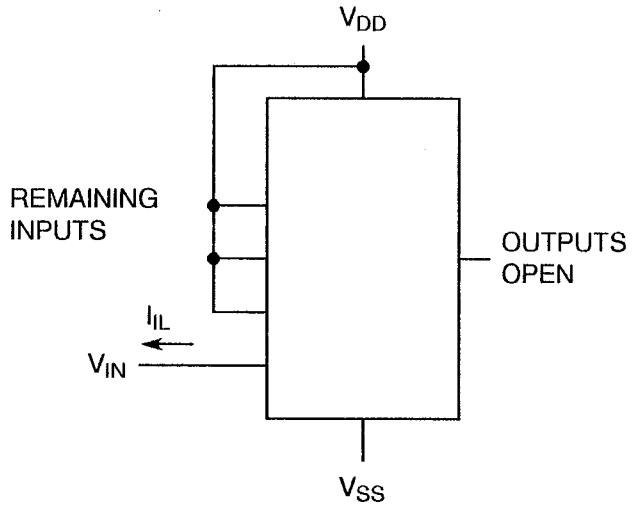
TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
						MIN	MAX	
451 to 452	Write Data Valid to Read Data Delay (Master Only)	t_{DDDM}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9 Variants 01, 02 Variants 03, 04	 65 55	 - -	ns
453 to 454	Arbitration Priority Setup Time	t_{APS}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9	5.0	-	ns
455 to 456	$\overline{\text{BUSY}}$ Disable to Valid Data	t_{BDD}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7, 9 and 10	-		ns
457 to 458	Write Pulse to Data Delay	t_{WDDM}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9 Variants 01, 02 Variants 03, 04	 80 70	 - -	ns
459 to 460	Write Data Valid to Read Data Delay (Slave Only)	t_{DDDS}	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9 Variants 01, 02 Variants 03, 04	 65 55	 - -	ns
461 to 462	Address Setup Time (Interrupt)	TAS	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9	0	-	ns
463 to 464	Write Recovery Time (Interrupt)	TWR	3004	4(j)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9	0	-	ns

NOTES: See Page 39.

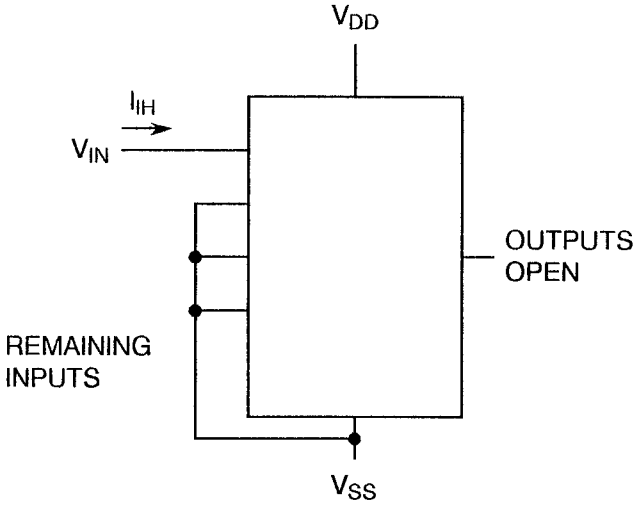
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - INPUT CURRENT LOW LEVEL



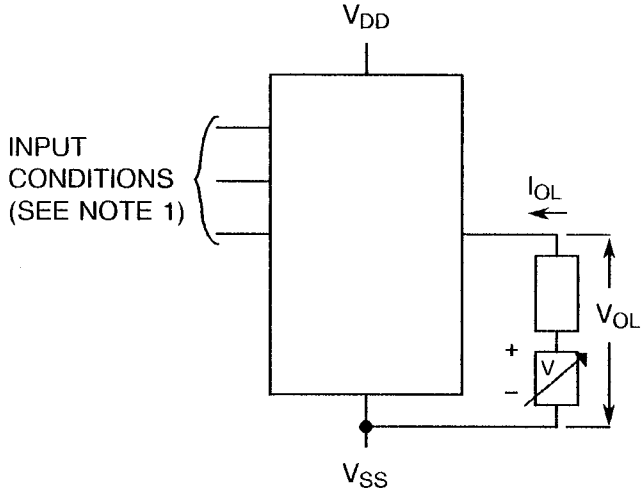
NOTES
1. Each input to be tested separately.

FIGURE 4(b) - INPUT CURRENT HIGH LEVEL



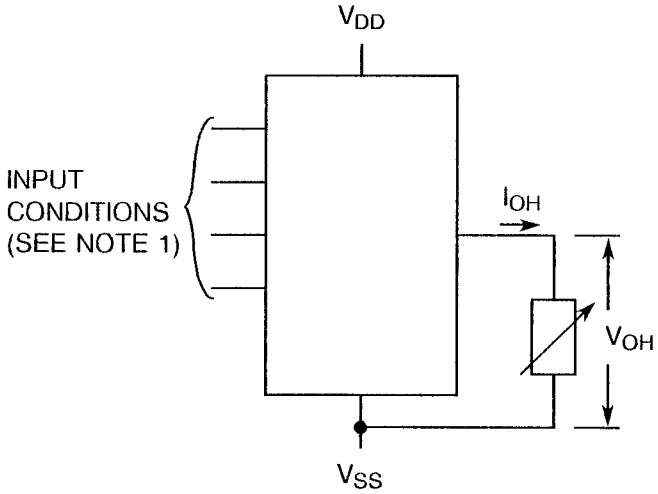
NOTES
1. Each input to be tested separately.

FIGURE 4(c) - OUTPUT VOLTAGE LOW LEVEL



NOTES
1. See Note 2 to Table 2.
2. Each output to be tested separately.

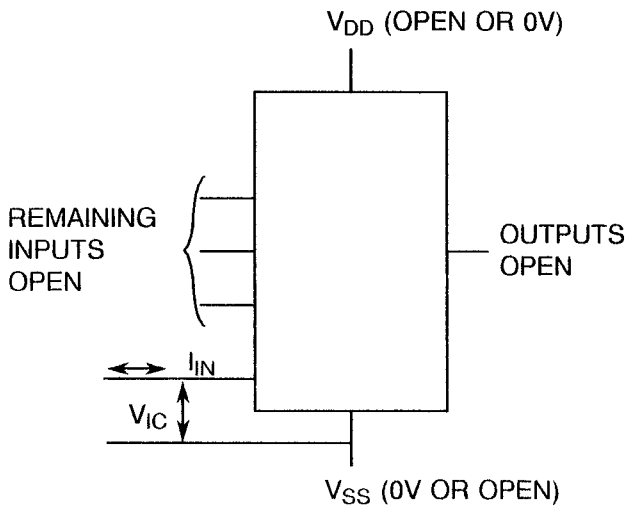
FIGURE 4(d) - OUTPUT VOLTAGE HIGH LEVEL



NOTES
1. See Note 3 to Table 2.
2. Each output to be tested separately.

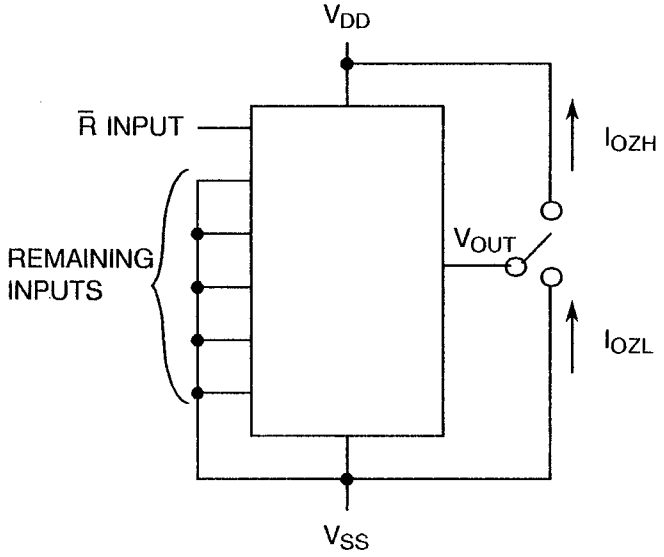
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(e) - INPUT CLAMP VOLTAGE



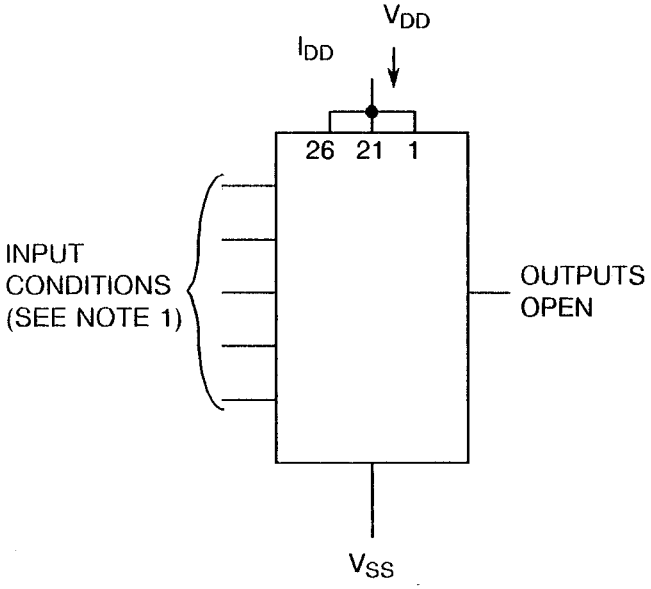
NOTES
1. Each input to be tested separately.

FIGURE 4(f) - OUTPUT LEAKAGE CURRENT THIRD STATE



NOTES
1. Each output to be tested separately.

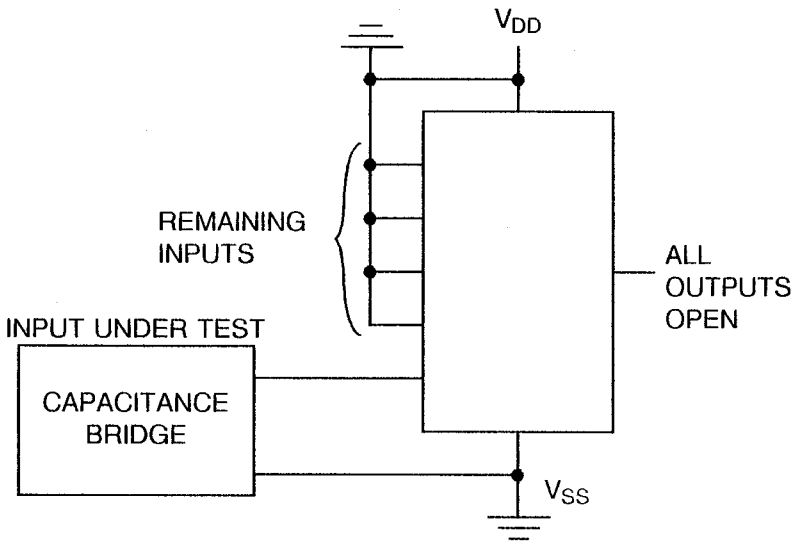
FIGURE 4(g) - SUPPLY CURRENT



NOTES
1. As per Table 2 or 3.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

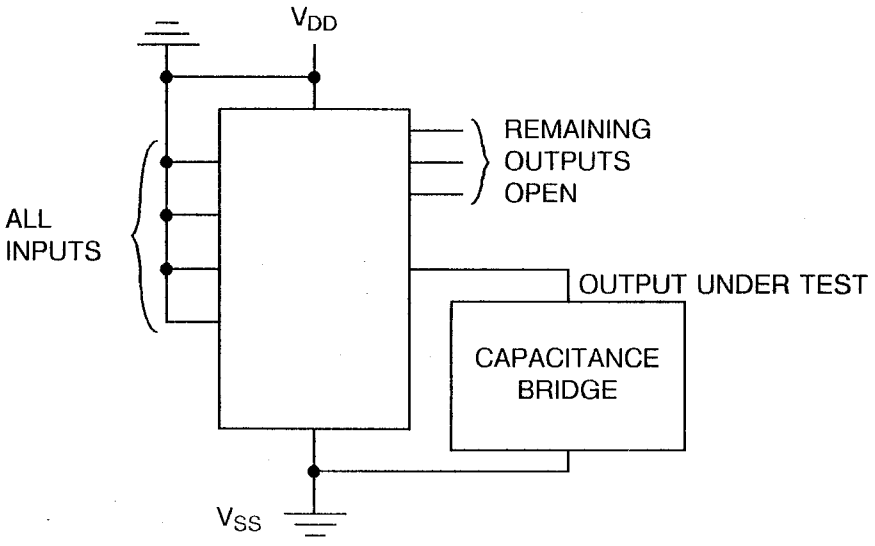
FIGURE 4(h) - INPUT CAPACITANCE



NOTES

1. Each input to be tested separately.
2. f = 100kHz to 1MHz.

FIGURE 4(i) - OUTPUT CAPACITANCE

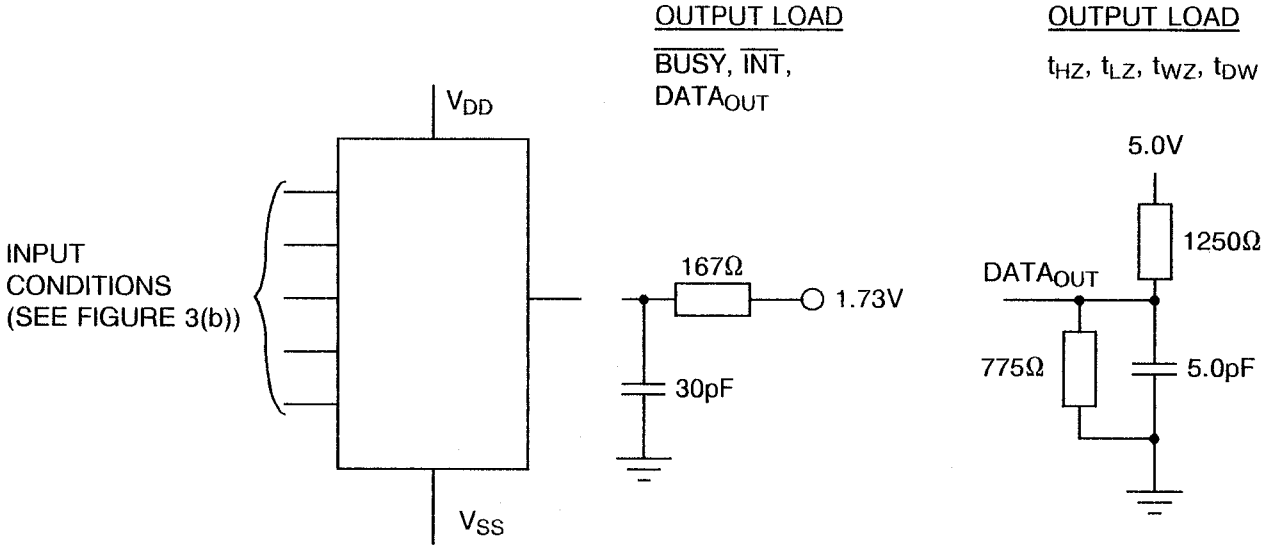


NOTES

1. Each output to be tested separately.
2. f = 100kHz to 1MHz.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - PROPAGATION DELAY



NOTES

1. Voltage Waveforms as per Figure 3(b).

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
42 to 80	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	± 0.1	µA
81 to 119	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	± 0.1	µA
120 to 155	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	± 0.1	V
156 to 191	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	± 0.1	V
229 to 260	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	± 0.1	µA
261 to 292	Output Leakage Current Third State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	± 0.1	µA
293	Supply Current (Standby)	I_{DDSB1}	As per Table 2	As per Table 2	± 1.0	mA
294	Supply Current (Power Down)	I_{DDSB2}	As per Table 2	As per Table 2	± 40	µA
298	Data Retention Current	I_{DDDR}	As per Table 2	As per Table 2	± 5.0	µA

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0−5)	°C
2	Outputs - (Pins 61-62-65-66)	V_{OUT}	$V_{DD}/2$	V
3	Inputs - (Pins 44-63-83)	V_{IN}	V_{DD}	V
4	Inputs - (Pins 3-6-8-10-12-14-16-19-23-25-28-30-32-34-36-38)	V_{IN}	S19 (Note 1)	Vac
5	Inputs - (Pins 4-7-9-11-13-15-17-20-24-27-29-31-33-35-37-40)	V_{IN}	S20 (Note 1)	Vac
6	Inputs - (Pins 48-49-50-51-52-53-54-55-56-57-58-59-60-67-68-69-70-71-72-73-74-75-76-77-78-79)	V_{IN}	S6 to S18 as per Figure 5(b) (Note 1)	Vac
7	Input - (Pin 84)	V_{IN}	S1 (Note 2)	Vac
8	Input - (Pin 42)	V_{IN}	S2 (Note 2)	Vac
9	Inputs - (Pins 2-41)	V_{IN}	S3 (Note 2)	Vac
10	Inputs - (Pins 45-46-47)	V_{IN}	S4 (Note 2)	Vac
11	Inputs - (Pins 80-81-82)	V_{IN}	S5 (Note 2)	Vac
12	Pulse Voltage	V_{GEN}	0V to V_{DD}	Vac
13	Pulse Frequency Square Wave	f0	360	kHz
14	Positive Supply Voltage (Pins 1-21-26)	V_{DD}	5.0(+0.5−0)	V
15	Negative Supply Voltage (Pins 5-18-22-39-43-64)	V_{SS}	0	V

NOTES

1. Input Protection Resistor = Output Load Resistor = 1.0kΩ.
2. Input Timings:

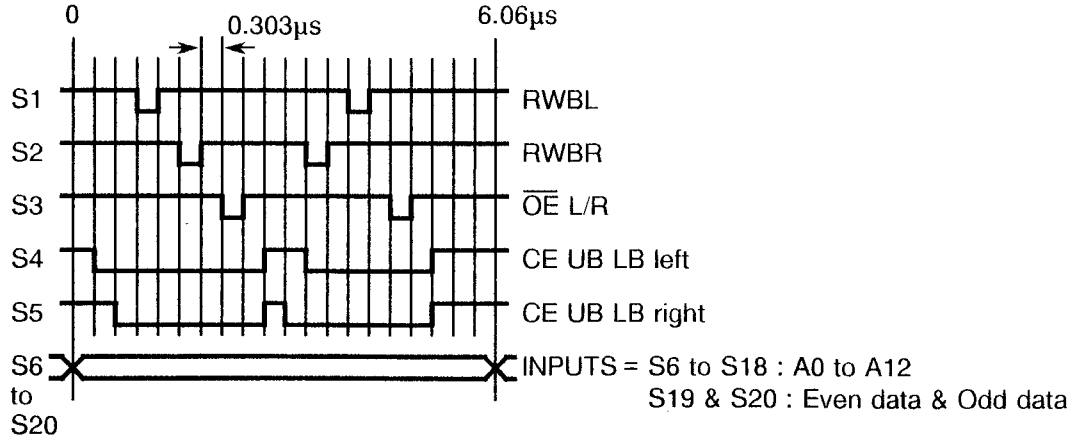
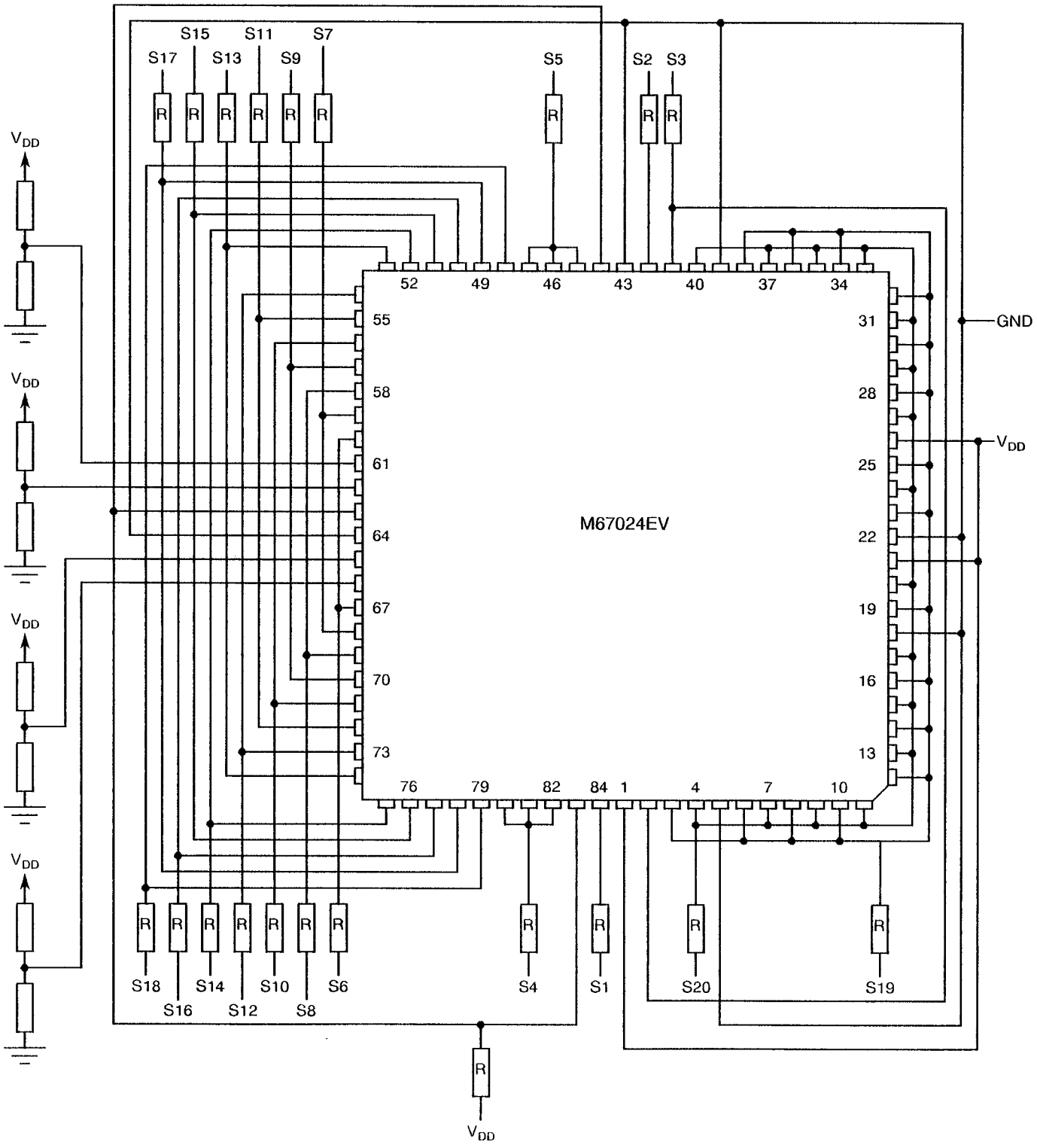


FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



NOTES

1. R = 1.0kΩ.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION No. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(b) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

4.9 TOTAL DOSE IRRADIATION TESTING

4.9.1 Application

If specified in Para. 4.2.1 of this specification, total dose irradiation testing shall be performed in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.9.2 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6 of this specification.

4.9.3 Electrical Measurements

The parameters to be measured prior to irradiation exposure are scheduled in Table 2 of this specification. Only devices which meet the requirements of Table 2 shall be included in the test sample.

The parameters to be measured during and on completion of irradiation testing are scheduled in Table 7 of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	ABSOLUTE LIMITS		UNIT
						MIN	MAX	
1 to 27	Functional Test 1 (Nominal Inputs)	-	As per Table 2	As per Table 2	-	-	-	-
28 to 35	Functional Test 2 (Worst Case Inputs)	-	As per Table 2	As per Table 2	-	-	-	-
36 to 41	Functional Test 3 (Worst Case Outputs)	-	As per Table 2	As per Table 2	-	-	-	-
42 to 80	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	±0.1	-	−1.0	µA
81 to 119	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	±0.1	-	1.0	µA
120 to 155	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	±0.1	-	0.4	V
156 to 191	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	±0.1	2.4	-	V
229 to 260	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	±0.1	-	−1.0	µA
261 to 292	Output Leakage Current Third State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	±0.1	-	1.0	µA
293	Supply Current (Standby)	I_{DDSB1}	As per Table 2	As per Table 2	±1.0	-	10	mA
294	Supply Current (Power Down)	I_{DDSB2}	As per Table 2	As per Table 2	±40	-	400	µA
295	Supply Current (Both Ports Active)	I_{DDOP1}	As per Table 2	As per Table 2 Variants 01, 02 Variants 03, 04	 - -	 - -	 250 320	mA
296	Supply Current (Left Port Active, Right Port Standby)	I_{DDOP2L}	As per Table 2	As per Table 2 Variants 01, 02 Variants 03, 04	 - -	 - -	 160 180	mA
297	Supply Current (Right Port Active, Left Port Standby)	I_{DDOP2R}	As per Table 2	As per Table 2 Variants 01, 02 Variants 03, 04	 - -	 - -	 160 180	mA

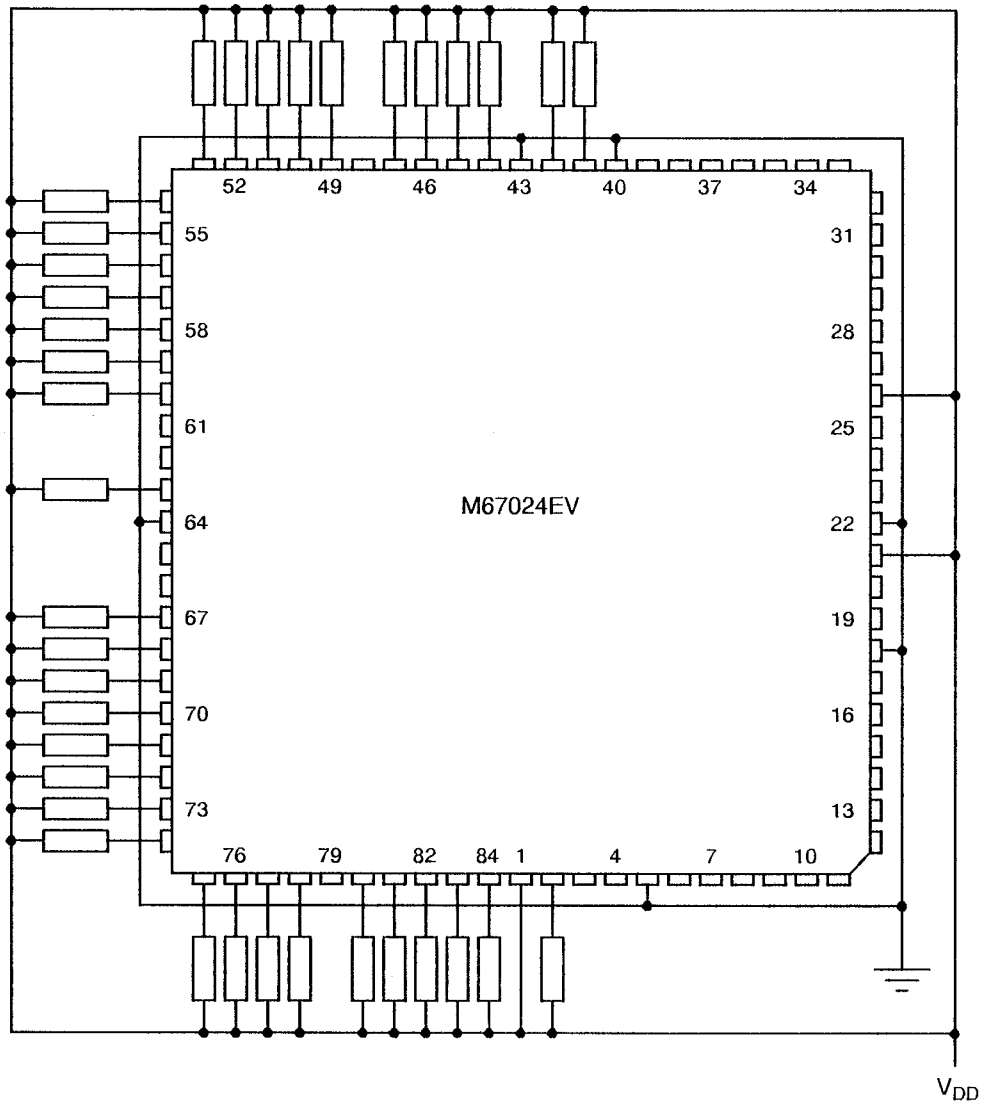
TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	ABSOLUTE LIMITS		UNIT
						MIN	MAX	
298	Data Retention Current	I_{DDDR}	As per Table 2	As per Table 2	±5.0	-	40	µA
299	Data Retention	DR	As per Table 2	As per Table 2	-	-	-	-
373 to 384	Functional Test 4 (Nominal Inputs)	-	As per Table 2	As per Table 2	-	-	-	-
399 to 400	Address Access Time	t_{AA}	As per Table 2	As per Table 2 Variants 01, 02 Variants 03, 04	 - -	 - -	 55 45	ns
401 to 402	Chip Select Access Time	t_{ACS}	As per Table 2	As per Table 2 Variants 01, 02 Variants 03, 04	 - -	 - -	 55 45	ns
403 to 404	Byte Enable Access Time	t_{ABE}	As per Table 2	As per Table 2 Variants 01, 02 Variants 03, 04	 - -	 - -	 55 45	ns
405 to 406	Output Enable Access Time	t_{AOE}	As per Table 2	As per Table 2 Variants 01, 02 Variants 03, 04	 - -	 - -	 30 25	ns
407 to 408	Address Setup Time	t_{AS}	As per Table 2	As per Table 2	-	0	-	ns
409 to 410	Data Hold Time	t_{DH}	As per Table 2	As per Table 2	-	0	-	ns
411 to 412	Write Pulse Width	t_{WP}	As per Table 2	As per Table 2 Variants 01, 02 Variants 03, 04	 - -	 - -	 45 35	ns
413 to 414	$\overline{\text{BUSY}}$ Access Time to Address	t_{BAA}	As per Table 2	As per Table 2 Variants 01, 02 Variants 03, 04	 - -	 - -	 45 35	ns
415 to 416	$\overline{\text{BUSY}}$ Disable Time to Address	t_{BDA}	As per Table 2	As per Table 2 Variants 01, 02 Variants 03, 04	 - -	 - -	 40 30	ns
417 to 418	$\overline{\text{BUSY}}$ Access Time to Chip Select	t_{BAC}	As per Table 2	As per Table 2 Variants 01, 02 Variants 03, 04	 - -	 - -	 40 30	ns
419 to 420	$\overline{\text{BUSY}}$ Disable Time to Chip Select	t_{BDC}	As per Table 2	As per Table 2 Variants 01, 02 Variants 03, 04	 - -	 - -	 35 25	ns

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	ABSOLUTE LIMITS		UNIT
						MIN	MAX	
421 to 422	Write to $\overline{\text{BUSY}}$ Input	t_{WB}	As per Table 2	As per Table 2	-	0	-	ns
423 to 424	Write Hold after $\overline{\text{BUSY}}$	t_{WH}	As per Table 2	As per Table 2	-	-	30	ns
425 to 426	Interrupt Set Time	t_{INS}	As per Table 2	As per Table 2 Variants 01, 02 Variants 03, 04	 - -	 - -	 40 35	ns
427 to 428	Interrupt Reset Time	t_{INR}	As per Table 2	As per Table 2 Variants 01, 02 Variants 03, 04	 - -	 - -	 40 35	ns

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING



NOTES

1. Input Protection Resistor = 1.0kΩ.

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	ABSOLUTE LIMITS		UNIT
					MIN	MAX	
1 to 27	Functional Test 1 (Nominal Inputs)	-	As per Table 2	As per Table 2	-	-	-
28 to 35	Functional Test 2 (Worst Case Inputs)	-	As per Table 2	As per Table 2	-	-	-
36 to 41	Functional Test 3 (Worst Case Outputs)	-	As per Table 2	As per Table 2	-	-	-
42 to 80	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	-	−5.0	µA
81 to 119	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	-	5.0	µA
120 to 155	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	-	0.4	V
156 to 191	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	2.4	-	V
229 to 260	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	-	−5.0	µA
261 to 292	Output Leakage Current Third State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	-	−5.0	µA
293	Supply Current (Standby)	I_{DDSB1}	As per Table 2	As per Table 2	-	20	mA
294	Supply Current (Power Down)	I_{DDSB2}	As per Table 2	As per Table 2	-	5.0	mA
295	Supply Current (Both Ports Active)	I_{DDOP1}	As per Table 2	As per Table 2 Variants 01, 02 Variants 03, 04	 - -	 300 350	mA

APPENDIX 'A'

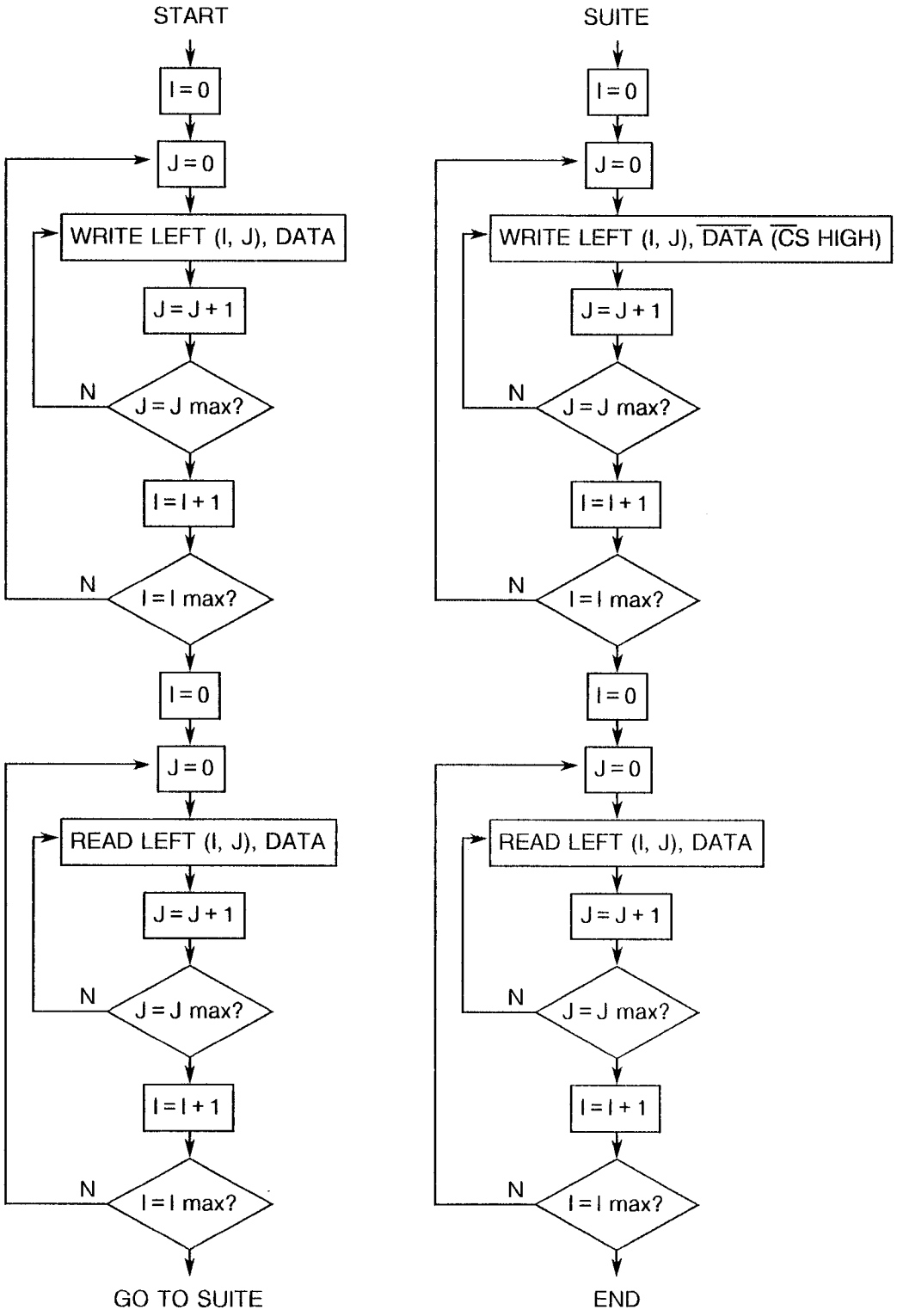
AGREED DEVIATIONS FOR MATRA-MHS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.2	Para. 9.9.3, "Electrical Measurements at Room Temperature". May be performed at High Temperature.
Para. 4.2.4 and 4.2.5	Para. 9.9.4, "Electrical Measurements at Room Temperature". May be performed in accordance with Table 2, but Parameter Drift Values must be calculated in accordance with Table 6 of this specification

APPENDIX 'A'

The following test patterns may be used:-

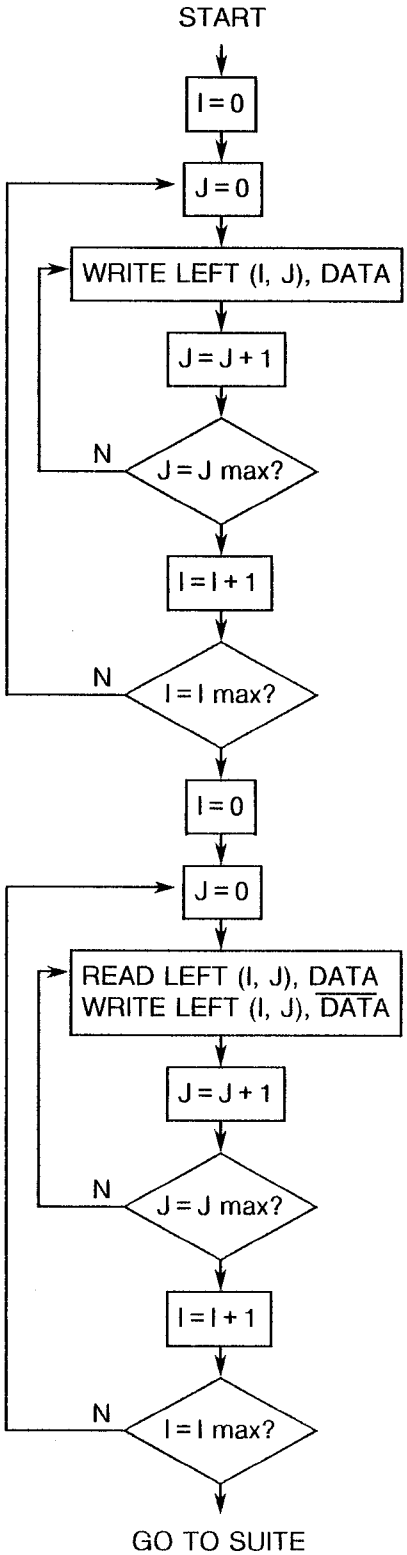
1. CEDES Pattern

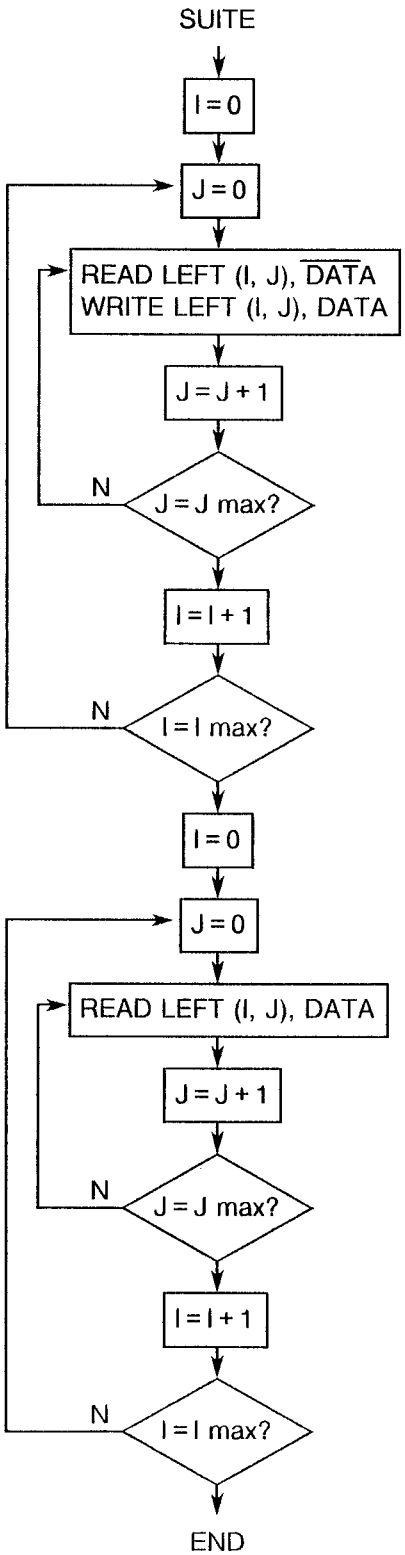


DATA FFH
I max = 256
J max = 16

APPENDIX 'A'

2. MARCH Pattern

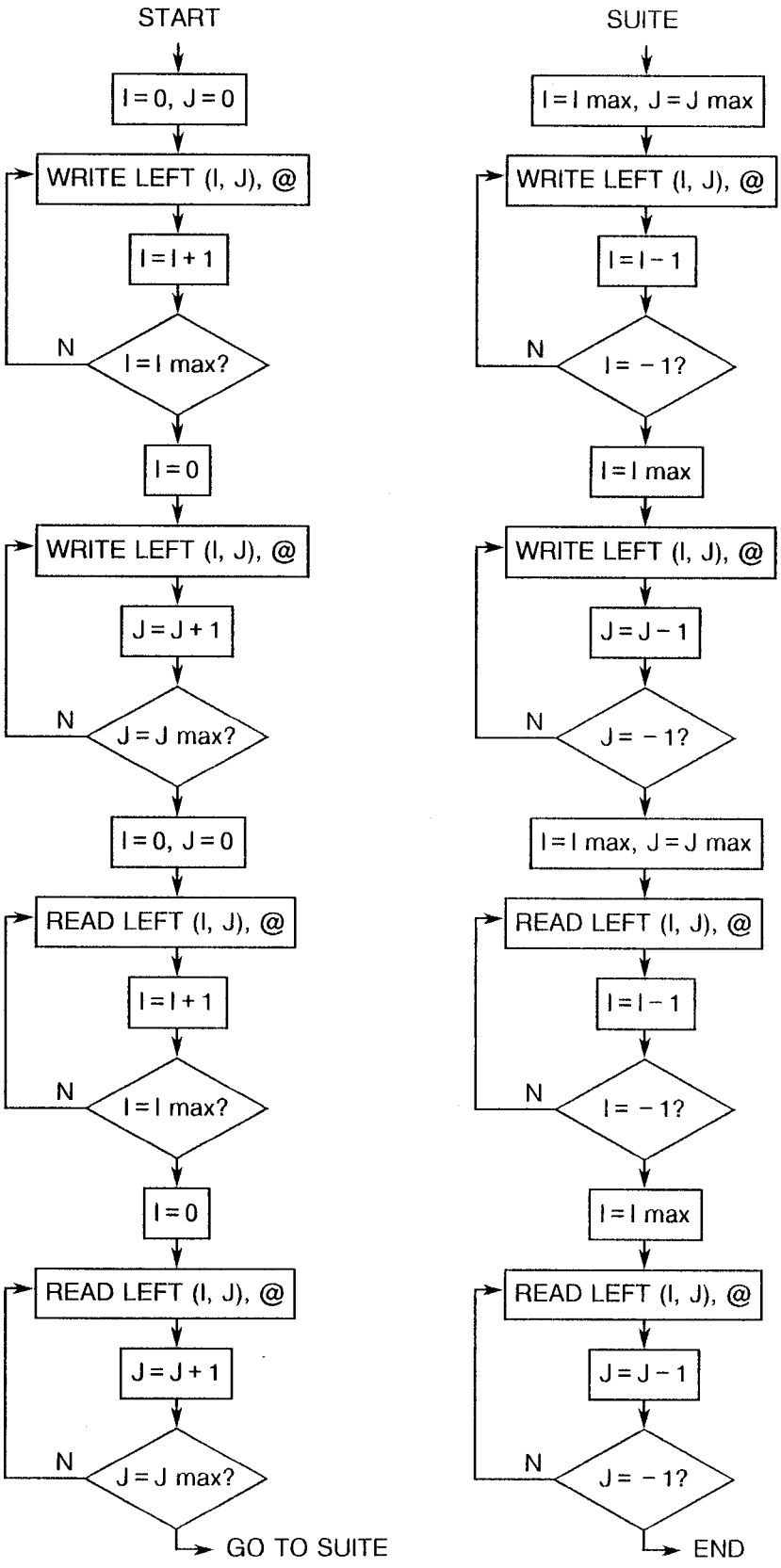




DATA OOH
I max = 256
J max = 16

APPENDIX 'A'

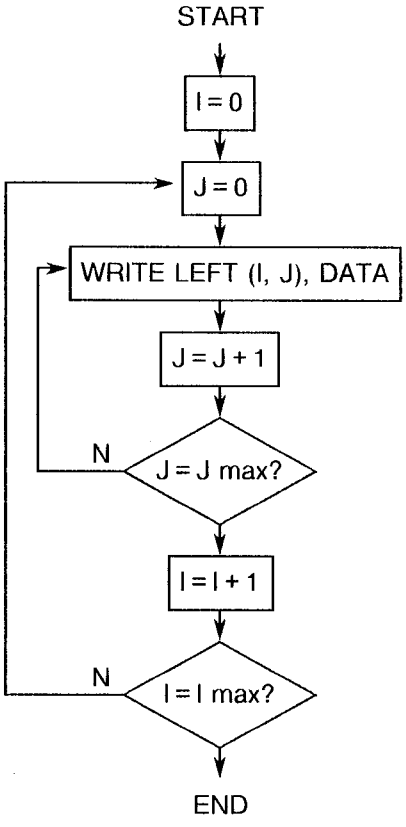
3. GRAY CODE Pattern



I max	=	255
J max	=	15

4. BUSY Pattern

TEST is good if BUSY Right is Low and BUSY Left is High.



I max	=	256
J max	=	16

5. INT Pattern

Write FF port Right at @ 3FEH ⇒ Check INTERRUPT Left port is set (INT = 0).
Read XX port Left at @ 3FEH ⇒ Check INTERRUPT Right port is reset (INT = 1).

Write FF port Left at @ 3FFH ⇒ Check INTERRUPT Right port is set (INT = 0).
Read XX port Right at @ 3FFH ⇒ Check INTERRUPT Left port is reset (INT = 1).

Write FF port Right at @ $\overline{3FEH}$ ⇒ Check INTERRUPT Left port not interpose (INT = 1).
Write FF port Left at @ $\overline{3FEH}$ ⇒ Check INTERRUPT Right port not interpose (INT = 1).

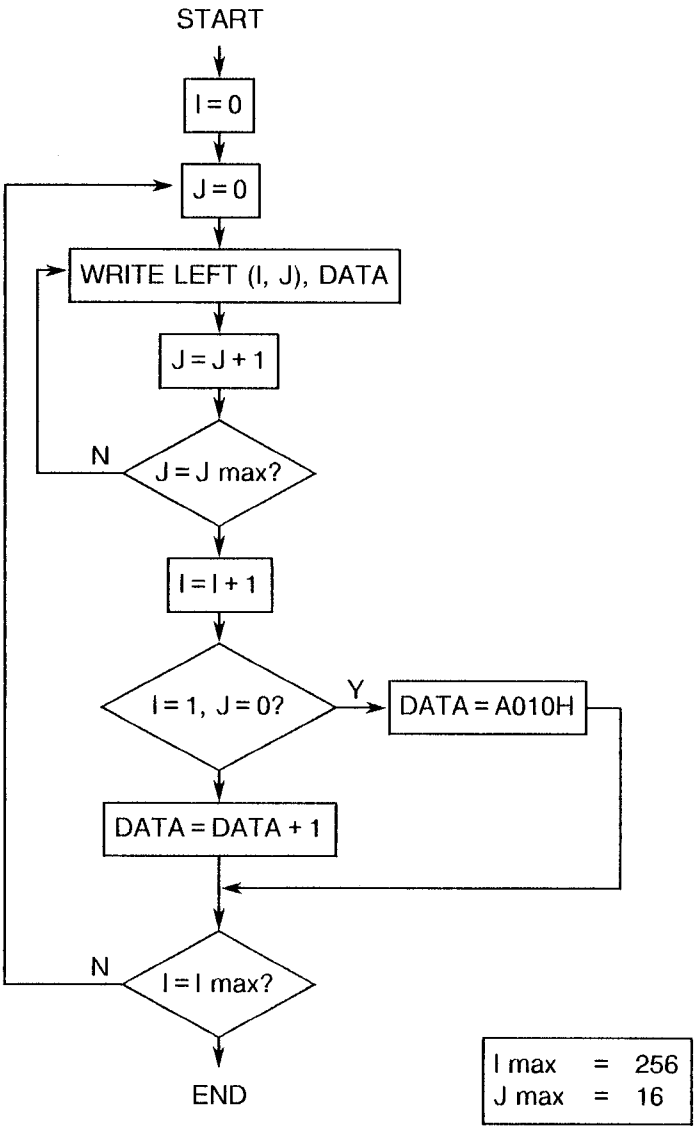
Write FF port Right at @ 3FEH with (INT = 1) ⇒ Check INTERRUPT Left port is set (INT = 0).
Write FF port Left at @ 3FFH with (INT = 0) ⇒ Check INTERRUPT Right port is set (INT = 0).

Read XX port Left at @ $\overline{3FEH}$ ⇒ Check INTERRUPT Right port not interpose (INT = 0).
Read XX port Right at @ $\overline{3FFH}$ ⇒ Check INTERRUPT Left port not interpose (INT = 0).

RESET INTERRUPT TWO PORTS (INT = 1)

Write FF port Right at @ $\overline{3FEH}$ ⇒ Check INTERRUPT Left port not interpose (INT = 1).
Write FF port Left at @ $\overline{3FFH}$ ⇒ Check INTERRUPT Right port not interpose (INT = 1).

6. L Pattern


START
I = 0
J = 0
WRITE LEFT (I, J), DATA
J = J + 1
N
J = J max?
I = I + 1
I = 1, J = 0?
Y
DATA = A010H
DATA = DATA + 1
N
I = I max?
END
I max = 256
J max = 16

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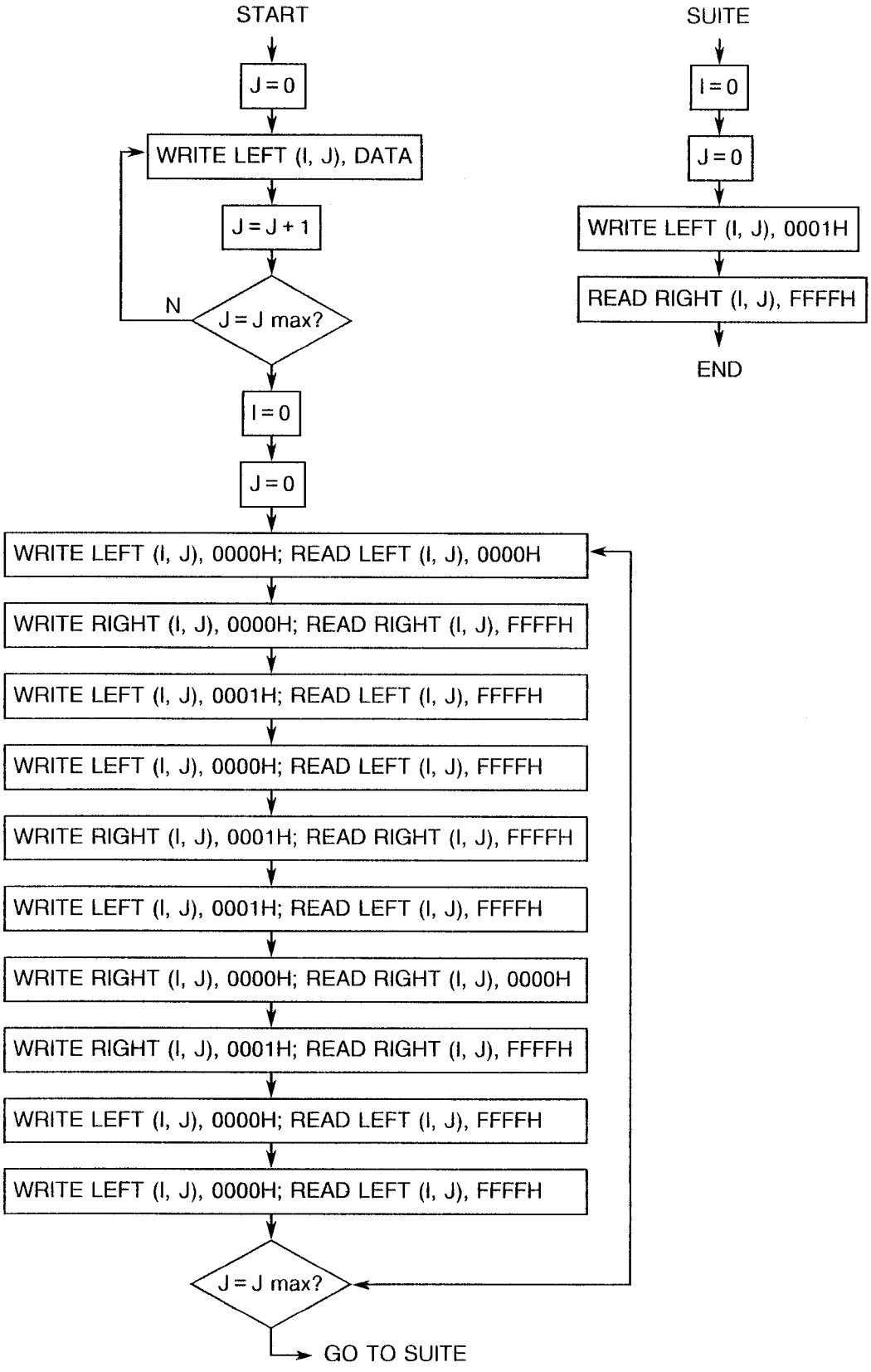
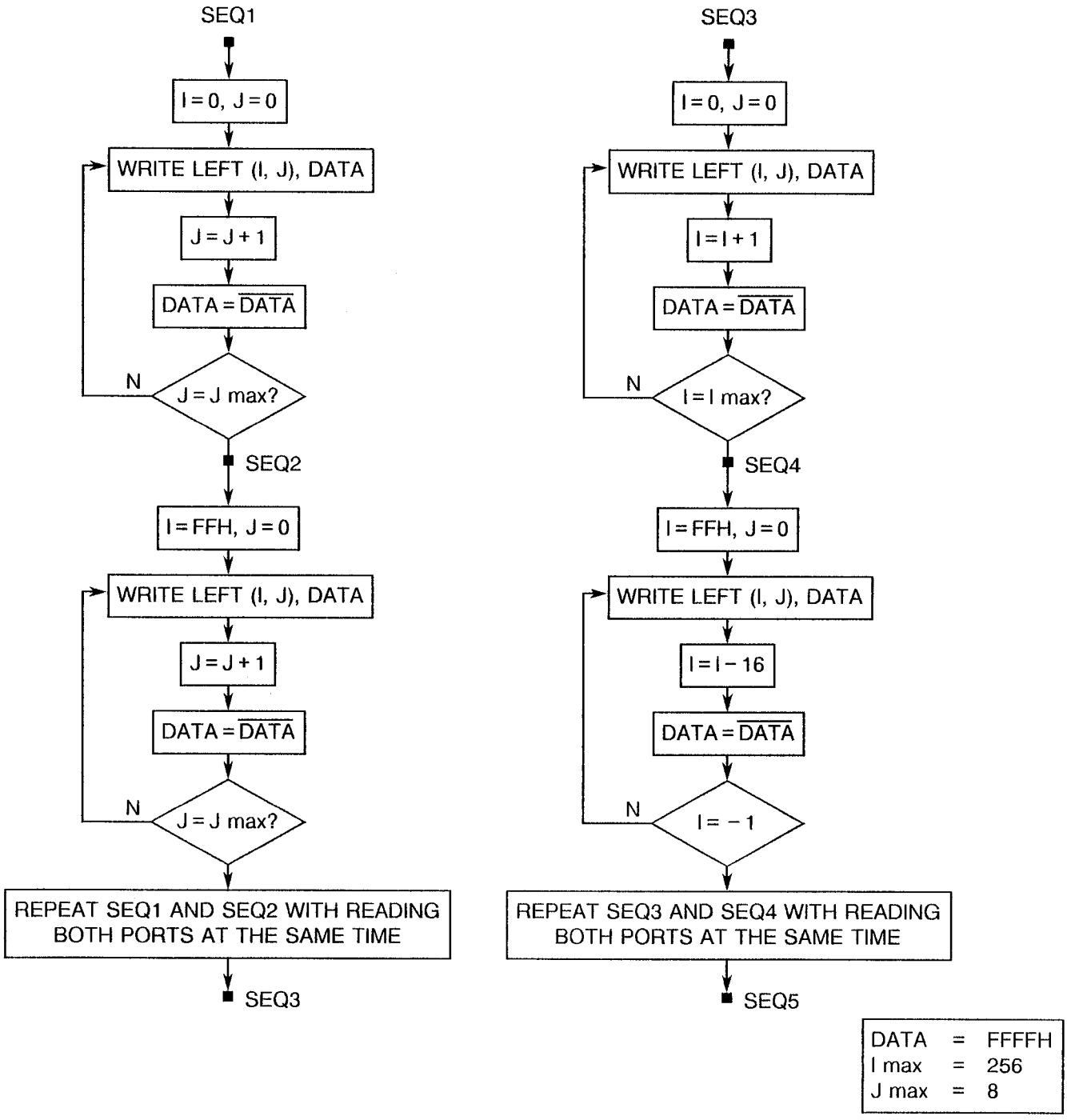
7. SEMAPHORE Pattern



I	=	FFH
J max	=	8

8. DUAL – PORT Pattern



DATA	=	FFFFH
I max	=	256
J max	=	8

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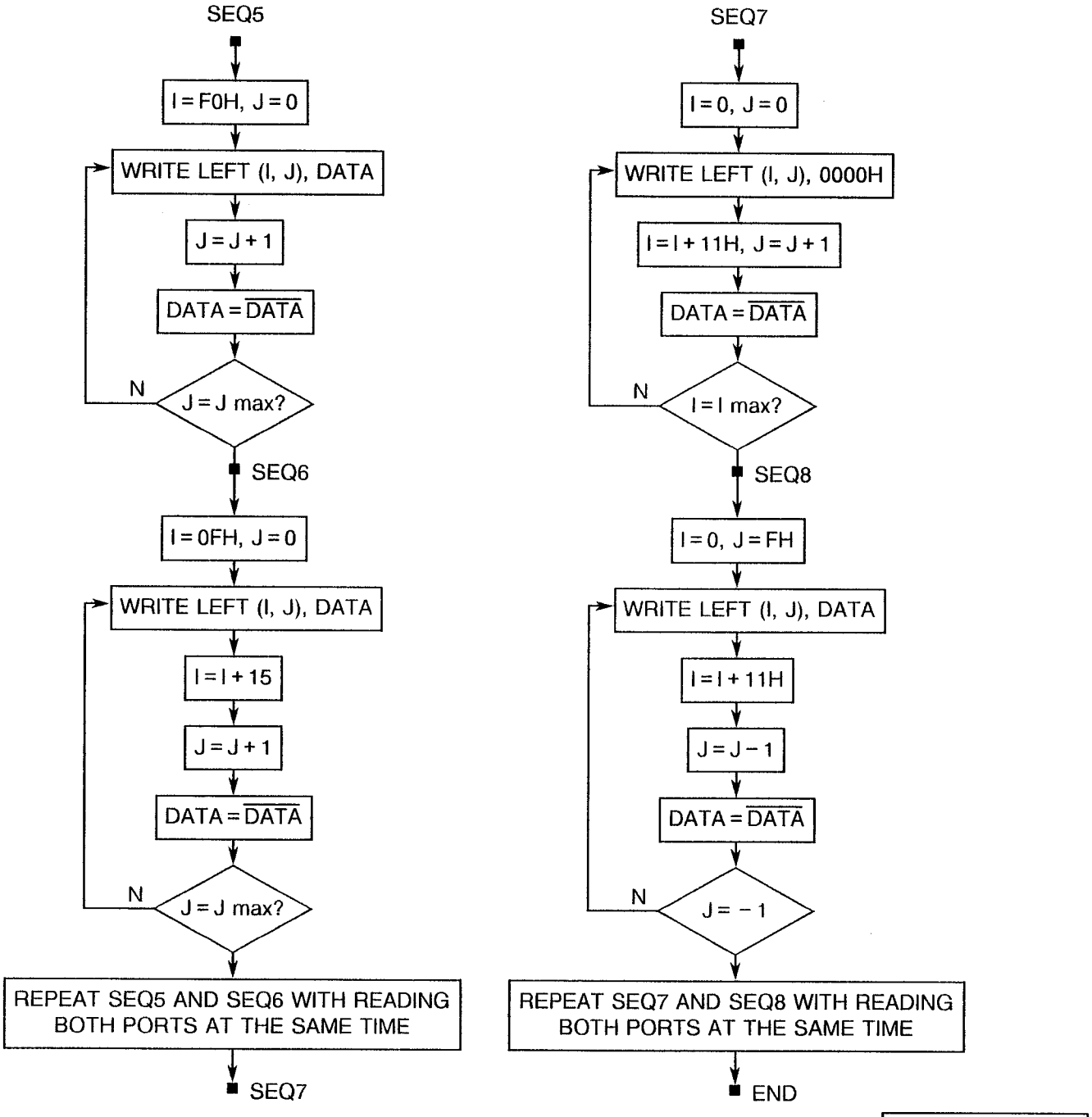
8. DUAL – PORT Pattern (Cont'd)



DATA	=	FFFFH
I max	=	256
J max	=	8

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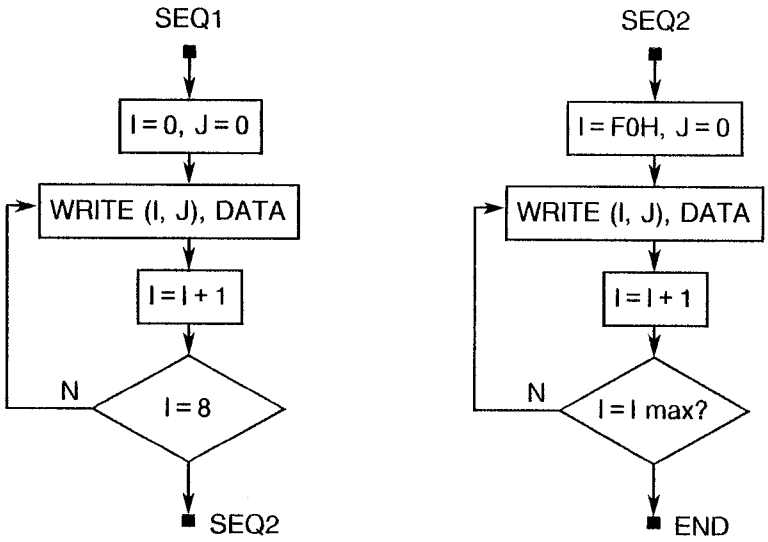
9. ARB – SLAVE Pattern



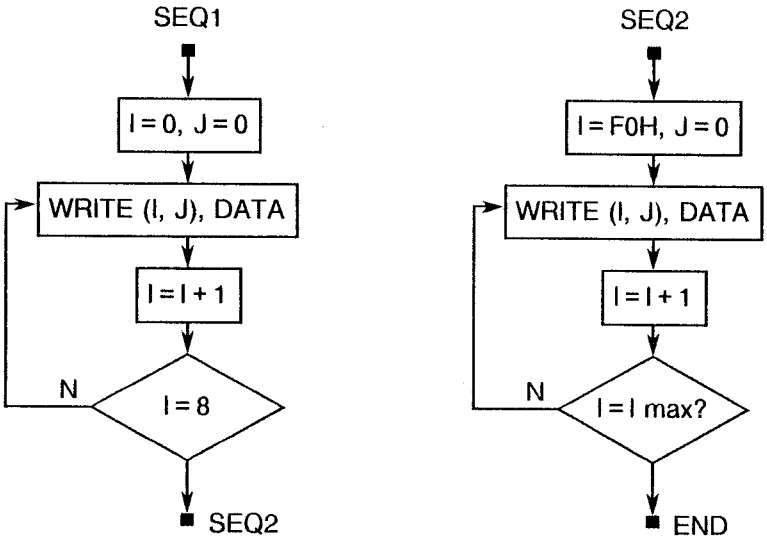
DATA	=	0000H
I max	=	256
J max	=	8

WRITE LEFT on SEQ1 and SEQ2 with DATA = 0000H and BUSY-L = High.
WRITE LEFT on SEQ1 and SEQ2 with DATA = FFFFH and BUSY-L = Low.
Remark: Timing relaxed rising edge busy left before rising edge write.
READ RIGHT on SEQ1 and SEQ2 with DATA = FFFFH.
WRITE LEFT on SEQ1 and SEQ2 with DATA = 0000 and BUSY-L = High.
WRITE LEFT on SEQ1 and SEQ2 with DATA = FFFFH and BUSY-L = Low.
Remark: Timing BUSY-L in phase with WRITE-L (inhibit left port).
READ RIGHT on SEQ1 and SEQ2 with DATA = 0000H.

WRITE RIGHT on SEQ1 and SEQ2 with DATA = 0000H and BUSY-R = High.
WRITE RIGHT on SEQ1 and SEQ2 with DATA = FFFFH and BUSY-R = Low.
Remark: Timing relaxed rising edge busy left before rising edge write.
READ LEFT on SEQ1 and SEQ2 with DATA = FFFFH.
WRITE RIGHT on SEQ1 and SEQ2 with DATA = 0000 and BUSY-R = High.
WRITE RIGHT on SEQ1 and SEQ2 with DATA = FFFFH and BUSY-R = Low.
Remark: Timing BUSY-R in phase with WRITE-R (inhibit right port).
READ LEFT on SEQ1 and SEQ2 with DATA = 0000H.

APPENDIX 'A'

10. ARB – MASTER Pattern



DATA	=	0000H
I max	=	256
J max	=	8

WRITE RIGHT on SEQ1 and SEQ2 with DATA = 0000H and BUSY-R = High.
ATTEMPT TO WRITE RIGHT PORT with DATA = FFFFH and BUSY-R = Low.
READ RIGHT PORT with DATA = 0000 on SEQ1 and SEQ2.

WRITE RIGHT on SEQ1 and SEQ2 with DATA = FFFFH and BUSY-R = Low.
Remark: Timing relaxed rising edge busy left before rising edge write.
READ LEFT on SEQ1 and SEQ2 with DATA = FFFFH.
WRITE RIGHT on SEQ1 and SEQ2 with DATA = 0000 and BUSY-R = High.
WRITE RIGHT on SEQ1 and SEQ2 with DATA = FFFFH and BUSY-R = Low.
Remark: Timing BUSY-R in phase with WRITE-R (inhibit right port).
READ LEFT on SEQ1 and SEQ2 with DATA = 0000H.