ESCC
European Space Components Coordination

Pages 1 to 25

TRANSISTORS, MICROWAVE, METAL SEMICONDUCTOR FIELD EFFECT, POWER GALLIUM ARSENIDE BASED ON TYPES CLY29 AND CLY32

ESCC Detail Specification No. 5614/006

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DCR No.	CHANGE DESCRIPTION
57	Specification upissued to incorporate editorial changes per DCR.

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APPENDICES (Applicable to specific Manufacturers only)

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a Transistor, Microwave, Metal Semiconductor Field Effect (MESFET), Power, Gallium Arsenide, based on Types CLY29 and CLY32. It shall be read in conjunction with ESCC Generic Specification No. 5010, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type components specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the components specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

The derating information applicable to the components specified herein is shown in Figure 1.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the components specified herein are shown in Figure 2.

1.6 FUNCTIONAL DIAGRAM

The functional diagram, showing lead identification of the components specified herein, is shown in Figure 3.

1.7 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore suitable precautions shall be employed for protection during all phases of manufacture test, packaging, shipping and handling.

These components are catagorised follows:

(a) Type Variants 01 to 03 (CLY32) - Class 2 with a Minimum Critical Path Failure Voltage of 1500V.

(b) Type Variants 04 to 06 (CLY29) - Class 2 with a Minimum Critical Path Failure Voltage of 1000V.

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 5010 for Discrete Microwave Semiconductor Components.

(b) MIL-STD-750, Test Methods for Semiconductor Devices.

TABLE 1(a) - TYPE VARIANTS

(1) VARIANT	(2) BASED ON TYPE	(3) CASE	(4) FIGURE	(6) MINIMUM OUTPUT POWER @ 2.3GHz (dBm)	(6) LEAD MATERIAL AND FINISH
01	CLY32-10	MWP25	2	32.5	D2
02	CLY32-05	MWP25	2	32.0	D2
03	CLY32-00	MWP25	2	31.5	D2
04	CLY29-10	MWP25	2	29.5	D2
05	CLY29-05	MWP25	2	29.0	D2
06	CLY29-00	MWP25	2	28.5	D2

TABLE 1(b) - MAXIMUM RATINGS

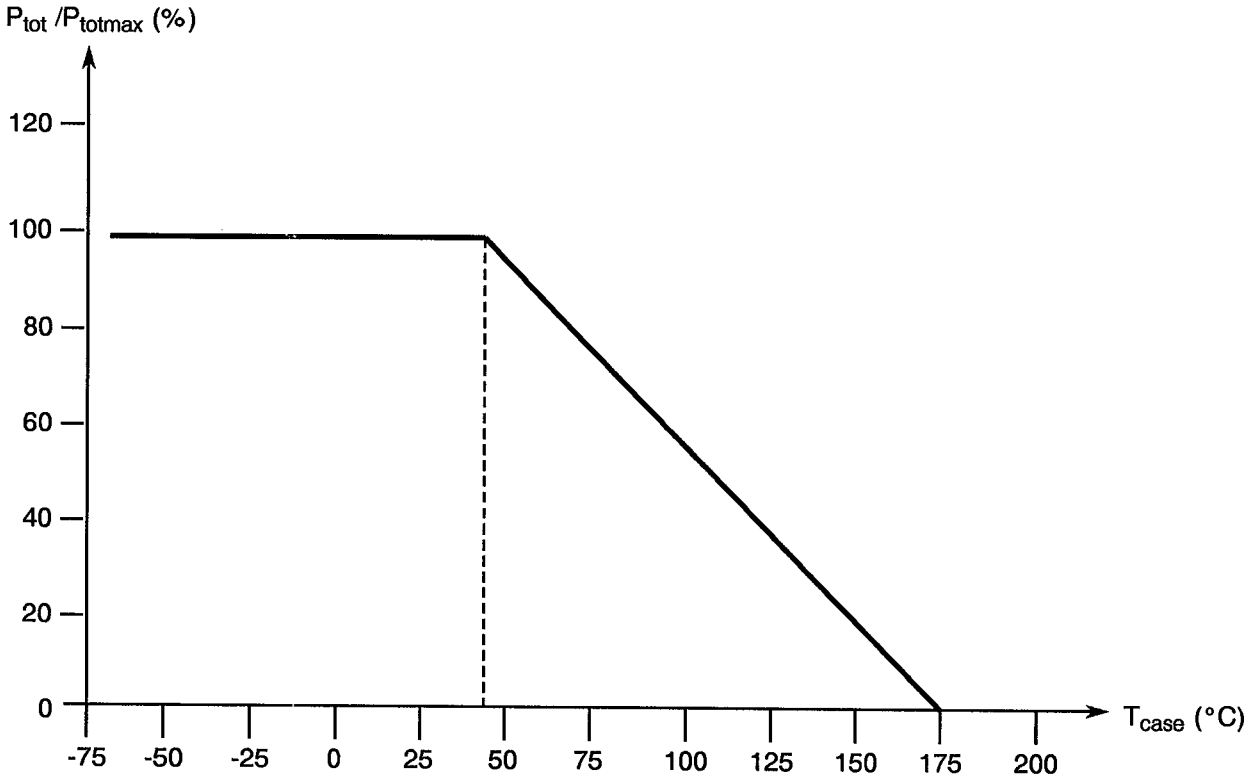
No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Drain-Source Voltage	V_{DS}	14	V	
2	Drain-Gate Voltage	V_{DG}	16	V	
3	Gate-Source Voltage	V_{GS}	-6.0	V	
4	Drain Current Variants 01 to 03 Variants 04 to 06	I_D	 1.4 at $V_{DS} \leq 4.8V$ 0.7 at $V_{DS} \leq 5.5V$	A	
5	Gate Current Variants 01 to 03 Variants 04 to 06	I_G	 8 4	mA	
6	Operational Gate DC Current Variants 01 to 03 Variants 04 to 06	I_{Go}	 -2 to +8 -1 to +4	mA	
7	Compression Level Variants 01 to 03 Variants 04 to 06	P_c	 1.5 at $V_{DS} \leq 9.0V$, $0.25A < I_D < 0.5A$ 2.5 at $V_{DS} \leq 8.0V$, $0.25A < I_D < 0.5A$ 3.5 at $V_{DS} \leq 7.0V$, $0.25A < I_D < 0.5A$ 1.5 at $V_{DS} \leq 9.0V$, $0.13A < I_D < 0.25A$ 2.5 at $V_{DS} \leq 8.0V$, $0.13A < I_D < 0.25A$ 3.5 at $V_{DS} \leq 7.0V$, $0.13A < I_D < 0.25A$	dB	Note 1
8	Power Dissipation Variants 01 to 03 Variants 04 to 06	P_{tot}	 6.75 3.85	W	Note 2
9	Channel Temperature Range	T_{ch}	-65 to +175	°C	
10	Storage Temperature Range	T_{stg}	-65 to +175	°C	
11	Soldering Temperature	T_{sol}	+230	°C	Note 3

NOTES: See Page 7

NOTES:
1. Under continuous wave.
2. At T_{case} = +40°C. For derating at T_{case} > +40°C, see Figure 1.
3. Duration 15 seconds maximum for the leads, 5 seconds maximum for the body. The same terminal shall not be resoldered until 3 minutes have elapsed.

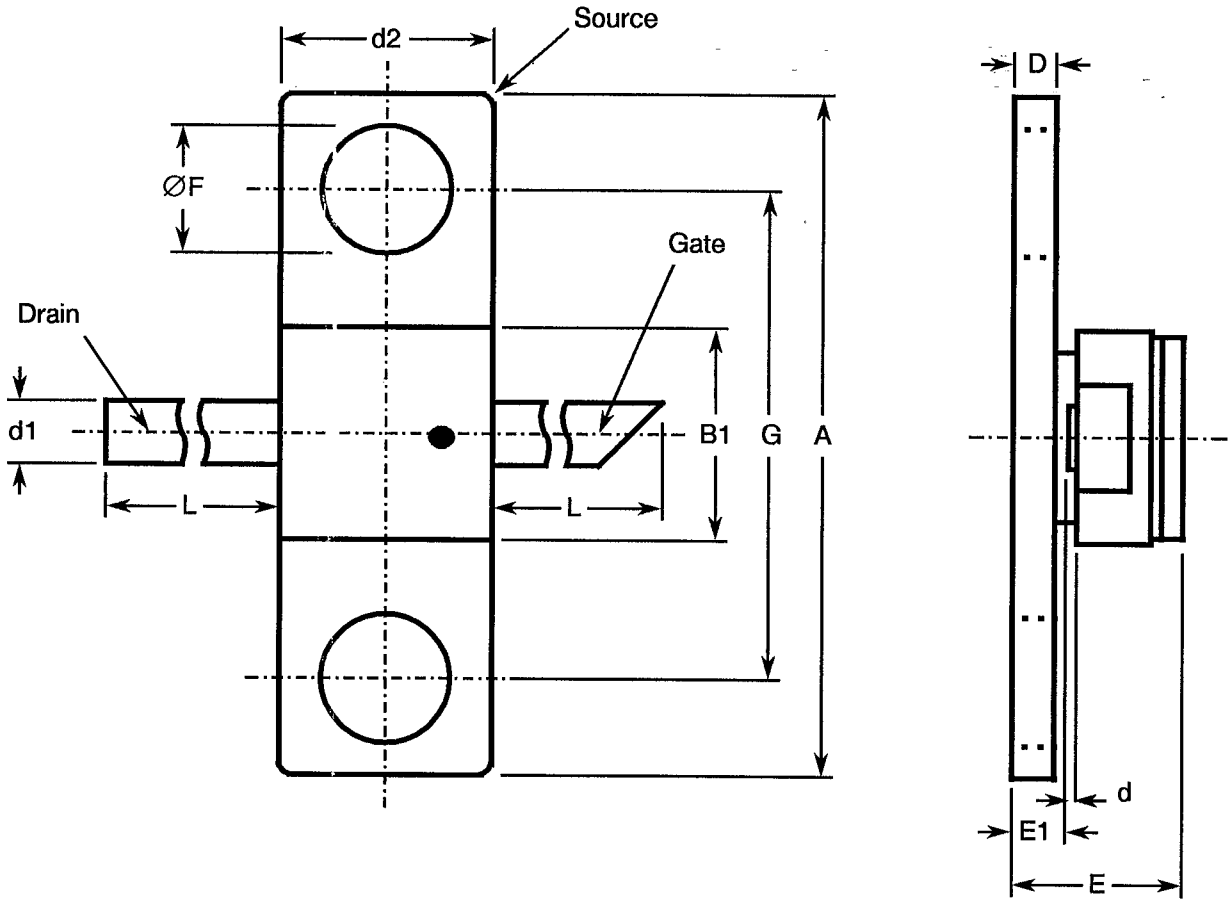
FIGURE 1 - PARAMETER DERATING INFORMATION

Power Dissipation versus Temperature



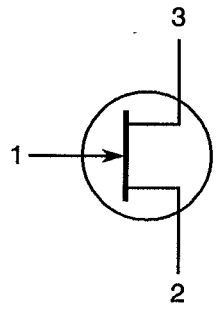
NOTES:
1. Thermal Resistance $R_{TH(ch-c)}$:
   Variants 01 to 03: 20°C/W
   Variants 04 to 06: 35°C/W.

FIGURE 2 - PHYSICAL DIMENSIONS



SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	8.30	8.70	
B1	2.30	2.70	
d	0.08	0.16	
d1	0.50	0.70	
d2	2.30	2.70	
D	0.50	0.70	
E	1.70	2.20	
E1	0.70	0.90	
ØF	1.50	1.70	
G	6.00	6.20	
L	2.70	3.70	

FIGURE 3 - FUNCTIONAL DIAGRAM



1. Gate
2. Source
3. Drain

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply. In addition, the following symbols are used:-

D	=	Drain.
G	=	Gate.
G_{lp}	=	Linear (small signal) Gain for Power Matching Condition.
G_p	=	Power Gain for Power Matching Condition.
g_m	=	Transconductance.
I_D	=	Drain Current.
I_{Do}	=	DC Drain Current under RF (Drain Operational Mean Current under RF Excitation).
$I_{Dpl, h, v}$	=	Drain Leakage current at Pinch-off (l: at low voltages, h: at high voltages, v: at excessive high voltages).
I_{Dss}	=	Drain Saturation Current for Shorted Gate ($V_{GS}=0$).
I_G	=	Gate Current.
I_{Go}	=	DC Gate Current under RF (Gate Operational Mean Current under RF Excitation).
$I_{Gpl, h}$	=	Gate Leakage current at Pinch-off (l: at low voltages, h: at high voltages).
PAE	=	Power Added Efficiency (= $[P_{out}-P_{in})/P_{DC}]$x100%).
P_c	=	Power Gain Compression Level.
P_{DC}	=	Dissipated DC Power.
P_{in}	=	RF Input Power.
P_{out}	=	RF Output Power.
P_{tot}	=	Power Dissipation (= $P_{DC} + P_{in}-P_{out}$).
PTC	=	Positive Temperature Coefficient Resistor.
R_D	=	External Drain Resistor.
R_G	=	External Gate Resistor.
R_S	=	External Source Resistor.
$R_{TH(ch-c)}$	=	Thermal Resistance, Channel to Case.
$R_{TH(C-HS)}$	=	Thermal Resistance, Case to Heatsink.
$R_{TH(HS-A)}$	=	Thermal Resistance, Heatsink to Ambient.
S	=	Source.
V_{DD}	=	Output Voltage from Drain Power Supply.
V_{DG}	=	Drain-Gate Voltage.
V_{DS}	=	Drain-Source voltage.
V_{GG}	=	Output Voltage from Gate Power Supply.
V_{GS}	=	Gate Source voltage.
V_{GSth}	=	Gate-source Threshold Voltage (Turn-on Voltage).
V_{SS}	=	Output Voltage from Source Power Supply (Ground).

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the components specified herein shall be as stated in this specification and ESCC Generic Specification No. 5010 for Discrete Microwave Semiconductor Components. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Production Control

None.

4.2.2 Deviations from Final Production Tests (Chart II(b))

(a) Para. 9.5, Thermal Shock: May also be performed in accordance with MIL-STD-883, Test Method 1010, Test Condition C.

(b) Para. 9.7, Particle Impact Noise Detection (PIND) Test: May be performed at any point after the position indicated in Chart II(b), but before final seal test, gross leak and fine leak.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III(b))

(a) Para. 9.9.2, Table 3 measurements: May be performed at any stage after power burn-in and shall be performed on the complete lot.

(b) Para. 9.9.3, Table 2 measurements: May be performed at any stage after power burn-in.

4.2.4 Deviations from Qualification Tests (Chart IV)

(a) Paras. 9.8.1 and 9.8.2, Seal Test: The tests following Para. 9.15, Constant Acceleration, shall not be performed.

(b) Para. 9.13, Shock Test: Shall not be performed.

(c) Para. 9.14, Vibration Test: Shall not be performed.

(d) Para. 9.15, Constant Acceleration: Shall not be performed.

(e) Para. 9.23, Special Testing: Shall not be performed.

(f) Assembly/Capability Tests (Subgroup II): In addition to the permitted electrical rejects, components rejected from radiographic inspection, seal test or external visual inspection may also be used for these tests, if they are considered capable of passing the Assembly/Capability Test sequence.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

(a) Paras. 9.8.1 and 9.8.2, Seal Test: The tests following Para. 9.15, Constant Acceleration, shall not be performed.

(b) Para. 9.13, Shock Test: Shall not be performed.

(c) Para. 9.14, Vibration Test: Shall not be performed.

(d) Para. 9.15, Constant Acceleration: Shall not be performed.

(e) Para. 9.23, Special Testing: Shall not be performed.

(f) Assembly/Capability Tests (Subgroup II): In addition to the permitted electrical rejects, components rejected from radiographic inspection, seal test or external visual inspection may also be used for these tests, if they are considered capable of passing the Assembly/Capability Test sequence.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the components specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the components specified herein shall be 0.2 grammes.

4.3.3 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESCC Generic Specification No. 5010. The test conditions shall be as follows:-

(a) Condition: 'A' (Tension).

(b) Force: 2.2N.

(c) Duration: 5 seconds.

4.3.4 Bond Strength

The requirements for bond strength are specified in Section 9 of ESCC Generic Specification No. 5010. The test conditions shall be as follows:-

(a) Condition: 'A'.

(b) Bond Strength: 0.03N force minimum, at pre-seal tests, 0.025N force minimum at post-seal tests.

4.3.5 Die Shear

The requirements for die shear are specified in Section 9 of ESCC Generic Specification No. 5010. The test conditions shall be alternatively as follows:-

(a) Minimum acceptable die shear strengths:

Variants 01 to 03: 4.2N

Variants 04 to 06: 2.6N.

(b) In the case that the clearances in the package do not allow application of a die shear force with a suitable tool, the chip shall be pushed away using a suitable tool and the die attach area inspected.

Sufficient die attach quality is achieved if objective evidence for sufficient mechanical and thermal contact is found, i.e. more than 50% semiconductor material remains.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the components specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body on an Au over Ni plated Cu flange.

4.4.2 Lead Material and Finish

The lead material shall be Type 'D' with Type '2' finish in accordance with the requirements of ESCC Basic Specification No. 23500.

4.5 MARKING

4.5.1 General

The marking of components delivered to this specification shall be in accordance with the

requirements of ESCC Basic Specification No. 21700 and the following paragraphs. When the component is too small to accommodate all of the marking as specified, as much as space permits shall be marked and the marking information, in full, shall accompany the component in its primary package.
The information to be marked and the order of precedence, shall be as follows:-

(a) Terminal Identification.

(b) The ESCC Component Number.

(c) Traceability Information.

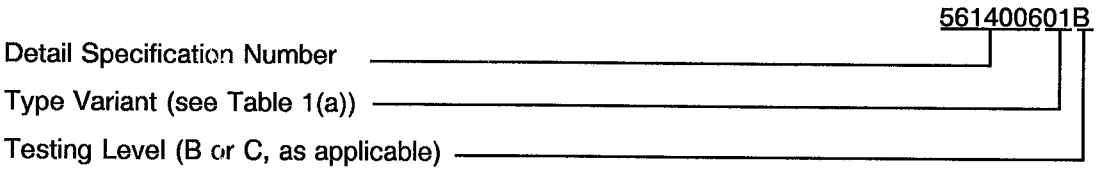
The primary package shall bear an "ESD sensitive" label.

4.5.2 Terminal Identification

Terminal identification shall be as shown in Figures 2 and 3 of this specification.

4.5.3 The ESCC Component Number

Each component shall bear the ESCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured at room temperature are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at T_{amb} = +25±3 °C.

Within their part types, those components which fail to achieve their specified RF Classification may be assigned to another type variant, after final electrical measurements.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. Unless otherwise specified, the measurements shall be performed at T_{amb} = +140(+0−5)°C.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Table 2 and Table 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

Burn-in shall be to Chart III(b) of ESCC Generic specification No. 5010.

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at T_{amb} = +25±3 °C. The

parameter drift values (Δ) applicable to the scheduled parameters shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-in

The requirements for high temperature reverse bias burn-in are specified in Section 9 of ESCC Generic Specification No. 5010. The conditions for high temperature reverse bias burn-in shall be as specified in Table 5(a) of this specification.

4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 9 of ESCC Generic Specification No. 5010. The conditions for power burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuit for High Temperature Reverse Bias Burn-in

The circuit for use in performing the high temperature reverse bias burn-in test is the general burn-in circuit shown in Figure 5 of this specification.

4.7.5 Electrical Circuit for Power Burn-in

The circuit for use in performing the power burn-in is the general burn-in circuit shown in Figure 5 of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - DC PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1	Drain Leakage Current at Pinch-off 1 (high V_{DS})	I_{Dph}	4(a)	V_{DS} = 12V, V_{GS} = -4V Variants 01 to 03 Variants 04 to 06	 - -	 120 60	µA
2	Gate Leakage Current at Pinch-off 1 (high V_{DS})	I_{Gph}	4(a)	V_{DS} = 12V, V_{GS} = -4V Variants 01 to 03 Variants 04 to 06	 - -	 -120 -60	µA
3	Drain Leakage Current at Pinch-off 2 (low V_{DS})	I_{Dpl}	4(a)	V_{DS} = 3V, V_{GS} = -3.8V Variants 01 to 03 Variants 04 to 06	 - -	 12 6	µA
4	Gate Leakage Current at Pinch-off 2 (low V_{DS})	I_{Gpl}	4(a)	V_{DS} = 3V, V_{GS} = -3.8V Variants 01 to 03 Variants 04 to 06	 - -	 -12 -6	µA
5	Drain Saturation Current	I_{Dss}	4(a)	V_{DS} = 2V, V_{GS} = 0V Variants 01 to 03 Variants 04 to 06	 0.6 0.3	 1.4 0.7	A
6	Gate Source Threshold Voltage	V_{GSth}	4(a)	V_{DS} = 3V Variants 01 to 03: I_D = 40mA Variants 04 to 06: I_D = 20mA	-1.6	-3.6	V
7	Transconductance	g_m	4(a)	V_{DS} = 3V Variants 01 to 03: I_D = 380mA Variants 04 to 06: I_D = 190mA	 300 150	 - -	mS
8	Thermal Resistance Channel to Case	$R_{TH(ch-c)}$	-	V_{DS} = 9V Variants 01 to 03: I_D = 380mA Variants 04 to 06: I_D = 190mA (Note 1)	 - -	 20 35	°C/W

NOTES: See Page 16.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - AC PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNIT
9	Linear Gain	G_{lp}	4(b)	V_{DS} = 9V, f = 2.3GHz (Note 2) Variants 01 to 03: I_{Dq} = 0.38A, $P_{in} \leq$ 11dBm Variants 01, 02 Variant 03 Variants 04 to 06: I_{Dq} = 0.19A, $P_{in} \leq$ 5dBm Variants 04, 05 Variant 06	 11.5 11 13.5 13	 - - - -	dB
10	Output Power	P_{out}	4(b)	V_{DS} = 9V, f = 2.3GHz (Note 2) Variants 01 to 03: I_{Dq} = 0.38A, P_{in} = 21.5dBm Variants 04 to 06: I_{Dq} = 0.19A, P_{in} = 16dBm	Note 3	-	dBm
11	Power Added Efficiency	PAE	4(b)	V_{DS} = 9V, f = 2.3GHz (Note 2) Variants 01 to 03: I_{Dq} = 0.38A, P_{in} = 21.5dBm Variants 01, 02 Variant 03 Variants 04 to 06: I_{Dq} = 0.19A, P_{in} = 16dBm Variants 04, 05 Variant 06	 45 40 45 40	 - - - -	%
12	Gate-Source Quiescent Voltage	V_{GSq}	4(b)	V_{DS} = 9.0V Variants 01 to 03: I_D = 0.38A Variants 04 to 06: I_D = 0.19A	Note 4		mV
13	Gate DC Current under RF	I_{Go}	4(b)	V_{DS} = 9V, f = 2.3GHz (Note 2) Variants 01 to 03: I_{Dq} = 0.38A, P_{in} = 21.5dBm Variants 04 to 06: I_{Dq} = 0.19A, P_{in} = 16dBm	Note 4		µA
14	Drain DC Current under RF	I_{Do}	4(b)	V_{DS} = 9V, f = 2.3GHz (Note 2) Variants 01 to 03: I_{Dq} = 0.38A, P_{in} = 21.5dBm Variants 04 to 06: I_{Dq} = 0.19A, P_{in} = 16dBm	Note 4		mA

NOTES:

1. Shall be performed on 5 assembled samples per wafer. If a failure occurs, 100% measurements shall be performed.
2. Input and output matched for maximum P_{out}.
3. See Column 5 of Table 1(a).
4. No specific limits applicable. The parameters are read and record for information only.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
1	Drain Leakage Current at Pinch-off 1 (high V_{DS})	I_{Dph}	4(a)	As per Table 2 Variants 01 to 03 Variants 04 to 06	 - -	 1.2 0.6	mA
2	Gate Leakage Current at Pinch-off 1 (high V_{DS})	I_{Gph}	4(a)	As per Table 2 Variants 01 to 03 Variants 04 to 06	 - -	 -1.2 -0.6	mA
3	Drain Leakage Current at Pinch-off 2 (low V_{DS})	I_{Dpl}	4(a)	As per Table 2 Variants 01 to 03 Variants 04 to 06	 - -	 0.24 0.12	mA
4	Gate Leakage Current at Pinch-off 2 (low V_{DS})	I_{Gpl}	4(a)	As per Table 2 Variants 01 to 03 Variants 04 to 06	 - -	 -0.24 -0.12	mA
6	Gate Source Threshold Voltage	V_{GSth}	4(a)	As per Table 2 Variants 01 to 03: I_D = 40mA Variants 04 to 06: I_D = 20mA (Note 1)	-1.4	-3.8	V
7	Transconductance	g_m	4(a)	As per Table 2 Variants 01 to 03: I_D = 380mA Variants 04 to 06: I_D = 190mA (Note 1)	 250 125	 - -	mS

NOTES:

1. Shall be performed on 5 assembled samples per wafer. If a failure occurs, 100% measurements shall be performed.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - TEST CIRCUIT FOR DC PARAMETERS

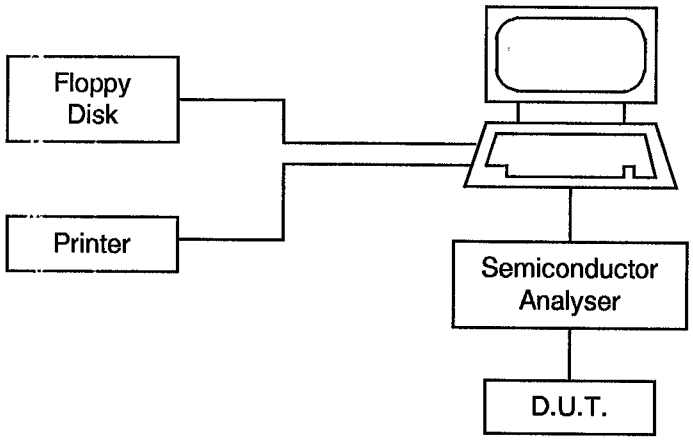
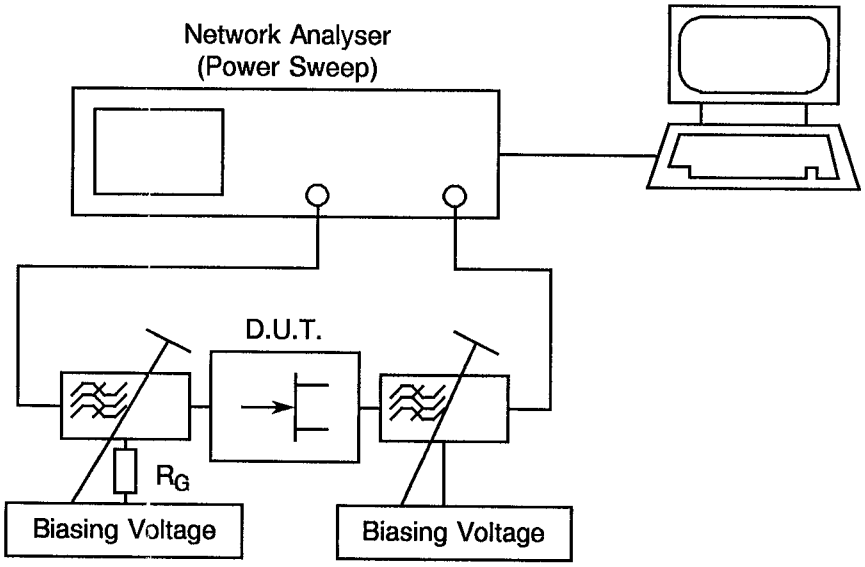


FIGURE 4(b) - TEST CIRCUIT FOR AC PARAMETERS



NOTES

1. DC Gate Resistance = 100Ω.

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
3	Drain Leakage Current at Pinch-off 2 (low V_{DS})	I_{Dpl}	4(a)	As per Table 2 Variants 01 to 03 Variants 04 to 06	 ±6 ±3	µA
4	Gate Leakage Current at Pinch-off 2 (low V_{DS})	I_{Gpl}	4(a)	As per Table 2 Variants 01 to 03 Variants 04 to 06	 ±6 ±3	µA
5	Drain Saturation Current	I_{Dss}	4(a)	As per Table 2 Variants 01 to 03 Variants 04 to 06	 ±125 ±55	mA
6	Gate Source Threshold Voltage	V_{GSth}	4(a)	As per Table 2	±0.2	V
7	Transconductance	g_m	4(a)	As per Table 2 Variants 01 to 03 Variants 04 to 06	 ±30 ±12	mS
10	Output Power	P_{out}	4(b)	As per Table 2	+0.5, -0.2	dB

NOTES:

1. Δ1 = Δ2.

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

No.	CHARACTERISTICS	SYMBOL	CONDITIONS	UNIT
1	Ambient Temperature	T_{amb}	+140(+0 -5)	°C
2	Gate to Source Voltage	V_{GS}	−6.0(+0.2 -0)	V
3	Drain Source Voltage	V_{DS}	10(+0 -0.2)	V

TABLE 5(b) - CONDITIONS FOR BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITIONS	UNIT
1	Ambient Temperature	T_{amb}	+90 (Note 1)	°C
2	Channel Temperature	T_{ch}	+175(+0 −5)	°C
3	Drain Source Voltage	V_{DS}	9(+0 -0.2)	V
4	Drain Current	I_D	Variants 01 to 03: 330 Variants 04 to 06: 205 (±10%, Note 2)	mA

NOTES:

Because the components are mechanically clamped to the burn-in fixture, an additional thermal resistance case to heatsink, e.g. $R_{TH(C-HS)} = 5°C/W$ must be considered for the calculation of T_{ch}. Furthermore, the heatsink temperature will rise above the ambient (oven) temperature, characterised by a futher $R_{TH(HS-A)} = 3°C/W$ per component.

1. T_{amb} shall be adjusted to provide the required T_{ch}.
2. The limits given for T_{ch} shall not be exceeded.

FIGURE 5 - ELECTRICAL CIRCUIT FOR BURN-IN

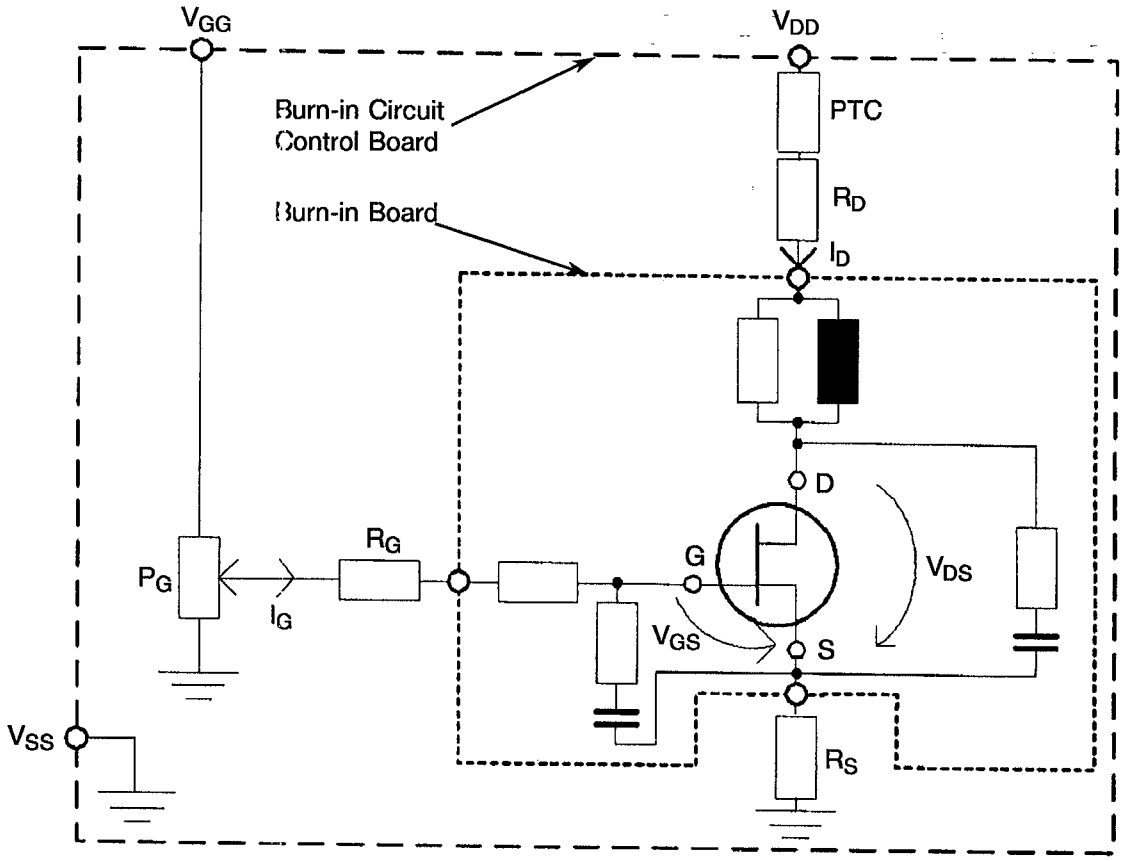
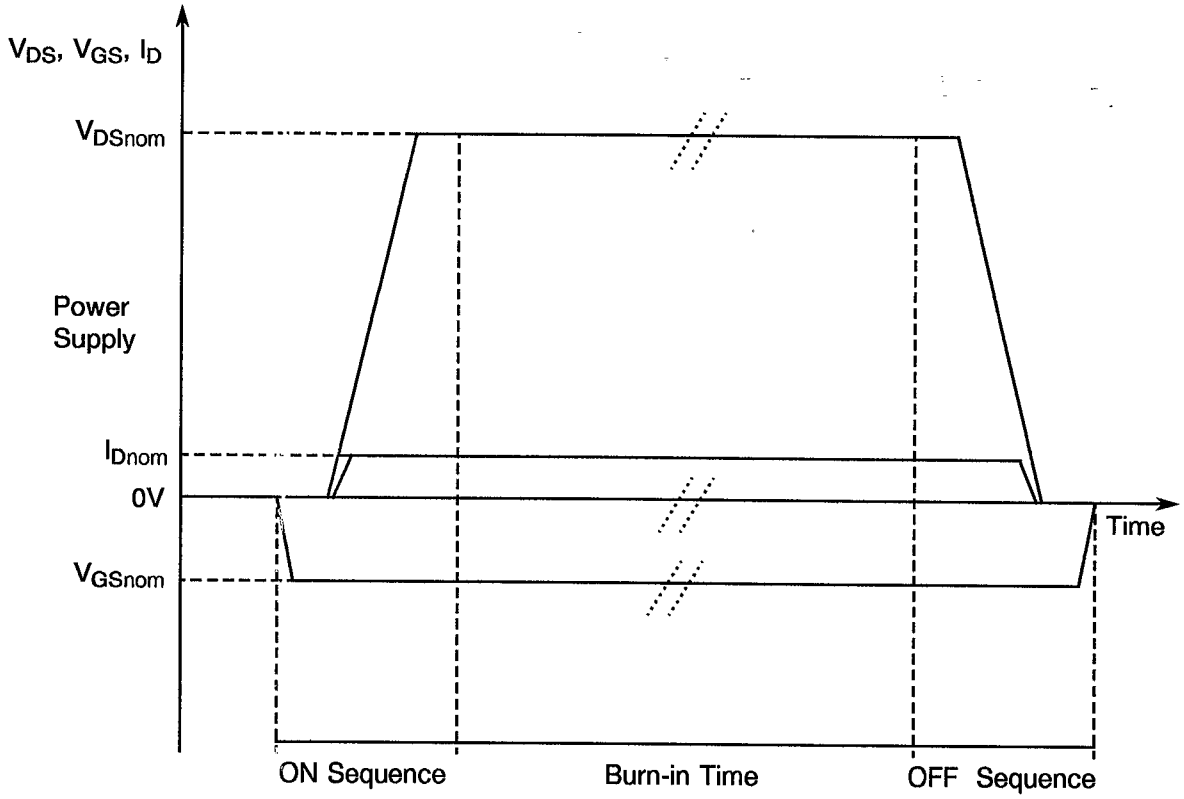
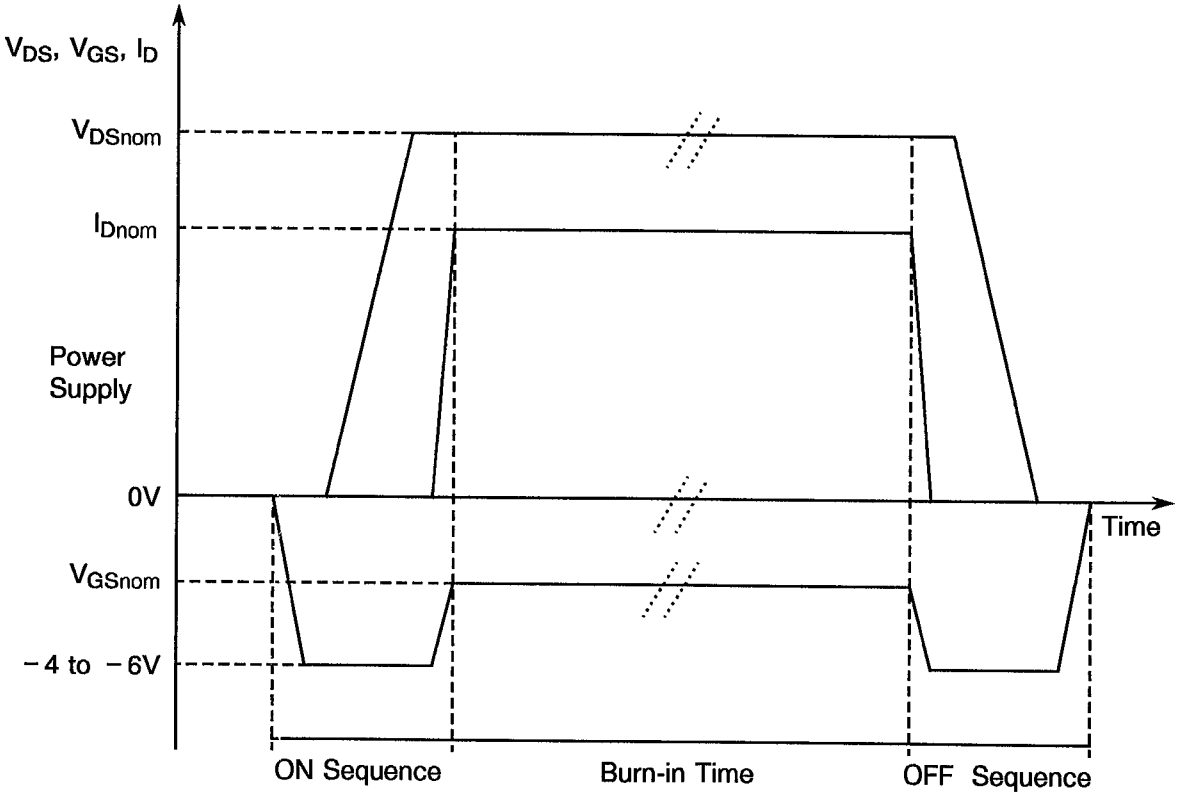


FIGURE 5 - ELECTRICAL CIRCUIT FOR BURN-IN (CONTINUED)



TIMING SEQUENCE FOR HTRB ON/OFF BIASING



TIMING SEQUENCE FOR POWER BURN-IN ON/OFF BIASING

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESCC GENERIC SPECIFICATION No. 5010)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 2. Unless otherwise stated, the measurements shall be performed at T_{amb} = +25 ± 3 °C.

4.8.2 Electrical Measurements at Intermediate Points and on Completion of Endurance Tests

The parameters to be measured at intermediate points and on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at T_{amb} = +25 ± 3 °C.

4.8.3 Conditions for Operating Life Test (Part of Endurance Testing)

The requirements for operating life testing are specified in Section 9 of ESCC Generic Specification No. 5010. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.4 Electrical Circuit for Operating Life Test

The circuit for use in performing the operating life test is the general burn-in circuit shown in Figure 5 of this specification.

4.9 TOTAL DOSE IRRADIATION TESTING

Not applicable.

4.10 SPECIAL TESTING

Not applicable.

TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS	LIMITS		CHANGE LIMITS (Δ)	UNIT
					MIN.	MAX.		
3	Drain Leakage Current at Pinch-off 2 (low V_{DS})	I_{Dpl}	4(a)	As per Table 2 Variants 01 to 03 Variants 04 to 06	 - -	 15 7.5	 ±6 ±3	µA
4	Gate Leakage Current at Pinch-off 2 (low V_{DS})	I_{Gpl}	4(a)	As per Table 2 Variants 01 to 03 Variants 04 to 06	 - -	 -15 -7.5	 ±6 ±3	µA
5	Drain Saturation Current	I_{Dss}	4(a)	As per Table 2 Variants 01 to 03 Variants 04 to 06	 0.5 0.25	 1.6 0.8	 ±0.125 ±0.055	A
6	Gate Source Threshold Voltage	V_{GSth}	4(a)	As per Table 2	-1.5	-3.7	±0.2	V
7	Transconductance	g_m	4(a)	As per Table 2 Variants 01 to 03 Variants 04 to 06	 280 140	 - -	 ±30 ±12	mS
10	Output Power	P_{out}	4(b)	As per Table 2	Note 1	-	±0.3	dB

NOTES:
1. As per Table 2, reduced by 0.2dB.

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING

Not applicable.

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING

Not applicable.

APPENDIX 'A'

AGREED DEVIATIONS FOR INFINEON TECHNOLOGIES (D)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.1	Paras. 5.2.4 and 10.5: If Wafer Lot Acceptance Test Data is specified in the purchase order, such data will not be delivered but will be available for review at Infineon Technologies.
Para. 4.2.2	Para. 9.11, Dimension Check: May be performed on a 100% basis using a gauge (ie. RF test fixture) during RF measurements.
Para. 4.2.3	Paras. 9.12 and 10.8.1, Radiographic Inspection: May be replaced by an Internal (pre-encapsulation) Visual Inspection for verifying the length, height and shape of the wire bonding. Paras. 9.2.1, HTRB and 9.22, Power Burn-in: The Infineon proprietary Burn-in Circuit which provides closed loop feedback of I_D to V_{GS} may be used to replace Figure 5.
Para. 4.2.4	Para. 9.20.1, Operating Life During Qualification Testing: The Infineon proprietary Burn-in Circuit which provides closed loop feedback of I_D to V_{GS} may be used to replace Figure 5.
Para. 4.2.5	Para. 9.20.2, Operating Life During Lot Acceptance Tests: The Infineon proprietary Burn-in Circuit which provides closed loop feedback of I_D to V_{GS} may be used to replace Figure 5.