INTEGRATED CIRCUITS, MONOLITHIC,

SILICON ON SAPPHIRE, CMOS VIRTUAL

CHANNEL ASSEMBLER,

BASED ON TYPE 12399

ESCC Detail Specification No. 9544/005

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Pages 1 to 85

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ESA/SCC Detail Specification No. 9544/005

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'A'	Jan. '97	P1. Cover page	: Part Number amended	221376
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		P4. T of C	: Appendix 'A' entry amended	221376
		P5. Para. 1.1	: In the first sentence, Part Number amended	221376
		P67. Figure 5(b)	: Part Number amended	221376
		P77. Figure 6	: Part Number amended	221376
		P84. Appendix 'A'	: Title amended	221376
			: For Para. 4.2.3 entry, Item "(b)" added	221376

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FIGURES

APPENDICES (Applicable to specific Manufacturers only)

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a monolithic, Silicon on Sapphire CMOS Virtual Channel Assembler, based on Type 12399. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

As per Figure 3(b).

1.8 CIRCUIT DESCRIPTION

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 with a Minimum Critical Path Failure Voltage of 1500Volts.

1.11 INPUT/OUTPUT PROTECTION NETWORKS

Protection networks shall be incorporated into each input and output as shown in Figure 3(e).

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND FINISH
01	FLAT	2(a)	D2

TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage	V_{DD}	– 0.5 to + 7.0	V	-
2	Input Voltage	V_{IN}	– 0.5 to V_{DD} + 0.5	V	-
3	DC Input Current	I_{IN}	20	mA	-
4	DC Output Current	I_{OUT}	10	mA	Note 1
5	Device Dissipation (Continuous)	P_D	200	mWdc	-
6	Output Dissipation	P_{DSO}	50	mWdc	Note 1
7	Operating Temperature Range	T_{op}	– 55 to + 125	°C	T_{amb}
8	Storage Temperature Range	T_{stg}	– 65 to + 150	°C	-
9	Soldering Temperature	T_{sol}	+ 260	°C	Note 2

NOTES

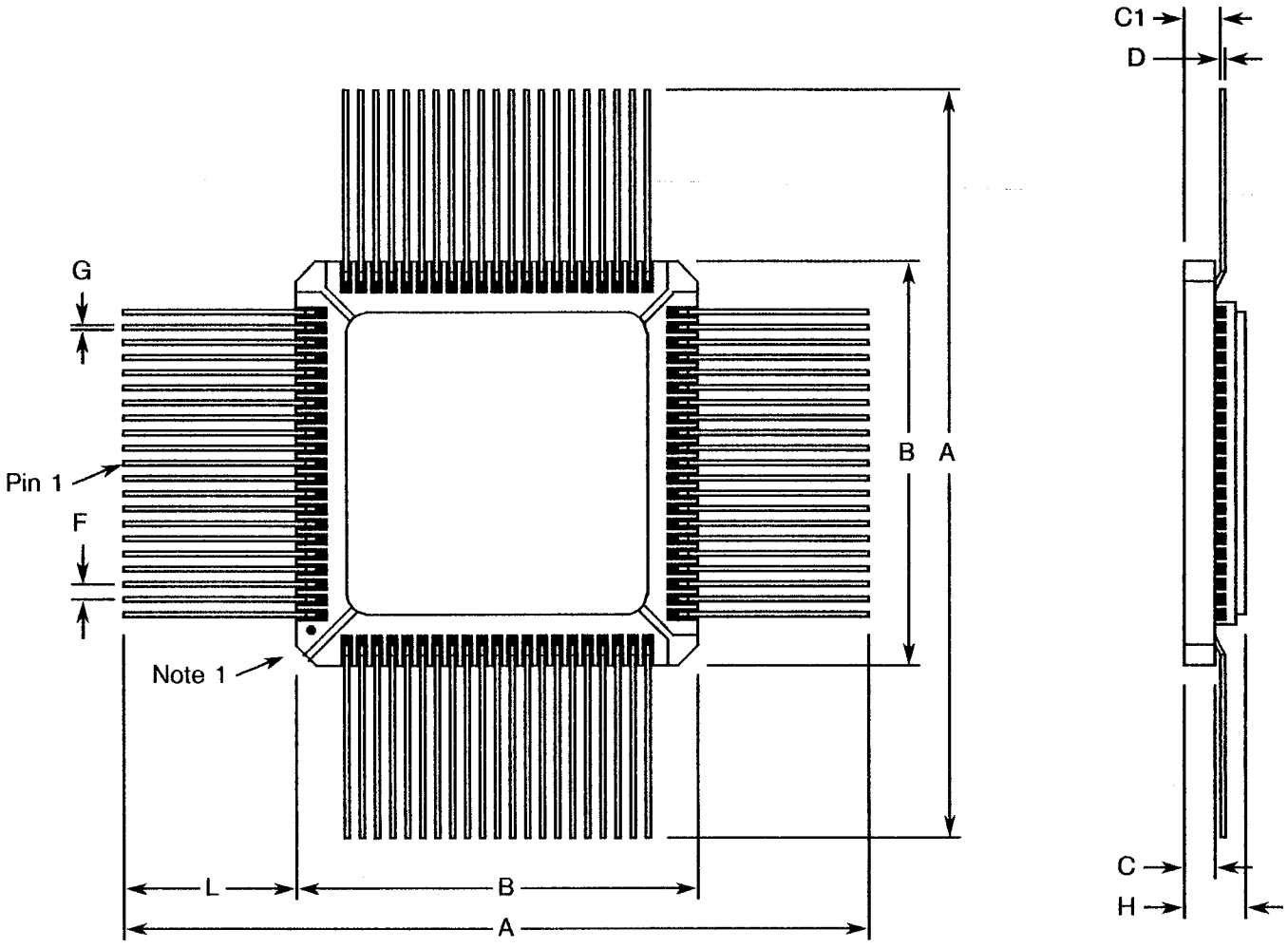
1. Single output.
2. Duration 5 seconds maximum at a distance of not less than 1.0mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION

Not applicable.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - FLAT PACKAGE, 84-PIN



SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	33.5	35.0	
B	16.2	16.7	
C	1.0	1.5	
C1	1.2	1.7	2, 5
D	0.1	0.2	
F	0.5	0.7	3, 4
G	0.2	0.3	2
H	1.9	2.4	
L	8.2	9.5	2

NOTES: See Page 8.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURE 2(a)

1. Index area; the index shall be as defined in Figure 2(a).
2. All leads.
3. 80 spaces for flat packages.
4. The true position pin spacing is 0.635mm between centre lines. Each pin centreline shall be located within ±0.1mm of its true longitudinal position relative to Pin 1 and the highest pin number.
5. The dimension shall be measured at the point of exit of the lead from the body.

FIGURE 3(a) - PIN ASSIGNMENT

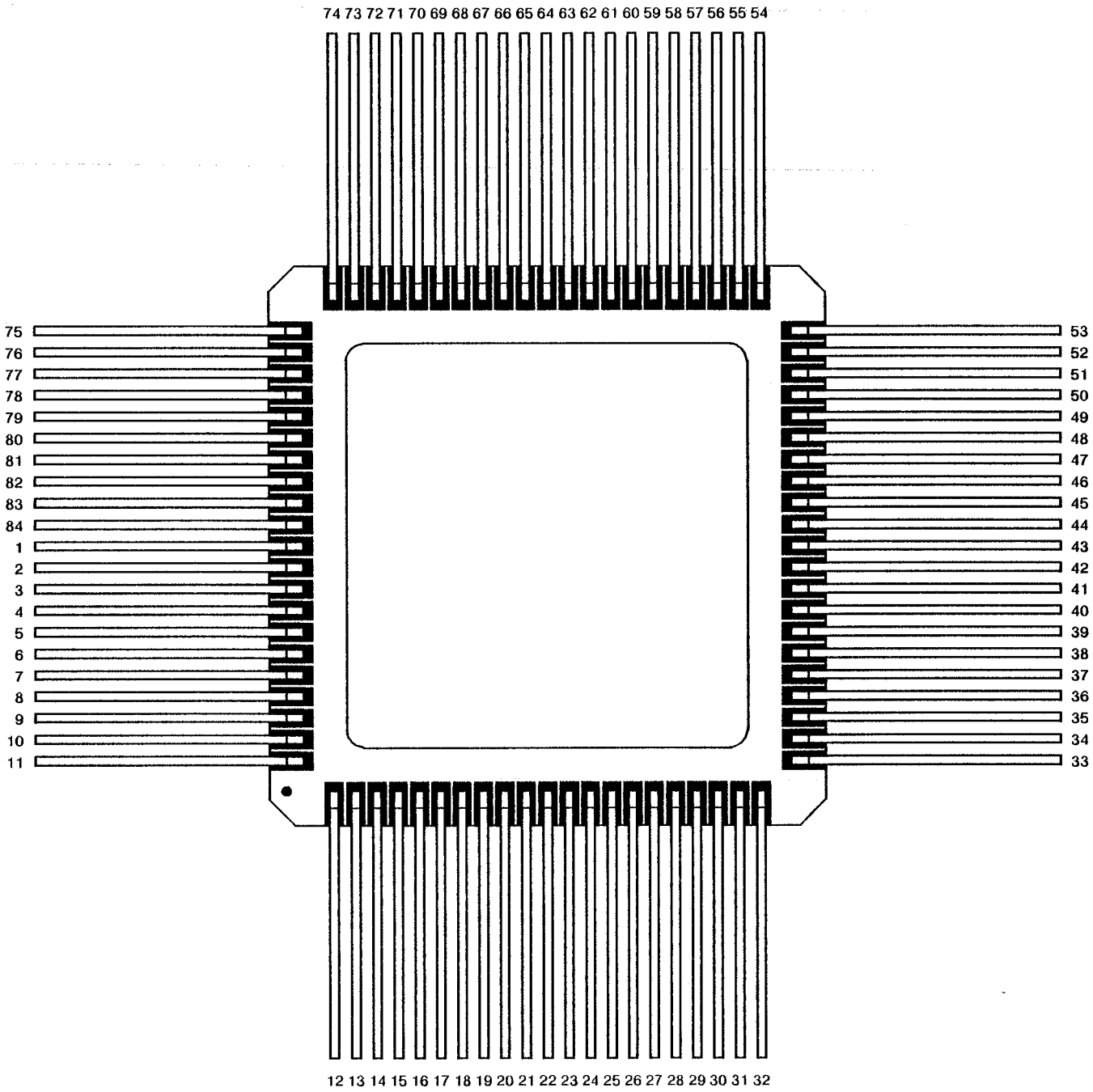


FIGURE 3(a) - PIN ASSIGNMENT (CONTINUED)

PIN DESCRIPTION

SYMBOL	FUNCTION	DESCRIPTION	PIN NUMBER
V_{DD}	Input	Positive Supply	1
D5	Data Input, Parallel Interface	TTL Input	2
D6	Data Input, Parallel Interface	TTL Input	3
V_{SS}	Input	Negative Supply	4
D7	Data Input, Parallel Interface	TTL Input	5
$\overline{BUSY}$	VCA Busy	Output	6
VCAR	VCA Ready	Output	7
SCLK	Clock, Serial Interface	CMOS Input	8
SIN	Data Input, Serial Interface	CMOS Input	9
SVALID	Data Valid, Serial Interface	CMOS Input	10
SMODE	Mode Selection	CMOS Input	11
$\overline{RESET}$	Master Reset	Schmitt Trigger Input	12
CLK	Clock	CMOS Input	13
NC	Not Connected	-	14
$\overline{ERR}$	Internal Error	Output	15
TEST1	Test Control	CMOS Input	16
TEST0	Test Control	CMOS Input	17
PROG2	Poll Programme	CMOS Input	18
PROG1	Poll Programme	CMOS Input	19
PROG0	Poll Programme	CMOS Input	20
V_{DD}	Input	Positive Supply	21
V_{SS}	Input	Negative Supply	22
OPCF	Operational Control Field	CMOS Input	23
FECW	Frame Error Control Word	CMOS Input	24
LEN1	Transfer Frame Length	CMOS Input	25
LEN0	Transfer Frame Length	CMOS Input	26
SYNCF	Synchronisation Flag	CMOS Input	27
PKTVER	Packet Version for Idle Telemetry Packets	CMOS Input	28
SECHEAD	Secondary Header Flag	CMOS Input	29
LSEG1	Segmentation Length Identifier	CMOS Input	30
LSEG0	Segmentation Length Identifier	CMOS Input	31
PKTORD	Packet Order Flag	CMOS Input	32
RANDOM	Pseudo-Random Data	Output	33
IFILL	Idle Fill Data	CMOS Input	34
TMODE3	Timing Strobe Mode	CMOS Input	35
TMODE2	Timing Strobe Mode	CMOS Input	36
TMODE1	Timing Strobe Mode	CMOS Input	37
TMODE0	Timing Strobe Mode	CMOS Input	38

FIGURE 3(a) - PIN ASSIGNMENT (CONTINUED)

PIN DESCRIPTION (CONTINUED)

SYMBOL	FUNCTION	DESCRIPTION	PIN NUMBER
V_{SS}	Input	Negative Supply	39
TESTOUT	Production Test Output	Output	40
TIME	Time Sampling Strobe	Output	41
CLKMODE	Clock Mode	CMOS Input	42
BITCLK	Bit Clock	CMOS Input	43
RTS	Ready To Send	Output	44
PVCF	Partial Virual Frame Data	Output	45
CTS	Clear To Send	CMOS Input	46
POLL	Device Poll	CMOS Input	47
V_{DD}	Input	Positive Supply	48
ERT	External RAM Test	CMOS Input	49
RD3	RAM Data	TTL Input/Output	50
RD4	RAM Data	TTL Input/Output	51
RD2	RAM Data	TTL Input/Output	52
RD1	RAM Data	TTL Input/Output	53
RD5	RAM Data	TTL Input/Output	54
RD0	RAM Data	TTL Input/Output	55
RD6	RAM Data	TTL Input/Output	56
V_{SS}	Input	Negative Supply	57
RA0	RAM Address	Output	58
RD7	RAM Data	TTL Input/Output	59
RA1	RAM Address	Output	60
$\overline{RCS}$	RAM Chip Select	Output	61
RA2	RAM Address	Output	62
RA10	RAM Address	Output	63
V_{SS}	Input	Negative Supply	64
V_{DD}	Input	Positive Supply	65
RA3	RAM Address	Output	66
$\overline{OE}$	RAM Output Enable Control	Output	67
RA4	RAM Address	Output	68
RA11	RAM Address	Output	69
RA5	RAM Address	Output	70
RA9	RAM Address	Output	71
RA6	RAM Address	Output	72
RA8	RAM Address	Output	73
V_{SS}	Input	Negative Supply	74
RA7	RAM Address	Output	75
RA12	RAM Address	Output	76

FIGURE 3(a) - PIN ASSIGNMENT (CONTINUED)

PIN DESCRIPTION (CONTINUED)

SYMBOL	FUNCTION	DESCRIPTION	PIN NUMBER
R/$\overline{W}$	RAM Read/Write Control	Output	77
$\overline{VPD}$	Valid Packet Data for Parallel Interface	TTL Input	78
$\overline{CS}$	Chip Select, Parallel Interface	TTL Input	79
D0	Data Input, Parallel Interface	TTL Input	80
D1	Data Input, Parallel Interface	TTL Input	81
D2	Data Input, Parallel Interface	TTL Input	82
D3	Data Input, Parallel Interface	TTL Input	83
D4	Data Input, Parallel Interface	TTL Input	84

FIGURE 3(b) - TRUTH TABLE

TIMING DIAGRAMS

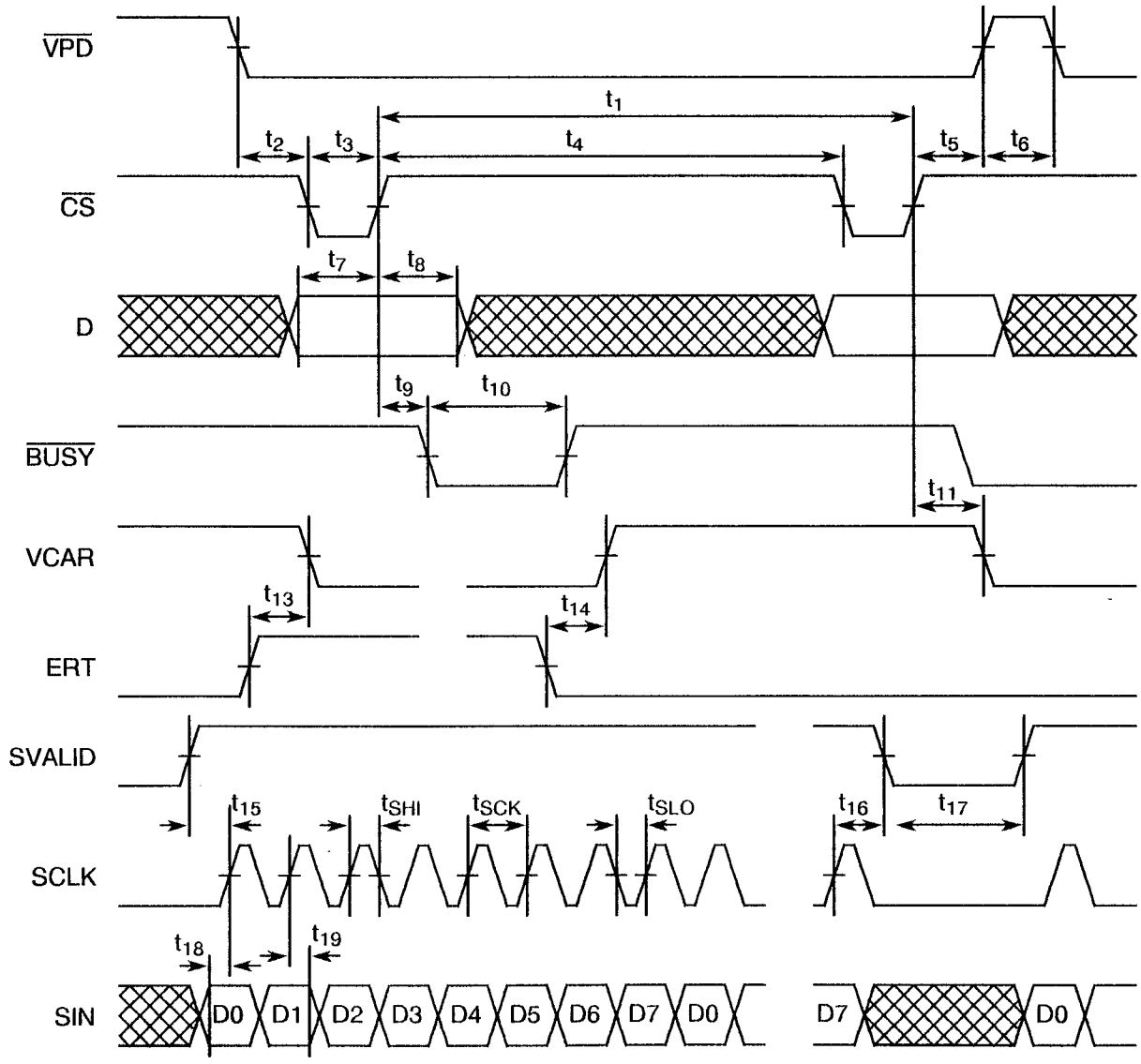


FIGURE 3(b) - TRUTH TABLE (CONTINUED)

TIMING DIAGRAMS (CONTINUED)

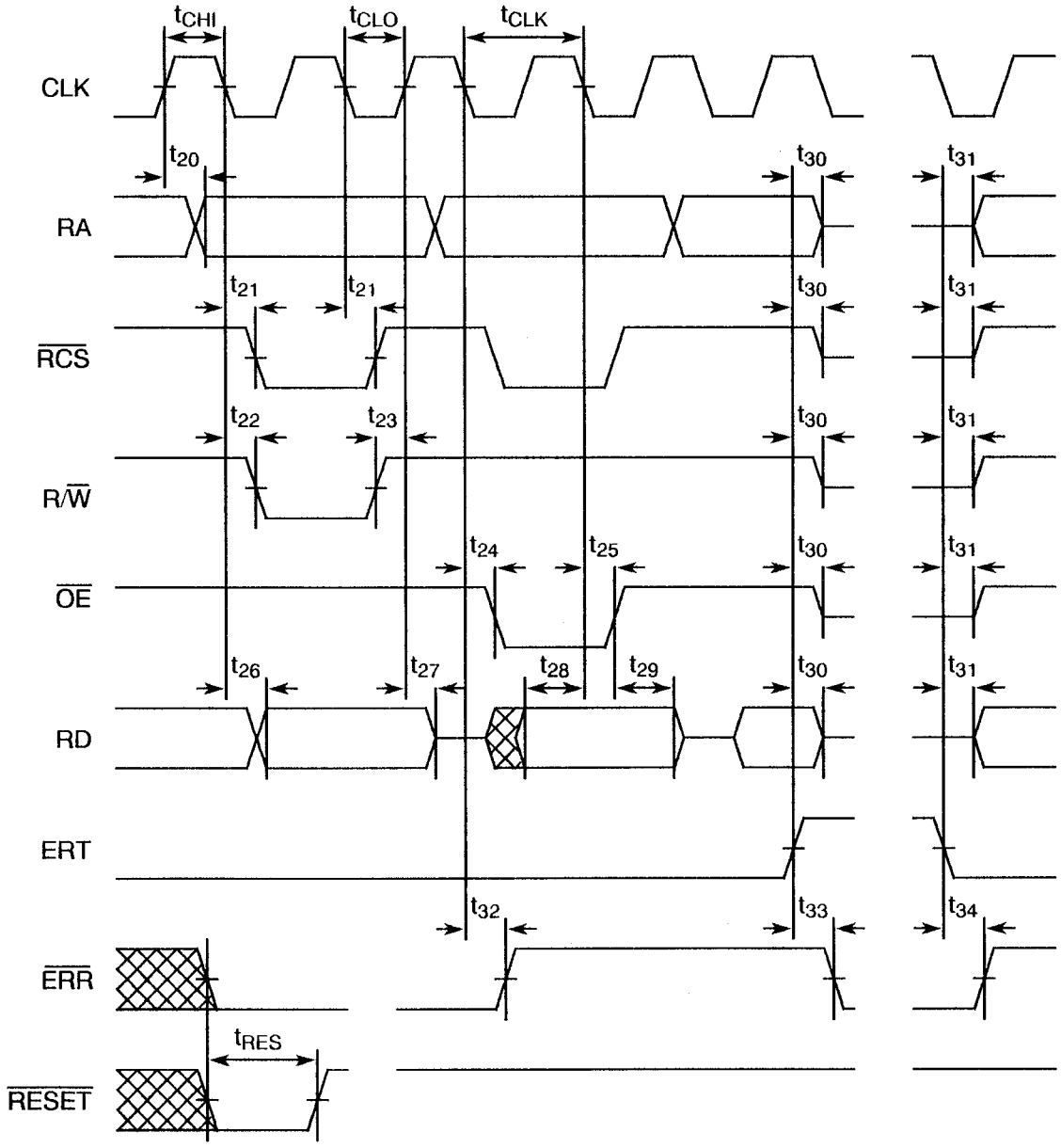


FIGURE 3(b) - TRUTH TABLE (CONTINUED)

TIMING DIAGRAMS (CONTINUED)

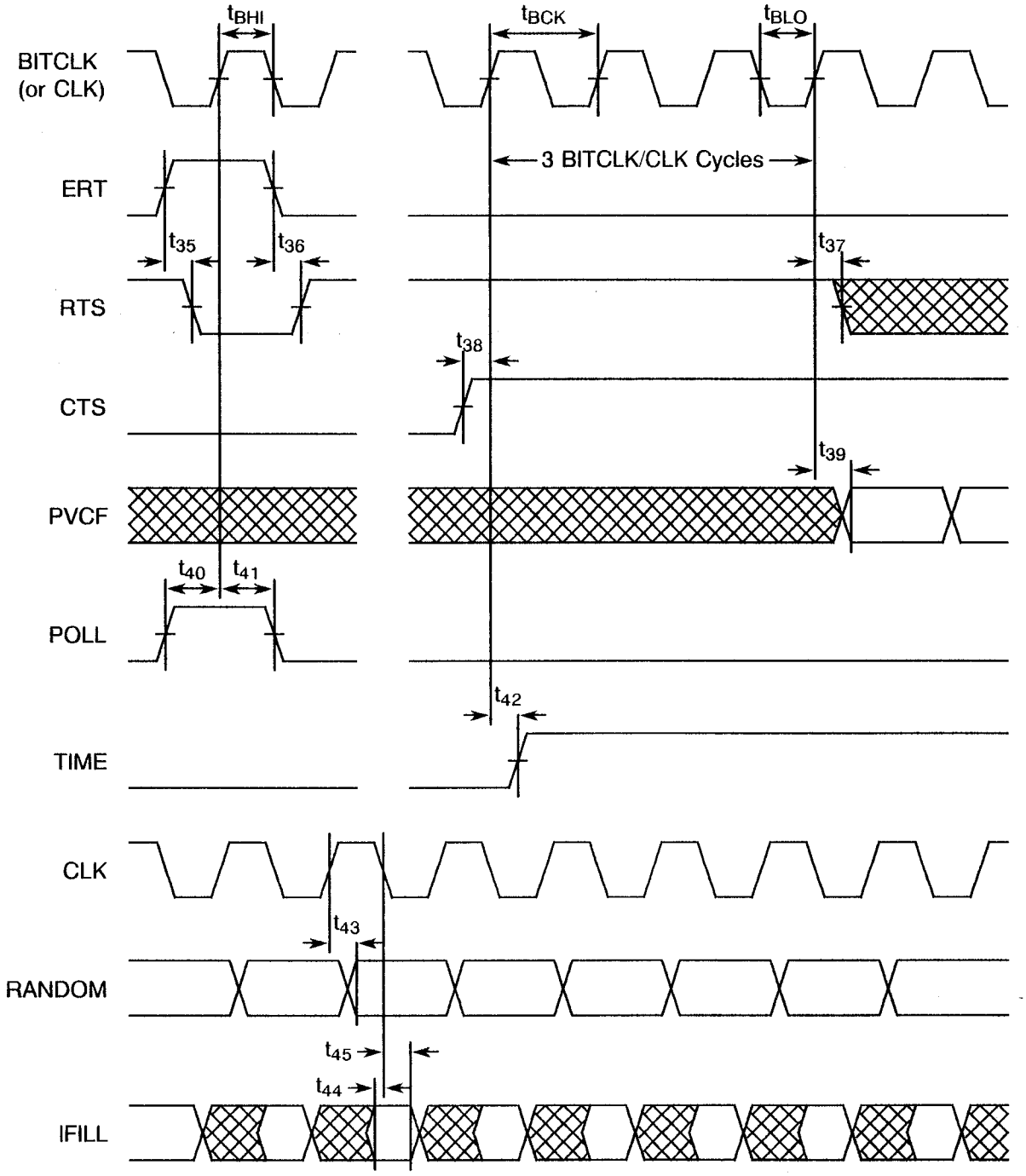


FIGURE 3(c) - CIRCUIT DESCRIPTION

SUMMARY OF OPERATION

After reset and the optional self-test, the VCA provides the following functions:

- Reception of data from the OBDH system, which is stored in an external RAM together with header data.
- When requested by the VCM, a partial Transfer Frame is output, consisting of the PVCF Header, optionally including a Secondary Header, and the Transfer Frame Data Field.
- If enough data is not available, a partial Idle Transfer Frame is output instead.
- Optional generation of Idle Telemetry Packets to fill up incomplete Transfer Frames.
- Generation of Pseudo-random Idle Fill data, used for the generation of partial Idle Telemetry Packets and Idle Transfer Frames.
- Generation of a Time sampling strobe.

In order to complete the Transfer Frame the VCM performs the following functions:

- Generation of the 32 bit Synchronisation Marker.
- Generation of the first three octets of the Transfer Frame Primary Header.
- Feed-through of the PVCF data as part of the Transfer Frame.
- Generation of an optional Transfer Frame Trailer.
- Optionally leaving space for a Reed-Solomon code check block.

FUNCTIONS NOT INCLUDED IN THE VCA

The VCA does not perform segmentation of Source Packets, which should be done by the data source. The VCA can handle Telemetry Packets and data blocks longer than 8k octets, though only a part of the data will reside in the external RAM at a time.

The VCA does not check the contents or the format of the Telemetry Packets provided by the source. Thus the VCA is independent of the Telemetry Packet format and any data structure can be used. The only exception is the Idle Telemetry Packets that can be optionally generated by the VCA itself, which have a predefined structure.

PARALLEL INPUT INTERFACE

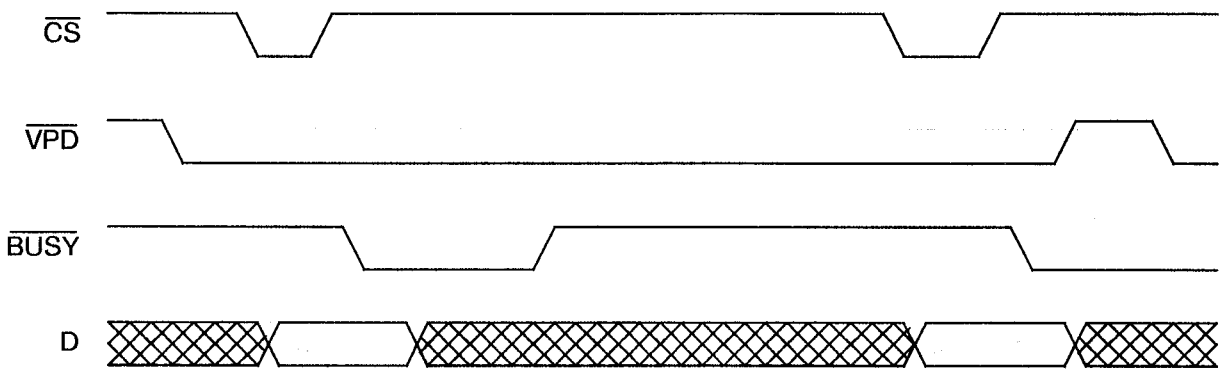
The parallel interface, shown in Figure I, is active when SMODE = "0". The serial interface inputs SCLK, SVALID and SIN are then disabled but should be held to a defined logic level.

The main functions of the parallel input interface are:

- To latch data from the input bus and into the VCA.
- To inform the data source that the VCA has space in the external RAM.
- To detect the beginning of Telemetry Packets or data blocks being sent from the source and to set the First Header Pointer accordingly.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

FIGURE I - PARALLEL INPUT INTERFACE



Data is input from the data source using the eight-bit-wide data bus (D0 - D7), and the chip select, $\overline{CS}$. The interface is asynchronous. Data is latched into the VCA on the rising $\overline{CS}$ edge, as shown in Figure I.

N.B. D0 is the MSB.

The active low Valid Packet Data ($\overline{VPD}$) input defines when a new Telemetry Packet (data block in asynchronous mode) starts. The VCA stores data latched by the input interface when the $\overline{VPD}$ input is enabled ($\overline{VPD}$ = "0"). The $\overline{VPD}$ input should be continuously enabled while a Telemetry Packet is being input. The timing of $\overline{VPD}$ is shown in Figure I. $\overline{VPD}$ is also used to set the First Header Pointer.

Data may be supplied at any rate up to one octet transfer every four CLK cycles, allowing a maximum peak input data rate of 25MBit/s when operating at the maximum clock frequency of 12.5MHz. If data is input at a higher rate, data could be lost.

In the case of using Telemetry Packets with a limited length (LSEG≠"11"), the VCA Ready (VCAR) output is enabled when there is room for at least one maximum-length Telemetry Packet in the external RAM. Otherwise the VCAR output is enabled when there is room for at least one Transfer Frame Data Field.

This output is enabled (= "1") when the VCA has place to store data in the external RAM, as defined below. VCAR changes state on the falling CLK edge. VCAR is also disabled when ERT is enabled (= "1") since the RAM is not then accessible. The values correspond to one maximum length packet or data field, respectively.

SYNCF	LSEG0	LSEG1	VCAR Threshold
0	0	0	≥262 (256 + 6)
0	0	1	≥518 (512 + 6)
0	1	0	≥1030 (1024 + 6)
0	1	1	≥Length of Transfer Frame Data Field
1	-	-	≥Length of Transfer Frame Data Field

NOTES

1. Logic Level Definitions: 0 = Low Level, 1 = High Level.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

Since VCAR is enabled when there is room for a predefined amount of data (one maximum-length Telemetry Packet or alternatively one Transfer Frame Data Field), this data can be transferred in its entirety without needing to check VCAR again.

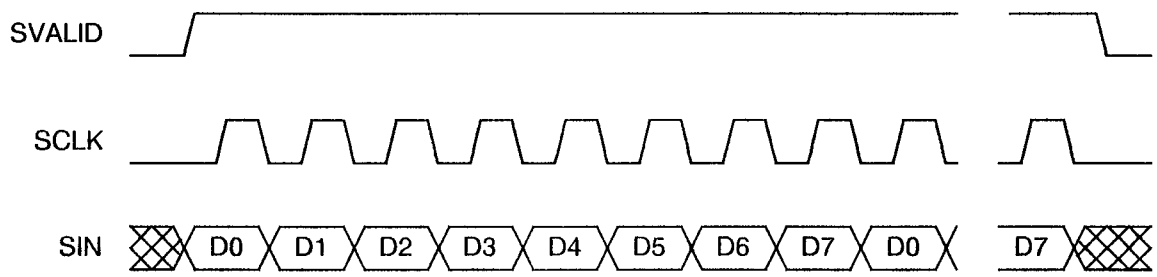
The $\overline{\text{BUSY}}$ (VCA Busy) output is enabled ($\overline{\text{BUSY}}$ = "0") immediately after an octet has been written into the VCA (i.e. the rising $\overline{\text{CS}}$ edge). $\overline{\text{BUSY}}$ is disabled at the next falling CLK edge three CLK cycles after the rising $\overline{\text{CS}}$ edge. Since $\overline{\text{CS}}$ may be asynchronous, the actual duration of $\overline{\text{BUSY}}$ enabled can vary between three and four CLK cycles. $\overline{\text{BUSY}}$ is also enabled when there is no space for more octets in the external RAM. If $\overline{\text{CS}}$ is enabled while $\overline{\text{BUSY}}$ is enabled, no data will be latched.

The VCAR output alone can be used together with data sources that provide data with a transfer rate which is less than the maximum possible, while the $\overline{\text{BUSY}}$ output can be used with fast data sources that need acknowledgement on the octet level, such as a CPU.

SERIAL INPUT INTERFACE

The serial input interface, shown in Figure II, is enabled when SMODE = "1". The parallel interface inputs $\overline{\text{CS}}$, $\overline{\text{VPD}}$ and D0 - D7 are disabled, but should be held to a defined logic level. The VCAR and $\overline{\text{BUSY}}$ outputs and all other functions of the VCA behave the same as for the parallel input interface, although they are probably less useful for the serial interface.

FIGURE II - SERIAL INPUT INTERFACE



Serial data is clocked in on the rising SCLK edge, when SVALID = "1". The serial data is assembled in a shift register and when eight bits have been input, the resulting octet is internally forwarded to the parallel interface. Data should consist of multiples of eight bits otherwise the last bits will be lost.

The input signal SVALID is used to delimit Telemetry Packets (data blocks in asynchronous mode), in the same way as $\overline{\text{VPD}}$ is used for the parallel interface. It shall be enabled while a Telemetry Packet (data block) is being input. In addition, SVALID defines the octet boundaries in the input data stream, the first octet explicitly and the following octets each subsequent eight SCLK cycles; the first bit received after SVALID has been enabled is bit 0. SVALID shall be enabled when data is input.

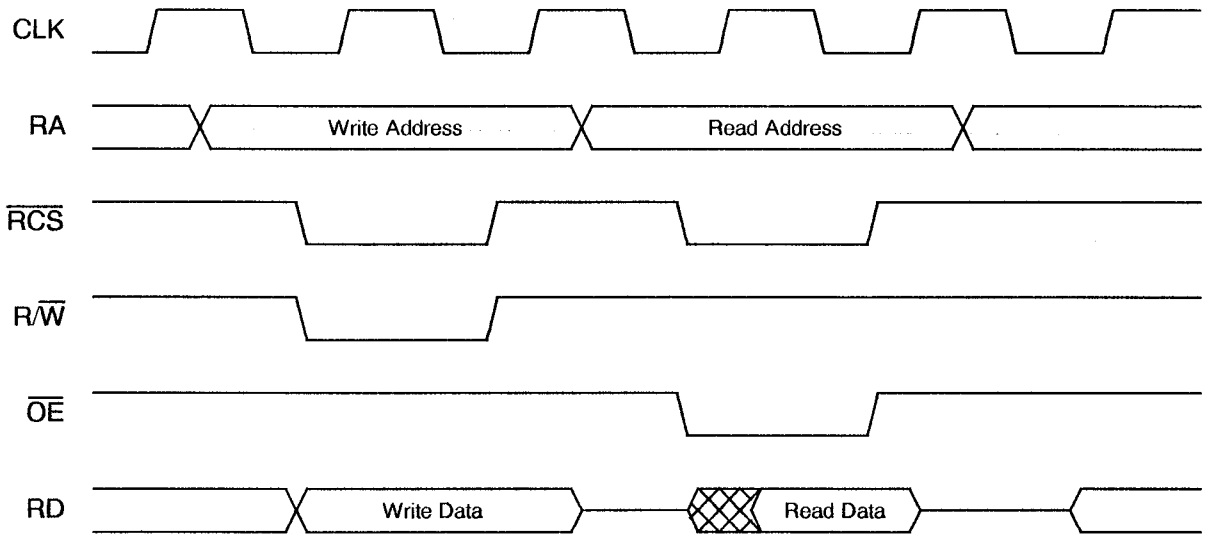
SCLK is asynchronous and thus need not be correlated to the CLK, except for the maximum input data transfer rate (one octet per four CLK cycles).

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

STORAGE OF DATA IN EXTERNAL RAM

The VCA interfaces to an external 8k × 8 static RAM to store PVCF data until the VCM requests it. The VCA RAM interface is shown in Figure III. The interface timing ensures that no bus collisions occur due to the VCA and RAM driving output data at the same time and this also applies for consecutive read and write cycles. The VCA can be used with RAMs such as MA9264 from GEC Plessey Semiconductors and HM65664 from Matra MHS, among others.

FIGURE III - RAM INTERFACE TIMING



The VCA is capable of storing a variable number of PVCFs, ranging from 7 of the maximum length PVCFs to 36 of minimum length. Table I shows the relationship between the Transfer Frame length and the maximum number of PVCFs that can be stored.

TABLE I - TRANSFER FRAME LENGTH VERSUS MAXIMUM NUMBER OF PVCFs STORED

TRANSFER FRAME LENGTH	MAXIMUM NUMBER OF PVFCs THAT CAN BE STORED
223	36
446	18
892	9
1115	7

The VCA generates the RAM address (RA0 - RA12), the Chip Select ($\overline{RCS}$), the Read/Write strobe (R/$\overline{W}$) and the Output Enable ($\overline{OE}$). Data is transferred to and from the RAM over the bidirectional data bus (RD0 - RD7). The duration of the read and write cycles generated by the VCA is two CLK cycles. When the VCA does not access the RAM, the RD data bus is still driven to ensure that the bus is not left floating.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

Once a PVCF transfer to the VCM has started, the VCA continues to output the PVCF data without interruption. Therefore, during the output of a PVCF to the VCM, the VCA reads PVCF data from the RAM once every eight CLK cycles (BITCLK cycles, when CLKMODE = "1").

The maximum input data rate is one octet every four CLK cycles, and thus the VCA may be required to write input data to the RAM once every four CLK cycles. In addition, Transfer Frame Header data and Idle Telemetry Packets are written to the RAM without disturbing the above RAM accesses.

VIRTUAL CHANNEL FRAME COUNTER

To verify that all Virtual Channel Frames have been received and in the correct order, the VCA has a 32 bit wrap-around Virtual Channel Frame Counter, which is incremented for each PVCF, normal and idle.

The VCA assigns the eight LSBs of the Virtual Channel Frame Counter to the Virtual Channel Frame Count field in the Primary Header. When the Secondary Header is present (SECHEAD = "1") the VCA assigns the 24 MSBs of the Virtual Channel Frame Counter to the Secondary Header Data field.

MSB	32-bit Virtual Channel Frame Counter				LSB
0			23	24	31
MSB	Secondary Header Data	LSB	MSB	VC Frame Count	LSB
0		23	0		7

FIRST HEADER POINTER

The First Header Pointer is required for the Telemetry Packet chaining process during Telemetry Packet de-multiplexing at the ground (Earth). The VCA generates partial Transfer Frames in one of two possible states; active or idle, as defined in RD1. The data contained in an active Transfer Frame can be either Telemetry Packets (SYNCF = "0") or non-packet data delimited into data blocks (SYNCF = "1"). Telemetry Packets are referred to as synchronous data in RD1 whereas non-packet data is referred to as asynchronous data.

In the active state, Telemetry Packets may be of varying lengths. It is unlikely that an integer number of Telemetry Packets will be exactly contained within a Transfer Frame, so some Telemetry Packets will be split between two Transfer Frames. The VCA calculates the position of the first octet of the first Telemetry Packet to be placed in each Transfer Frame, in accordance with RD1, then inserts this value into the header of the PVCF.

For the VCA, the above also applies to non-packet data, allowing data blocks to be identified in the data stream. This is an extension to RD1, permitting the First Header Pointer also to be set for non-packet data in the same way as it is set for Telemetry Packets. This feature is activated by using the $\overline{\text{VPD}}$ signal for the parallel interface (SVALID signal for the serial interface) to delimit data blocks, in the same way as for delimiting Telemetry Packets. For serial input mode, SVALID has the same functions as $\overline{\text{VPD}}$ in parallel input mode.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

The First Header Pointer is initiated to "all ones" at reset, allowing the VCA to operate in full compliance with RD1 for non-packet data by permanently connecting $\overline{VPD}$ to logic "0" (SVALID to logic "1" when SMODE = "1"). This means that when using Telemetry Packets (or when using the First Header Pointer for non-packet data), the $\overline{VPD}$ input should be held at logic "1" (SVALID at logic "0" when SMODE = "1") until six CLK cycles after $\overline{RESET}$ has been disabled, to be disabled before writing the first Telemetry Packet or data block. Otherwise the First Header Pointer for the first transmitted non-Idle Transfer Frame after reset would have the First Header Pointer set to "all ones" instead of "all zeros".

IF $\overline{VPD}$ (SVALID when SMODE = "1") was not disabled while all the data filling up a Transfer Frame was input, e.g. if a Telemetry Packet or data block is longer than the data field of the Transfer Frame, the First Header Pointer is set to "all ones"; First Header Pointer = "11111111111".

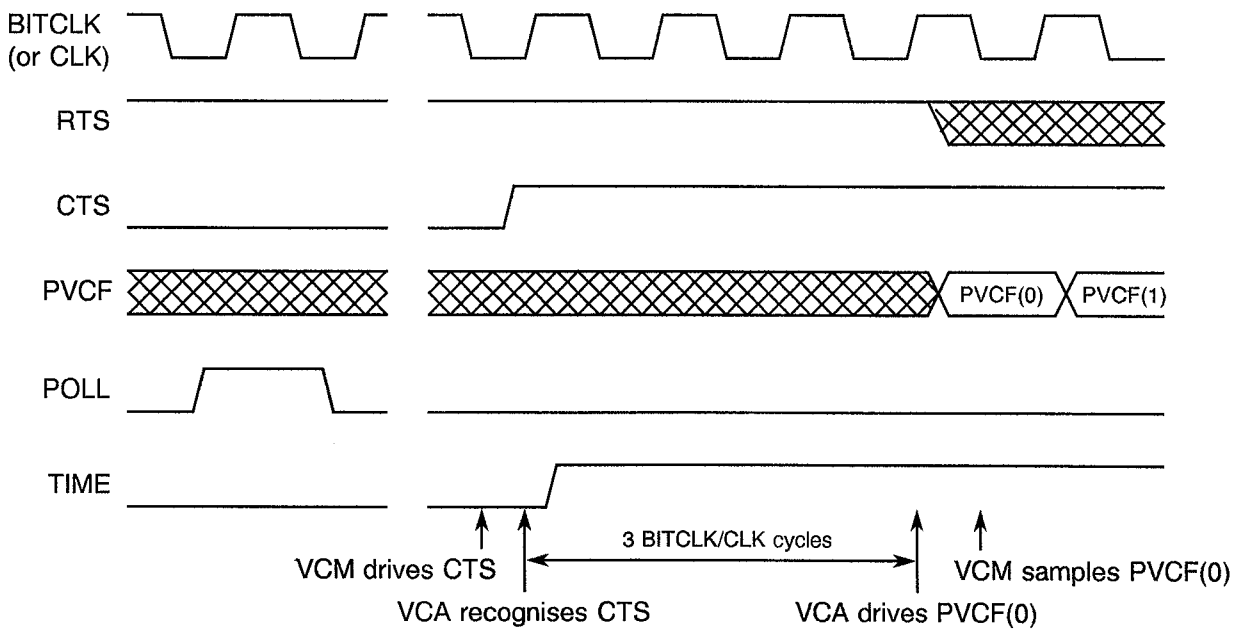
In the idle state, the VCA sends a partial Idle Transfer Frame and the First Header Pointer is set to the predefined Idle First Header Pointer code. This code is the same both for Telemetry Packets and non-packet data; First Header Pointer = "11111111110".

The VCA fully supports the First Header Pointer and has therefore no requirements on aligning the data with the Transfer Frame boundary, contrary to other implementations.

VCA/VCM INTERFACE

The VCA/VCM interface, shown in Figure IV, is for the serial transfer of partial Transfer Frames to the VCM. The VCA relates its operations to the rising CLK edge (rising BITCLK edge, when CLKMODE = "1"), whereas the VCM relates its operations to the falling BITCLK edge, to minimise potential skew problems. The VCA has a Clear To Send (CTS) and a device POLLed (POLL) input, and a Ready To Send (RTS) and a Partial Virtual Channel Frame data (PVCF) output.

FIGURE IV - TIMING OF VCA/VCM INTERFACE



NOTES

1. The RTS signal will stay asserted if there are more PVCFs available.
2. If there are no more PVCFs the RTS signal will be de-asserted.
3. PVCF(1) = Bit 1 of PVCF.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

The VCA/VCM interface can operate relative to the BITCLK signal for bit rates up to 3MBit/s or relative to the CLK signal for bit rates up to 12.5MBit/s. When CLKMODE = "0", the VCA/VCM interface uses the CLK signal; when CLKMODE = "1", the interface uses the asynchronous BITCLK signal. BITCLK is then sampled internally by the VCA generating an internal enable signal when the rising BITCLK edge is detected. This signal enables the interface signals (RTS, POLL, CTS, PVCF) to be sampled/driven during the next CLK cycle.

Using the BITCLK signal enables the VCA to operate at a higher clock frequency than the VCM, allowing a bit rate independent of input data rate. In addition, the RAM power dissipation might decrease due to the chip select being enabled for a shorter time, depending on the RAM device used.

The VCA enables the output signal RTS when it has stored a complete PVCF in RAM. RTS will remain enabled as long as there is one or more complete PVCFs in RAM, excluding a PVCF currently being output. When the VCM is ready to receive data from the VCA, it enables the CTS signal. Three CLK (or BITCLK) cycles after the VCA has detected the enabled CTS input, it will start to output PVCF data. The PVCF data is output at the rate of one bit per CLK (or BITCLK) cycle without interrupt until the complete PVCF has been output. The CTS input shall be enabled for a minimum of 16 CLK cycles, and it shall be disabled before the end of the PVCF.

If the VCM enables the CTS signal when the VCA has not enabled RTS, the VCA outputs an Idle PVCF.

IDLE TRANSFER TIMES

An Idle PVCF, which will be finalised into an Idle Transfer Frame by the VCM, will be produced when the VCA has not stored a complete PVCF in RAM, when CTS is enabled. Idle PVCFs are not stored in RAM but generated while being output. The timing and the length of an Idle PVCF is identical to a normal PVCF. Idle Transfer Frames should not be confused with Idle Telemetry Packets.

The Idle PVCF Data Field contains no useful data. It will be filled with data from the Idle Fill data input (IFILL). One bit per CLK cycle (BITCLK cycle, when CLKMODE = "1") is sampled and used for Idle PVCF data.

IDLE TELEMETRY PACKET INSERTION

The VCA can optionally generate and insert Idle Telemetry Packets, to fill up an incomplete Transfer Frame. This ensures that Telemetry Packets do not remain inaccessible due to an incomplete Transfer Frame being resident in the RAM. This feature is only available when the VCA is operating with Telemetry Packets, referred to as synchronous data in RD1. Idle Telemetry Packets should not be confused with Idle Transfer Frames.

The Idle Telemetry Packet insertion process starts when all of the following conditions are met:

- The VCA operates with Telemetry Packets (SYNCF = "0").
- The source is not sending a Telemetry Packet ($\overline{\text{VPD}}$ = "1" or SVALID = "0", respectively).
- The VCA is not Ready To Send data (RTS = "0").
- An incomplete PVCF (containing non-Idle Telemetry Packets or part of a non-Idle Telemetry Packet) is resident in the external RAM.
- The value of the Poll Programme inputs, PPROG0 to PPROG2, is not equal to "111".
- The appropriate number of device polls have been counted by the Poll Counter.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

When the Idle Telemetry Packet insertion process has filled the PVCF, the VCA enables the RTS output. The Idle Telemetry Packet insertion process stops after the last Idle Telemetry Packet has been stored in the RAM. In the case that the last Idle Telemetry Packet spilled over, it will be written to the next PVCF. The time required for the VCA to complete a PVCF with Idle Telemetry Packets depends on how much space there is left to be filled. The worst case is when the longest possible data field in a Transfer Frame of 1115 octets contains only one octet of Telemetry Packet data, which will take less than 12 000 CLK cycles to complete the PVCF data field.

Should $\overline{\text{VPD}}$ (SVALID when SMODE = "1") be enabled after the Idle Telemetry Packet insertion process has started, the current Idle Telemetry Packet is completed in parallel with the storing of Telemetry Packet data and then the Idle Telemetry Packet insertion process is suspended. As soon as $\overline{\text{VPD}}$ (SVALID) is disabled, indicating the end of the normal Telemetry Packet, the Idle Telemetry Packet insertion process resumes and continues until the PVCF has been completed (it will not stop due to a new Telemetry Packet being received) unless the PVCF was already completely filled with normal Telemetry Packets.

The VCA is able to receive Telemetry Packets and send PVCFs simultaneously with the insertion of an Idle Telemetry Packet.

When a Transfer Frame contains no Telemetry packets or when it contains only part of an Idle Telemetry Packet, the Idle Telemetry Packet insertion process will not start. The situation where a PVCF contains only part of an Idle Telemetry Packet occurs when an Idle Packet spilled over from the previous Transfer Frame and it is the only data in the Transfer Frame.

POLL COUNTER

In the previous section, six conditions were listed for the Idle Telemetry Packet insertion process to commence. When the VCA detects that the first five conditions are met, it enables the Poll Counter. The Poll Counter is reset and disabled when either of the following conditions is met:

- The source asserts $\overline{\text{VPD}}$ or SVALID in preparation for sending Telemetry Packets, OR
- The Idle Telemetry Packet insertion process is active.

When the Poll Counter is enabled, it increments by one at every rising CLK edge (rising BITCLK edge, when CLKMODE = "1") when the POLL input is enabled. The VCM asserts POLL every time it checks the RTS signal of the VCA, while selecting which VCA to output the next PVCF. The Poll Counter increments until it reaches the number of programmed polls, ranging from 1 to 1024, as indicated by the value of PPROG0 to PPROG2 and then it enables the Idle Telemetry Packet insertion process.

The Poll Counter is enabled when:

- (SYNCF = "0") AND,
- ($\overline{\text{VPD}}$ = "1") or SVALID = "0", respectively) AND,
- (RTS = "0") AND,
- ("000" < PPROG[0...2] < "111") AND,
- (The incomplete PVCF contains non-Idle Telemetry Packet data) AND,
- (The Idle Telemetry Packet insertion process is not active),

otherwise the Poll Counter is reset and disabled.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

The Poll Counter is incremented by one at every rising CLK edge (rising BITCLK edge, when CLKMODE = "1") when:

- (Poll Counter enabled) AND (POLL = "1").

The Idle Telemetry Packet insertion process starts when:

- [(POLL Counter enabled) AND,
- (POLL Counter = Threshold value as defined in Table II)] OR,
- [(PPROG[0...2] = "000") AND,
- (SYNCF = "0") AND,
- ($\overline{VPD}$ = "1") AND,
- (RTS = "0") AND,
- (The incomplete PVCF contains non-Idle Telemetry Packet data)).]

The Idle Telemetry Packet insertion process stops when:

- The PVCF is complete and the remainder of the last Idle Telemetry Packet has been stored in the next PVCF, if the Idle Telemetry Packet spills over from the last PVCF.

The relationship between the signals POLL and $\overline{VPD}$ or SVALID has to allow for internal synchronisation of the signals in the VCA.

TABLE II - POLL COUNTER THRESHOLD

PPROG2	PPROG1	PPROG0	Poll Counter Threshold
0	0	0	Immediate Idle Telemetry Packet Insertion (1)
0	0	1	1 device poll
0	1	0	4 device polls
0	1	1	16 device polls
1	0	0	64 device polls
1	0	1	256 device polls
1	1	0	1024 device polls
1	1	1	Idle Telemetry Packet insertion process will not be started

NOTES

1. Idle Telemetry Packet insertion process starts when all relevant conditions are met.

IDLE TELEMETRY PACKET

The VCA generates the Idle Telemetry Packet Header and inserts the pre-defined values into the appropriate fields.

The data field of an Idle Telemetry Packet is filled with data from the Idle Fill data input (IFILL). One bit per CLK cycle is sampled and used for Idle Telemetry Packet data.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

PSEUDO-RANDOM IDLE FILL DATA

The Pseudo-random Idle Fill data is generated to provide fill data for the data fields of Idle Telemetry Packets and Idle PVCFs. The pseudo-random data generator generates the RANDOM output signal, which can be connected to the Idle Fill data input pin (IFILL). The data output rate is one bit per CLK cycle. The pseudo-random Data generator is free-running, and will not be initialised by any event except reset ($\overline{\text{RESET}}$ = "0"). The pseudo-random data generator polynomial is $x^9 + x^5 + 1$.

The design of the generator ensures that a Single Event Upset (SEU) or any other spurious event will not cause the generator to jump to an invalid state and produce a continuous output of ones or zeros.

TIME SAMPLING STROBE

The VCA provides the active high TIME strobe for sampling the on-board time according to Section 7.4 of RD1. TIME is enabled one CLK cycle (two CLK cycles after the rising BITCLK edge, when CLKMODE = "1") after CTS has been asserted, when the eight LSBs of the Virtual Channel Frame Counter for the partial Transfer Frame to be sent out contain the value(s) selected by the four TMODE pins. This allows all intervals defined in RD1 to be selected. TIME will remain asserted for 128 CLK cycles, regardless of the CLKMODE value.

This means that the TIME strobe will be enabled 51 CLK cycles (51 BITCLK plus two CLK cycles after the rising BITCLK edge, when CLKMODE = "1") after the leading edge of the Synchronisation Marker has been output from the VCM. This can be regarded as compliant with the requirements of RD1 since the delay relative to the rising edge of the first bit of the Synchronisation Marker is fixed and known.

If it nevertheless is required to sample the on-board time exactly at the rising edge of the Synchronisation Marker, the time can be sampled at this edge for every Transfer Frame generated but only read out when the TIME strobe is asserted.

The TIME strobe from the VCA associated with Virtual Channel 0 should be used for sampling the on-board spacecraft time.

TEST

The VCA features Built-in Self Test (BIST) with a fault coverage of 89.5%. The BIST runs for 4996 CLK cycles after $\overline{\text{RESET}}$ has been released. The BIST result does not depend on the state of any of the inputs. The BIST can be disabled by connecting the TEST0 input to logic "1"; after releasing $\overline{\text{RESET}}$, the VCA will be reset but no BIST will be performed.

If an error is detected by the BIST, the $\overline{\text{ERR}}$ output remains enabled ($\overline{\text{ERR}}$ = "0"), until the next reset occurs. The VCA will try to continue to operate in normal mode. If no internal error was detected, the $\overline{\text{ERR}}$ output is disabled, and the VCA starts working in normal mode.

When $\overline{\text{RESET}}$ is enabled and during BIST, the $\overline{\text{RCS}}$, $\overline{\text{OE}}$ and R/$\overline{\text{W}}$ outputs are driven to logic "1" and all other outputs except RANDOM are driven to logic "0" so as not to trigger connected devices. The RD data bus is driven to logic "0" to ensure that it is not left floating. Due to design reasons, the RANDOM pin outputs pseudo-random data also during BIST.

FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

The active high input External Ram Test (ERT) can be used to 3-state all outputs from the VCA to the external RAM, to allow for RAM test. When ERT is enabled the outputs $\overline{ERR}$, VCAR and RTS are held at logic "0" since the VCA can no longer control the RAM. When ERT is disabled, control of the RAM interface, VCAR, $\overline{RTS}$ and $\overline{ERR}$ is returned to the VCA. ERT is asynchronous and only disables the outputs, without any other impact on the VCA.

The production test for the VCA has a fault coverage higher then 96%, and is performed at a CLK frequency of 10MHz. The TEST1 input is used for the production test and shall be tied to logic "0" during normal operation.

The fault coverage figures are based on stuck-at-0/1 faults at the gate level, faulting all nets (gate outputs).

STATE AFTER RESET

After reset, or after reset and completion of BIST, the VCA is initialised as follows:

- The Virtual Channel Frame Counter has the value 0.
- The First Header Pointer is initialised to "all ones".
- The Poll Counter has the value 0.

Since the VCA BIST takes fewer CLK cycles than the VCM BIST, the VCA will always be ready when the VCM requires the first Transfer Frame (except for the unrealistic case when the VCA performs BIST and the VCM does not).

FIGURE 3(d) - FUNCTIONAL DIAGRAM

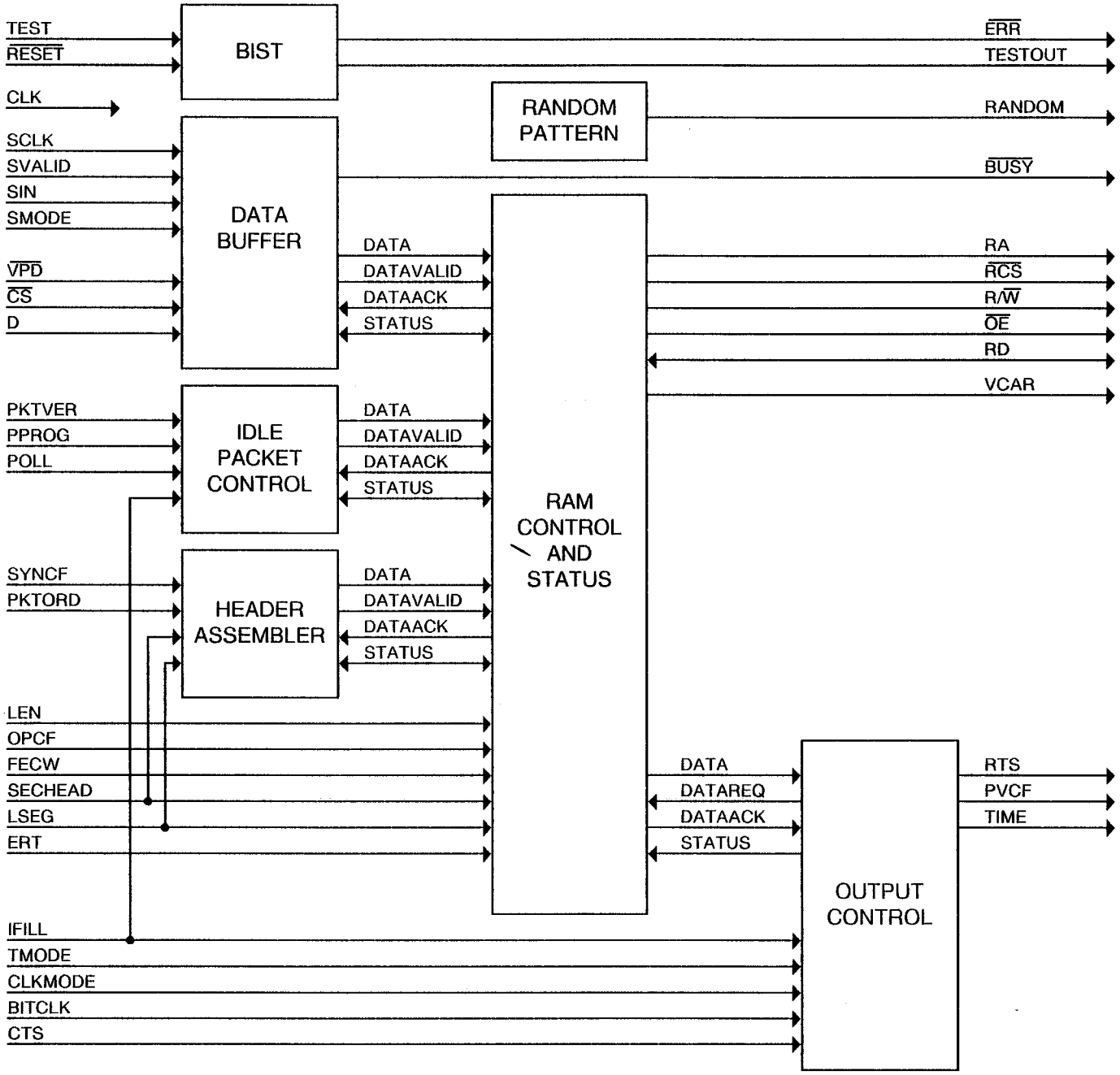
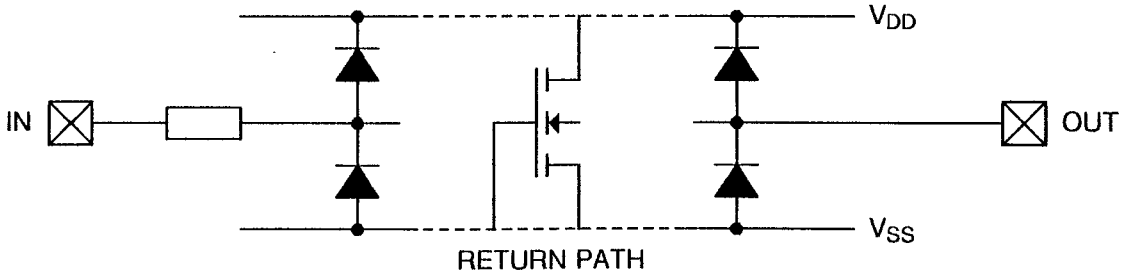


FIGURE 3(e) - INPUT/OUTPUT PROTECTION NETWORKS



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

(c) ESA PSS-04-106, Packet Telemetry Standard.

(d) ESA PSS-04-107, Packet Telecommand Standard.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviation is used:-

V_{IC} - Input/Output Clamp Voltage.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

(a) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during qualification and maintenance of qualification.

(b) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during procurement on a lot acceptance basis at the total dose irradiation level specified in the Purchase Order.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

(a) Para. 7.1.1(a), "High Temperature Reverse Bias" test and subsequent electrical measurements related to this test shall be omitted.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 5.0 grammes.

4.3.3 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESA/SCC Basic Specification No. 9000. The test conditions shall be as follows:-

Applied Force: 1.0 ± 0.1 Newtons, 3 bends at 45°.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body and the lids shall be pre-form soldered.

4.4.2 Lead Material and Finish

The material shall be Type 'D' with Type '2' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

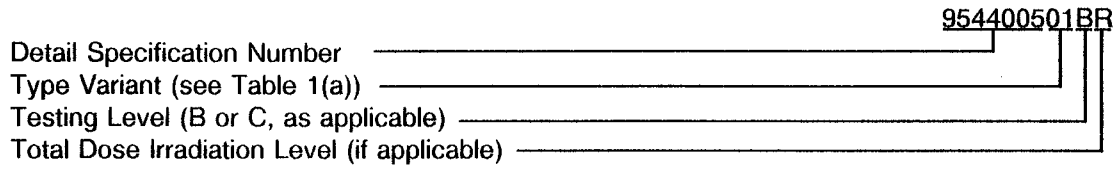
(c) Traceability Information.

4.5.2 Lead Identification

An index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



The Total Dose Irradiation Level designation shall be added for those devices for which a sample has been successfully tested to the level in question. For these devices, a code shall be added in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ °C and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for H.T.R.B. Burn-in

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for Power Burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for Power Burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for H.T.R.B. Burn-in

Not applicable.

4.7.5 Electrical Circuits for Power Burn-in

A circuit for use in performing the Power Burn-in test is shown in Figure 5(b) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
1 to 8	V_{SS} and V_{DD} Continuity	-	-	4(a)	I_{OUT} = 10µA V_{DD} = V_{SS} = 0V (Pins 1-4-21-22-39-48-57-74 to 64 + 65)	-	100	mV
9	Functional Test 1 (Basic)	-	3014	-	Verify Device Operation with Load V_{IL} = 0V, V_{IH} = 5.0V V_{OL} = 1.0V, V_{OH} = 4.0V I_{OUT} = ± 2.0mA C_L = 100pF ± 20% V_{DD} = 5.0V, V_{SS} = 0V Pattern = Note 1	-	-	-
10	Functional Test 2 (Nominal Voltage)	-	3014	-	Verify Device Operation with Load V_{IL}, V_{IH} = Note 2 V_{OL} = 1.0V, V_{OH} = 4.0V I_{OUT} = ± 2.0mA C_L = 100pF ± 20% V_{DD} = 5.0V, V_{SS} = 0V Pattern = Note 2	-	-	-
11	Functional Test 3 (High Voltage)	-	3014	-	Verify Device Operation with Load V_{IL}, V_{IH} = Note 2 V_{OL} = 1.0V, V_{OH} = 4.5V I_{OUT} = ± 2.0mA C_L = 100pF ± 20% V_{DD} = 5.5V, V_{SS} = 0V Pattern = Note 2	-	-	-
12	Functional Test 4 (Low Voltage)	-	3014	-	Verify Device Operation with Load V_{IL}, V_{IH} = Note 2 V_{OL} = 1.0V, V_{OH} = 3.5V I_{OUT} = ± 2.0mA C_L = 100pF ± 20% V_{DD} = 4.5V, V_{SS} = 0V Pattern = Note 2	-	-	-
13	Quiescent Current	I_{DD}	3005	4(b)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V All Outputs Open Note 3 (Pins 1 + 21 + 48 + 65)	-	0.5	mA

NOTES: See Page 34.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
14 to 54	Input Current Low Level	I_{IL}	3009	4(c)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-3-5-8-9-10-11-12-13-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49-78-79-80-81-82-83-84)	-	− 1.0	µA
55 to 95	Input Current High Level	I_{IH}	3009	4(d)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-3-5-8-9-10-11-12-13-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49-78-79-80-81-82-83-84)	-	1.0	µA
96 to 127	Output Voltage Low Level	V_{OL}	3007	4(e)	V_{IL}, V_{IH} = Note 2 I_{OL} = 4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 6-7-15-33-40-41-44-45-50-51-52-53-54-55-56-58-59-60-61-62-63-66-67-68-69-70-71-72-73-75-76-77)	-	0.4	V
128 to 159	Output Voltage High Level 1	V_{OH1}	3006	4(f)	V_{IL}, V_{IH} = Note 2 I_{OL} = − 4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 6-7-15-33-40-41-44-45-50-51-52-53-54-55-56-58-59-60-61-62-63-66-67-68-69-70-71-72-73-75-76-77)	3.9	-	V
160 to 191	Output Voltage High Level 2	V_{OH2}	3006	4(f)	V_{IL}, V_{IH} = Note 2 I_{OL} = − 0.5mA V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 6-7-15-33-40-41-44-45-50-51-52-53-54-55-56-58-59-60-61-62-63-66-67-68-69-70-71-72-73-75-76-77)	4.2	-	V

NOTES: See Page 34.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
192 to 209	Threshold Voltage Low Level 1 (TTL Inputs)	V_{THN1}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 2-3-5-50-51-52-53-54-55-56-59-78-79-80-81-82-83-84)	0.8	-	V
210 to 227	Threshold Voltage High Level 1 (TTL Inputs)	V_{THP1}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 2-3-5-50-51-52-53-54-55-56-59-78-79-80-81-82-83-84)	-	2.0	V
228 to 257	Threshold Voltage Low Level 2 (CMOS Inputs)	V_{THN2}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 8-9-10-11-13-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49)	1.3	-	V
258 to 287	Threshold Voltage High Level 2 (CMOS Inputs)	V_{THP2}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 8-9-10-11-13-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49)	-	3.2	V
288	Threshold Voltage Low Level 3 (SCHMITT Trigger Input)	V_{THN3}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pin 12)	1.0	2.8	V
289	Threshold Voltage High Level 3 (SCHMITT Trigger Input)	V_{THP3}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pin 12)	1.5	3.3	V
290	Hysteresis Voltage	V_H	-	4(h)	V_{DD} = 4.5V, V_{SS} = 0V Note 5 (Pin 12)	0.5	-	V
291 to 308	Threshold Voltage Low Level 4 (TTL Inputs)	V_{THN4}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-3-5-50-51-52-53-54-55-56-59-78-79-80-81-82-83-84)	0.8	-	V
309 to 326	Threshold Voltage High Level 4 (TTL Inputs)	V_{THP4}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-3-5-50-51-52-53-54-55-56-59-78-79-80-81-82-83-84)	-	2.0	V

NOTES: See Page 34.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
327 to 366	Threshold Voltage Low Level 5 (CMOS Inputs)	V_{THN5}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 8-9-10-11-13-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49)	1.7	-	V
367 to 396	Threshold Voltage High Level 5 (CMOS Inputs)	V_{THP5}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 8-9-10-11-13-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49)	-	3.9	V
397	Threshold Voltage Low Level 6 (SCHMITT Trigger Input)	V_{THN6}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pin 12)	1.2	3.8	V
398	Threshold Voltage High Level 6 (SCHMITT Trigger Input)	V_{THP6}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pin 12)	1.7	4.3	V
399 to 471	Input/Output Clamp Voltage (to V_{SS})	V_{IC1}	3022	4(i)	I_{IN} = − 100µA V_{DD} = V_{SS} = 0V (Pins 2-3-5-6-7-8-9-10-11-12-13-15-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-33-34-35-36-37-38-40-41-42-43-44-45-46-47-49-50-51-52-53-54-55-56-58-59-60-61-62-63-66-67-68-69-70-71-72-73-75-76-77-78-79-80-81-82-83-84)	-	−2.0	V
472 to 544	Input/Output Clamp Voltage (to V_{DD})	V_{IC2}	3022	4(i)	I_{IN} = 100µA V_{DD} = V_{SS} = 0V (Pins 2-3-5-6-7-8-9-10-11-12-13-15-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-33-34-35-36-37-38-40-41-42-43-44-45-46-47-49-50-51-52-53-54-55-56-58-59-60-61-62-63-66-67-68-69-70-71-72-73-75-76-77-78-79-80-81-82-83-84)	-	2.0	V

NOTES: See Page 34.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
545 to 552	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	3006	4(j)	V_{IN} (3-State Control) = Note 6 V_{OUT} = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 50-51-52-53-54-55-56-59)	-	−10	µA
553 to 560	Output Leakage Current Third State (High Level Applied)	I_{OZH}	3006	4(j)	V_{IN} (3-State Control) = Note 6 V_{OUT} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 50-51-52-53-54-55-56-59)	-	10	µA
561	Supply Current 1 (During BIST)	I_{DDS1}	3005	4(b)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V f = 12.5MHz (Note 7)	-	55	mA
562	Supply Current 2 (During Normal Operation)	I_{DDS2}	3005	4(b)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V f = 12.5MHz (Note 8)	-	45	mA

NOTES

1. During Functional Test 1:-

   busy = 1.0MHz, cslong = 1.25MHz, csshort = 1.25MHz, ert = 1.25MHz, poclk = 1.25MHz, poll = 1.25MHz, psft = 1.25MHz, s01 = 2.0MHz, sclkh = 1.25MHz, sclkl = 1.25MHz, slft = 1.25MHz, t1103 = 1.25MHz, t207 = 1.25MHz.

2. During Functional Tests 2, 3 and 4:-

   Functional Test 2: V_{IL} = 0.5V, V_{IH} = 4.5V,
   Functional Test 3: V_{IL} = 0.5V, V_{IH} = 5.0V,
   Functional Test 4: V_{IL} = 0.5V, V_{IH} = 4.0V,

   busy = 10MHz, cslong = 12.5MHz, csshort = 12.5MHz, ert = 12.5MHz, poclk = 12.5MHz, poll = 12.5MHz, psft = 12.5MHz, s01 = 20MHz, sclkh = 12.5MHz, sclkl = 12.5MHz, slft = 12.5MHz, t1103 = 12.5MHz, t207 = 12.5MHz.

3. Measurement is performed with the device having been initialised using functional test pattern POLL, stopped at test vector 7. Total combined current for all V_{DD} Pins.
4. The output pin under test is configured into correct state for the measurement by using a functional test pattern on the inputs which produces a low or high at the pin, as appropriate.
5. Hysteresis is a calculated value from measurements for each pin from $V_{THP3} - V_{THN3} = V_H$.
6. The device is configured using a functional test pattern so that the pin under test is in the Third-State condition for the measurement. The measurement includes the input currents I_{IL} and I_{IH}.
7. Test vectors 0 to 4990 of functional test pattern slft are used for measurement of I_{DDS1}.
8. Test vectors 0 to 8236 of functional test pattern t1103 are used for measurement of I_{DDS2}.
9. Guaranteed but not tested. Characterised after major process changes.
10. Parameters tested go-no-go during Functional Tests 2, 3 and 4.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
563 to 601	Input Capacitance 1	C_{IN1}	3012	4(k)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 9 (Pins 2-3-5-8-9-10-11-12-13-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49-50-51-52-53-54-55-56-59-78-79-80-81-82-83-84)	-	5.0	pF
602	Input Capacitance 2	C_{IN2}	3012	4(k)	V_{IN} (Not Under Test) = 0V $V_{DD} = V_{SS} = 0V$ Note 9 (Pin 13)	-	15	pF
603 to 605	Rise and Fall Time (TTL and CMOS Inputs)	t_r1/t_f1	3004	-	Note 9	-	100	ns
606 to 608	Rise and Fall Time (SCHMITT Trigger Input)	t_r2/t_f2	3004	-	Note 9	-	1.0	µs
609 to 611	$\overline{\text{RESET}}$ Activated	t_{RES}	3003	-	Note 10	$4t_{BCK}$	-	-
612 to 614	Clock Period for CLK	t_{CLK}	3003	-	Note 10	80	-	ns
615 to 617	Clock Low Pulse Width for CLK	t_{CLO}	3003	-	Note 10	40	-	ns
618 to 620	Clock High Pulse Width for CLK	t_{CHI}	3003	-	Note 10	40	-	ns
621 to 623	Clock Period for BITCLK	t_{BCK}	3003	-	Note 10	$4t_{CLK}$	-	-
624 to 626	Clock Low Pulse Width for BITCLK	t_{BLO}	3003	-	Note 10	$4t_{CLO}$	-	-
627 to 629	Clock High Pulse Width for BITCLK	t_{BHI}	3003	-	Note 10	$4t_{CHI}$	-	-

NOTES: See Page 34.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
630 to 632	Clock Period for SCLK	t_{SCK}	3003	-	Note 10	$t_{CLK}/2$	-	-
633 to 635	Clock Low Pulse Width for SCLK	t_{SLO}	3003	-	Note 10	20	-	ns
636 to 638	Clock High Pulse Width for SCLK	t_{SHI}	3003	-	Note 10	20	-	ns
639 to 641	$\overline{CS}$ Cycle Time	t_1	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	$4t_{CLK}$	-	-
642 to 644	$\overline{VPD}$ Active to $\overline{CS}$ Active	t_2	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	5.0	-	ns
645 to 647	$\overline{CS}$ Pulse Width Activated	t_3	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	30	-	ns
648 to 650	$\overline{CS}$ Pulse Width De-activated	t_4	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	30	-	ns
651 to 653	$\overline{CS}$ De-activated to $\overline{VPD}$ De-activated	t_5	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	0	-	ns
654 to 656	$\overline{VPD}$ Pulse Width De-activated	t_6	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	$2t_{CLK}$	-	-
657 to 659	D Setup Time	t_7	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	8.0	-	ns
660 to 662	D Hold Time	t_8	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	15	-	ns
663 to 665	$\overline{CS}$ De-activated to $\overline{BUSY}$ Activated	t_9	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	-	50	ns

NOTES: See Page 34.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
666 to 668	$\overline{BUSY}$ Pulse Width Activated	t_{10}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	$3t_{CLK}$	$4t_{CLK}$	-
669 to 671	$\overline{CS}$ De-activated to VCAR De-activated	t_{11}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	2.5 t_{CLK}	3.5 t_{CLK}	-
672 to 674	CLK Low to VCAR Valid	t_{12}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	50	ns
675 to 677	ERT High to VCAR Low	t_{13}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	50	ns
678 to 680	ERT Low to VCAR Valid	t_{14}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	50	ns
681 to 683	SVALID High to SCLK High	t_{15}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	50	-	ns
684 to 686	SCLK High to SVALID Low	t_{16}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	50	-	ns
687 to 689	SVALID Pulse Width De-activated	t_{17}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	$2t_{CLK}$	-	-
690 to 692	SIN Setup Time	t_{18}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	5.0	-	ns
693 to 695	SIN Hold Time	t_{19}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	15	-	ns
696 to 698	CLK High to RA Valid	t_{20}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	50	ns
699 to 701	CLK Low to $\overline{RCS}$ Valid	t_{21}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	52	ns

NOTES: See Page 34.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
702 to 704	CLK Low to R/$\overline{W}$ Low	t_{22}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	52	ns
705 to 707	CLK Low to R/$\overline{W}$ High	t_{23}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	52	ns
708 to 710	CLK Low to $\overline{OE}$ Low	t_{24}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	52	ns
711 to 713	CLK Low to $\overline{OE}$ High	t_{25}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	52	ns
714 to 716	CLK Low to RD Write Data Valid	t_{26}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	56	ns
717 to 719	CLK High to RD 3-State	t_{27}	3003	-	I_{OUT} ±5.0mA C_L = 100pF ± 20% Note 10	-	40	ns
720 to 722	Read Data Setup Time	t_{28}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	19	-	ns
723 to 725	$\overline{OE}$/$\overline{RCS}$ High to RD Invalid	t_{29}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	0	-	ns
726 to 728	ERT High to RA, $\overline{RCS}$, R/$\overline{W}$, $\overline{OE}$, RD 3-State	t_{30}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	30	ns
729 to 731	ERT Low to RA, $\overline{RCS}$, R/$\overline{W}$, $\overline{OE}$, RD Valid	t_{31}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	30	ns
732 to 734	CLK Low to $\overline{ERR}$ Valid	t_{32}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	50	ns
735 to 737	ERT High to $\overline{ERR}$ Low	t_{33}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	43	ns
738 to 740	ERT Low to $\overline{ERR}$ Valid	t_{34}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	43	ns

NOTES: See Page 34.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
741 to 743	ERT High to RTS Low	t_{35}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	39	ns
744 to 746	ERT Low to RTS Valid	t_{36}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	39	ns
747 to 749	CLK High to RTS Stable	t_{37}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	52	ns
750 to 752	CTS Setup Time	t_{38}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	6.0	-	ns
753 to 755	CLK High to PVCF Stable	t_{39}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	48	ns
756 to 758	POLL Setup Time	t_{40}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	5.0	-	ns
759 to 761	POLL Hold Time	t_{41}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	10	-	ns
762 to 764	CLK High to TIME Active	t_{42}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	50	ns
765 to 767	CLK High to RANDOM Valid	t_{43}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	50	ns
768 to 770	IFILL Setup Time	t_{44}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	10	-	ns
771 to 773	IFILL Hold Time	t_{45}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	5.0	-	ns

NOTES: See Page 34.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
9	Functional Test 1 (Basic)	-	3014	-	Verify Device Operation with Load V_{IL} = 0V, V_{IH} = 5.0V V_{OL} = 1.0V, V_{OH} = 4.0V I_{OUT} = ± 2.0mA C_L = 100pF ± 20% V_{DD} = 5.0V, V_{SS} = 0V Pattern = Note 1	-	-	-
10	Functional Test 2 (Nominal Voltage)	-	3014	-	Verify Device Operation with Load V_{IL}, V_{IH} = Note 2 V_{OL} = 1.0V, V_{OH} = 4.0V I_{OUT} = ± 2.0mA C_L = 100pF ± 20% V_{DD} = 5.0V, V_{SS} = 0V Pattern = Note 2	-	-	-
11	Functional Test 3 (High Voltage)	-	3014	-	Verify Device Operation with Load V_{IL}, V_{IH} = Note 2 V_{OL} = 1.0V, V_{OH} = 4.5V I_{OUT} = ± 2.0mA C_L = 100pF ± 20% V_{DD} = 5.5V, V_{SS} = 0V Pattern = Note 2	-	-	-
12	Functional Test 4 (Low Voltage)	-	3014	-	Verify Device Operation with Load V_{IL}, V_{IH} = Note 2 V_{OL} = 1.0V, V_{OH} = 3.5V I_{OUT} = ± 2.0mA C_L = 100pF ± 20% V_{DD} = 4.5V, V_{SS} = 0V Pattern = Note 2	-	-	-
13	Quiescent Current	I_{DD}	3005	4(b)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V All Outputs Open Note 3 (Pins 1 + 21 + 48 + 65)	-	4.5	mA

NOTES: See Page 34.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
14 to 54	Input Current Low Level	I_{IL}	3009	4(c)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-3-5-8-9-10-11-12-13-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49-78-79-80-81-82-83-84)	-	− 1.0	µA
55 to 95	Input Current High Level	I_{IH}	3009	4(d)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-3-5-8-9-10-11-12-13-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49-78-79-80-81-82-83-84)	-	1.0	µA
96 to 127	Output Voltage Low Level	V_{OL}	3007	4(e)	V_{IL}, V_{IH} = Note 2 I_{OL} = 4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 6-7-15-33-40-41-44-45-50-51-52-53-54-55-56-58-59-60-61-62-63-66-67-68-69-70-71-72-73-75-76-77)	-	0.4	V
128 to 159	Output Voltage High Level 1	V_{OH1}	3006	4(f)	V_{IL}, V_{IH} = Note 2 I_{OL} = − 4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 6-7-15-33-40-41-44-45-50-51-52-53-54-55-56-58-59-60-61-62-63-66-67-68-69-70-71-72-73-75-76-77)	3.9	-	V
160 to 191	Output Voltage High Level 2	V_{OH2}	3006	4(f)	V_{IL}, V_{IH} = Note 2 I_{OL} = − 0.5mA V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 6-7-15-33-40-41-44-45-50-51-52-53-54-55-56-58-59-60-61-62-63-66-67-68-69-70-71-72-73-75-76-77)	4.2	-	V

NOTES: See Page 34.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
192 to 209	Threshold Voltage Low Level 1 (TTL Inputs)	V_{THN1}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 2-3-5-50-51-52-53-54-55-56-59-78-79-80-81-82-83-84)	0.8	-	V
210 to 227	Threshold Voltage High Level 1 (TTL Inputs)	V_{THP1}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 2-3-5-50-51-52-53-54-55-56-59-78-79-80-81-82-83-84)	-	2.0	V
228 to 257	Threshold Voltage Low Level 2 (CMOS Inputs)	V_{THN2}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 8-9-10-11-13-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49)	1.3	-	V
258 to 287	Threshold Voltage High Level 2 (CMOS Inputs)	V_{THP2}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 8-9-10-11-13-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49)	-	3.2	V
288	Threshold Voltage Low Level 3 (SCHMITT Trigger Input)	V_{THN3}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pin 12)	1.0	2.8	V
289	Threshold Voltage High Level 3 (SCHMITT Trigger Input)	V_{THP3}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pin 12)	1.5	3.3	V
290	Hysteresis Voltage	V_H	-	4(h)	V_{DD} = 4.5V, V_{SS} = 0V Note 5 (Pins 12)	0.5	-	V
291 to 308	Threshold Voltage Low Level 4 (TTL Inputs)	V_{THN4}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-3-5-50-51-52-53-54-55-56-59-78-79-80-81-82-83-84)	0.8	-	V
309 to 326	Threshold Voltage High Level 4 (TTL Inputs)	V_{THP4}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-3-5-50-51-52-53-54-55-56-59-78-79-80-81-82-83-84)	-	2.0	V

NOTES: See Page 34.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
327 to 366	Threshold Voltage Low Level 5 (CMOS Inputs)	V_{THN5}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 8-9-10-11-13-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49)	1.7	-	V
367 to 396	Threshold Voltage High Level 5 (CMOS Inputs)	V_{THP5}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 8-9-10-11-13-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49)	-	3.9	V
397	Threshold Voltage Low Level 6 (SCHMITT Trigger Input)	V_{THN6}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pin 12)	1.2	3.8	V
398	Threshold Voltage High Level 6 (SCHMITT Trigger Input)	V_{THP6}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pin 12)	1.7	4.3	V
399 to 471	Input/Output Clamp Voltage (to V_{SS})	V_{IC1}	3022	4(i)	I_{IN} = −100µA V_{DD} = V_{SS} = 0V (Pins 2-3-5-6-7-8-9-10-11-12-13-15-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-33-34-35-36-37-38-40-41-42-43-44-45-46-47-49-50-51-52-53-54-55-56-58-59-60-61-62-63-66-67-68-69-70-71-72-73-75-76-77-78-79-80-81-82-83-84)	-	−2.0	V
472 to 544	Input/Output Clamp Voltage (to V_{DD})	V_{IC2}	3022	4(i)	I_{IN} = 100µA V_{DD} = V_{SS} = 0V (Pins 2-3-5-6-7-8-9-10-11-12-13-15-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-33-34-35-36-37-38-40-41-42-43-44-45-46-47-49-50-51-52-53-54-55-56-58-59-60-61-62-63-66-67-68-69-70-71-72-73-75-76-77-78-79-80-81-82-83-84)	-	2.0	V

NOTES: See Page 34.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
545 to 552	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	3006	4(j)	V_{IN} (3-State Control) = Note 6 V_{OUT} = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 50-51-52-53-54-55-56-59)	-	−20	µA
553 to 560	Output Leakage Current Third State (High Level Applied)	I_{OZH}	3006	4(j)	V_{IN} (3-State Control) = Note 6 V_{OUT} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 50-51-52-53-54-55-56-59)	-	20	µA
561	Supply Current 1 (During BIST)	I_{DDS1}	3005	4(b)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V f = 12.5MHz (Note 7)	-	60	mA
562	Supply Current 2 (During Normal Operation)	I_{DDS2}	3005	4(b)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V f = 12.5MHz (Note 8)	-	50	mA

NOTES: See Page 34.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
603 to 605	Rise and Fall Time (TTL and CMOS Inputs)	t_r1/t_f1	3004	-	Note 9	-	100	ns
606 to 608	Rise and Fall Time (SCHMITT Trigger Input)	t_r2/t_f2	3004	-	Note 9	-	1.0	µs
609 to 611	$\overline{\text{RESET}}$ Activated	t_{RES}	3003	-	Note 10	$4t_{BCK}$	-	-
612 to 614	Clock Period for CLK	t_{CLK}	3003	-	Note 10	80	-	ns
615 to 617	Clock Low Pulse Width for CLK	t_{CLO}	3003	-	Note 10	40	-	ns
618 to 620	Clock High Pulse Width for CLK	t_{CHI}	3003	-	Note 10	40	-	ns
621 to 623	Clock Period for BITCLK	t_{BCK}	3003	-	Note 10	$4t_{CLK}$	-	-
624 to 626	Clock Low Pulse Width for BITCLK	t_{BLO}	3003	-	Note 10	$4t_{CLO}$	-	-
627 to 629	Clock High Pulse Width for BITCLK	t_{BHI}	3003	-	Note 10	$4t_{CHI}$	-	-
630 to 632	Clock Period for SCLK	t_{SCK}	3003	-	Note 10	$t_{CLK}/2$	-	-
633 to 635	Clock Low Pulse Width for SCLK	t_{SLO}	3003	-	Note 10	20	-	ns
636 to 638	Clock High Pulse Width for SCLK	t_{SHI}	3003	-	Note 10	20	-	ns
639 to 641	$\overline{\text{CS}}$ Cycle Time	t_1	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	$4t_{CLK}$	-	-

NOTES: See Page 34.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
642 to 644	$\overline{VPD}$ Active to $\overline{CS}$ Active	t_2	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	5.0	-	ns
645 to 647	$\overline{CS}$ Pulse Width Activated	t_3	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	30	-	ns
648 to 650	$\overline{CS}$ Pulse Width De-activated	t_4	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	30	-	ns
651 to 653	$\overline{CS}$ De-activated to $\overline{VPD}$ De-activated	t_5	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	0	-	ns
654 to 656	$\overline{VPD}$ Pulse Width De-activated	t_6	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	$2t_{CLK}$	-	-
657 to 659	D Setup Time	t_7	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	8.0	-	ns
660 to 662	D Hold Time	t_8	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	15	-	ns
663 to 665	$\overline{CS}$ De-activated to $\overline{BUSY}$ Activated	t_9	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	50	ns
666 to 668	$\overline{BUSY}$ Pulse Width Activated	t_{10}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	$3t_{CLK}$	$4t_{CLK}$	-
669 to 671	$\overline{CS}$ De-activated to VCAR De-activated	t_{11}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	2.5 t_{CLK}	3.5 t_{CLK}	-
672 to 674	CLK Low to VCAR Valid	t_{12}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	50	ns
675 to 677	ERT High to VCAR Low	t_{13}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	50	ns
678 to 680	ERT Low to VCAR Valid	t_{14}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	50	ns

NOTES: See Page 34.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
681 to 683	SVALID High to SCLK High	t_{15}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	50	-	ns
684 to 686	SCLK High to SVALID Low	t_{16}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	50	-	ns
687 to 689	SVALID Pulse Width De-activated	t_{17}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	$2t_{CLK}$	-	-
690 to 692	SIN Setup Time	t_{18}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	5.0	-	ns
693 to 695	SIN Hold Time	t_{19}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	15	-	ns
696 to 698	CLK High to RA Valid	t_{20}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	-	50	ns
699 to 701	CLK Low to $\overline{RCS}$ Valid	t_{21}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	-	52	ns
702 to 704	CLK Low to R/$\overline{W}$ Low	t_{22}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	-	52	ns
705 to 707	CLK Low to R/$\overline{W}$ High	t_{23}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	-	52	ns
708 to 710	CLK Low to $\overline{OE}$ Low	t_{24}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	-	52	ns
711 to 713	CLK Low to $\overline{OE}$ High	t_{25}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	-	52	ns
714 to 716	CLK Low to RD Write Data Valid	t_{26}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	-	56	ns
717 to 719	CLK High to RD 3-State	t_{27}	3003	-	I_{OUT} ±5.0mA C_L = 100pF ±20% Note 10	-	40	ns

NOTES: See Page 34.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
720 to 722	Read Data Setup Time	t_{28}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	19	-	ns
723 to 725	$\overline{OE}/\overline{RCS}$ High to RD Invalid	t_{29}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	0	-	ns
726 to 728	ERT High to RA, $\overline{RCS}$, R/$\overline{W}$, $\overline{OE}$, RD 3-State	t_{30}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	-	30	ns
729 to 731	ERT Low to RA, $\overline{RCS}$, R/$\overline{W}$, $\overline{OE}$, RD Valid	t_{31}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	-	30	ns
732 to 734	CLK Low to $\overline{ERR}$ Valid	t_{32}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	-	50	ns
735 to 737	ERT High to $\overline{ERR}$ Low	t_{33}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	-	43	ns
738 to 740	ERT Low to $\overline{ERR}$ Valid	t_{34}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	-	43	ns
741 to 743	ERT High to RTS Low	t_{35}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	-	39	ns
744 to 746	ERT Low to RTS Valid	t_{36}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	-	39	ns
747 to 749	CLK High to RTS Stable	t_{37}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	-	52	ns
750 to 752	CTS Setup Time	t_{38}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	6.0	-	ns
753 to 755	CLK High to PVCF Stable	t_{39}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	-	48	ns
756 to 758	POLL Setup Time	t_{40}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	5.0	-	ns

NOTES: See Page 34.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
759 to 761	POLL Hold Time	t_{41}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	10	-	ns
762 to 764	CLK High to TIME Active	t_{42}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	-	50	ns
765 to 767	CLK High to RANDOM Valid	t_{43}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	-	50	ns
768 to 770	IFILL Setup Time	t_{44}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	10	-	ns
771 to 773	IFILL Hold Time	t_{45}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ±20% Note 10	5.0	-	ns

NOTES: See Page 34.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - d.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
9	Functional Test 1 (Basic)	-	3014	-	Verify Device Operation with Load V_{IL} = 0V, V_{IH} = 5.0V V_{OL} = 1.0V, V_{OH} = 4.0V I_{OUT} = ± 2.0mA C_L = 100pF ± 20% V_{DD} = 5.0V, V_{SS} = 0V Pattern = Note 1	-	-	-
10	Functional Test 2 (Nominal Voltage)	-	3014	-	Verify Device Operation with Load V_{IL}, V_{IH} = Note 2 V_{OL} = 1.0V, V_{OH} = 4.0V I_{OUT} = ± 2.0mA C_L = 100pF ± 20% V_{DD} = 5.0V, V_{SS} = 0V Pattern = Note 2	-	-	-
11	Functional Test 3 (High Voltage)	-	3014	-	Verify Device Operation with Load V_{IL}, V_{IH} = Note 2 V_{OL} = 1.0V, V_{OH} = 4.5V I_{OUT} = ± 2.0mA C_L = 100pF ± 20% V_{DD} = 5.5V, V_{SS} = 0V Pattern = Note 2	-	-	-
12	Functional Test 4 (Low Voltage)	-	3014	-	Verify Device Operation with Load V_{IL}, V_{IH} = Note 2 V_{OL} = 1.0V, V_{OH} = 3.5V I_{OUT} = ± 2.0mA C_L = 100pF ± 20% V_{DD} = 4.5V, V_{SS} = 0V Pattern = Note 2	-	-	-
13	Quiescent Current	I_{DD}	3005	4(b)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V All Outputs Open Note 3 (Pins 1 + 21 + 48 + 65)	-	0.5	mA

NOTES: See Page 34.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
14 to 54	Input Current Low Level	I_{IL}	3009	4(c)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-3-5-8-9-10-11-12-13-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49-78-79-80-81-82-83-84)	-	− 1.0	µA
55 to 95	Input Current High Level	I_{IH}	3009	4(d)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-3-5-8-9-10-11-12-13-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49-78-79-80-81-82-83-84)	-	1.0	µA
96 to 127	Output Voltage Low Level	V_{OL}	3007	4(e)	V_{IL}, V_{IH} = Note 2 I_{OL} = 4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 6-7-15-33-40-41-44-45-50-51-52-53-54-55-56-58-59-60-61-62-63-66-67-68-69-70-71-72-73-75-76-77)	-	0.4	V
128 to 159	Output Voltage High Level 1	V_{OH1}	3006	4(f)	V_{IL}, V_{IH} = Note 2 I_{OL} = − 4.0mA V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 6-7-15-33-40-41-44-45-50-51-52-53-54-55-56-58-59-60-61-62-63-66-67-68-69-70-71-72-73-75-76-77)	3.9	-	V
160 to 191	Output Voltage High Level 2	V_{OH2}	3006	4(f)	V_{IL}, V_{IH} = Note 2 I_{OL} = − 0.5mA V_{DD} = 4.5V, V_{SS} = 0V Note 4 (Pins 6-7-15-33-40-41-44-45-50-51-52-53-54-55-56-58-59-60-61-62-63-66-67-68-69-70-71-72-73-75-76-77)	4.2	-	V

NOTES: See Page 34.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
192 to 209	Threshold Voltage Low Level 1 (TTL Inputs)	V_{THN1}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 2-3-5-50-51-52-53-54-55-56-59-78-79-80-81-82-83-84)	0.8	-	V
210 to 227	Threshold Voltage High Level 1 (TTL Inputs)	V_{THP1}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 2-3-5-50-51-52-53-54-55-56-59-78-79-80-81-82-83-84)	-	2.0	V
228 to 257	Threshold Voltage Low Level 2 (CMOS Inputs)	V_{THN2}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 8-9-10-11-13-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49)	1.3	-	V
258 to 287	Threshold Voltage High Level 2 (CMOS Inputs)	V_{THP2}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pins 8-9-10-11-13-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49)	-	3.2	V
288	Threshold Voltage Low Level 3 (SCHMITT Trigger Input)	V_{THN3}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pin 12)	1.0	2.8	V
289	Threshold Voltage High Level 3 (SCHMITT Trigger Input)	V_{THP3}	-	4(g)	V_{DD} = 4.5V, V_{SS} = 0V (Pin 12)	1.5	3.3	V
290	Hysteresis Voltage	V_H	-	4(h)	V_{DD} = 4.5V, V_{SS} = 0V Note 5 (Pin 12)	0.5	-	V
291 to 308	Threshold Voltage Low Level 4 (TTL Inputs)	V_{THN4}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-3-5-50-51-52-53-54-55-56-59-78-79-80-81-82-83-84)	0.8	-	V
309 to 326	Threshold Voltage High Level 4 (TTL Inputs)	V_{THP4}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 2-3-5-50-51-52-53-54-55-56-59-78-79-80-81-82-83-84)	-	2.0	V

NOTES: See Page 34.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
327 to 366	Threshold Voltage Low Level 5 (CMOS Inputs)	V_{THN5}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 8-9-10-11-13-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49)	1.7	-	V
367 to 396	Threshold Voltage High Level 5 (CMOS Inputs)	V_{THP5}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pins 8-9-10-11-13-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49)	-	3.9	V
397	Threshold Voltage Low Level 6 (SCHMITT Trigger Input)	V_{THN6}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pin 12)	1.2	3.8	V
398	Threshold Voltage High Level 6 (SCHMITT Trigger Input)	V_{THP6}	-	4(g)	V_{DD} = 5.5V, V_{SS} = 0V (Pin 12)	1.7	4.3	V
399 to 471	Input/Output Clamp Voltage (to V_{SS})	V_{IC1}	3022	4(i)	I_{IN} = −100µA V_{DD} = V_{SS} = 0V (Pins 2-3-5-6-7-8-9-10-11-12-13-15-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-33-34-35-36-37-38-40-41-42-43-44-45-46-47-49-50-51-52-53-54-55-56-58-59-60-61-62-63-66-67-68-69-70-71-72-73-75-76-77-78-79-80-81-82-83-84)	-	−2.0	V
472 to 544	Input/Output Clamp Voltage (to V_{DD})	V_{IC2}	3022	4(i)	I_{IN} = 100µA V_{DD} = V_{SS} = 0V (Pins 2-3-5-6-7-8-9-10-11-12-13-15-16-17-18-19-20-23-24-25-26-27-28-29-30-31-32-33-34-35-36-37-38-40-41-42-43-44-45-46-47-49-50-51-52-53-54-55-56-58-59-60-61-62-63-66-67-68-69-70-71-72-73-75-76-77-78-79-80-81-82-83-84)	-	2.0	V

NOTES: See Page 34.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
545 to 552	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	3006	4(j)	V_{IN} (3-State Control) = Note 6 V_{OUT} = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 50-51-52-53-54-55-56-59)	-	−10	µA
553 to 560	Output Leakage Current Third State (High Level Applied)	I_{OZH}	3006	4(j)	V_{IN} (3-State Control) = Note 6 V_{OUT} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 50-51-52-53-54-55-56-59)	-	10	µA
561	Supply Current 1 (During BIST)	I_{DDS1}	3005	4(b)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V f = 12.5MHz (Note 7)	-	55	mA
562	Supply Current 2 (During Normal Operation)	I_{DDS2}	3005	4(b)	V_{IL} = 0V, V_{IH} = 5.5V V_{DD} = 5.5V, V_{SS} = 0V f = 12.5MHz (Note 8)	-	45	mA

NOTES: See Page 34.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - a.c. PARAMETERS

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
603 to 605	Rise and Fall Time (TTL and CMOS Inputs)	t_r1/t_f1	3004	-	Note 9	-	100	ns
606 to 608	Rise and Fall Time (SCHMITT Trigger Input)	t_r2/t_f2	3004	-	Note 9	-	1.0	µs
609 to 611	$\overline{\text{RESET}}$ Activated	t_{RES}	3003	-	Note 10	$4t_{BCK}$	-	-
612 to 614	Clock Period for CLK	t_{CLK}	3003	-	Note 10	80	-	ns
615 to 617	Clock Low Pulse Width for CLK	t_{CLO}	3003	-	Note 10	40	-	ns
618 to 620	Clock High Pulse Width for CLK	t_{CHI}	3003	-	Note 10	40	-	ns
621 to 623	Clock Period for BITCLK	t_{BCK}	3003	-	Note 10	$4t_{CLK}$	-	-
624 to 626	Clock Low Pulse Width for BITCLK	t_{BLO}	3003	-	Note 10	$4t_{CLO}$	-	-
627 to 629	Clock High Pulse Width for BITCLK	t_{BHI}	3003	-	Note 10	$4t_{CHI}$	-	-
630 to 632	Clock Period for SCLK	t_{SCK}	3003	-	Note 10	$t_{CLK}/2$	-	-
633 to 635	Clock Low Pulse Width for SCLK	t_{SLO}	3003	-	Note 10	20	-	ns
636 to 638	Clock High Pulse Width for SCLK	t_{SHI}	3003	-	Note 10	20	-	ns
639 to 641	$\overline{\text{CS}}$ Cycle Time	t_1	3003	-	I_{OUT} ± 2.0mA C_L = 100pF ± 20% Note 10	$4t_{CLK}$	-	-

NOTES: See Page 34.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
642 to 644	$\overline{VPD}$ Active to $\overline{CS}$ Active	t_2	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	5.0	-	ns
645 to 647	$\overline{CS}$ Pulse Width Activated	t_3	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	30	-	ns
648 to 650	$\overline{CS}$ Pulse Width De-activated	t_4	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	30	-	ns
651 to 653	$\overline{CS}$ De-activated to $\overline{VPD}$ De-activated	t_5	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	0	-	ns
654 to 656	$\overline{VPD}$ Pulse Width De-activated	t_6	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	$2t_{CLK}$	-	-
657 to 659	D Setup Time	t_7	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	8.0	-	ns
660 to 662	D Hold Time	t_8	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	15	-	ns
663 to 665	$\overline{CS}$ De-activated to $\overline{BUSY}$ Activated	t_9	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	50	ns
666 to 668	$\overline{BUSY}$ Pulse Width Activated	t_{10}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	$3t_{CLK}$	$4t_{CLK}$	-
669 to 671	$\overline{CS}$ De-activated to VCAR De-activated	t_{11}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	2.5 t_{CLK}	3.5 t_{CLK}	-
672 to 674	CLK Low to VCAR Valid	t_{12}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	50	ns
675 to 677	ERT High to VCAR Low	t_{13}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	50	ns
678 to 680	ERT Low to VCAR Valid	t_{14}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	50	ns

NOTES: See Page 34.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
681 to 683	SVALID High to SCLK High	t_{15}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	50	-	ns
684 to 686	SCLK High to SVALID Low	t_{16}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	50	-	ns
687 to 689	SVALID Pulse Width De-activated	t_{17}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	$2t_{CLK}$	-	-
690 to 692	SIN Setup Time	t_{18}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	5.0	-	ns
693 to 695	SIN Hold Time	t_{19}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	15	-	ns
696 to 698	CLK High to RA Valid	t_{20}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	50	ns
699 to 701	CLK Low to $\overline{RCS}$ Valid	t_{21}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	52	ns
702 to 704	CLK Low to R/$\overline{W}$ Low	t_{22}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	52	ns
705 to 707	CLK Low to R/$\overline{W}$ High	t_{23}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	52	ns
708 to 710	CLK Low to $\overline{OE}$ Low	t_{24}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	52	ns
711 to 713	CLK Low to $\overline{OE}$ High	t_{25}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	52	ns
714 to 716	CLK Low to RD Write Data Valid	t_{26}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	56	ns
717 to 719	CLK High to RD 3-State	t_{27}	3003	-	I_{OUT} ±5.0mA C_L = 100pF ± 20% Note 10	-	40	ns

NOTES: See Page 34.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
720 to 722	Read Data Setup Time	t_{28}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	19	-	ns
723 to 725	$\overline{OE}$/$\overline{RCS}$ High to RD Invalid	t_{29}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	0	-	ns
726 to 728	ERT High to RA, $\overline{RCS}$, R/$\overline{W}$, $\overline{OE}$, RD 3-State	t_{30}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	30	ns
729 to 731	ERT Low to RA, $\overline{RCS}$, R/$\overline{W}$, $\overline{OE}$, RD Valid	t_{31}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	30	ns
732 to 734	CLK Low to $\overline{ERR}$ Valid	t_{32}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	50	ns
735 to 737	ERT High to $\overline{ERR}$ Low	t_{33}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	43	ns
738 to 740	ERT Low to $\overline{ERR}$ Valid	t_{34}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	43	ns
741 to 743	ERT High to RTS Low	t_{35}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	39	ns
744 to 746	ERT Low to RTS Valid	t_{36}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	39	ns
747 to 749	CLK High to RTS Stable	t_{37}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	52	ns
750 to 752	CTS Setup Time	t_{38}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	6.0	-	ns
753 to 755	CLK High to PVCF Stable	t_{39}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	48	ns
756 to 758	POLL Setup Time	t_{40}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	5.0	-	ns

NOTES: See Page 34.

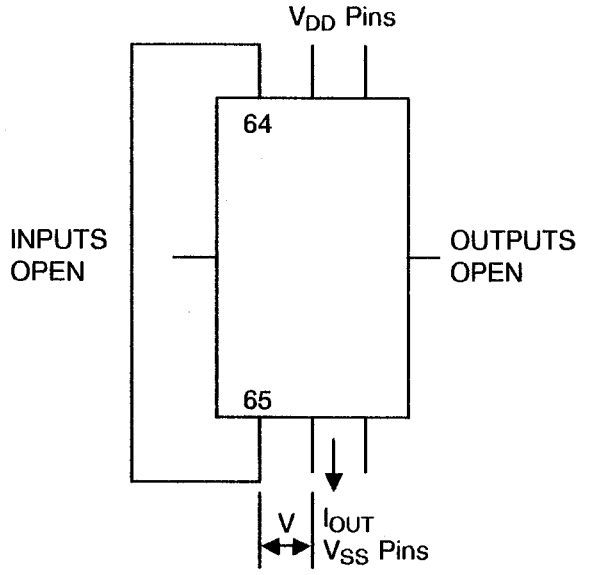
TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE - a.c. PARAMETERS (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
759 to 761	POLL Hold Time	t_{41}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	10	-	ns
762 to 764	CLK High to TIME Active	t_{42}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	50	ns
765 to 767	CLK High to RANDOM Valid	t_{43}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	-	50	ns
768 to 770	IFILL Setup Time	t_{44}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	10	-	ns
771 to 773	IFILL Hold Time	t_{45}	3003	-	I_{OUT} ±2.0mA C_L = 100pF ± 20% Note 10	5.0	-	ns

NOTES: See Page 34.

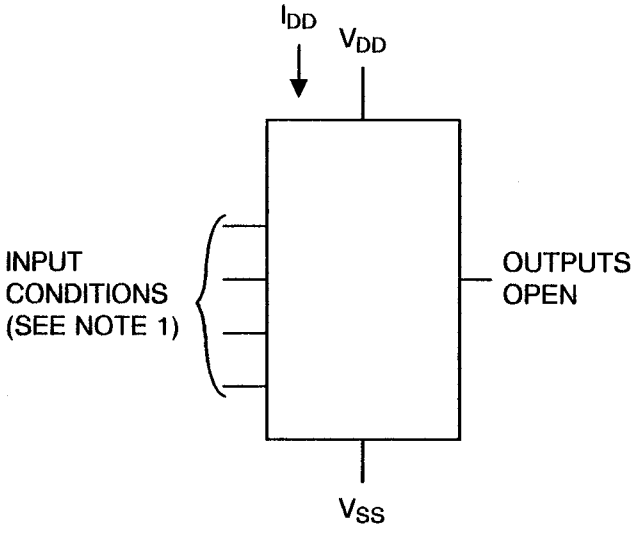
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - V_{SS}, V_{DD} CONTINUITY



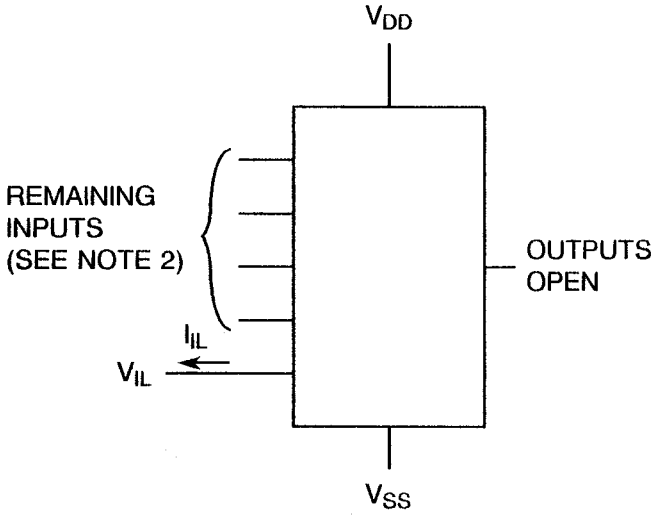
NOTES
1. Each power pin tested separately.

FIGURE 4(b) - QUIESCENT CURRENT



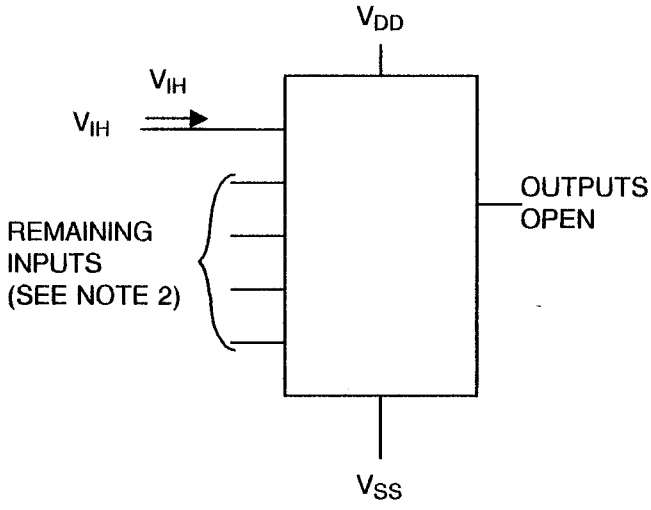
NOTES
1. Input conditions as per Table 2.

FIGURE 4(c) - INPUT CURRENT LOW LEVEL



NOTES
1. Each input to be tested separately.
2. Input conditions as per Table 2.

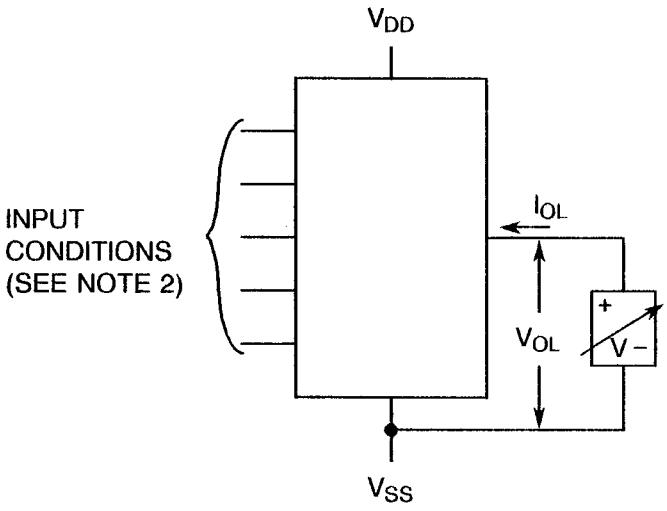
FIGURE 4(d) - INPUT CURRENT HIGH LEVEL



NOTES
1. Each input to be tested separately.
2. Input conditions as per Table 2.

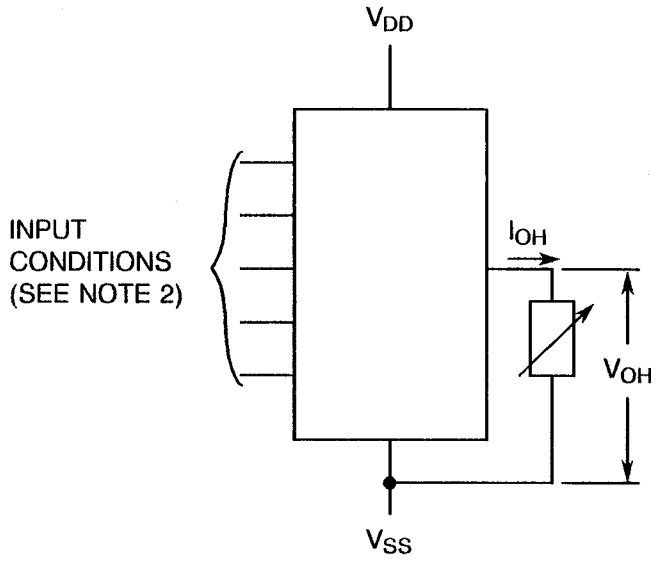
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(e) - OUTPUT VOLTAGE LOW LEVEL



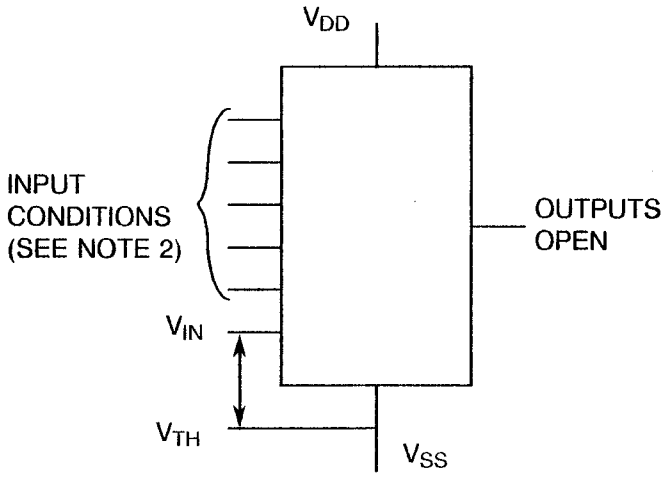
NOTES
1. Each output to be tested separately.
2. Input conditions as per Table 2.

FIGURE 4(f) - OUTPUT VOLTAGE HIGH LEVEL



NOTES
1. Each output to be tested separately.
2. Input conditions as per Table 2.

FIGURE 4(g) - THRESHOLD VOLTAGE



NOTES
1. Each input to be tested separately.
2. Input conditions as per Table 2.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(h) - HYSTERESIS VOLTAGE

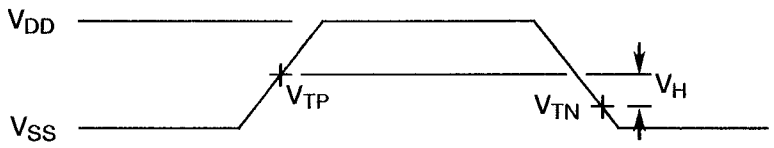
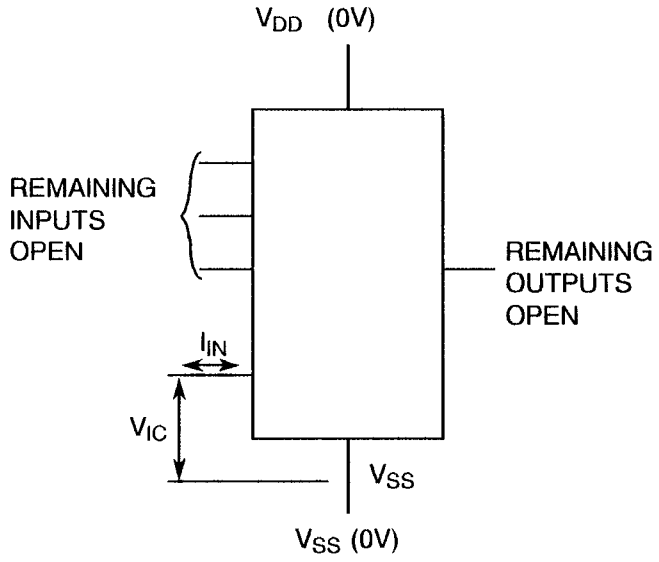


FIGURE 4(i) - INPUT/OUTPUT CLAMP VOLTAGE

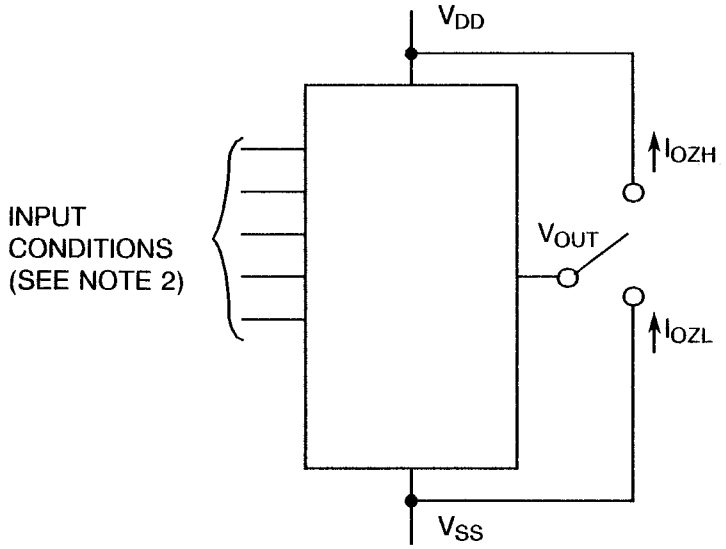


NOTES

1. Each input and output to be tested separately.

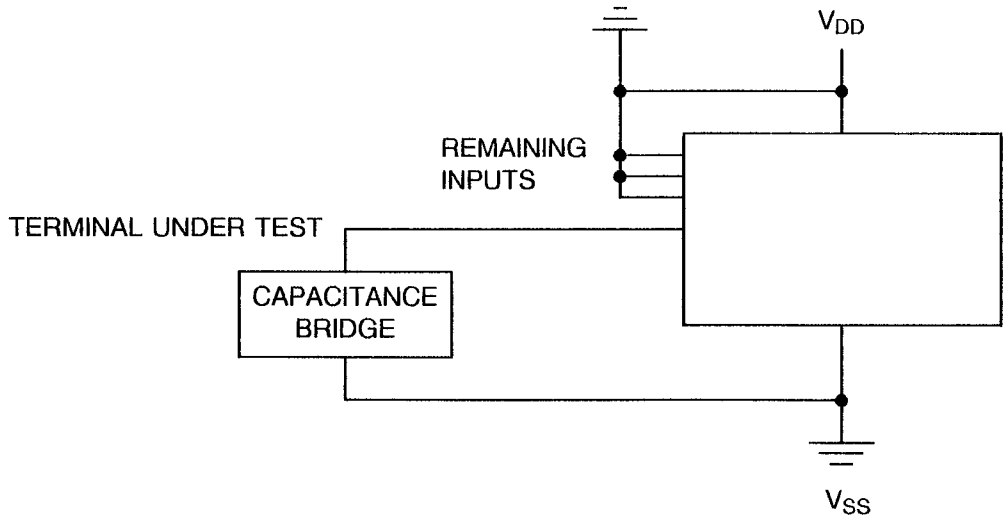
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(j) - OUTPUT LEAKAGE CURRENT THIRD STATE



NOTES
1. Each output to be tested separately.
2. Input conditions as per Table 2.

FIGURE 4(k) - INPUT CAPACITANCE



NOTES
1. Test frequency = 1.0MHz.
2. Each input and input/output is to be tested separately.

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
13	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	±250	µA
14 to 54	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	±200	nA
55 to 95	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	±200	nA
96 to 127	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	±200	mV
128 to 159	Output Voltage High Level 1	V_{OH1}	As per Table 2	As per Table 2	±300	mV
545 to 552	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	±2.0	µA
553 to 560	Output Leakage Current Third State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	±2.0	µA

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

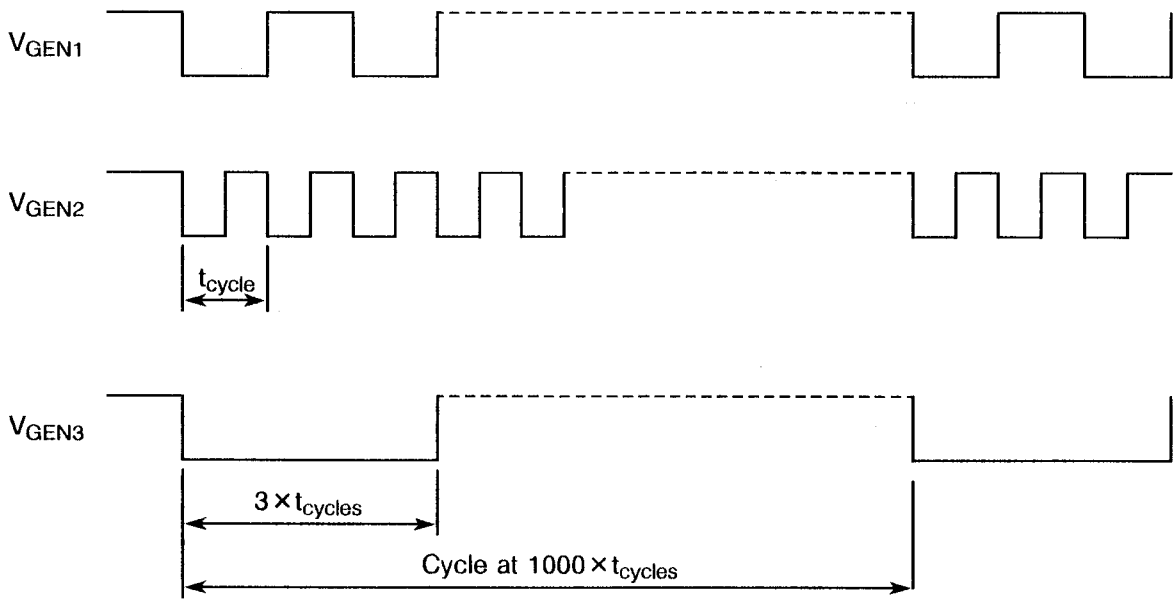
No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+ 125(+ 0 – 5)	°C
2	Outputs - (Pins 6-7-15-33-40-41-44-45-58-60-61-62-63-66-67-68-69-70-71-72-73-75-76-77)	V_{OUT}	$V_{DD}/2$	V
3	Input - (Pin 16)	V_{IN}	V_{DD}	V
4	Input - (Pin 17)	V_{IN}	V_{SS}	V
5	Inputs - (Pin 2-3-5-8-9-10-11-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49-50-51-52-53-54-55-56-59-78-79-80-81-82-83-84)	V_{IN}	V_{GEN1}	Vac
6	Input - (Pin 12)	V_{IN}	V_{GEN3}	Vac
7	Input - (Pin 13)	V_{IN}	V_{GEN2}	Vac
8	Pulse Voltage	V_{GEN}	0V to V_{DD}	Vac
9	Pulse Frequency Square Wave	f_{GEN1} f_{GEN2}	$f_{GEN2}/2$ 250k 50% Duty Cycle	Hz
10	Pulse Square Wave	GEN3	Pulse width at lower level = 3 cycles of GEN2 repeated after 1000 cycles of GEN2	-
11	Positive Supply Voltage (Pins 1-21-48-65)	V_{DD}	5.5(+ 0 – 0.5)	V
12	Negative Supply Voltage (Pins 4-22-39-57-64-74)	V_{SS}	0	V

NOTES: See Page 66.

TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS (CONT'D)

NOTES

1. Input Protection Resistor = Output Load = 10kΩ.

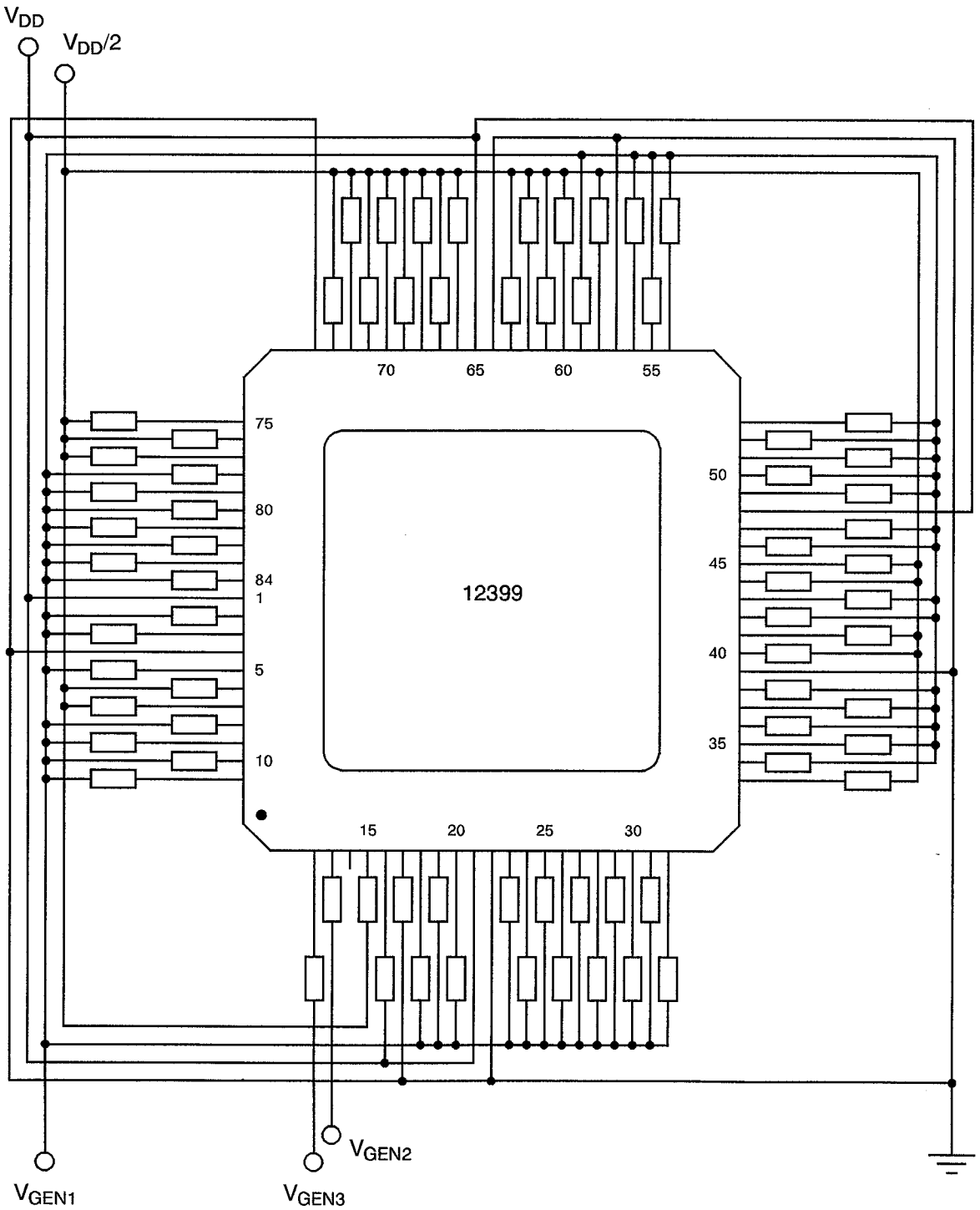


$t_{cycle} = 4.0\mu s$.

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(b) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

4.9 TOTAL DOSE IRRADIATION TESTING

4.9.1 Application

If specified in Para. 4.2.1 of this specification, total dose irradiation testing shall be performed in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.9.2 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6.

4.9.3 Electrical Measurements

The parameters to be measured prior to irradiation exposure are scheduled in Table 2 of this specification. Only devices which meet the requirements of Table 2 shall be scheduled in the test sample.

The parameters to be measured during and on completion of irradiation testing are scheduled in Table 7 of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
9	Functional Test 1 (Basic)	-	As per Table 2	As per Table 2	-	-	-
10	Functional Test 2 (Nominal Voltage)	-	As per Table 2	As per Table 2	-	-	-
11	Functional Test 3 (High Voltage)	-	As per Table 2	As per Table 2	-	-	-
12	Functional Test 4 (Low Voltage)	-	As per Table 2	As per Table 2	-	-	-
13	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	-	0.5	mA
14 to 54	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	-	−1.0	µA
55 to 95	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	-	1.0	µA
96 to 127	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	-	0.4	V
128 to 159	Output Voltage High Level 1	V_{OH1}	As per Table 2	As per Table 2	3.9	-	V
160 to 191	Output Voltage High Level 2	V_{OH2}	As per Table 2	As per Table 2	4.2	-	V
192 to 209	Threshold Voltage Low Level 1 (TTL Inputs)	V_{THN1}	As per Table 2	As per Table 2	0.8	-	V
210 to 227	Threshold Voltage High Level 1 (TTL Inputs)	V_{THP1}	As per Table 2	As per Table 2	-	2.0	V
228 to 257	Threshold Voltage Low Level 2 (CMOS Inputs)	V_{THN2}	As per Table 2	As per Table 2	1.3	-	V
258 to 287	Threshold Voltage High Level 2 (CMOS Inputs)	V_{THP2}	As per Table 2	As per Table 2	-	3.2	V
288	Threshold Voltage Low Level 3 (SCHMITT Trigger Input)	V_{THN3}	As per Table 2	As per Table 2	1.0	2.8	V

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
289	Threshold Voltage High Level 3 (SCHMITT Trigger Input)	V_{THP3}	As per Table 2	As per Table 2	1.5	3.3	V
290	Hysteresis Voltage	V_H	As per Table 2	As per Table 2	0.5	-	V
291 to 308	Threshold Voltage Low Level 4 (TTL Inputs)	V_{THN4}	As per Table 2	As per Table 2	0.8	-	V
309 to 326	Threshold Voltage High Level 4 (TTL Inputs)	V_{THP4}	As per Table 2	As per Table 2	-	2.0	V
327 to 366	Threshold Voltage Low Level 5 (CMOS Inputs)	V_{THN5}	As per Table 2	As per Table 2	1.7	-	V
367 to 396	Threshold Voltage High Level 5 (CMOS Inputs)	V_{THP5}	As per Table 2	As per Table 2	-	3.9	V
397	Threshold Voltage Low Level 6 (SCHMITT Trigger Input)	V_{THN6}	As per Table 2	As per Table 2	1.2	3.8	V
398	Threshold Voltage High Level 6 (SCHMITT Trigger Input)	V_{THP6}	As per Table 2	As per Table 2	1.7	4.3	V
399 to 471	Input/Output Clamp Voltage (to V_{SS})	V_{IC1}	As per Table 2	As per Table 2	-	−2.0	V
472 to 544	Input/Output Clamp Voltage (to V_{DD})	V_{IC2}	As per Table 2	As per Table 2	-	2.0	V
545 to 552	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	-	−10	µA
553 to 560	Output Leakage Current Third State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	-	10	µA
561	Supply Current 1 (During BIST)	I_{DDS1}	As per Table 2	As per Table 2	-	60	mA
562	Supply Current 2 (During Normal Operation)	I_{DDS2}	As per Table 2	As per Table 2	-	15	mA

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
609 to 611	$\overline{\text{RESET}}$ Activated	t_{RES}	As per Table 2	As per Table 2	$4t_{BCK}$	-	-
612 to 614	Clock Period for CLK	t_{CLK}	As per Table 2	As per Table 2	80	-	ns
615 to 617	Clock Low Pulse Width for CLK	t_{CLO}	As per Table 2	As per Table 2	40	-	ns
618 to 620	Clock High Pulse Width for CLK	t_{CHI}	As per Table 2	As per Table 2	40	-	ns
621 to 623	Clock Period for BITCLK	t_{BCK}	As per Table 2	As per Table 2	$4t_{CLK}$	-	-
624 to 626	Clock Low Pulse Width for BITCLK	t_{BLO}	As per Table 2	As per Table 2	$4t_{CLO}$	-	-
627 to 629	Clock High Pulse Width for BITCLK	t_{BHI}	As per Table 2	As per Table 2	$4t_{CHI}$	-	-
630 to 632	Clock Period for SCLK	t_{SCK}	As per Table 2	As per Table 2	$t_{CLK}/2$	-	-
633 to 635	Clock Low Pulse Width for SCLK	t_{SLO}	As per Table 2	As per Table 2	20	-	ns
636 to 638	Clock High Pulse Width for SCLK	t_{SHI}	As per Table 2	As per Table 2	20	-	ns
639 to 641	$\overline{\text{CS}}$ Cycle Time	t_1	As per Table 2	As per Table 2	$4t_{CLK}$	-	-
642 to 644	$\overline{\text{VPD}}$ Active to $\overline{\text{CS}}$ Active	t_2	As per Table 2	As per Table 2	5.0	-	ns
645 to 647	$\overline{\text{CS}}$ Pulse Width Activated	t_3	As per Table 2	As per Table 2	30	-	ns
648 to 650	$\overline{\text{CS}}$ Pulse Width De-activated	t_4	As per Table 2	As per Table 2	30	-	ns

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
651 to 653	$\overline{CS}$ De-activated to $\overline{VPD}$ De-activated	t_5	As per Table 2	As per Table 2	0	-	ns
654 to 656	$\overline{VPD}$ Pulse Width De-activated	t_6	As per Table 2	As per Table 2	$2t_{CLK}$	-	-
657 to 659	D Setup Time	t_7	As per Table 2	As per Table 2	8.0	-	ns
660 to 662	D Hold Time	t_8	As per Table 2	As per Table 2	15	-	ns
663 to 665	$\overline{CS}$ De-activated to $\overline{BUSY}$ Activated	t_9	As per Table 2	As per Table 2	-	50	ns
666 to 668	$\overline{BUSY}$ Pulse Width Activated	t_{10}	As per Table 2	As per Table 2	$3t_{CLK}$	$4t_{CLK}$	-
669 to 671	$\overline{CS}$ De-activated to VCAR De-activated	t_{11}	As per Table 2	As per Table 2	2.5 t_{CLK}	3.5 t_{CLK}	-
672 to 674	CLK Low to VCAR Valid	t_{12}	As per Table 2	As per Table 2	-	50	ns
675 to 677	ERT High to VCAR Low	t_{13}	As per Table 2	As per Table 2	-	50	ns
678 to 680	ERT Low to VCAR Valid	t_{14}	As per Table 2	As per Table 2	-	50	ns
681 to 683	SVALID High to SCLK High	t_{15}	As per Table 2	As per Table 2	50	-	ns
684 to 686	SCLK High to SVALID Low	t_{16}	As per Table 2	As per Table 2	50	-	ns
687 to 689	SVALID Pulse Width De-activated	t_{17}	As per Table 2	As per Table 2	$2t_{CLK}$	-	-
690 to 692	SIN Setup Time	t_{18}	As per Table 2	As per Table 2	5.0	-	ns

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
693 to 695	SIN Hold Time	t_{19}	As per Table 2	As per Table 2	15	-	ns
696 to 698	CLK High to RA Valid	t_{20}	As per Table 2	As per Table 2	-	50	ns
699 to 701	CLK Low to $\overline{RCS}$ Valid	t_{21}	As per Table 2	As per Table 2	-	52	ns
702 to 704	CLK Low to R/$\overline{W}$ Low	t_{22}	As per Table 2	As per Table 2	-	52	ns
705 to 707	CLK Low to R/$\overline{W}$ High	t_{23}	As per Table 2	As per Table 2	-	52	ns
708 to 710	CLK Low to $\overline{OE}$ Low	t_{24}	As per Table 2	As per Table 2	-	52	ns
711 to 713	CLK Low to $\overline{OE}$ High	t_{25}	As per Table 2	As per Table 2	-	52	ns
714 to 716	CLK Low to RD Write Data Valid	t_{26}	As per Table 2	As per Table 2	-	56	ns
717 to 719	CLK High to RD 3-State	t_{27}	As per Table 2	As per Table 2	-	40	ns
720 to 722	Read Data Setup Time	t_{28}	As per Table 2	As per Table 2	19	-	ns
723 to 725	$\overline{OE}$/$\overline{RCS}$ High to RD Invalid	t_{29}	As per Table 2	As per Table 2	0	-	ns
726 to 728	ERT High to RA, $\overline{RCS}$, R/$\overline{W}$, $\overline{OE}$, RD 3-State	t_{30}	As per Table 2	As per Table 2	-	30	ns
729 to 731	ERT Low to RA, $\overline{RCS}$, R/$\overline{W}$, $\overline{OE}$, RD Valid	t_{31}	As per Table 2	As per Table 2	-	30	ns
732 to 734	CLK Low to $\overline{ERR}$ Valid	t_{32}	As per Table 2	As per Table 2	-	50	ns

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
735 to 737	ERT High to $\overline{ERR}$ Low	t_{33}	As per Table 2	As per Table 2	-	43	ns
738 to 740	ERT Low to $\overline{ERR}$ Valid	t_{34}	As per Table 2	As per Table 2	-	43	ns
741 to 743	ERT High to RTS Low	t_{35}	As per Table 2	As per Table 2	-	39	ns
744 to 746	ERT Low to RTS Valid	t_{36}	As per Table 2	As per Table 2	-	39	ns
747 to 749	CLK High to RTS Stable	t_{37}	As per Table 2	As per Table 2	-	52	ns
750 to 752	CTS Setup Time	t_{38}	As per Table 2	As per Table 2	6.0	-	ns
753 to 755	CLK High to PVCF Stable	t_{39}	As per Table 2	As per Table 2	-	48	ns
756 to 758	POLL Setup Time	t_{40}	As per Table 2	As per Table 2	5.0	-	ns
759 to 761	POLL Hold Time	t_{41}	As per Table 2	As per Table 2	10	-	ns
762 to 764	CLK High to TIME Active	t_{42}	As per Table 2	As per Table 2	-	50	ns
765 to 767	CLK High to RANDOM Valid	t_{43}	As per Table 2	As per Table 2	-	50	ns
768 to 770	IFILL Setup Time	t_{44}	As per Table 2	As per Table 2	10	-	ns
771 to 773	IFILL Hold Time	t_{45}	As per Table 2	As per Table 2	5.0	-	ns

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING

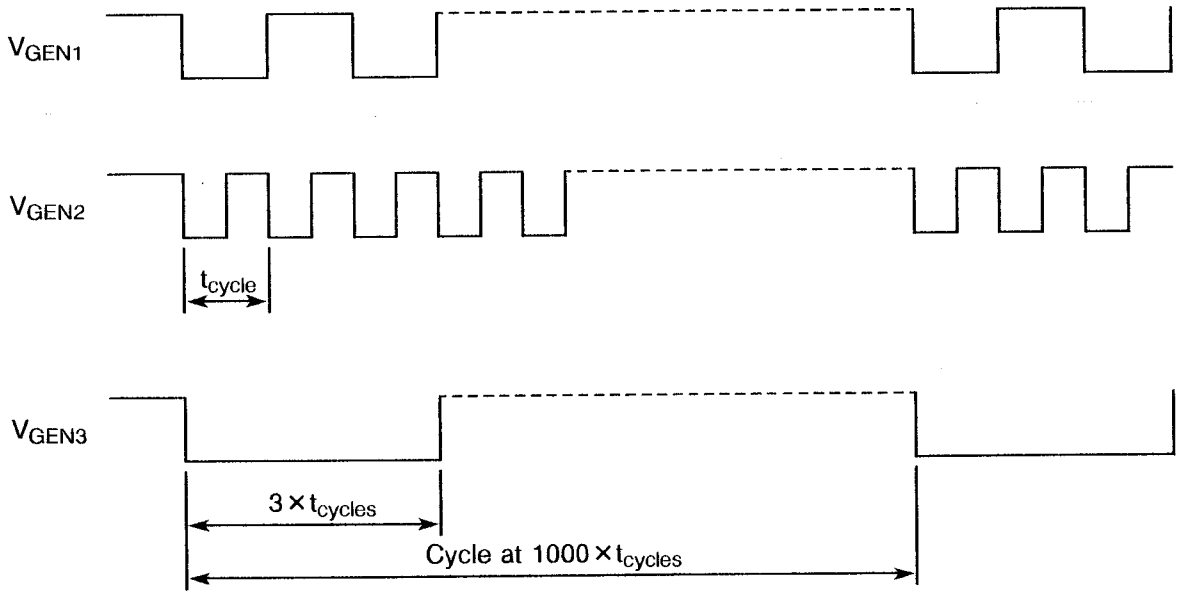
No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0−5)	°C
2	Outputs - (Pins 6-7-15-33-40-41-44-45-58-60-61-62-63-66-67-68-69-70-71-72-73-75-76-77)	V_{OUT}	$V_{DD}/2$	V
3	Input - (Pin 16)	V_{IN}	V_{DD}	V
4	Input - (Pin 17)	V_{IN}	V_{SS}	V
5	Inputs - (Pins 2-3-5-8-9-10-11-18-19-20-23-24-25-26-27-28-29-30-31-32-34-35-36-37-38-42-43-46-47-49-50-51-52-53-54-55-56-59-78-79-80-81-82-83-84)	V_{IN}	V_{GEN1}	Vac
6	Input - (Pin 12)	V_{IN}	V_{GEN3}	Vac
7	Input - (Pin 13)	V_{IN}	V_{GEN2}	Vac
8	Pulse Voltage	V_{GEN}	0V to V_{DD}	Vac
9	Pulse Frequency Square Wave	f_{GEN1} f_{GEN2}	$f_{GEN2}/2$ 250k 50% Duty Cycle	Hz
10	Pulse Square Wave	GEN3	Pulse width at lower level = 3 cycles of GEN2 repeated after 1000 cycles of GEN2	-
11	Positive Supply Voltage (Pins 1-21-48-65)	V_{DD}	5.5(+0−0.5)	V
12	Negative Supply Voltage (Pins 4-22-39-57-64-74)	V_{SS}	0	V

NOTES: See Page 76.

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING (CONT'D)

NOTES

1. Input Protection Resistor = Output Load = 10kΩ.



$t_{cycle} = 4.0\mu s$.

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING (CONT'D)

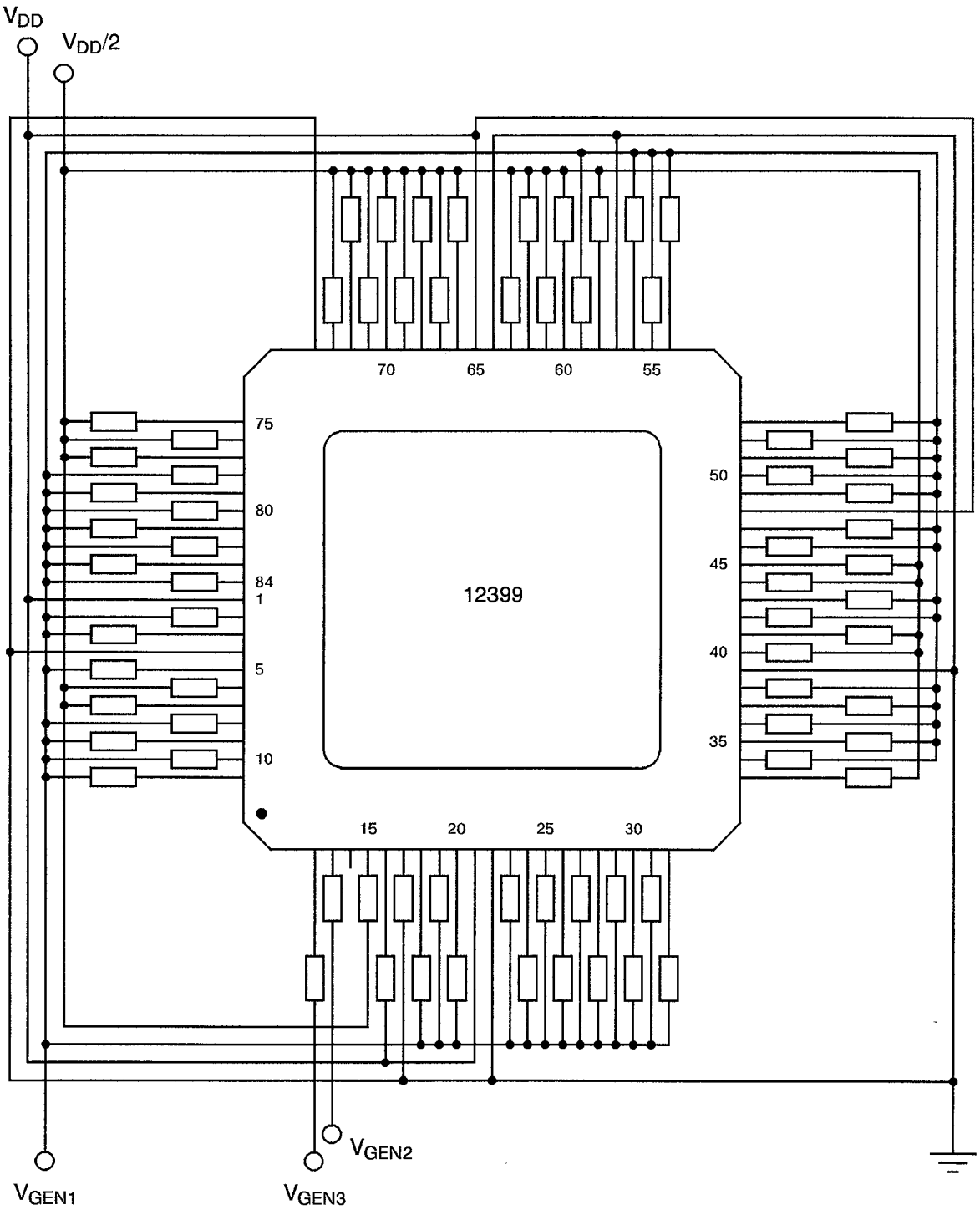


TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
9	Functional Test 1 (Basic)	-	As per Table 2	As per Table 2	-	-	-
10	Functional Test 2 (Nominal Voltage)	-	As per Table 2	As per Table 2	-	-	-
11	Functional Test 3 (High Voltage)	-	As per Table 2	As per Table 2	-	-	-
12	Functional Test 4 (Low Voltage)	-	As per Table 2	As per Table 2	-	-	-
13	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	-	3.5	mA
14 to 54	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	-	−1.0	µA
55 to 95	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	-	1.0	µA
96 to 127	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	-	0.4	V
128 to 159	Output Voltage High Level 1	V_{OH1}	As per Table 2	As per Table 2	3.9	-	V
160 to 191	Output Voltage High Level 2	V_{OH2}	As per Table 2	As per Table 2	4.2	-	V
192 to 209	Threshold Voltage Low Level 1 (TTL Inputs)	V_{THN1}	As per Table 2	As per Table 2	0.8	-	V
210 to 227	Threshold Voltage High Level 1 (TTL Inputs)	V_{THP1}	As per Table 2	As per Table 2	-	2.0	V
228 to 257	Threshold Voltage Low Level 2 (CMOS Inputs)	V_{THN2}	As per Table 2	As per Table 2	1.3	-	V
258 to 287	Threshold Voltage High Level 2 (CMOS Inputs)	V_{THP2}	As per Table 2	As per Table 2	-	3.2	V
288	Threshold Voltage Low Level 3 (SCHMITT Trigger Input)	V_{THN3}	As per Table 2	As per Table 2	1.0	2.8	V

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
289	Threshold Voltage High Level 3 (SCHMITT Trigger Input)	V_{THP3}	As per Table 2	As per Table 2	1.5	3.3	V
290	Hysteresis Voltage	V_H	As per Table 2	As per Table 2	0.5	-	V
291 to 308	Threshold Voltage Low Level 4 (TTL Inputs)	V_{THN4}	As per Table 2	As per Table 2	0.8	-	V
309 to 326	Threshold Voltage High Level 4 (TTL Inputs)	V_{THP4}	As per Table 2	As per Table 2	-	2.0	V
327 to 366	Threshold Voltage Low Level 5 (CMOS Inputs)	V_{THN5}	As per Table 2	As per Table 2	1.7	-	V
367 to 396	Threshold Voltage High Level 5 (CMOS Inputs)	V_{THP5}	As per Table 2	As per Table 2	-	3.9	V
397	Threshold Voltage Low Level 6 (SCHMITT Trigger Input)	V_{THN6}	As per Table 2	As per Table 2	1.2	3.8	V
398	Threshold Voltage High Level 6 (SCHMITT Trigger Input)	V_{THP6}	As per Table 2	As per Table 2	1.7	4.3	V
399 to 471	Input/Output Clamp Voltage (to V_{SS})	V_{IC1}	As per Table 2	As per Table 2	-	−2.0	V
472 to 544	Input/Output Clamp Voltage (to V_{DD})	V_{IC2}	As per Table 2	As per Table 2	-	2.0	V
545 to 552	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	-	−20	µA
553 to 560	Output Leakage Current Third State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	-	20	µA
561	Supply Current 1 (During BIST)	I_{DDS1}	As per Table 2	As per Table 2	-	60	mA
562	Supply Current 2 (During Normal Operation)	I_{DDS2}	As per Table 2	As per Table 2	-	15	mA

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
609 to 611	$\overline{\text{RESET}}$ Activated	t_{RES}	As per Table 2	As per Table 2	$4t_{BCK}$	-	-
612 to 614	Clock Period for CLK	t_{CLK}	As per Table 2	As per Table 2	80	-	ns
615 to 617	Clock Low Pulse Width for CLK	t_{CLO}	As per Table 2	As per Table 2	40	-	ns
618 to 620	Clock High Pulse Width for CLK	t_{CHI}	As per Table 2	As per Table 2	40	-	ns
621 to 623	Clock Period for BITCLK	t_{BCK}	As per Table 2	As per Table 2	$4t_{CLK}$	-	-
624 to 626	Clock Low Pulse Width for BITCLK	t_{BLO}	As per Table 2	As per Table 2	$4t_{CLO}$	-	-
627 to 629	Clock High Pulse Width for BITCLK	t_{BHI}	As per Table 2	As per Table 2	$4t_{CHI}$	-	-
630 to 632	Clock Period for SCLK	t_{SCK}	As per Table 2	As per Table 2	$t_{CLK}/2$	-	-
633 to 635	Clock Low Pulse Width for SCLK	t_{SLO}	As per Table 2	As per Table 2	20	-	ns
636 to 638	Clock High Pulse Width for SCLK	t_{SHI}	As per Table 2	As per Table 2	20	-	ns
639 to 641	$\overline{\text{CS}}$ Cycle Time	t_1	As per Table 2	As per Table 2	$4t_{CLK}$	-	-
642 to 644	$\overline{\text{VPD}}$ Active to $\overline{\text{CS}}$ Active	t_2	As per Table 2	As per Table 2	5.0	-	ns
645 to 647	$\overline{\text{CS}}$ Pulse Width Activated	t_3	As per Table 2	As per Table 2	30	-	ns
648 to 650	$\overline{\text{CS}}$ Pulse Width De-activated	t_4	As per Table 2	As per Table 2	30	-	ns

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
651 to 653	$\overline{CS}$ De-activated to $\overline{VPD}$ De-activated	t_5	As per Table 2	As per Table 2	0	-	ns
654 to 656	$\overline{VPD}$ Pulse Width De-activated	t_6	As per Table 2	As per Table 2	$2t_{CLK}$	-	-
657 to 659	D Setup Time	t_7	As per Table 2	As per Table 2	8.0	-	ns
660 to 662	D Hold Time	t_8	As per Table 2	As per Table 2	15	-	ns
663 to 665	$\overline{CS}$ De-activated to $\overline{BUSY}$ Activated	t_9	As per Table 2	As per Table 2	-	50	ns
666 to 668	$\overline{BUSY}$ Pulse Width Activated	t_{10}	As per Table 2	As per Table 2	$3t_{CLK}$	$4t_{CLK}$	-
669 to 671	$\overline{CS}$ De-activated to VCAR De-activated	t_{11}	As per Table 2	As per Table 2	2.5 t_{CLK}	3.5 t_{CLK}	-
672 to 674	CLK Low to VCAR Valid	t_{12}	As per Table 2	As per Table 2	-	50	ns
675 to 677	ERT High to VCAR Low	t_{13}	As per Table 2	As per Table 2	-	50	ns
678 to 680	ERT Low to VCAR Valid	t_{14}	As per Table 2	As per Table 2	-	50	ns
681 to 683	SVALID High to SCLK High	t_{15}	As per Table 2	As per Table 2	50	-	ns
684 to 686	SCLK High to SVALID Low	t_{16}	As per Table 2	As per Table 2	50	-	ns
687 to 689	SVALID Pulse Width De-activated	t_{17}	As per Table 2	As per Table 2	$2t_{CLK}$	-	-
690 to 692	SIN Setup Time	t_{18}	As per Table 2	As per Table 2	5.0	-	ns

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
693 to 695	SIN Hold Time	t_{19}	As per Table 2	As per Table 2	15	-	ns
696 to 698	CLK High to RA Valid	t_{20}	As per Table 2	As per Table 2	-	50	ns
699 to 701	CLK Low to $\overline{RCS}$ Valid	t_{21}	As per Table 2	As per Table 2	-	52	ns
702 to 704	CLK Low to R/$\overline{W}$ Low	t_{22}	As per Table 2	As per Table 2	-	52	ns
705 to 707	CLK Low to R/$\overline{W}$ High	t_{23}	As per Table 2	As per Table 2	-	52	ns
708 to 710	CLK Low to $\overline{OE}$ Low	t_{24}	As per Table 2	As per Table 2	-	52	ns
711 to 713	CLK Low to $\overline{OE}$ High	t_{25}	As per Table 2	As per Table 2	-	52	ns
714 to 716	CLK Low to RD Write Data Valid	t_{26}	As per Table 2	As per Table 2	-	56	ns
717 to 719	CLK High to RD 3-State	t_{27}	As per Table 2	As per Table 2	-	40	ns
720 to 722	Read Data Setup Time	t_{28}	As per Table 2	As per Table 2	19	-	ns
723 to 725	$\overline{OE}$/$\overline{RCS}$ High to RD Invalid	t_{29}	As per Table 2	As per Table 2	0	-	ns
726 to 728	$\overline{ERT}$ High to RA, $\overline{RCS}$, R/$\overline{W}$, $\overline{OE}$, RD 3-State	t_{30}	As per Table 2	As per Table 2	-	30	ns
729 to 731	$\overline{ERT}$ Low to RA, $\overline{RCS}$, R/$\overline{W}$, $\overline{OE}$, RD Valid	t_{31}	As per Table 2	As per Table 2	-	30	ns
732 to 734	CLK Low to $\overline{ERR}$ Valid	t_{32}	As per Table 2	As per Table 2	-	50	ns

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING (CONT'D)

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN.	MAX.	
735 to 737	ERT High to $\overline{ERR}$ Low	t_{33}	As per Table 2	As per Table 2	-	43	ns
738 to 740	ERT Low to $\overline{ERR}$ Valid	t_{34}	As per Table 2	As per Table 2	-	43	ns
741 to 743	ERT High to RTS Low	t_{35}	As per Table 2	As per Table 2	-	39	ns
744 to 746	ERT Low to RTS Valid	t_{36}	As per Table 2	As per Table 2	-	39	ns
747 to 749	CLK High to RTS Stable	t_{37}	As per Table 2	As per Table 2	-	52	ns
750 to 752	CTS Setup Time	t_{38}	As per Table 2	As per Table 2	6.0	-	ns
753 to 755	CLK High to PVCF Stable	t_{39}	As per Table 2	As per Table 2	-	48	ns
756 to 758	POLL Setup Time	t_{40}	As per Table 2	As per Table 2	5.0	-	ns
759 to 761	POLL Hold Time	t_{41}	As per Table 2	As per Table 2	10	-	ns
762 to 764	CLK High to TIME Active	t_{42}	As per Table 2	As per Table 2	-	50	ns
765 to 767	CLK High to RANDOM Valid	t_{43}	As per Table 2	As per Table 2	-	50	ns
768 to 770	IFILL Setup Time	t_{44}	As per Table 2	As per Table 2	10	-	ns
771 to 773	IFILL Hold Time	t_{45}	As per Table 2	As per Table 2	5.0	-	ns

APPENDIX 'A'

AGREED DEVIATIONS FOR MITEL (S)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.2	Paragraph 4.4 - Marking (plus Serialisation for Level B): May be performed to follow Paragraph 9.3 (Encapsulation). Paragraph 9.1 - Visual Inspection MIL-STD-883C, Method 2010.10, Paragraph 3.1.3: Scribing and die defects, "high magnification": Clauses c and d shall not be applicable for the device. Instead, the following criteria shall be used: - No device shall be acceptable if it exhibits cracks that:- (a) Come closer than 0.25mil to any operating metallisation or other functional circuit element. (b) Exceed 3.0mil in length pointing toward any operating metallisation or other functional circuit element. - For areas which are metallised, MIL-STD-883C, Method 2010.10, Paragraph 3.1.3 d is applicable without exception.
Para. 4.2.3	Paragraph 9.12 - Radiographic Inspection (a) ESA/SCC Basic Specification No. 20990, Paragraph 4.1: Inspection for foreign particles, voids and seal defects only may be performed. (b) Para. 9.9.2, Electrical Measurements at High and Low Temperatures: May be performed after Paras. 9.8.1 and 9.8.2, Seal Test.
Para's 4.2.4 and 4.2.5	Paragraph 9.18 - Solderability (a) A manually controlled dipping device may be used.

The following test patterns may be used:-

1. PRODUCTION TEST PATTERN

30k of test vectors are used for the production test of the VCA. The test is combined from 6 different test stimuli: Pad-to-chip-test (88 test vectors), production selftest (5017 test vectors), s01-1 of the compliance matrix (3270 test vectors), functional-test-207 (3440 test vectors), functional-test-1103 (10k test vectors).

The pad-to-chip-test checks the path: External chip input pin → VCA core → [Input Register] → internal Output Registers → VCA output pin.

N.B. Some static input pins are not buffered in input registers.

The production selftest is the selftest with toggling output pads except for the PVCF and RTS pins.

The s01-1 is taken from the compliance matrix. It runs in serial input mode and CLKMODE = "1". One frame is read in and the first 8 octets are given out by the PVCF pin.

APPENDIX 'A'

Functional – test – 207 is a test with idle packet insertion, frame inputs and outputs, where PPROG = "1"; FECW = "1"; OPCF = "1"; LEN = "0"; SYNCF = "0"; SECHEAD = "1"; PKTVER = "0"; PKTORD = "0".

Functional – test – 1103 is a test with idle packet insertion, frame inputs and outputs, where PPROG = "1"; FECW = "1"; OPCF = "1"; LEN = "3"; SYNCF = "0"; SECHEAD = "1"; PKTVER = "0"; PKTORD = "0".

Para – test is a parametric test. All inputs, except ERT, including RD (input direction), are logical and combined. The input level sweeps very slowly (against gate delay time) to its alternate state and then slowly returns to test the input buffers.

The strategy for production test is to first run the production – selftest and then run a number of functional test programmes after production BIST is completed. In contrast to the selftest in production – selftest, all outputs are externally visible to increase the fault coverage and to decrease the simulation time for a BIST run. After the production test BIST (production – selftest) is finished, 4 functional test programmes are applied to the VCA inputs to detect faults not covered by the BIST. Since the BIST has already detected 89.7% of faults, the additional fault runs were applied as incremental fault runs, only simulating the remaining undetected faults. All the additional patterns start with reset and are independent from each other.

2. FUNCTIONAL TEST PATTERNS

TEST NAME	NUMBER OF TEST VECTORS
busy	108
cslong	74
csshort	959
ert	20
poclk	931
poll	11453
psft	4997
s01	1856
sclkh	99
sclkl	99
slft	4589
t1103	9999
t207	3439