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EUROPEAN SPACE AGENCY CONTRACT REPORT

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Title

28F800CV-B, 8 MBIT FLASH FROM INTEL

TOTAL IONISING DOSE CHARACTERIZATIONTEST REPORT

ESA/ESTEC Contract No. 11755/95/NL/NB-WO1/CO1

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Document type	Nb WBS	Summary : Low voltage memories were tested under total ionising dose irradiation to study the effect of supply voltage on the radiation sensitivity. This report presents the results obtained on 8 Mbit INTEL FLASH.

SUMMARY OF RESULTS

Test sample characteristics :

Part Name :	28F800CV-B	Function :	1 M x 8 Flash
Technology :	CMOS, 0.5 µm	Package :	48-pin plastic TSOP
Manufacturer :	Intel	Location :	USA
Sample size :	3 (5 V), 3 (3.3 V)	Date Code :	95XX

TID results

Functional test

The following table indicates the results of functional test:

S/N	V_{CC} V	Dose at erasure failure krad(Si)	Annealing	Remarks
09	5	15.2	No functional recovery	Erasure failure
10	5	15.2	No functional recovery	Erasure failure
11	5	15.2	No functional recovery	Erasure failure
27	3.3	14.8	No functional recovery	Erasure failure
28	3.3	14.8	No functional recovery	Erasure failure
29	3.3	14.8	No functional recovery	Erasure failure

Only erasure failures were detected. No read nor write error occured during the test up to the maximum dose.

Functional test conclusion

The results of these experiments demonstrate that on the average 8 Mbit Flash 28F800CV-B from Intel, there is no difference in radiation sensitivity in terms of erasure failure.

Parametric test

The following table summarises the average dose levels for both bias at which sensitive parameters have drifted **20%**:

Symbol	Parameter	Dose Level/krad(Si)	
		V_{CC} = 5 V	V_{CC} = 3.3 V
I_{CCSB}	Standby Supply Current	10	15
I_{CCOP}	Operating Supply Current	10	15
I_{IL}	Input Current Low Level	20	20
I_{IH}	Input Current High Level	20	20
I_{OZL}	Output Leakage Current High Impedance Low level Applied	30	>60
I_{OZH}	Output Leakage Current High Impedance High Level Applied	20	20
V_{OL}	Output Voltage Low Level	12	12
V_{OH}	Output Voltage High Level	12	12
T_{ACS}	Chip Select Access Time	35	35

Before the erasure failure, the parameters are rather insensitive to dose. After the erasure failure, the change in output voltage parameters at 15 krad(Si) is evident and at 30 krad(Si) the supply current parameters have increased considerably. However, due to the loss of functionality the parameters do not describe the proper behaviour of the devices. No device recovered in the high temperature annealing.

Parametric test conclusion

The results of these experiments demonstrate that 8 Mbit Flash 28F800CV-B from Intel biased at 5 V is slightly more sensitive to ionising radiation than when biased at 3.3 V.

DOCUMENT CHANGE LOG

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Issue of this document comprises the following pages at the issue shown

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1. INTRODUCTION

The aim of this work is to investigate radiation effects in low voltage technologies. The study is focused on memory devices, which require lower voltage to achieve higher integration. Parts selected consists of SRAMs (1 Mbit, 2 types), DRAMs (16 Mbit, 2 types), and FLASH memories (8 Mbit, 2 types).

The object of this document is to describe the irradiations performed on the Intel 8 Mbit 28F800CV-B, in order to measure the influence of two different supply voltage levels on the total ionising dose sensitivity.

Irradiations were performed in March 1997 (10th-17th) according to the procedures referenced in the following paragraph.

This work was performed in the frame of the WO1/CO1 for ESTEC Contract n°11755/95/NL/NB.

2. REFERENCE DOCUMENTS

[1] ESA/SCC 22900-4 ESA Basic Specification for Total Dose Steady-State Irradiation

[2] Intel Manufacturer Data Sheet

[3] Description of the VTT memory tester, AUT/PRO/76/96 (in Finnish)

3. PART DETAILS

3.1. DEVICE IDENTIFICATION

3.1.1. References

Type	:	28F800CV-B
Manufacturer	:	Intel
Place	:	USA
Packaging	:	48-pin plastic TSOP

3.1.2. Function

1 M x 8 Flash

3.1.3. Technology

CMOS, 0.5 µm (See next page for further details)

3.1.4. Part Procurement

Origin	:	VTT Automation, Finland
Level	:	Standard Level
Temperature range	:	-25°C, +85°C (Industrial)
Date code	:	-
Screening	:	/
Sample size	:	3 (biased at 5 V), 3 (biased at 3.3 V)
Manufacturer Marking	:	Intel E28F800 CVB70 U6250516A M C '92'95 Flash (Package)
Detailed specifications	:	Manufacturer Data sheet

3.1.5. Previous TID details/history

No radiation data on this device

3.2. TECHNICAL INFORMATION

The 8 Mbit 28F800CV-B Flash from Intel is a device with wide supply voltage range. The device can be operated at 3.3V or at 5V.

The functionality and the parametric integrity of the devices were examined prior to irradiation. No screening nor burn-in were carried out during this study.

General information

Name	Intel 28F800CV-B
Package Marking	Intel E28F800 CVB70 U6250516A Θ © '92'95 Flash
Access time/ns at 5V	70
Temperature range/°C	-25, +85
Organisation	1 M x 8
Supply Voltage/V	2.7-5.5

Technology

Name	Intel 28F800CV-B
CMOS	yes
Mask	*
Epitaxial layer	*
Design rules	*
Die size	*
Cell type	*
Cell size	*

* The missing information was unsuccessfully required from the manufacturer.

4. TEST DESCRIPTION

4.1. IRRADIATION FACILITY

Name MMS Cobalt 60-source, model Shepherd 484

Location Matra Marconi Space France
37, avenue Louis Bréguet
78146 VELIZY-VILLACOUBLAY Cedex
France

Activity < 8.9 curies.

Calibration 10/03/97.

4.2. TID TEST SET-UP

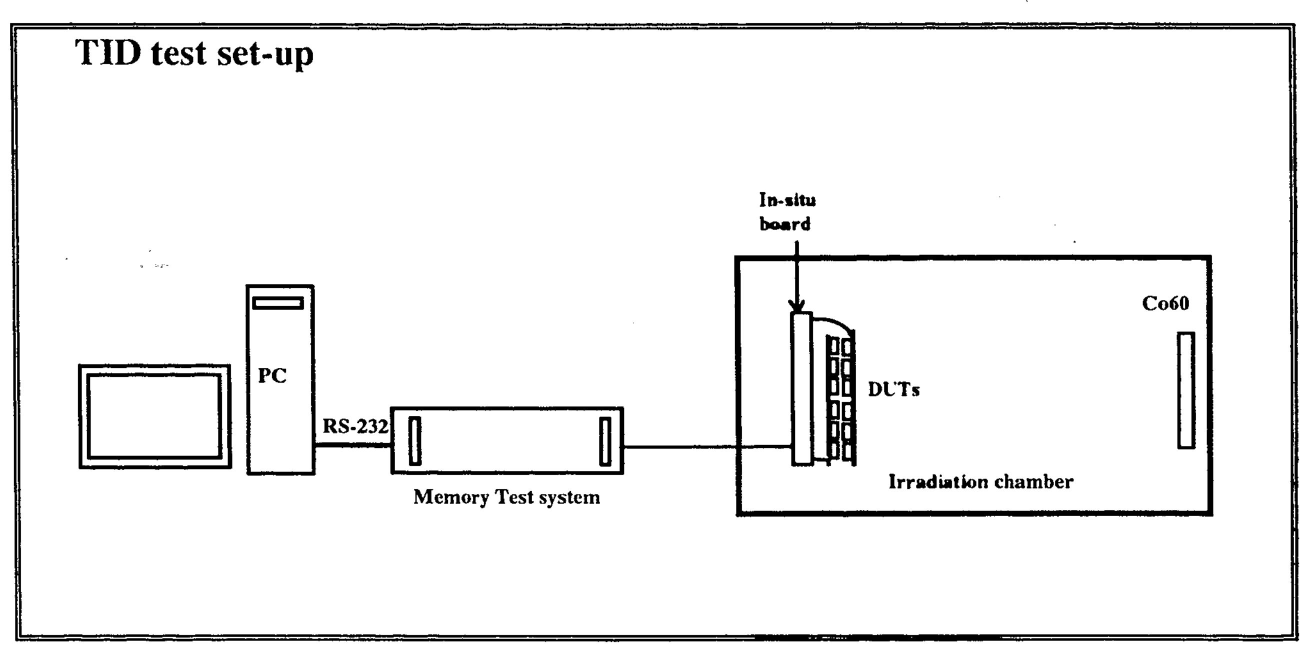

Fig. 4.1. Description of the TID test set-up.

The DUTs were soldered on small PCB's with pin headers. They were mounted on the two large PCBs that were biased at 5 V and 3.3 V. The distance between 5 V and 3.3 V devices were 2 mm from package to package. The difference in dose rates was taken into account when computing the doses received by the devices.

The device under test was selected by a chip select logic located in the In-situ board. The supply voltage was provided by the memory tester. A complete description of the memory tester is given in [3].

The test flow chart is given in fig. 4.2.

Test sequence for FLASH

Set parameters for selected DUT

Radiation?

Yes

No

Initialize DUT

Read DUT and compare with CB-pattern

Continue test for another DUT

Initializion sequence

Set address=0

Erase DUT

Write CB-pattern to addr

Increase address

End of DUT?

No

Yes

Continue test

Read sequence

Set address=0

Read current address and compare it

Error?

Yes

Reread current address

Read current addr. again

Store error to logfile

No

Increase address

End of DUT?

No

Yes

Continue test

Fig. 4.2. The test flow chart of an individual device with write and read sequencies.

The write and read cycles during functional test were as follows:

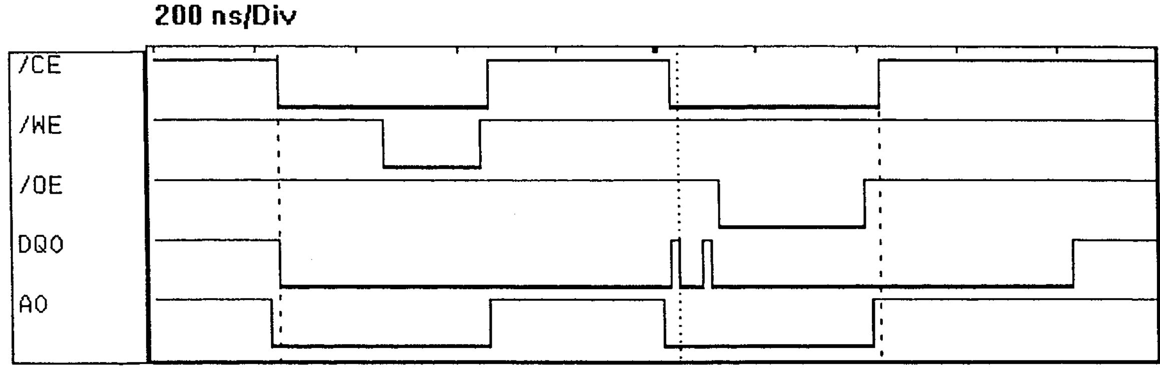

Fig. 4.3. Write Cycle of Intel Flash device during functional test.

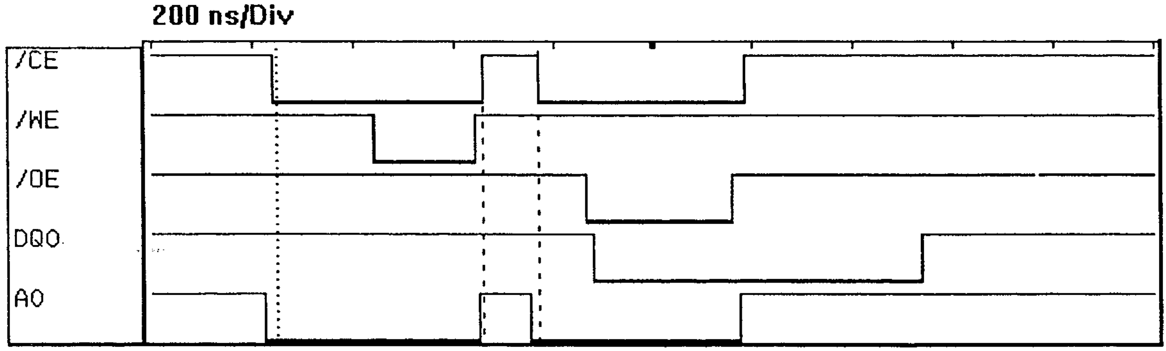

Fig. 4.4. Read Cycle of Intel Flash device during functional test.

5. TOTAL IONISING DOSE EXPERIMENTAL RESULTS

5.1. TID IRRADIATION TEST SEQUENCE

During irradiation all the devices were functionally tested 3 times per hour automatically in the exposure chamber, and the results were stored on a hard disk of the measuring computer. The memory test started with the write of a CB (checkerboard) pattern to the memory device. The erasure time of the devices was 45 s anf the write time of a device was approx. 7 s. Thereafter the memory contents of the device was read and it was compared to the original pattern. In-situ in the irradiation chamber the memory devices were only read. Prior to the parametric tests, the devices were systematically erased and rewritten. During the irradiation, the memory contents was the CB pattern.

If errors were encountered, the corrupted data was immediately reread. Due to the limitation of the measuring computer, the maximum number of recorded corrupted bytes was set to 100. TTL levels were applied in control, address and data signals. 5 V bias was applied to devices s/n 09-11 and 3.3 V bias was applied to devices s/n 27-29.

In the time between the irradiation, the parameters were measured (after erasure and rewritting of the CB pattern) remotely at the end of each step within two hours with the VTT parametric tester in another room. Except the measurement, the devices were unbiased during this time. The resolution of the voltage measurements was better than 1 mV.

The irradiation was accomplished in seven steps. The average dose rates were 390 rad(Si)/h and 380 rad(Si)/h for 5 V and 3.3 V devices, correspondingly The dose rates and cumulative doses with durations of each irradiation are given in table 5.1.

Table 5.1. Dose rates, durations and cumulative doses for 5 V and 3.3 V Intel Flash.

Step	Dose rate 5 V rad(Si)/h	Dose rate 3.3 V rad(Si)/h	Duration h	Total Dose 5 V krad(Si)	Total Dose 3.3 V krad(Si)
1	262	258.1	20.00	5.2	5.1
2	327.5	317.3	19.00	11.5	11.2
3	471.6	458.1	8.00	15.2	14.8
4	471.6	458.1	12.00	20.9	20.4
5	471.6	458.1	19.17	29.9	29.1
6	471.6	458.1	7.18	33.3	32.4

The devices were irradiated only to 33.3 krad(Si) for 5 V and 32.4 krad(Si) for 3.3 V devices because their supply current consumption was 220 mA and 100 mA, correspondingly and the surface temperature was approx. 90°C. After a 60 h unbiased period, the devices were were put into a heat chamber for an annealing period of 168 h at 85°C. The devices were biased continously and

5.1.1. Problems encountered/Discussion

No specific problem was encountered during irradiations.

5.2. TID TEST RESULTS

Functional test

The following table summarises the functional test result:

Table 5.2. Failure doses.

S/N	V_{CC} V	Dose at erasure failure krad(Si)	Annealing	Remarks
09	5	15.2	No functional recovery	Erasure failure
10	5	15.2	No functional recovery	Erasure failure
11	5	15.2	No functional recovery	Erasure failure
27	3.3	14.8	No functional recovery	Erasure failure
28	3.3	14.8	No functional recovery	Erasure failure
29	3.3	14.8	No functional recovery	Erasure failure

The devices failed due to the erasure failure that occured during parametric test. No read errors were encountered during irradiation.

Further tests need to be done to reveal if there is difference in read errors.

Functional test conclusion

The results of these experiments demonstrate that, there is no difference in radiation sensitivity of 8 Mbit Flash 28F800CV-B from Intel in terms of erasure failure.

Parametric test

The following table summarises the average dose levels for both bias at which sensitive parameters have drifted **20%**:

Symbol	Parameter	Dose Level/krad(Si)	
		V_{CC} = 5 V	V_{CC} = 3.3 V
I_{CCSB}	Standby Supply Current	10	15
I_{CCOP}	Operating Supply Current	10	15
I_{IL}	Input Current Low Level	20	20
I_{IH}	Input Current High Level	20	20
I_{OZL}	Output Leakage Current High Impedance Low level Applied	30	>60
I_{OZH}	Output Leakage Current High Impedance High Level Applied	20	20
V_{OL}	Output Voltage Low Level	12	12
V_{OH}	Output Voltage High Level	12	12
T_{ACS}	Chip Select Access Time	35	35

Before the erasure failure, the parameters are rather insensitive to dose. After the erasure failure, the change in output voltage parameters at 15 krad(Si) is evident and at 30 krad(Si) the supply current parameters have increased considerably. However, due to the loss of functionality the parameters do not describe the proper behaviour of the devices. No device recovered in the high temperature annealing.

Parametric test results are given as graphs in appendix 1.

Parametric test conclusion

The results of these experiments demonstrate that there is 8 Mbit Flash 28F800CV-B from Intel biased at 5 V is slightly more sensitive to ionising radiation than when biased at 3.3 V.

6. CONCLUSION

Ionising dose tests were performed on the 8 Mbit 28F800CV-B Flash from Intel with 3.3 Vand 5 V bias.

The erasure failure makes the comparison of the devices difficult. In terms of erasure failure, there is no difference. However, the effect of supply voltage tends to modify the TID sensitivity: the 5 V devices are more sensitive to dose in terms of parametric changes.

APPENDIX 1. Parametric test results for Intel Flash devices.

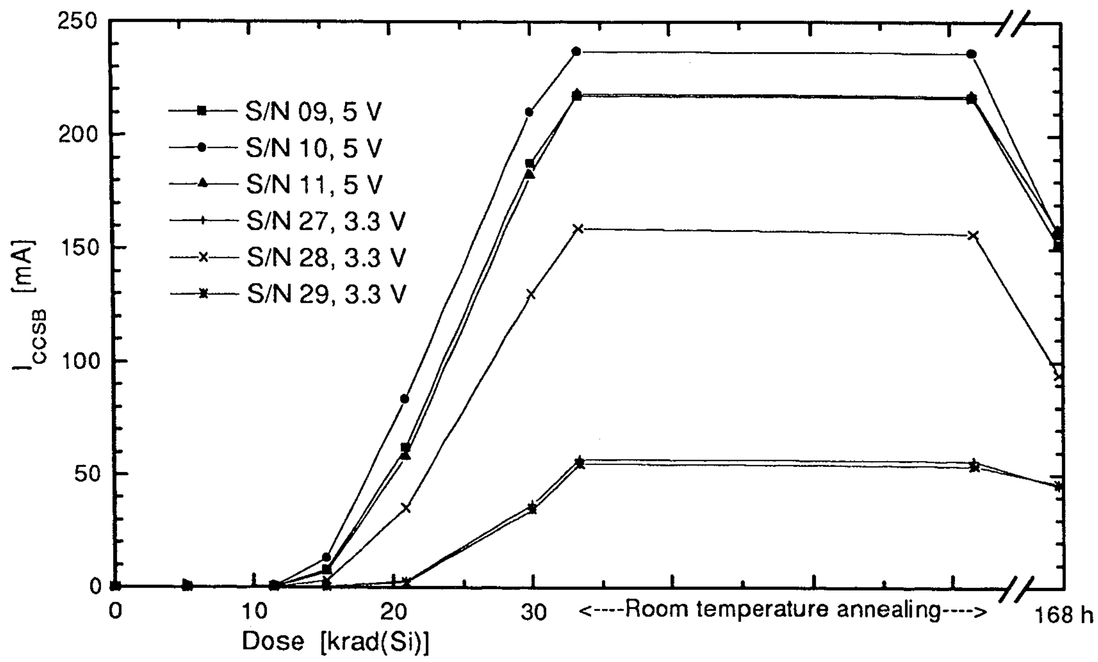

Fig. 1. Standby supply current versus dose and after annealing for Intel Flash devices.

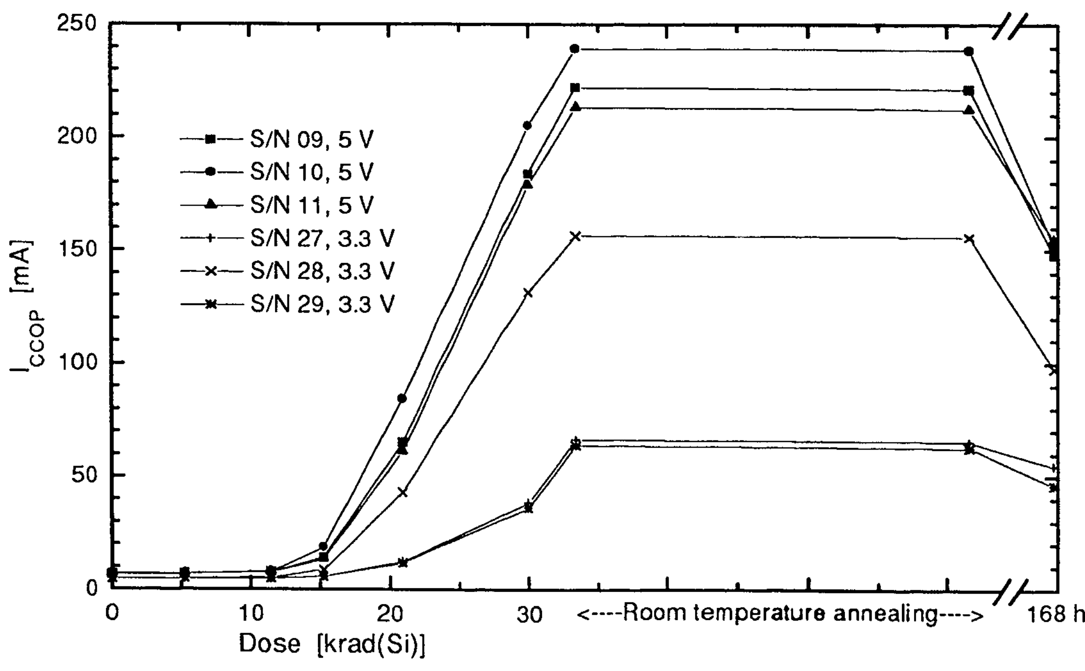

Fig. 2. Operating supply current versus dose and after annealing for Intel Flash devices.

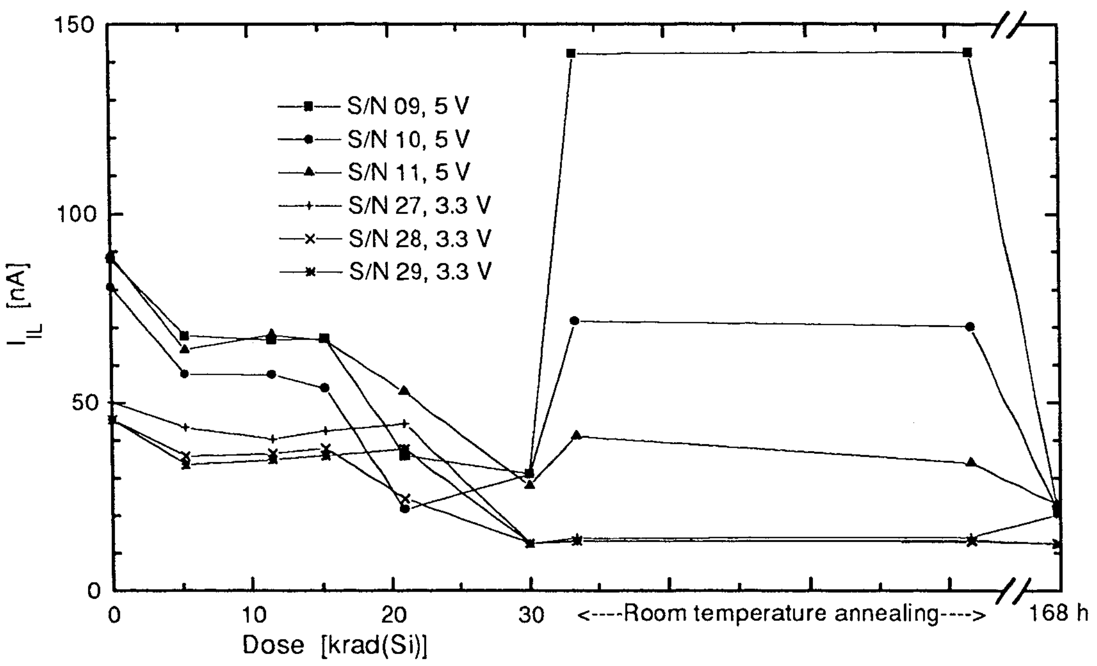

Fig. 3. Input current low level versus dose and after annealing for Intel Flash devices.

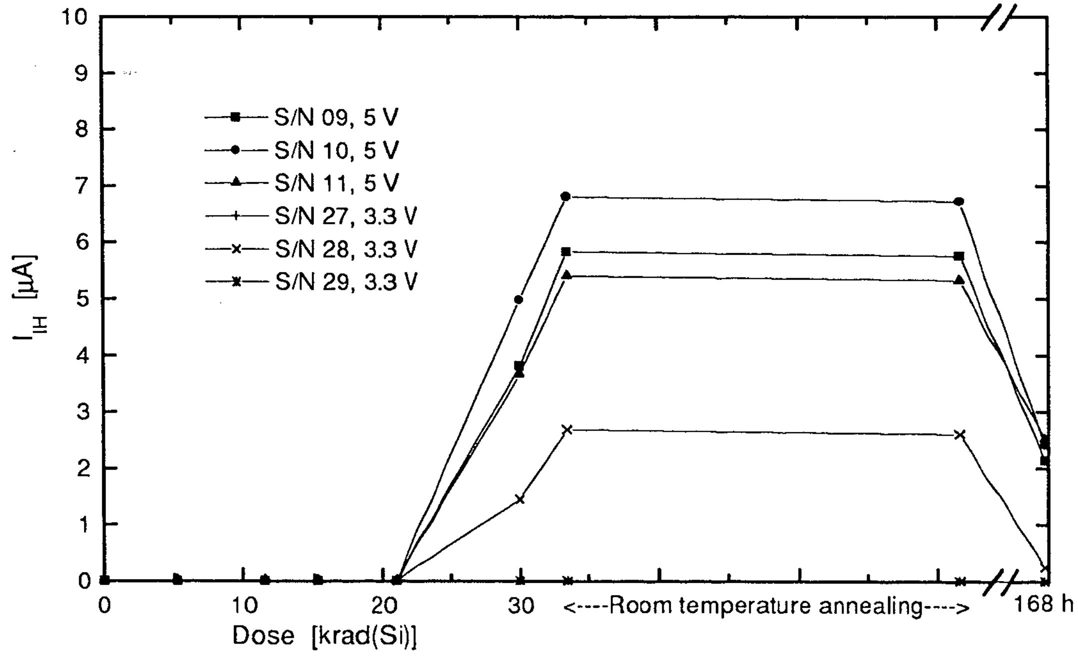

Fig. 4. Input current high level versus dose and after annealing for Intel Flash devices.

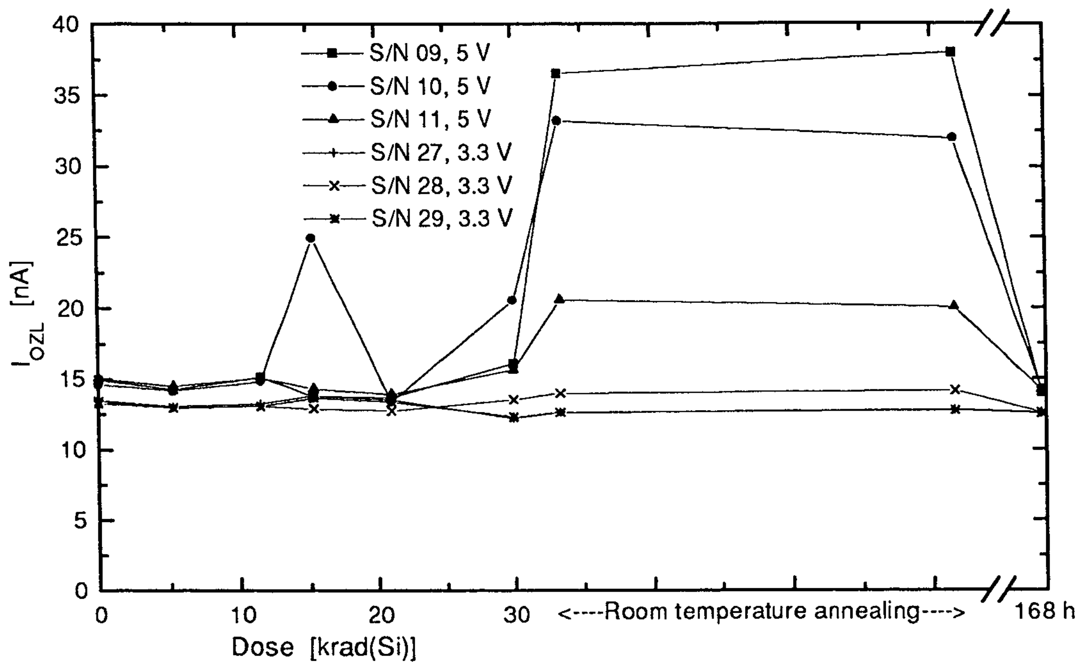

Fig. 5. Output leakage current third state low level applied versus dose and after annealing for Intel Flash devices.

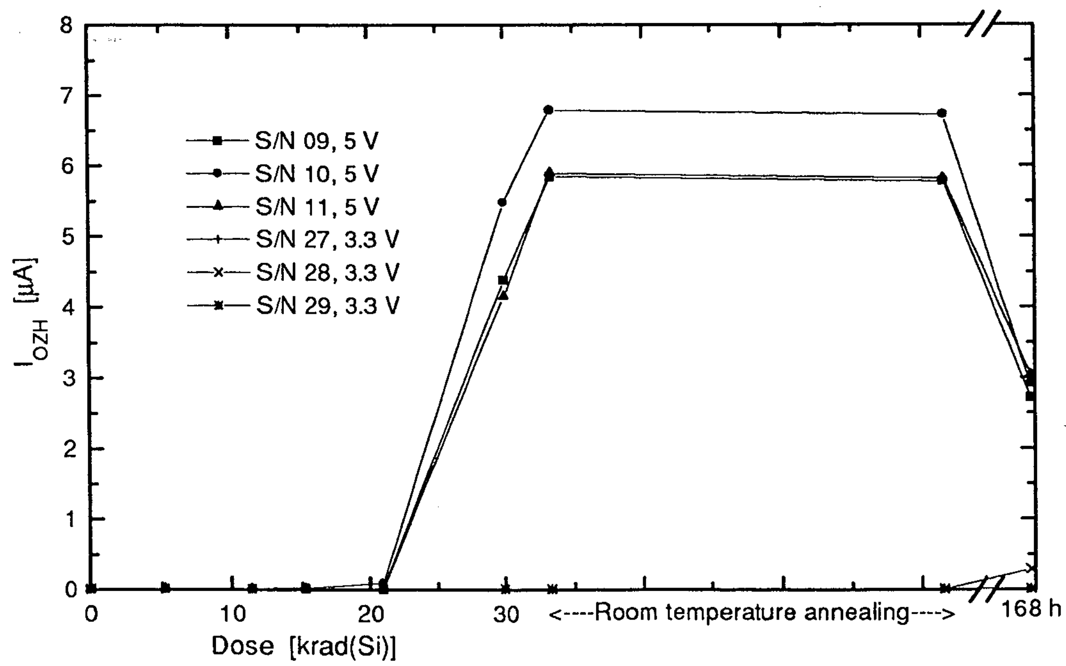

Fig. 6. Output leakage current third state high level applied versus dose and after annealing for Intel Flash devices.

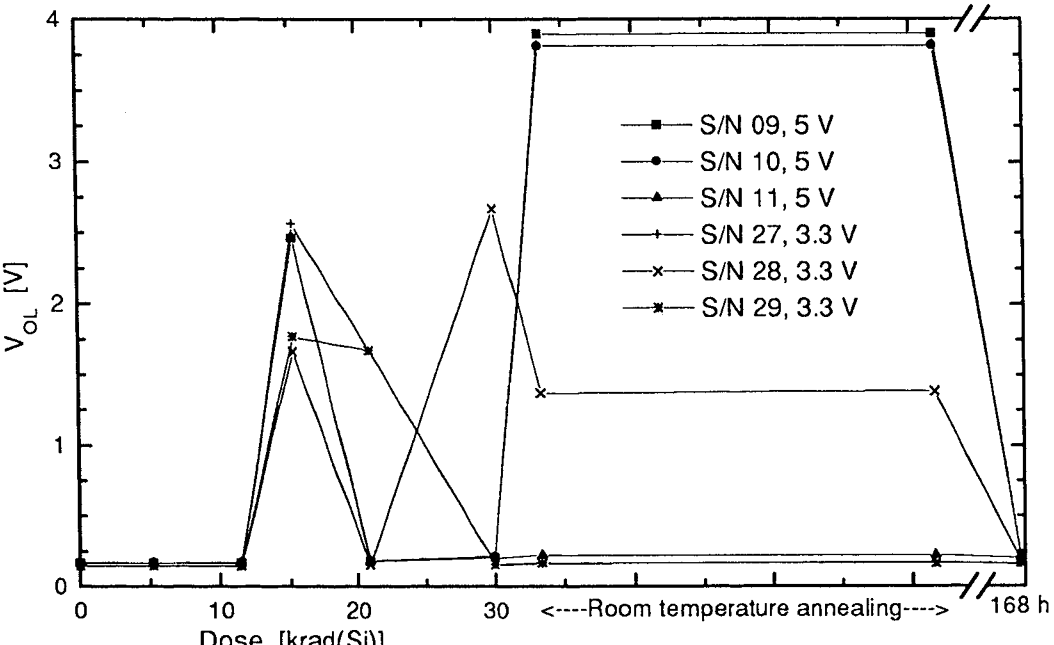

Fig. 7. Output voltage low level versus dose and after annealing for Intel Flash devices.

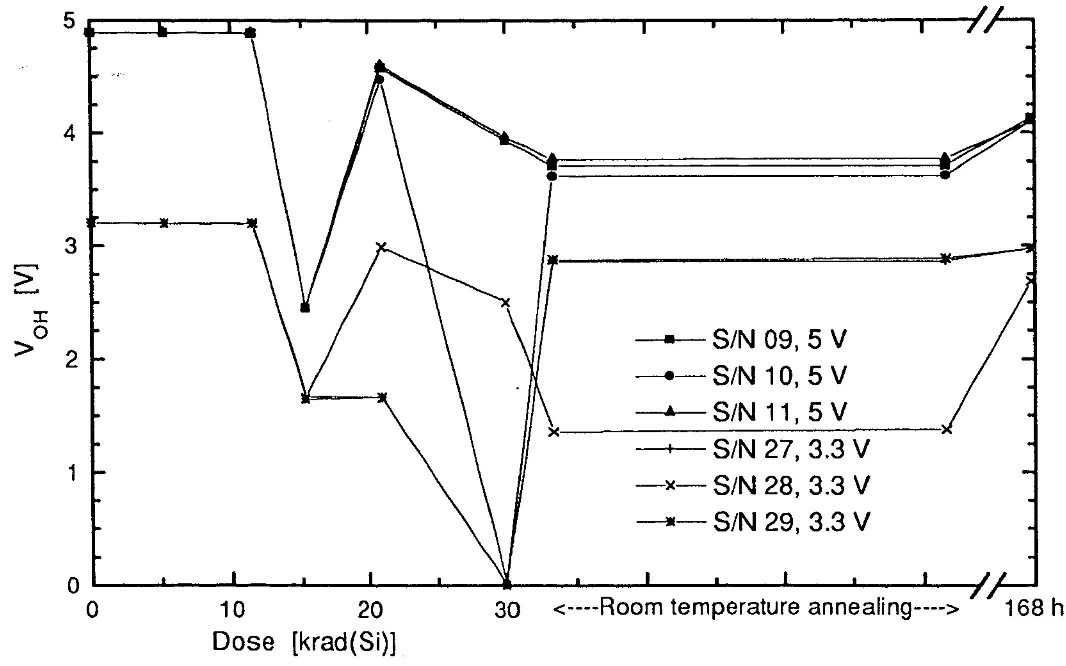

Fig. 8. Output voltage high level versus dose and after annealing for Intel Flash devices.

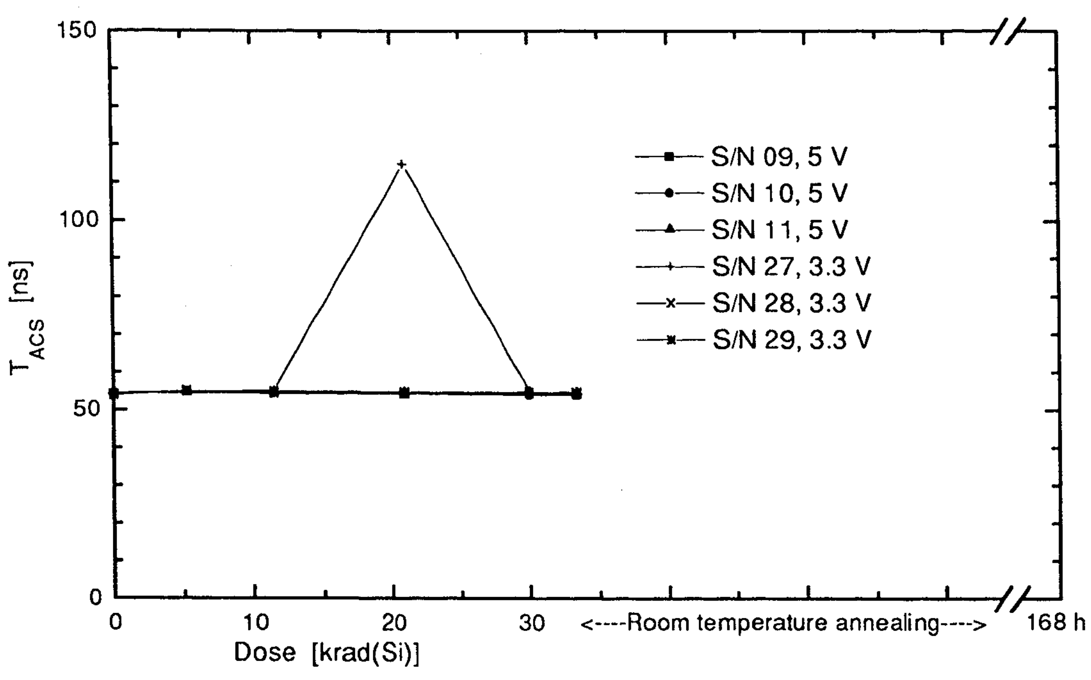

Fig. 9. Chip select access time versus dose and after annealing for Intel Flash devices.