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Work Package 5

Radiation effects on selected memory parts

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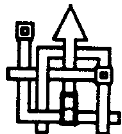

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The HITACHI devices were irradiated and characterized at the Hahn-Meitner Institut in Berlin. Unlike the SEEQ parts, they were not cycled during irradiation and only a limited electrical characterization was done at intermediate total doses. The test sequence and results are presented in the second part of this report.

PART 1: SEEQ DM258C256-250

1. Test description and set-up

1.1. Introduction

The aim of the test exercise was not to test for all possible applications of EEPROMs in a radiation environment, but rather to perform a limited test in order to obtain a first assessment of the radiation behaviour of this type of memories. Despite the limited aim of the exercise, the test plan was conceived in such a way that information could be obtained on various parameters that can influence the radiation behaviour, such as the programming and the read frequency, the bit pattern, the operation mode of the memory (writing or reading) and possible annealing or rebound effects.

The radiation tests were performed using the ESTEC Co-60 gamma radiation source. This source provides a collimated beam of approximately 30° into a room of max. 6m. The areas covered are 28 X 20 cm^2 at the exit of the collimator window to 250 X 200 cm^2 at the end of the room. The parts were tested in an in-situ and in a remote mode. Remote testing was done on the Tektronix VLSI-tester. In-situ tests were performed using a dedicated and newly designed test system. This system allowed real time monitoring, ability to control the programming frequency, the possibility to use various bit patterns and to test only a limited part of the memory.

1.2. Dose and dose rate.

The devices were irradiated up to a total dose of 18krad(Si). At that level, they had all failed. The dose rate used was 92 rad(Si)/min, which was the maximum value that could be achieved. Testing at lower dose rates is only meaningful if the dose rate can be changed by an order of magnitude. This was unrealistic in view of the limited test time, so the tests were performed at one dose rate only. A calibrated standard ion chamber was used for dosimetry with an accuracy of better than 2 %. The particular ion chamber/electronic combination is calibrated to 0.5 %.

1.3. Programming and read frequencies.

Three programming frequencies were used and tested simultaneously. From results in the literature, total doses of 40 krad were expected to be sufficient, so a maximum total dose of 40 krad(Si) was taken into account when making the test plan. Since a maximum of 10,000 cycles were allowed within the total test time, the maximum allowable frequency was 10,000 cyles/435 min, or 23 cycles/min. However, when testing 12 parts simultaneously (which was the case in our test), this would lead to a complete cycle time (writing and reading of 12 parts) of 41 seconds, representing a maximum programming frequency of about 1.5 cycles/min, a value that is mainly limited by the time necessary for sequential reading of the parts. In order to solve this problem, it was decided to read the memory after each write cycle, but to avoid performing the write and read cycles on all 32 kbytes of the memory. The number of bytes written and read each cycle was limited in such a way that a maximum programming frequency of about 20 cycles/min could be obtained. The two other frequencies were chosen to be one and two decades lower, i.e. 2 cycles/min and 0.2 cycles/min (or 1 cycle/5min) respectively. The bytes were read immediately before and after each write cycle, which brought the uncertainty in determining the failure dose level (for a dose rate of 92 rad/min) to 4.6 rad for 20 cycles/min, to 46 rad for 2 cycles/min and 460 rad for 0.2 cycles/min.

1.4. Cycle sequences and bit patterns.

During irradiation, the parts were programmed and read in-situ in order to detect failures. Each memory part was devided into three blocks: a first block (4 pages) was written and read during irradiation; a second block (4 pages) was only read during irradiation, while the rest of the memory (504 pages) was initialized to a certain pattern before the test and read out at intermittent time points on the VLSI-tester (remote testing).

The fractions of the memories that were both written and read during radiation were read twice for every write cycle: a first read cycle was performed immediately after the write cycle to check the correct programming; a second read cycle was performed immediately before the next write cycle to check the ability of the bits to retain their information.

Therefore, the operation sequence for this part of the memory was as follows (W=write, R-read):

WRW R____RWR____RWR____RWR____RWR____RWR

The fractions of the memories that were only read during the irradiation were read at the same frequency as the parts that were written and read, i.e. they were read each time the other parts were read. The operation sequence was thus as follows:

WR R____R R____R R____R R____R R____R R

There were no separate memory parts that were tested completely in the read-only mode. The read-only mode was incorporated in each memory as a number of pages that were not changed during irradiation. As described above, the read frequency of these pages followed the read frequency of the pages that were written during each cycle. In this way information could be obtained on the dependence on both write and read frequencies.

So, in total 8 out of 512 pages per memory part were accessed during the test. This was done using various bit patterns. The pages and their corresponding bit patterns that were used are given in Table 1.1, together with the mode these pages were tested in. The alternation of the bit patterns occured throughout the pages as well as in time with each cycle.

When an error was detected, an error information record was written into the RAM memory of the system. Once an error had occurred in a single bit of a page, an error information record was stored after which the page was eliminated for further test. Such a page was still written and read during the test, but the result had no consequence for error storage. After detection of an error, further tests were done on the same page to distinguish between a random bit error, a full page error, an odd page error (errors occur on the odd addresses of the page) and even page errors (errors occur on the even addresses of the page).

Page nr	Bit pattern	Cycle mode
Page 1	AA-55, alternating	read/write/read
Page 2	55-AA, alternating	read/write/read
Page 3	00-FF, alternating	read/write/read
Page 4	FF-00, alternating	read/write/read
Page 5	AA-55, alternating	read-only
Page 6	00-FF, alternating	read-only
Page 7	00, All 0	read-only
Page 8	FF, All 1	read-only

Table 1.1: Bit pattern and cycle mode for the 8 pages to be accessed

1.5. Number of parts

16 memory devices were irradiated: 12 parts were tested under in-situ operation conditions (write/read and read-only), with 4 parts for each programming frequency. The four remaining parts were tested without bias (i.e. all pins grounded). This lead to four groups of devices: G1 (20 cycles/min), G2 (2 cycles/min), G3 (1 cycle/5min) and G4 (unbiased). Before the test, the parts were labeled: S41 to S44 for G1, S45 to S48 for G2, S49 to S52 for G3, S53, S54, S56 and S57 for G4

1.6. Hardware description of the test system

The hardware is based on a microprocessor-controlled system using a 6809 microprocessor. The test is started from an HP85 computer, that is located outside the radiation chamber and that is connected to the control system inside the radiation chamber through an HPIB-bus. This is shown in Fig.1.1.

As described above, 12 parts are monitored with the system. When an error is detected, several data such as address, type of error and time are stored. Therefore a board with real time clock (RTC) was made in order to store the data. This board is also provided with a RAM memory with battery back-up where all test data can be saved. A versitale Interface Adapter (VIA) forms

the interface between the micro-processor board and the board that connects the address-, data-, and control lines to the EEPROM boards. A block diagram of the test system is given in Fig. 1.2.

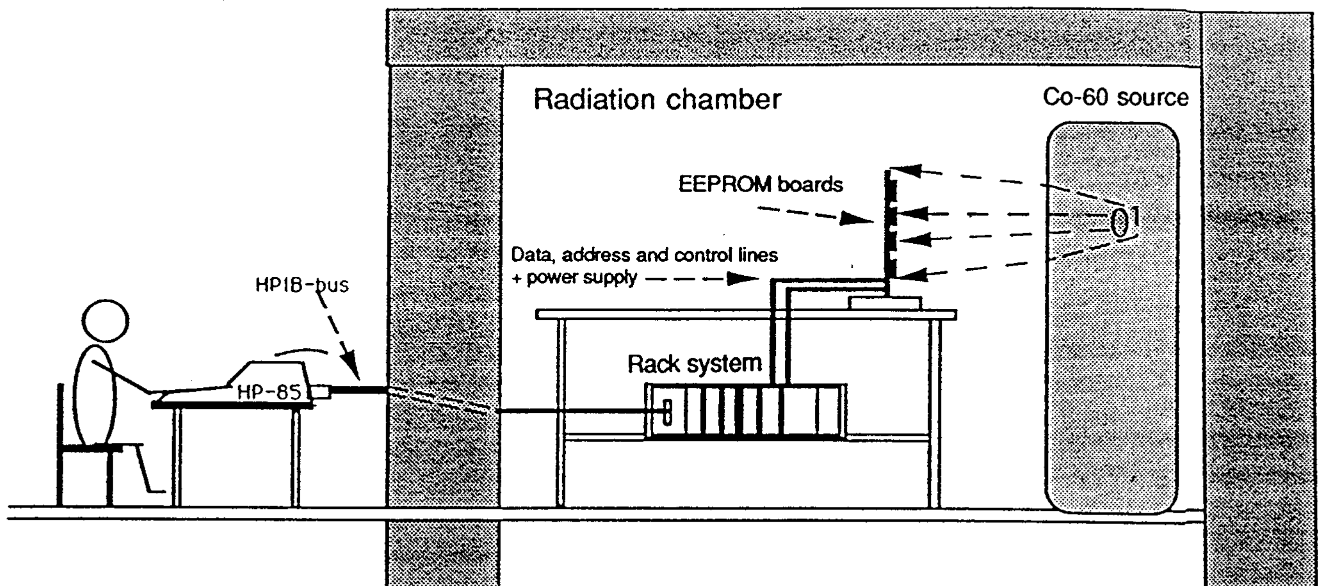

Fig. 1.1: measurement set-up

During irradiation no data can be requested with the HP-85, because of several reasons:

- Errors in the EEPROM memories can occur while the system is communicating. This would lead to uncertanties on the time and thus on the total dose.
- A communication error during reading of data can lead to loss of data stored in the RAM memory.

Therefore, in order to monitor the status of the test, a number of data are continuously provided via an LCD display. This display is, of course, located outside the radiation chamber. Because of the large distance between the LCD-display and the system inside the chamber, the data- and control signals have to be restored to their proper values. Therefore an RS422 line driver and line receiver board are available. When the irradiation is finished, more detailed information can be obtained via communication with the HP-85 computer.

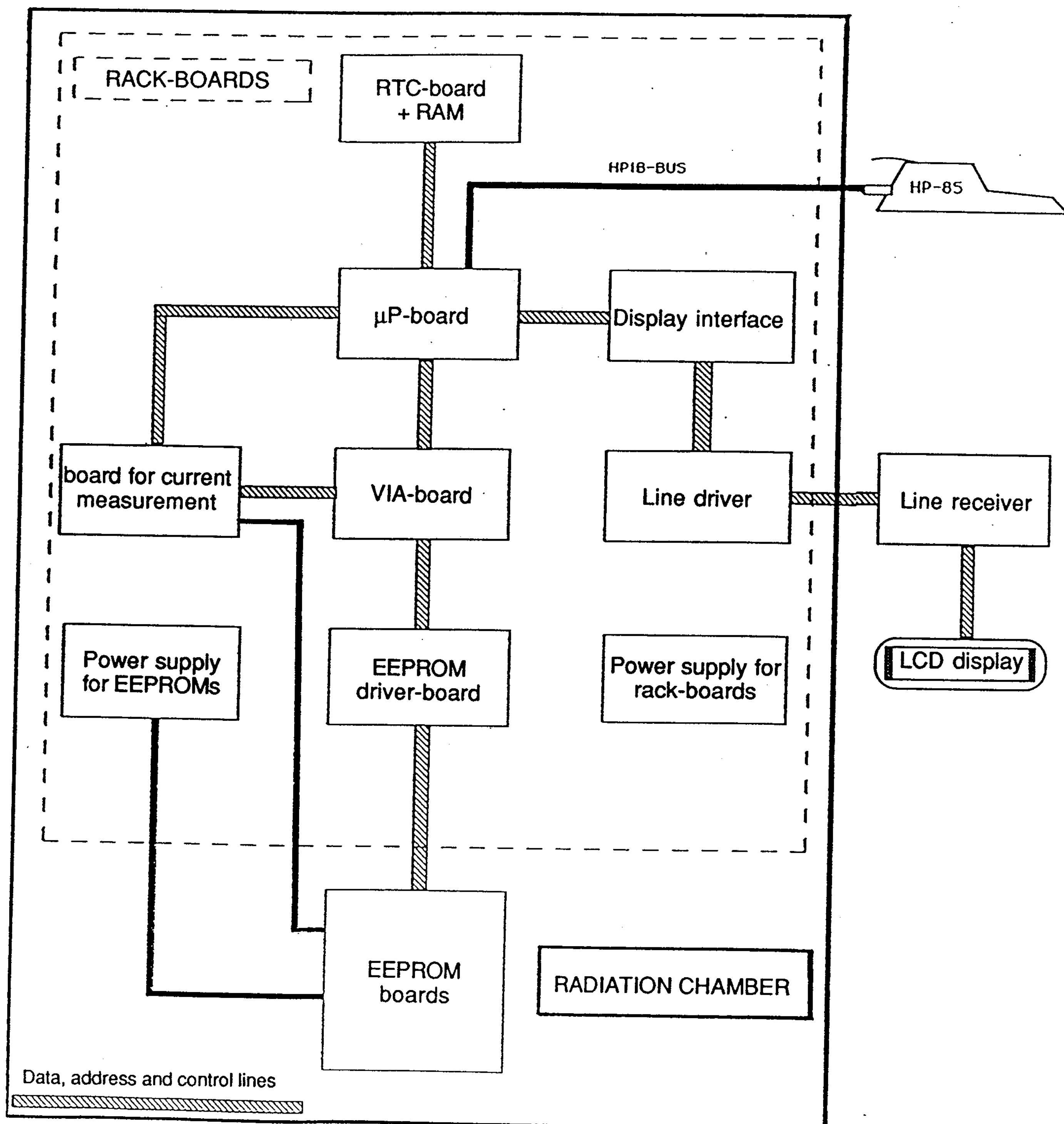

Fig. 1.2: set-up of the test system

During irradiation the supply current of the first memory part of each group is measured and displayed. A separate board was implemented to serve this purpose.

Two separate power supplies are used, one for all boards in the rack, for the display and the line receiver, and one for the boards containing the EEPROMs to be tested.

2. Experimental results

2.1. Initial characterization:

All 16 parts were initially characterized on the VLSI-tester. This characterization comprised measurement of DC and AC parameters and functional testing with writing and error locating of normal ("1") and inverse ("0") checkerboard at different supply voltages (4.5V, 5V and 5.5V) and temperatures (25°C and 125°C). After this test a checkerboard 1 bit pattern was written into the complete memory array. All devices passed this test successfully.

2.2. Irradiation

During irradiation all 16 parts were placed on one testboard: 12 parts under operating conditions with different write/read frequencies and 4 unbiased parts (grounded pins). The control circuitry together with the rest of the test system was placed on separate boards and mounted in a rack, that was placed inside the radiation chamber under shielded conditions. The test was started from an HP85 computer, that was located outside the radiation chamber and that was connected to the control system inside the radiation chamber through an HPIB-bus. As already mentioned above, only the first 8 pages of the devices of groups G1, G2, and G3 were addressed during irradiation.

The devices were irradiated up to a total dose of 18 krad. At intermittent points the radiation was interrupted to perform full characterization tests. At these points the parts of the memories that were not in-situ read and/or written, were read to detect any retention errors on the parts of the memories that were not addressed during irradiation. These memory blocks should contain checkerboard 1 patterns. Then the whole memories were tested at room temperature with measurement of DC and AC parameters, including functional testing with writing and error location. After these intermittent tests a bit pattern checkerboard 1 was again written into the complete memory arrays. The entire test sequence, along with the number of cycles applied to the several groups of devices, is depicted in Table 1.2:

Test	Accumulated total dose	# cycles G1	# cycles G2	# cycles G3	G4
Initial measurement					
Irradiation	1 krad	233	26	3	unbiased
Intermittent measurement					
Irradiation	2 krad	456	51	6	unbiased
Intermittent measurement					
Irradiation	5 krad	1113	123	13	unbiased
Intermittent measurement					
Irradiation	10 krad	2120	220	23	unbiased
Intermittent measurement					
Irradiation	18 krad	3879	410	41	unbiased
Final measurement					

Table 1.2: Test sequence and accumulated number of applied cycles

After an accumulated total dose of 18 krad(Si) all 16 memory devices had failed. An overview of the number of failing devices as a function of the total dose is listed in Table 1.3.

Total dose	# failing devices READ characterization	# failing devices FULL characterization
1 krad	0	1
2 krad	0	1
5 krad	2	10
10 krad	2	15
18 krad	4	16

Table 1.3: Number of failures as a function of total dose

The number of errors and their corresponding failure modes will be discussed in detail in the next sections.

1 krad

During the first irradiation step up to 1 krad, no in-situ errors were detected by the test system. As can be seen in Table 1.3, however, already after this 1 krad(Si) irrradiation step, 1 device (S48) failed the functional test during the full characterization. More specifically, a failure occurred at checkerboard 1 and 5.5V. This error had, however, disappeared during the error location. This is explained by the fact that the program, that located the errors, used somewhat weaker test conditions than did the functional test program. The results thus indicated that it concerned a marginal failure but that more problems were to be expected during the next radiation step.

# failing devices READ charact.	failure modes	# failing devices FULL charact.	failure modes
0	none	1 (marginal)	unknown

Table 1.4: Errors and failure modes after 1 krad

2 krad

Again, no in-situ errors were detected during the second step up to 2 krad. The same device (S48) again failed after 2 krad during the full characterization. No failures could be detected at checkerboard 1, which confirms the error at 1 krad was a marginal one. At checkerboard 0 and 5.5V, however, an error occurred on the last address of the memory (hex 7FFF), where all bits were expected to be 0. Analysis showed that these bits were indeed low, but that the output signals exhibited large spikes, just at the moment when the measurement took place (at 250ns after CE-transition). These peaks caused the bits to be interpreted as ones. Such peaks were also encountered in the endurance test, performed in workpackage 4 [3]. The number of failing bits on the mentioned address varied when repeating the measurement, which can be explained by random variations in the heights of the peaks.

# failing devices READ charact.	failure modes	# failing devices FULL charact.	failure modes
0	none	1	- no parametric failures - spike (7FFF)

Table 1.5: Errors and failure modes after 2 krad

5 krad

During the next irradiation step (accumalated total dose=5 krad), again no in-situ errors were detected. However, 2 devices failed the read characterization. These parts, together with the error location and failure modes are listed in Table 1.6.

READ characterization		
Device	**Location**	**failure mode**
S49	page 424	stuck to "1"
S54	page 157 page 191 page 253 page 445 page 190	stuck to "1" stuck to "1" stuck to "1" stuck to "1" flipped page

Table 1.6: failures during read characterization after 5 krad

1 device (S49) failed on all even adresses of 1 page (page 424). Analysis showed that all bits of this page were stuck to 1. The same occurred at 4 pages of the other failing part (S54). Moreover, this device showed 1 page, that had completely switched: all ones had become zeros and vice versa (flipped page). It is important to note that the latter part (S54) was unbiased during irradiation.

10 devices also failed the functional test during the full characterization, one of which was marginal, which means that the errors could not be detected

during the error location, because of the somewhat different test conditions. The failures are shown in Table 1.7.

WRITE characterization			
Device	**Location**	**Failure mode**	**18h anneal**
S41	random	spikes	idem
S42	random	spikes	passed
S46	random	spikes	passed
S47	random	spikes	passed
S48	random	spikes	idem
S49	page 424	stuck to "1"	idem
S50	random	spikes	idem
S51	random	spikes	idem
S54	page 157	stuck to "1"	idem
	page 191	stuck to "1"	idem
	page 253	stuck to "1"	idem
	page 445	stuck to "1"	idem
	page 189	flipped page	idem
S56	random	spikes	idem

Table 1.7: failures during full characterization after 5 krad

It is very important to mention that nearly all errors occurred on addresses ending on 3F, 7F, BF and FF, which are the last addresses of a page, when a 00 pattern was expected. Analysis showed that those errors were again caused by peaks on the output signal. There were, however, also a few other failing locations, most of which were caused by spikes as well. The influence of those spikes can clearly be seen on Fig.1.3, where the output of I/O-pin 4 is visualized for a device that failed at checkerboard 1 on address 3DFE. The measurement takes place 250ns after the CE-signal falls, which is at the edge of the specification. The measurement itself takes 20ns. As can be seen, the spike turns up just at this moment.

It must be emphasized that this kind of failures can not be detected when using a microprocessor system, since such systems have much longer measuring times and the signals would be seen as zeros. This explains why no errors were found during the in-situ tests, where a microprocessor-based

system was used, though errors were found in the first 8 pages during remote testing. Moreover, the detection of the spikes was only possible by measuring at the specification limit.

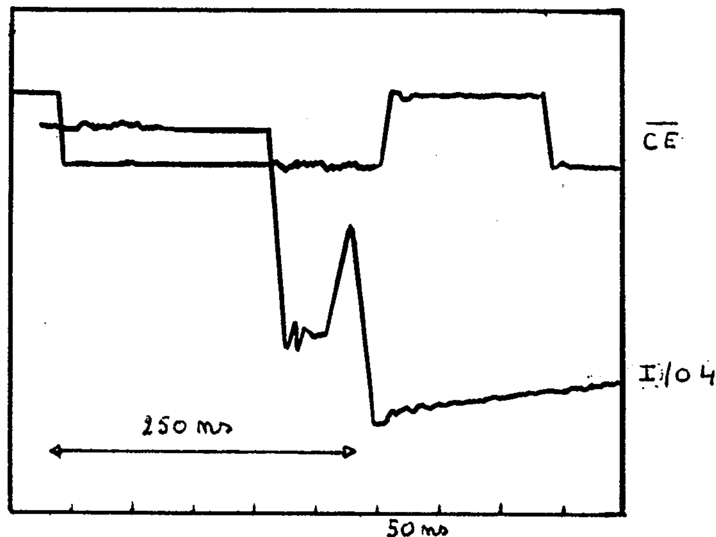

Fig. 1.3: Voltage spike

Further analysis showed that the appearance of the peaks was dependent on the pattern used. They were only seen when checkerboard 0 and 1 patterns were written. This is in complete agreement with results obtained during the endurance test. Furthermore, the heights of the spikes seemed to be very temperature dependent, with the peak decreasing at increasing temperature.

Besides this one, two other failure modes occurred:

- The pages that were stuck to 1 during the read characterization (devices S49 and S54) were also unable to be rewritten. All bits kept being 1.

- The device that had a page flip at page 190 and checkerboard 1 (read characterization), exhibited a page flip at page 189 and checkerboard 0 during the write characterization. Probably the page flip at page 190 was still present at checkerboard 1, but unfortunately this pattern was not checked during the write characterization of this device due to a

temporary problem with the VLSI-tester. The fact that page 190 failed at checkerboard 1, but did not at checkerboard 0, points to even addresses that are stuck to 1 and odd addresses stuck to 0. This could explain why a failure occurred at checker 1, while the device passed at checkerboard 0, since an inverse checkerboard pattern is then expected. The same holds, of course for page 189, with again the even bytes stuck to 1 and the odd bytes stuck to 0.

After this radiation step the devices were allowed to anneal for about 18 hours. 3 devices had completely annealed (see Table 1.7), while for most devices the number of failures had decreased, which points to annealing of the spikes, the more since the devices that had stuck-to-1 pages and flipped pages kept failing by the same failure mode.

10 krad

Also during irradiation up to 10krad, no in-situ errors were detected. On Table 1.8, it can be seen that the 2 devices that had failed the read characterization during the previous step, continued to fail. The number of stuck-to-1 and flipped pages had, however, largely increased. It is interesting to mention that a page that was stuck-to-1 had turned into a flipped page.

READ characterization		
Device	**Location**	**failure mode**
S49	page 129	stuck to "1"
	page 135	stuck to "1"
	page 141	stuck to "1"
	page 165	stuck to "1"
	page 197	stuck to "1"
	page 295	stuck to "1"
	page 389	stuck to "1"
	page 391	stuck to "1"
	page 424	flipped page
	page 431	stuck to "1"
S54	page 465 and following	flipped page

Table 1.8: failures during read characterization after 10 krad

As shown on Table 1.8, device S54 exhibited failures at pages 465 and all following pages. No information, however, was available on the previous pages, due to the limited error storage capacity of the VLSI-tester. Probably the device also failed at the pages that had failed before. The 2 devices were removed from further characterization. (though they were further irradiated and monitored in-situ).

The devices that failed the write characterization after 10 krad, together with their failure modes, are shown on Table 1.9. The error locations are not listed, since they had become too numerous. Only S57 passed the test completely without errors.

WRITE characterization	
Device	**Failure mode**
S41 to S48, S50 to S53 and S56	spikes; spiking only occurs for bit patterns 00/FF, not for AA/55, All1 or All0
S49 and S54	removed

Table 1.9: failures during full characterization after 10 krad

13 out of 14 remaining parts failed the functional test during the full characterization. No parametric errors, however, were seen. A great number of addresses again exhibited the previously mentioned peaks, which had increased as compared to the previous radiation step. It can be seen that also unbiased devices suffered from these peaks (S53 and S56). The fact that pages, that were in-situ written with 00-FF patterns, did not fail during irradiation, while they failed the functional test at the same patterns, again confirms that these kind of failures, which turned out to be very numerous, can only be spotted by using a VLSI-tester. Furthermore, this time the peaks seemed to occur at any adrress and not merely at the page endings (though these locations kept well-represented), which indicates that these page boundaries seem to be the weakest spots for the appearance of the spikes.

Since nearly all devices had failed the full characterization, but almost entirely by the appearance of spikes, it was decided to relax the access time and to measure at 500ns (i.s.o. 250 ns) after CE-fall in order to circumvent

these peaks and to look for other failure modes as the total dose increased, rather than to stop the test after 10 krad of radiation. The devices (except for S49 and S54) were first tested using the new access time specification. They all passed , which confirms that all errors were due to spikes.

18 krad

From this moment on, errors began to turn up during irradiation (in-situ tests), which pointed to failure modes, other than the spikes discussed above.The devices and their failing pages, together with the failing patterns are shown in Table 1.10a and 1.10b. Herein, "READ 1" corresponds to the first read operation in the RWR sequence or RR sequence (see section 4). "READ 2" points to the second read operation. Errors in the "READ 1"-table will thus correspond to retention failures (READ-failures), while errors in the "READ 2" table will nearly always correspond to WRITE-failures, since a page that is only read, is most likely to fail during the first read operation in the sequence RR.

We recall that, as soon as one bit of a page failed, the page was excluded after checking the kind of error. All errors that appeared were random bit errors, which means that the failures were not odd or even pages errors, nor full page errors. So, when e.g. only 1 bit of the whole page was correct, this was nevertheless denoted as a random failure. Device 49 was one of the devices that had failed the read characterization after 5 krad and had been excluded from remote testing.

	READ 1						
	Device Nr.	Address	Page	Exp. pattern	Faulty pattern	# Cycles	Dose (krad)
G2	48	006B	2	AA	A8 (bit 2)	332	14.54
G3	49	00EC	4	FF	7F (bit 8)	33	14.45
		0140	6	00	FF (all bits)	37	16.27
		0180	7	00	FF (all bits)	40	17.64

Table 1.10a: Read errors during irradiation (in-situ test)

	READ 2						
	Device Nr.	Address	Page	Exp. pattern	Faulty pattern	# Cycles	Dose (krad)
G1	41	0039	1	55	D5 (bit 8)	3713	17.08
		0079	2	55	D5 (Bit 8)	3744	17.22
	42	0007	1	55	D5 (bit 8)	3719	17.12
		007F	2	55	D5 (bit 8)	3768	17.33
	43	003D	1	55	D5 (bit 8)	3101	14.32
		007F	2	AA	A8 (bit 2)	3021	13.95
		0099	3	FF	FD (bit 2)	3031	14.00
		00F3	4	FF	FD (bit 2)	3024	13.97
	44	0021	1	55	D5 (bit 8)	3605	16.59
		007B	2	55	D5 (bit 8)	3664	16.86
G2	46	0017	1	55	D5 (bit 8)	406	17.59
	48	0016	1	AA	A8 (bit 2)	324	14.17
		0095	3	FF	FD (bit 2)	306	13.44
		00F7	4	FF	FD (bit 2)	329	14.40
G3	49	0010	1	AA	A2 (bit 4)	31	13.08
		0085	3	FF	7F (bit 8)	31	13.08
	51	0000	1	AA	A8 (bit 2)	41	17.64

Table 1.10b: Write errors during irradiation (in-situ test)

As described above, the devices of group G1 (S41 to S44) received the largest number of cycles (3879). Devices of group G2 (S45 to S48) were cycled about ten times less (410), those of G3 (S49 to S52) hundred times less (41). When looking at Tables 1.10a and 1.10b, the following conclusions can be drawn:

1. Most of the failures are caused by the write operation and thus occur in pages 1 to 4. Only four pages show retention failures (page 2 of device 8 and pages 4, 6 and 7 of device 9). Pages 2 and 4 were written and read, while 6 and 7 were only read.

2. There seems to be a tendency for the number of failures to increase as the number of programming cycles increases.

3. The majority of the errors occurs in pages where an AA-55 pattern was written, so this pattern seems to be worse than a 00-FF pattern. Furthermore, most devices that failed an AA-55 pattern during the in-situ test (first pages), showed no failures in these pages during the remote characterization, when a 00-FF pattern was tested.

During the remote read characterization (Table 1.11), 2 more devices (S43 and S57) failed as compared to the previous radiation step. One device (S43) exhibited a few I/O signals with a value between the 0 and 1 value. The other device (S57) suffered from stuck-to-1 failures. The number of failing pages increased as the supply voltage was increased. As an example, page 18 only failed at 5.5V, but not at 4.5V and 5V.

READ characterization		
Device	**Location**	**failure mode**
S43	random	I/O does not reach "1" level
S57	page 6	stuck to "1"
	page 18	stuck to "1"
	page 21	stuck to "1"
	page 24	stuck to "1"
	page 30	stuck to "1"
	page 150	stuck to "1"

Table 1.11: failures during remote read characterization after 18 krad

WRITE characterization			
Device	Parametric failure mode DC	Parametric failure mode AC	Fail functional
S41 to S48, S50	Standby supply current too high	VIL < IDL	YES
S53, S56, S57 "unbiased"	None	VIL < IDL	YES

Table 1.12: failures during remote full characterization after 18 krad

As mentioned above, the full characterization (Table 1.12) was performed with a relaxed access time. All devices, however, failed. This means that, this time, the failures were not caused by peaks on the output signals, but had to be caused by an other failure mechanism. This is in agreement with the fact that this time errrors had indeed occurred during the in-situ measurements, when a microprocessor system was used. Moreover, all biased devices showed DC and AC parametric failures: the TTL stand-by supply currents of some parts and the CMOS stand-by supply currents of all parts had exceeded their limit, while the VIL-value in the AC characterization had dropped below its limit of 800mV (see also Figs. 1.12, 1.13 and 1.20). This, of course, resulted in functional failures. The stand-by supply currents of the 3 remaining unbiased devices stayed within their specifications (see also Figs. 1.12 and 1.13); they showed no DC parametric failures. However, two of them completely failed the AC characterization: access time, input- and output levels could not be measured. The third unbiased device showed no parametric failures, but failed the functional test.

Further analysis showed that, for all devices, some failing pages were stuck to 1 or stuck to 0, while others showed a mixture of wrong and correct bits. A few locations flipped between high and low. The results of the write characterization are presented in Table 1.12.

After approximately 15 hours of annealing, the parts were again fully tested. The stand-by supply currents (SBSC) had clearly recovered. For the biased devices all TTL-SBSC had dropped below their limit. The CMOS values, however, kept failing. The VIL-values in the AC characterization continued to fail as well.

A summary of failures and failure modes is presented in Table 1.13. As a conclusion it can be stated that two levels of failure occurred as a result of the radiation:

1) At low to medium doses (2-5 krad), two kinds of failure modes occurred:

   a) read characterization failures, i.e. pages that lost their information after irradiation.

   b) write characterization failures, i.e. failures that occurred during reprogramming after the radiation step.

Total dose	# failures READ	failure modes	# failures WRITE	failure modes
1 krad	0	none	1 (marginal)	unknown
2 krad	0	none	1	- no parametric failures - spikes
5 krad	2	- stuck to 1 - page flip	10	- no parametric failures - spikes - page flip - stuck to 1
10 krad	2	- stuck to 1 - page flip	15	- no parametric failures - spikes - 2 page flip and ST1 devices removed
18 krad	4	- wrong I/O level - stuck to "1"	16	- SBSC - VIL<IDL - 2 devices had already been removed

Table 1.13: Overview of failures and failure modes

The occurrence of the first failure mode is shown on Fig. 1.4. These failures consist mainly of stuck-to-1 failures or flipped pages. The occurrence of the second failure mode is shown on Fig. 1.5. These failures consist exclusively of the spiking errors on the I/O lines. Devices 49 and 54 are indicated by "?" because it could not be determined whether they had spiking problems or not. These devices are the ones that had the read-characterization errors (stuck-to-1 or flipped page).

2) Due to the spiking problem, all but 1 part (S57) failed after 10 krad. If then the access time was relaxed, all parts that did not exhibit the reading error, but were failing due to the spiking problem, were functioning again. When further irradiating these parts, they started failing again at higher doses (10-20 krad), both due to DC-parametric errors and AC-parametric and functional errors. Fig. 1.6 summarizes the occurrence of the AC and functional errors (i.e. without the spiking problem), while Fig. 1.7 shows the same for the DC-parametric errors. As can be seen on Fig. 1.7, only the biased parts showed DC-parametric errors after 18 krad. At the end of the test, the unbiased parts still had not failed the DC characterization, but they did fail the AC and functional characterization.

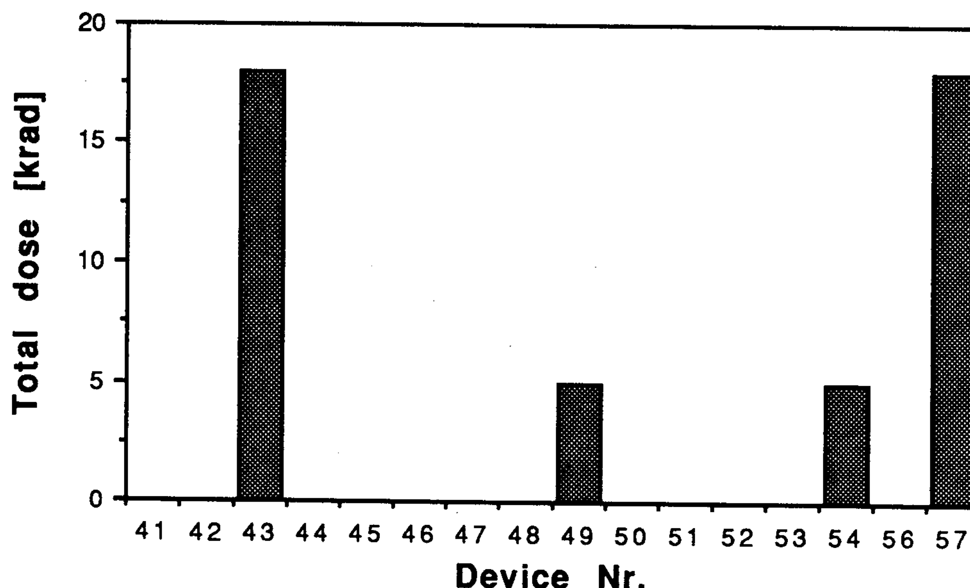

Fig. 1.4: Read characterization failure doses

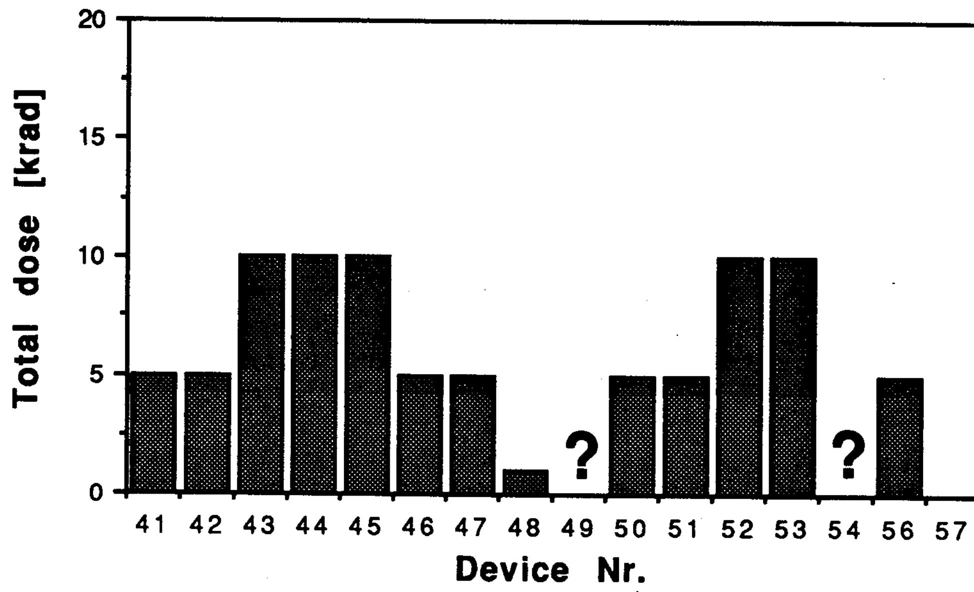

Fig. 1.5: Failure dose of devices exhibiting spikes

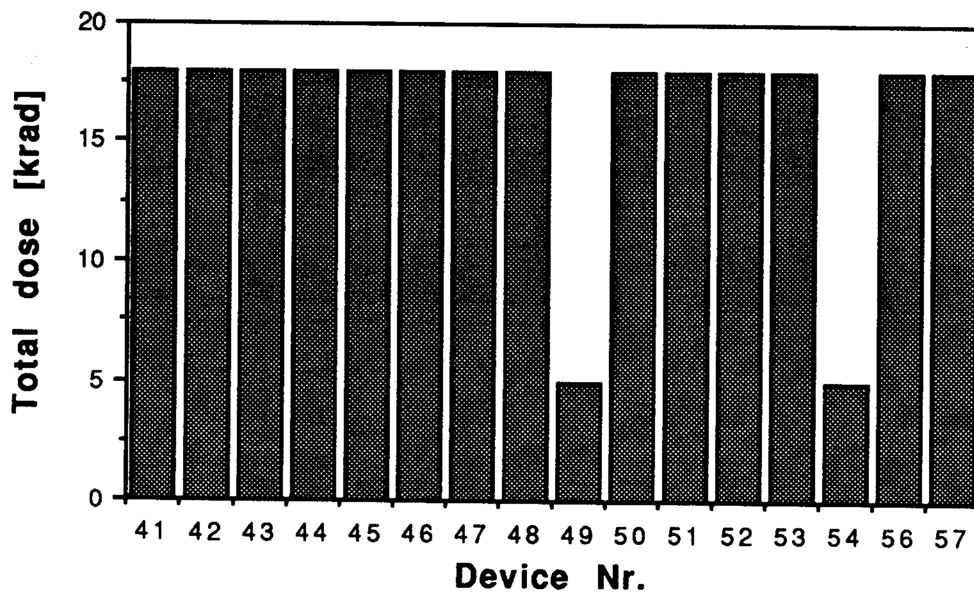

Fig. 1.6: Write characterization failure dose

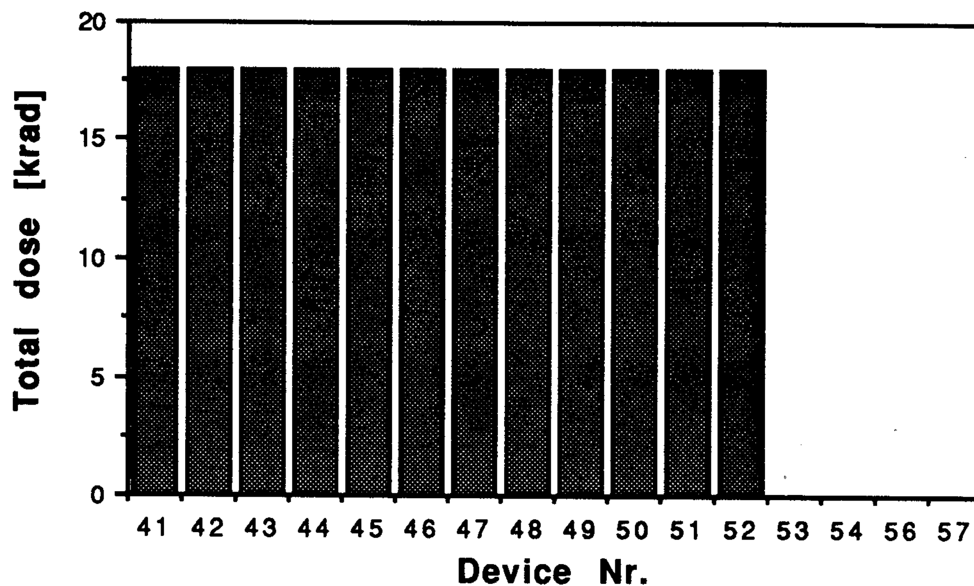

Fig. 1.7: DC characterization failure dose

Figs. 1.8 and 1.9 summarize the results of the in-situ test. The labels inside the figures indicate the failing pages while the blocks show the total dose these pages failed at. If more than one page of a device failed, they are plotted on top of each other, in this way indicating the failure level for each page.

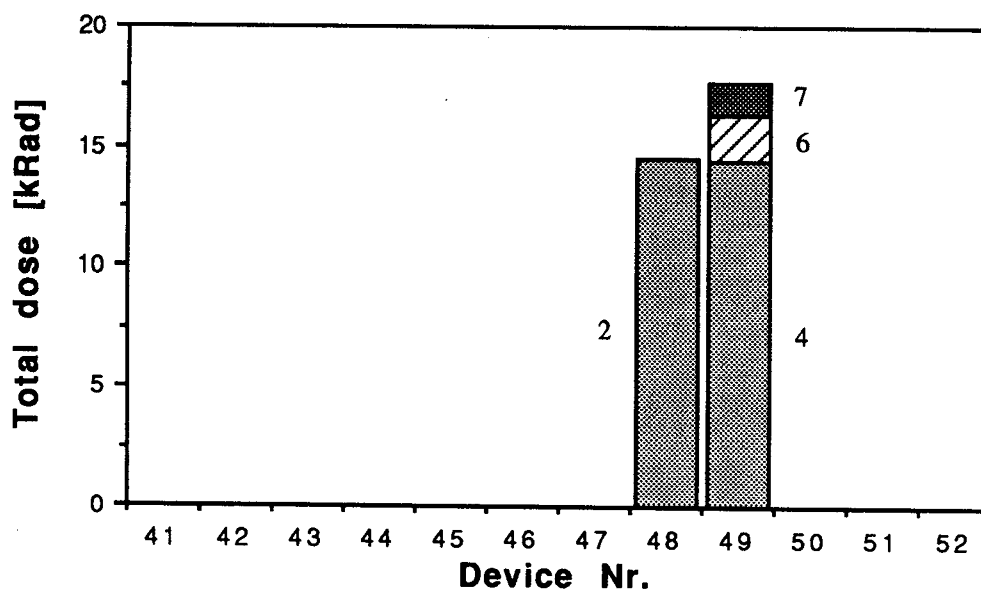

Fig. 1.8: In-situ read characterization failure dose

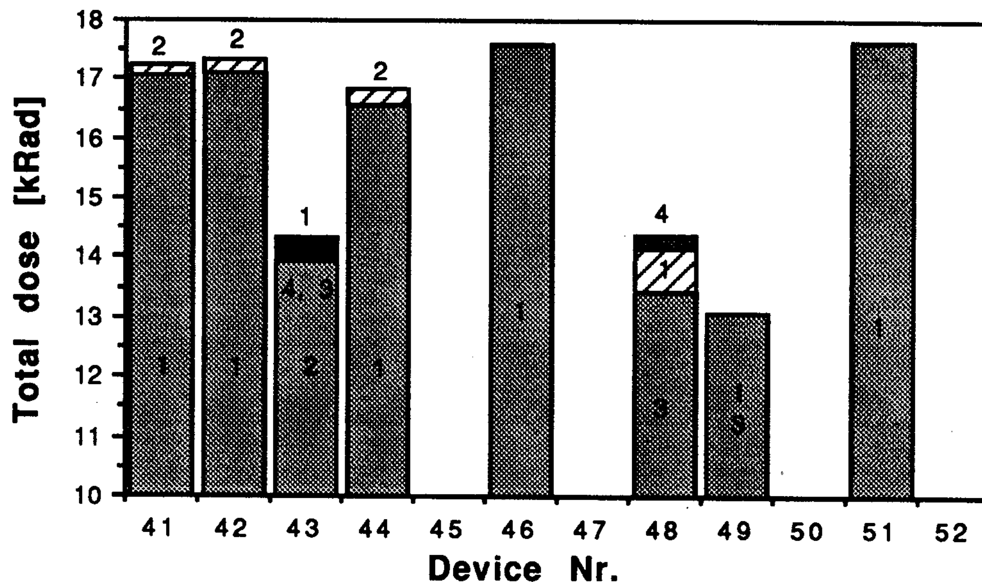

Fig. 1.9: In-situ write characterization failure dose

Anneal

The devices were tested again after approximately 1150 hours of annealing. 1 part (S53) passed the characterization and had thus completely recovered. Here, it must be mentioned that the functional test was performed, using an access time of 500ns (relaxed value) as was done in the characterization after 18krad. No DC parametric errors were detected at all, so all stand-by currents had recovered to a value below the specification limit. (see also Figs. 1.12 and 1.13). Except for 1 device (S48), all VIL values had recovered as well (see Fig. 1.20). Hereby it must be mentioned that for two devices (S49 and S57), it was impossible to measure the AC parameters, probably because of failures in the first 8 pages and that S49 and S54 had not been characterized after 18krad, because they had already been excluded from the test. These results are summarized in Table 1.14.

Though recovery of the DC and AC parameters was seen at nearly all devices, they nevertheless kept failing the functional test, except for S53. This device failed, however, when an access time of 250ns was used, which points to the fact that no annealing of the spikes at the bitlines had taken place.This could, indeed, be seen on an oscilloscope. When looking at the other devices, all bit lines seemed to have the correct value: no flipping bits, stuck to 1 or 0 pages a.s.o. could be seen. In turn, however, a second peak had turned up at many locations, which resulted in a failure, even when

testing with an access time of 500ns. The two peaks were seen almost only at the page boundaries. A few locations exhibited only 1 peak.

	WRITE CHARACTERIZATION			
	Device Nr.	Parametric DC	Parametric AC	Functional
G1	41	O.K.	O.K.	FAIL
	42	O.K.	O.K.	FAIL
	43	O.K.	O.K.	FAIL
	44	O.K.	O.K.	FAIL
G2	45	O.K.	O.K.	FAIL
	46	O.K.	O.K.	FAIL
	47	O.K.	O.K.	FAIL
	48	O.K.	VIL<IDL	FAIL
G3	49	O.K.	?	FAIL
	50	O.K.	O.K.	FAIL
	51	O.K.	O.K.	FAIL
	52	O.K.	O.K.	FAIL
G4	53	O.K.	O.K.	PASS
	54	O.K.	O.K.	FAIL
	56	O.K.	O.K.	FAIL
	57	O.K.	?	FAIL

Table 1.14: Overview of failures and failure modes after annealing

2.3. DC and AC parameters

Figs. 1.10 to 1.20 show the measured DC and AC parameters as a function of total dose. Also plotted on the right hand side of the dotted line are the values after annealing. The mean values are indicated by the symbols, while the minimum and maximum values are given by the error bars.

As can be seen on Figs. 1.12 and 1.13, the stand-by currents of the biased devices largely increase after 5-10krad. In fact all values of the CMOS stand-by current exceed the maximum specification limit after 18krad. All TTL stand-by currents stay below the limit up to 10 krad. At 18krad, however, a

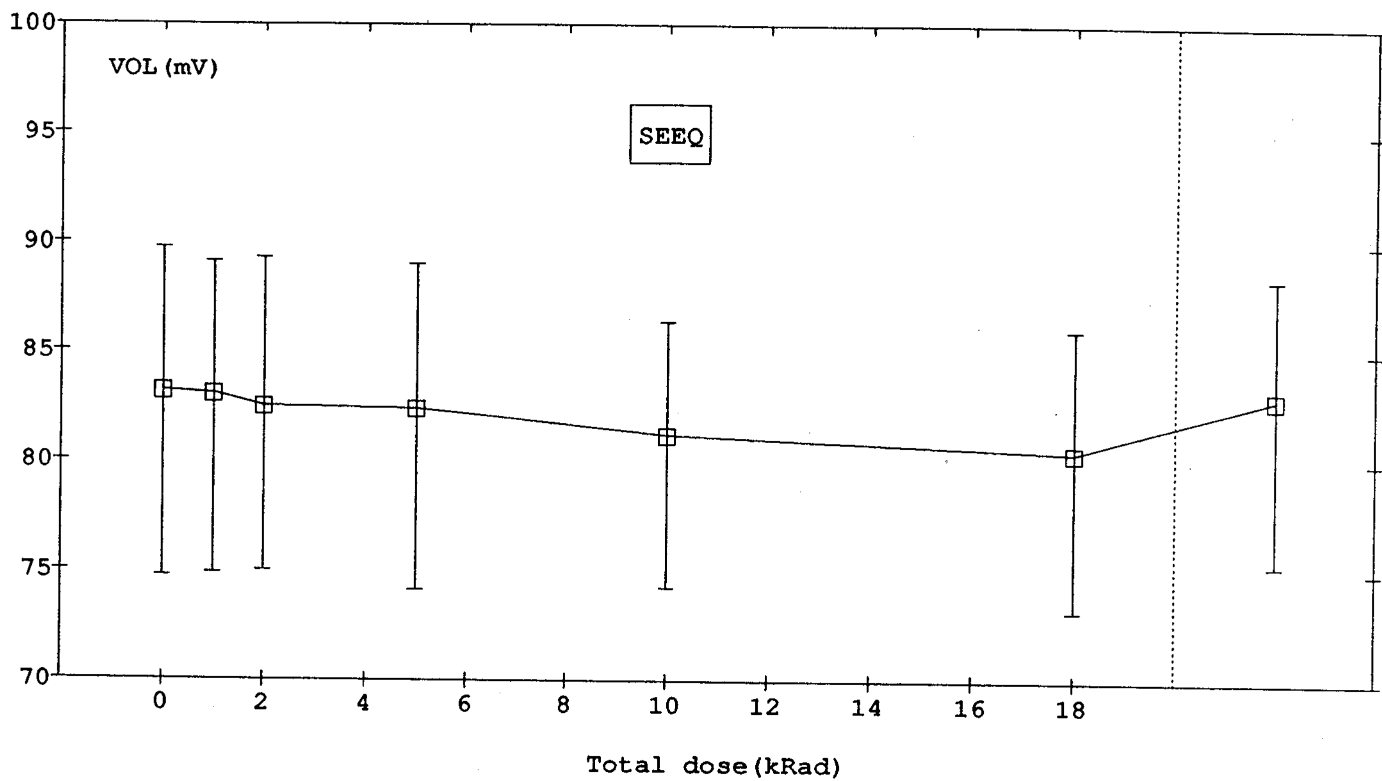

Fig. 1.10: VOL versus total dose

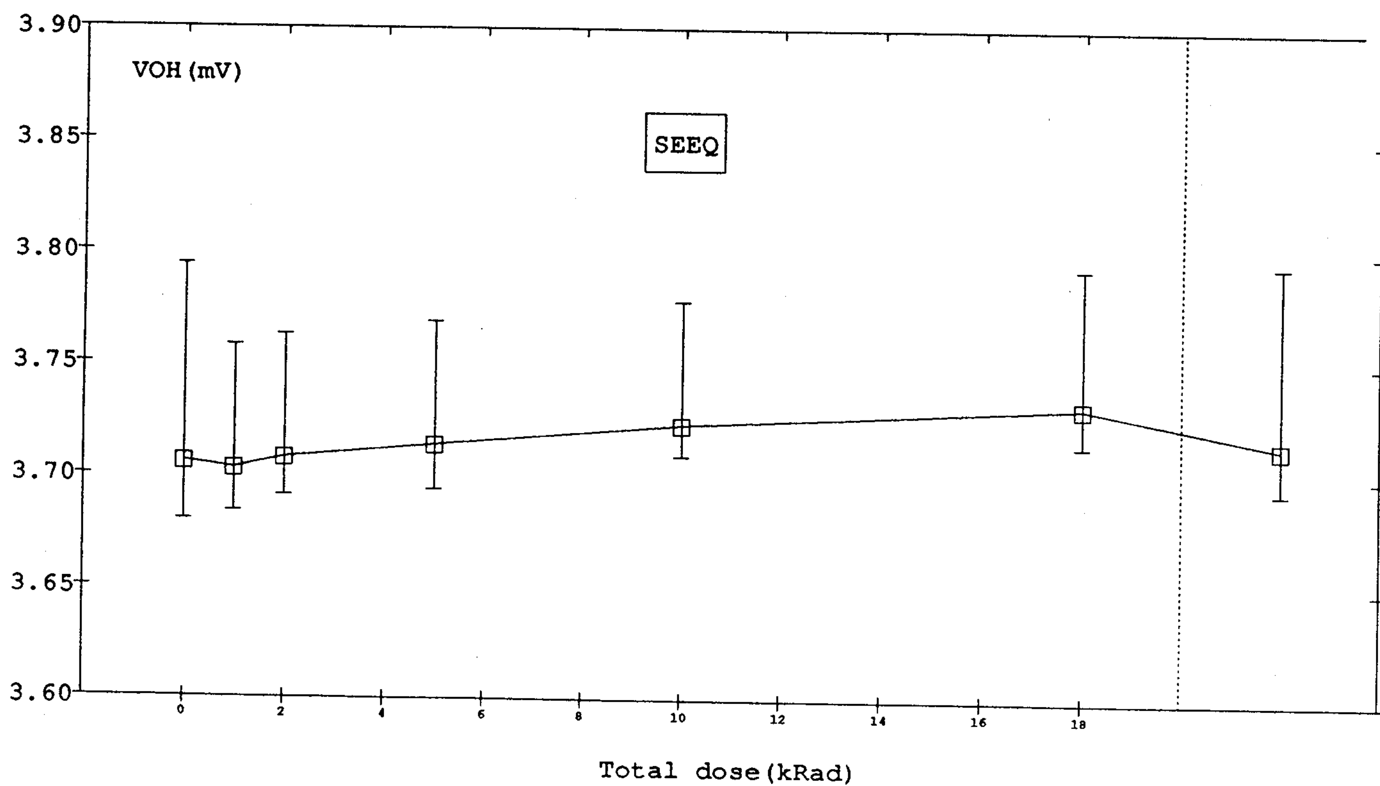

Fig. 1.11: VOH versus total dose

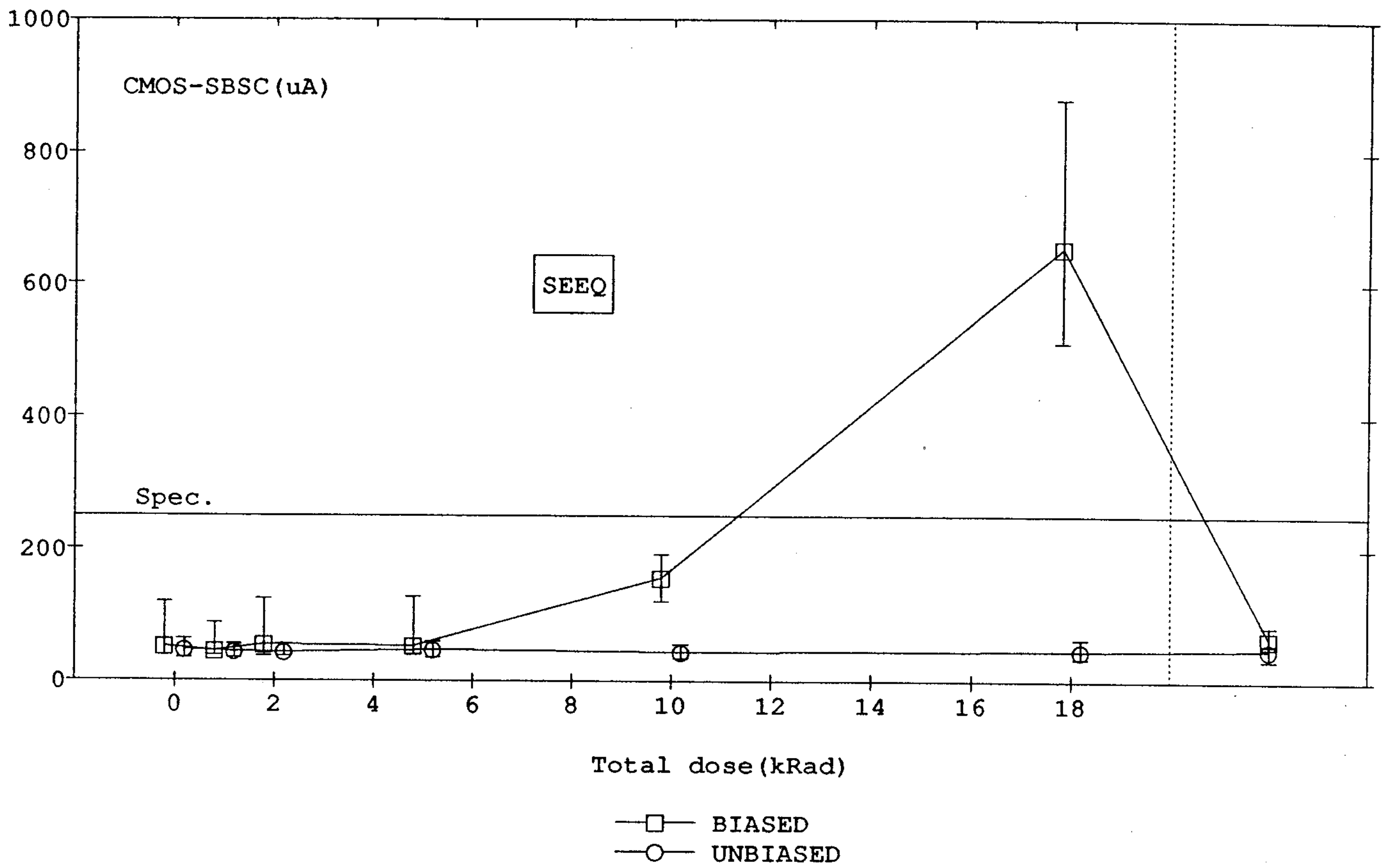

Fig. 1.12: CMOS stand-by supply current versus total dose

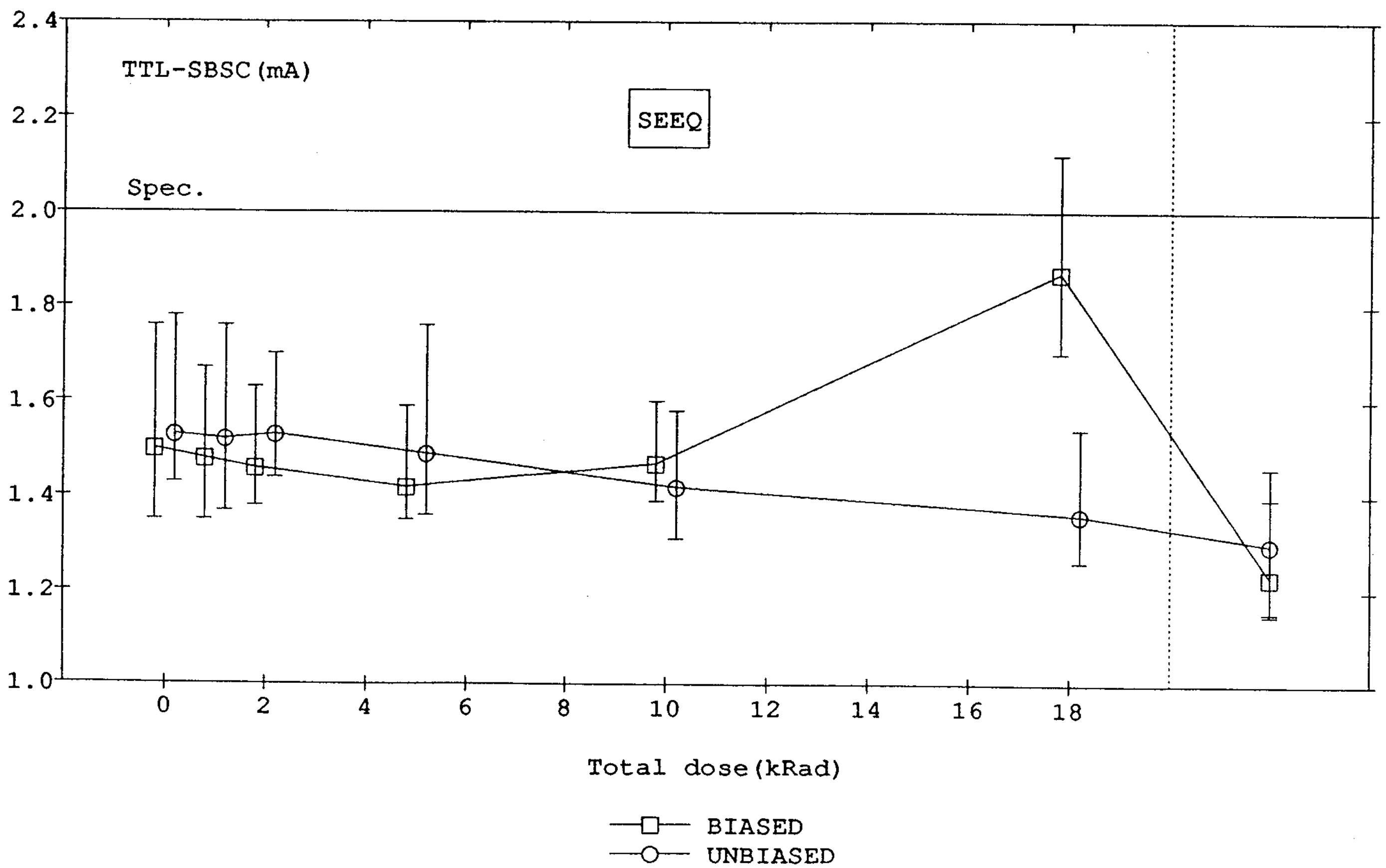

Fig. 1.13: TTL stand-by supply current versus total dose

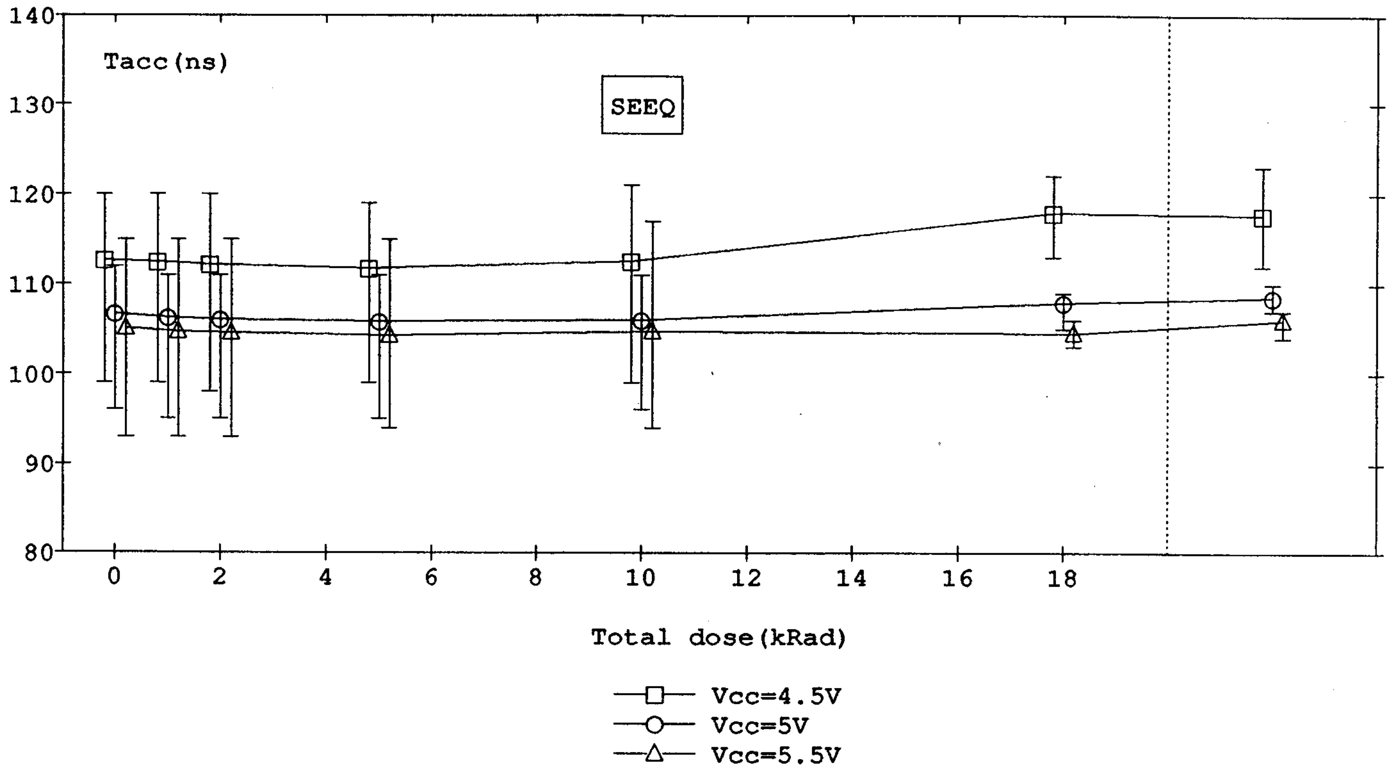

Fig. 1.14: Access time versus total dose

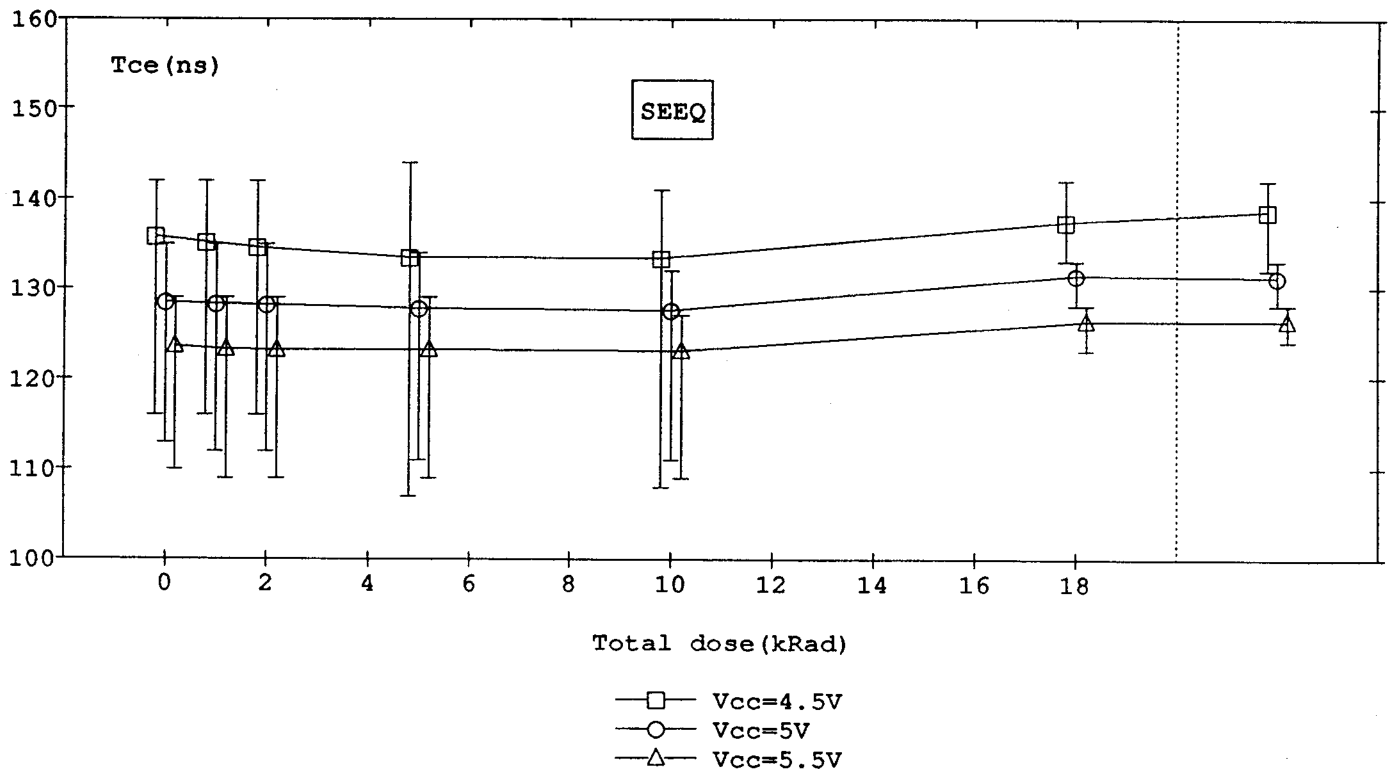

Fig. 1.15: Chip enable access time versus total dose

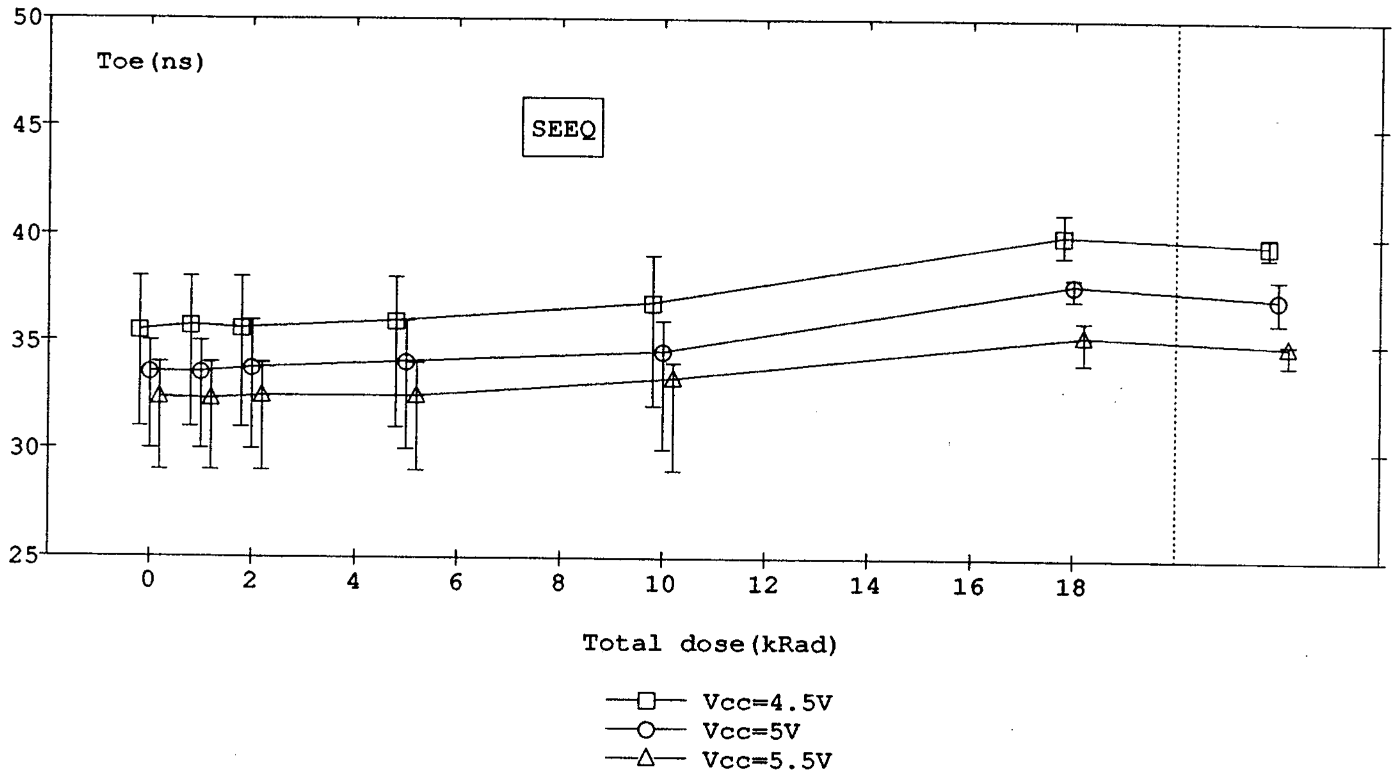

Fig. 1.16: Output enable access time versus total dose

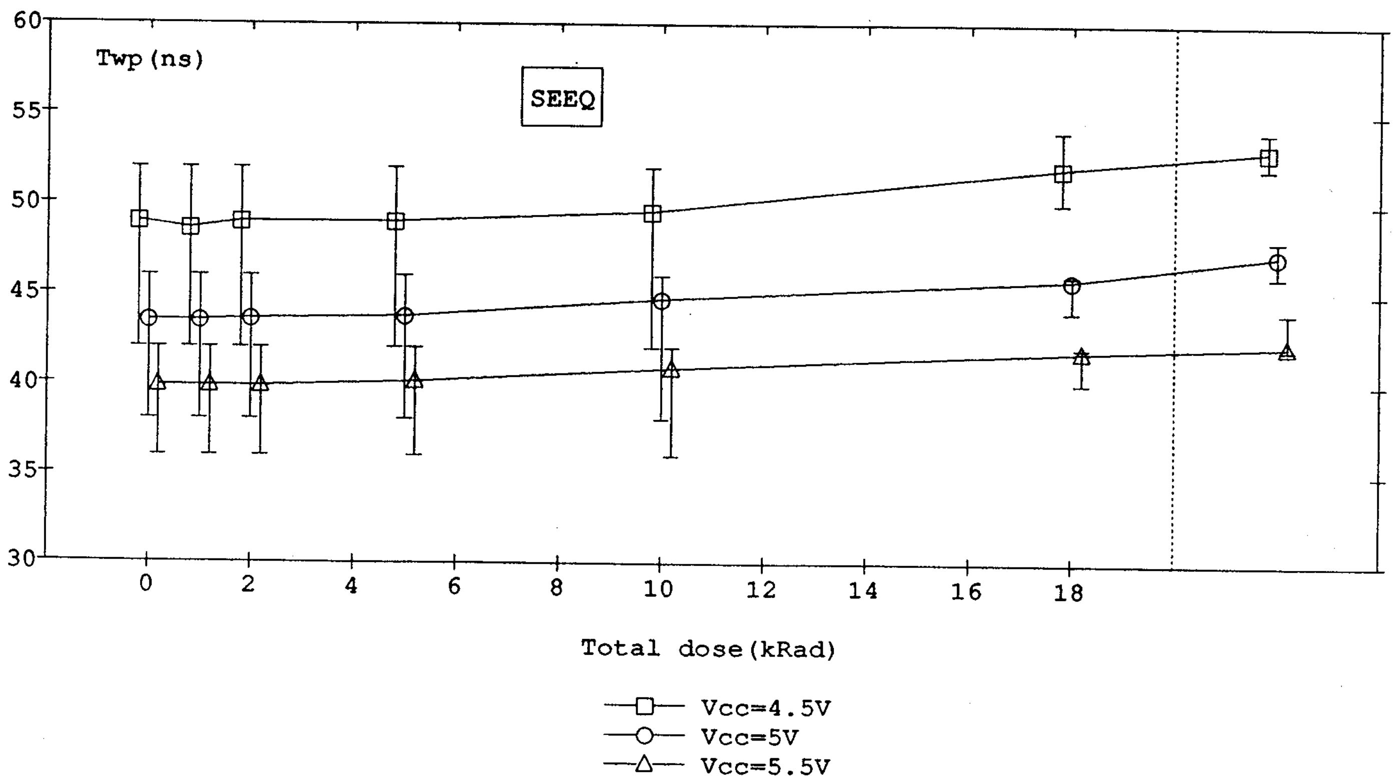

Fig. 1.17: Write pulse width versus total dose

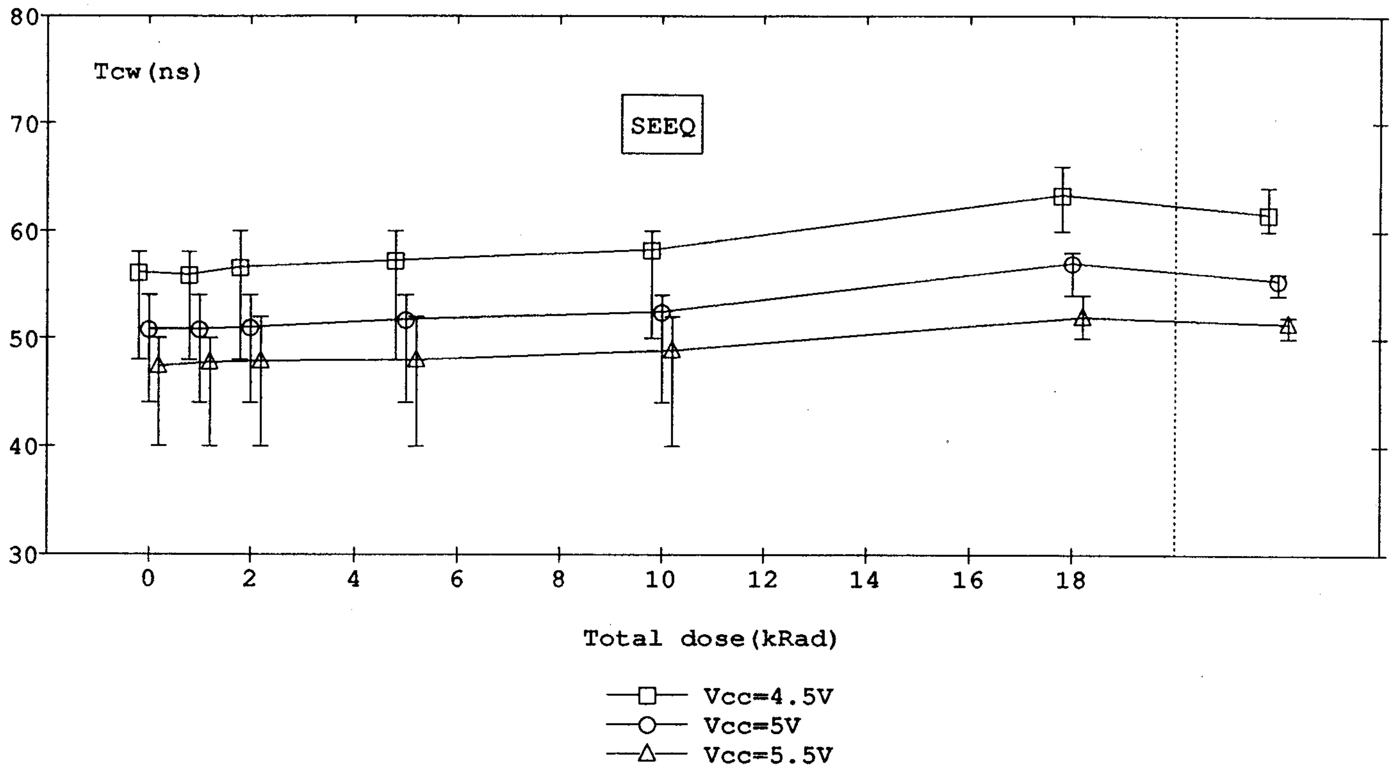

Fig. 1.18: Chip enable pulse width versus total dose

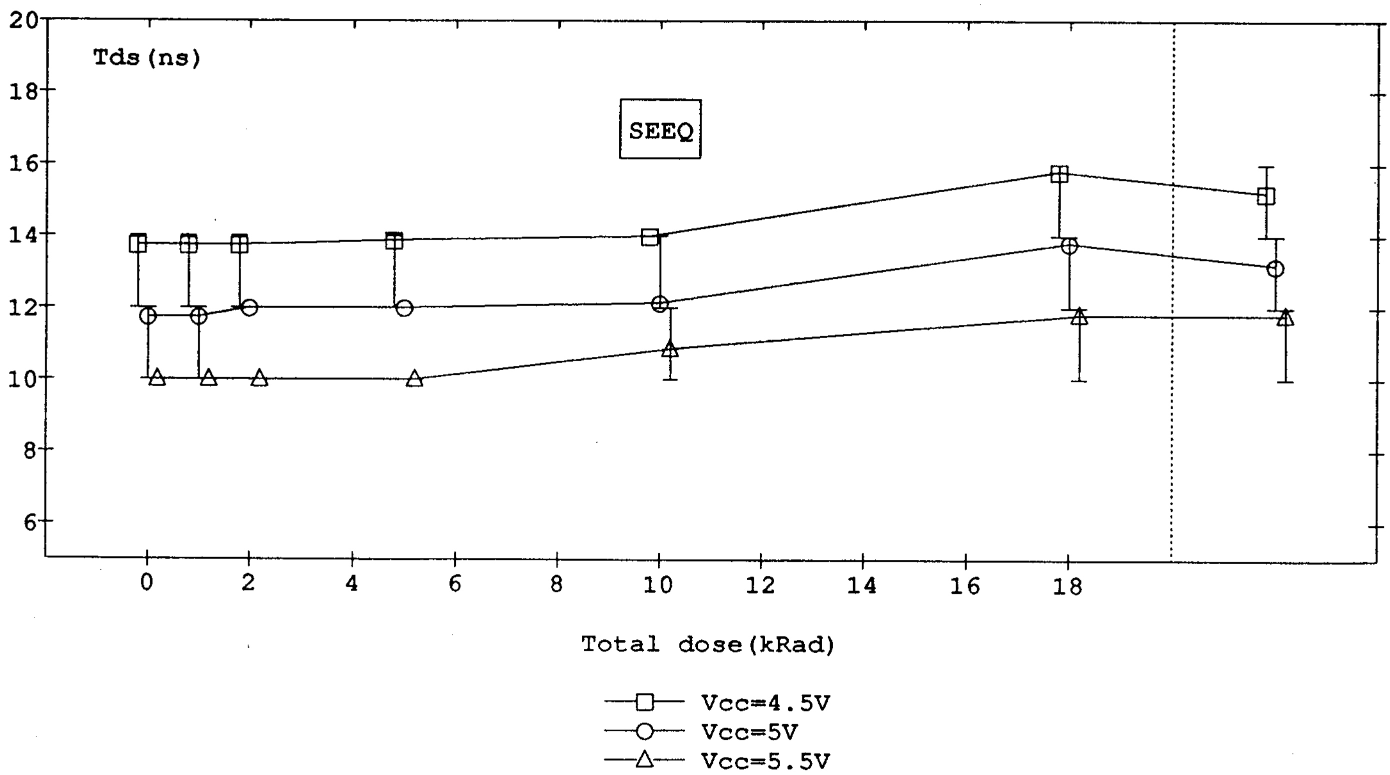

Fig. 1.19: Data set-up time versus total dose

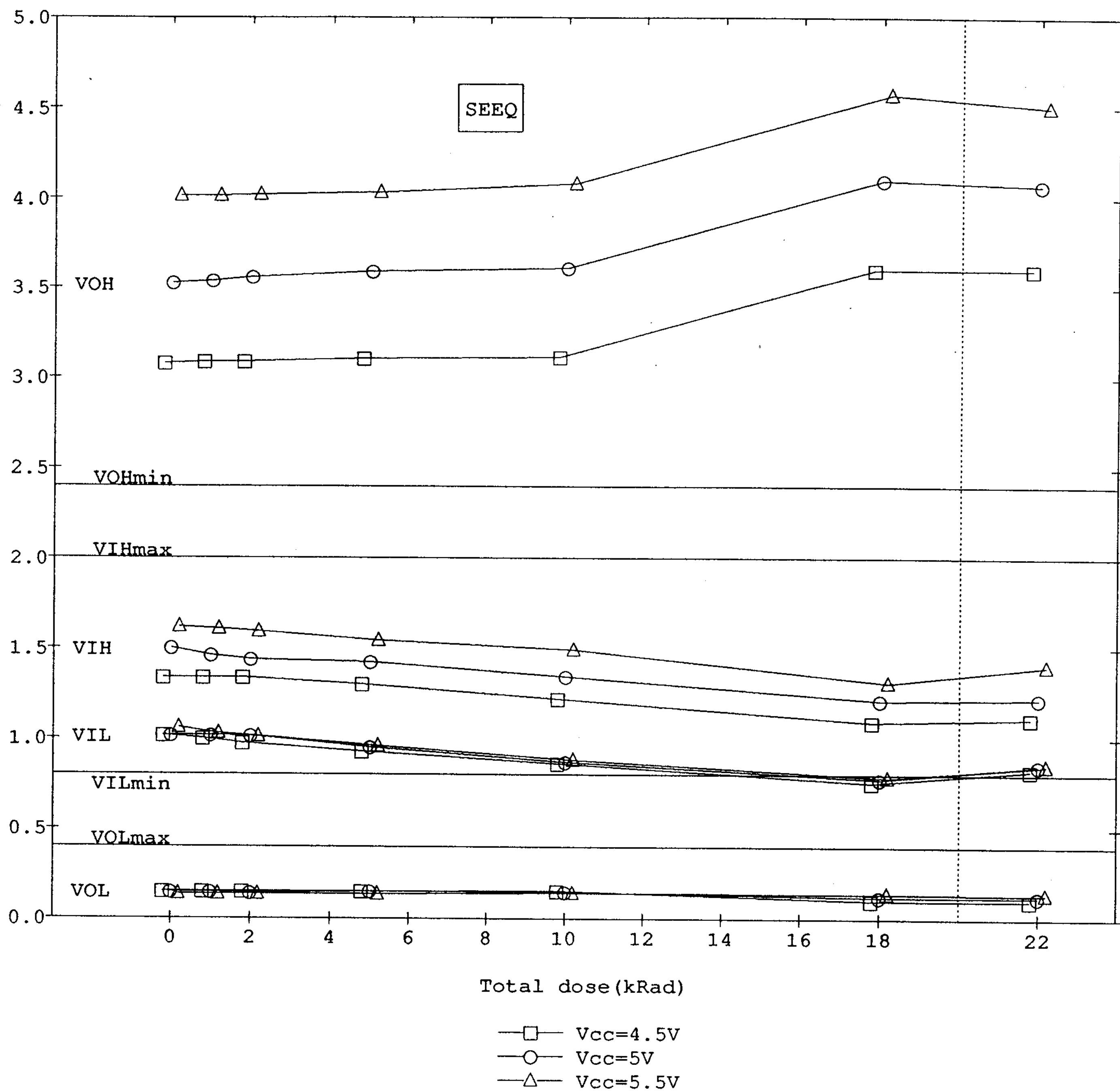

Fig. 1.20: Noise level tolerance parameters versus total dose

few devices exceed the specification (The mean value is below the limit, the maximum value exceeds it). After 1150 hours of annealing, the stand-by current have dropped below the specification limit to a value equal to that of the unbiased devices, so no DC errors were present anymore, as already described in the previous section.

On Figs. 1.14 to 1.19, it can be seen that the access times change only slightly as a function of total dose. It must be mentioned that the error bars are much smaller at 18krad than at the other dose steps. This has to be attributed to the fact that the devices represented by the upper and lower values of the error bars were excluded from the characterization at 18krad, because of complete failure (inability to measure access times, due to failures in the first pages). Fig. 1.20 shows the parameters of the functional test. Here, it can clearly be noticed that the mean value of the VIL parameter drops below its specification limit at 18krad, which of course results in lots of functional failures. During annealing, it starts to increase again to a value which is within specification. The VIH parameter decreases as well as a function of total dose, while VOH starts to increase sharply after 10krad of total dose.

3. Conclusion

The following conclusions can be drawn concerning the total dose radiation tests on the SEEQ-parts:

1) Depending on the total dose levels, three kinds of failures can be distinguished:

   a) At low dose levels (2-5 krad), voltage spikes occur at the output lines after reprogramming the parts. This leads to failures at the edge of the acces time specification. Similar voltage spikes were also encountered during the reliability testing, more specifically during the endurance test. It is not clear what is the exact cause of this failure mode. Also this failure mode does not disappear after a long storage time. The failure mode can be avoided by relaxing the access time specification.

   b) At medium dose levels (5 krad), another failure mode occurs, this time when reading the parts immediately after the irradiation. This failure

mode is characterized by full pages that have lost their information after irradiation, either by becoming stuck-to-one or flipped pages. The failing pages can also not be reprogrammed.

c) At higher doses (10-18 krad), all parts start to fail due to parametric (DC and AC) and functional failures. The functional failures show a slight tendency to occur earlier when the bit pattern AA-55 is used instead of 00-FF. The DC-parameters that cause the failures are the two stand-by supply currents (CMOS and TTL).

2) There is no clear evidence for difference in behaviour between parts that are in-situ cycled and others that are kept unbiased. Except for the stand-by supply current, all unbiased parts failed as well after 18 krad due to AC and functional failures. Moreover, the early failures (spiking and reading errors) also occurred for the unbiased parts.

3) There is only a slight influence of the programming frequency that is used during the in-situ cycling of the memory parts. The parts that are cycled with the highest programming frequency have the tendency to show somewhat more failures.

4) The DC and AC-parameters of nearly all devices recover after 1150h anneal time at room temperature, although they all still fail the functional test (except for one device). The TTL-stand-by current is already recovered after 15h, but after 1150h, all stand-by currents are fully recovered below the specification limit.

Acknowledgment:

The support of L. Adams, B. Johlander and M. Lopez of QCA at ESTEC in operating the Co-60 source and defining the radiation test program is gratefully acknowledged.

PART 2: HITACHI HN58C256P-20

1. Introduction

Due to limited access to the ESTEC radiation source, the tests on the HITACHI parts were performed at the Hahn-Meitner Institut in Berlin. Therefore, the aim of these tests was much more limited than for the SEEQ-parts. The parts were not cycled during irradiation, but only put under static bias conditions. Also the intermediate evaluations did not test the full parameter list of the data sheet, like for the SEEQ-parts, but only some DC-parameters and a limited functional test. No AC-parameters, like access time, write cycle time or data set-up time were tested.

2. Description of the test

The radiation test was performed at the Co-60 source of the Hahn-Meitner Institut in Berlin. The devices number 1-4 and 9-10 from lot 9016/01002310 were irradiated under static bias conditions, with V_{DD}=5V, all inputs connected to V_{DD} and all outputs open. The dose rate was 11 rad(Si)/sec and the devices were irradiated in steps of 2, 5, 10, 15, 20, 30, 35, 40 krad(Si). After 40 krad(Si) the irradiation steps were 10 or 20 krad(Si) up to the failure dose. Devices that did not fail after 40 krad(Si) were irradiated up to a dose where the first parametric or functional failure occurred.

The memory evaluation was done by a GENRAD 1734 memory tester. This tester is able to perform a quick, but limited parametric and functional test. It is however not able to determine AC-parameters very accurately, and therefore the AC-parameters were not monitored. Before the start of the test, the devices were initially programmed with a certain bit pattern. The devices with number 1-4 were programmed with an AA-55 pattern, and devices 9 and 10 with a pattern 00-FF. At the intermediate evaluation points, following limited set of DC-parameters were tested.

- Output voltage low and high: VOL (max. 0.4V), VOH (min 2.4V)
- Input leakage current: IIL (max. 2 µA), IIH (max. 2 µA)
- Active supply current: ICC3 (max. 30 mA)

• Standby supply current with CE to input high: ICC2 (max. 1 mA)
• Threshold voltages high and low: VTHH, VTHL
• Tri-state output leakage current low and high: IZL, IZH (both max. 2 μA)

The tri-state output leakage current was only monitored after it was discovered during the test that one of the parts failed due to this parameter. Before this, the parameter was not checked against the specifications.

Besides this a limited functional test was performed on the full memory. This functional test consisted of reading the whole memory and comparing the result with the pattern that was initially written. It was however not possible to detect the full list of addresses that gave an error: only the first failing address could be recorded. Reprogramming the devices at the intermediate time points was not done. Only for some devices, a reprogramming attempt was performed after the device had failed. After the occurence of a failure, the devices were re-measured after a 24h or 48hr anneal period, in order to check recovery of the failures. It was also not possible to perform an extensive electrical failure analysis to find out more detail about the exact failure mode that occurred.

Device number 5 was not irradiated, but kept as a control device. Device number 11, which came from a different lot (9004/2310) was irradiated first to control the test procedure and to get a first feeling of the radiation hardness of this type of devices.

3. Experimental results

Fig. 2.1 shows the overall results of the test, while Figs. 2.2 to 2.9 show the shifts in the parametric values of the different devices that were tested. For some parts, the radiation was continued after the occurrence of the first failure. This happened e.g. if the part recovered after a 24h or 48h annealing period (part 4 and 11). In some other cases (part 2 and 3), the occurence of the first failure was only discovered after the complete test was finished (see below).

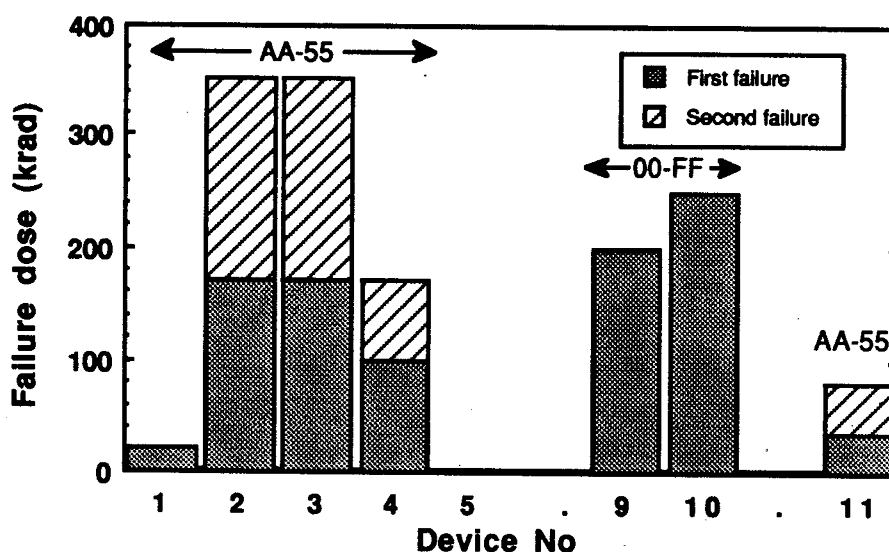

Fig. 2.1 Total dose radiation of Hitachi-parts

A first, and important conclusion that can be drawn from this figure is that all parts show a much higher tolerance against total dose radiation than the SEEQ-parts. The lowest failure dose was **20 krad(Si)**, while some parts even survived until doses **as high as 350 krad**. This is very much in contrast to the results of the SEEQ-parts, which were all failing after 18 krad.

Before discussing this more in detail, we first give a short description of the results for each individual device.

Device 11 was tested first to control the general test procedure and radiation hardness of this type of memory device. It was pre-programmed with an AA-55 bit pattern. The part showed a functional failure after 35 krad. This means that some addresses did not have the correct information after this amount of radiation. After 24h and 1 week storage at room temperature, the device kept failing at the same location and no annealing effect was observed. Then the device was reprogrammed with the same test pattern as was used initially. After this reprogramming, the device showed no parametric or functional failure anymore. This points to a real retention error, where some of the bits have lost their information after 35 krad, but are able to be reprogrammed to the correct pattern. After reprogramming, a second irradiation step was performed, and now the device again failed after 80 krad(Si), with the same functional failure as before. Again, no annealing effects were observed after 24h, and the functional test after reprogramming

showed no failure. This time, however, the old functional failure occurred again after a storage time of 10h.

Device 1 showed a failure after **20 krad(Si)**. The failure mode was that, independent of the address, all output lines showed a VOL>5V, by which no low levels could be detected anymore. This means that probably an error occurred at the output stages (e.g. the output buffers), by which the correct information could not be brought to the external pins any longer. Due to this problem, no functional test was possible anymore. After 48h anneal, no change was observed, which points to a hard error.

Device 2 showed a failure after **350 krad(Si)**. Here, the output lines 0 and 4 showed a VOH-value<100mV on the first few addresses, which seems to be related to the same kind of problem with the output stage as for device 1. Moreover, it was discovered (after the test) that, after **170 krad(Si)** the tri-state output leakage current high IZH had become larger than 2μA on the output lines 0, 2 and 4, which is out of specification. This confirms more or less the fact that something went wrong with the output stage of these lines. Due to the parameter IZH going out of specification, it was decided to monitor from then on also the parameters IZH and IZL, which were not monitored until then. Also due to these problems, a functional test was not possible after 350 krad..

Device 3 also had a tri-state output leakage current high IZH larger than 2.5 μA after **170 krad(Si)**, and consequently had a parametric failure after this radiation dose. Since this was only discovered after the test was stopped, the part was futher irradiated, and showed another failure after **350 krad(Si).** In this case, it concerned a functional (i.e reading) failure on output lines 5 and 7. These output lines failed both high and low levels on all addresses, which means that they were permanently in the "grey" zones.

Device 4 showed a failure after **100 krad(Si)**. Here, the VOH level was below 100 mV on output line 3, which again points to a problem is the output stage of this line. A functional test was not possible. This device, however, recovered after a 48 anneal time. Therefore, it was further irradiated beyond 100 krad. The second failure occurred after 170 krad, which was due to the same problem as the first failure.

Device 5 was not irradiated, but kept as a control device.

Device 9 showed a failure after **200 krad(Si)**, again due to VOH<100mV at output lines 0, 3 and 5. After 250 krad, also output line 7 showed the same failure. The functional test was not possible. For this device, it was tried to reprogram the memory, which did not succeed.

Device 10 failed after **250 krad(Si)** due to a functional failure at address 0000. It could however not be determined what was the cause for this failure, but it may be a timing problem.

On Figs. 2.2 to 2.9, the evolution of the different parameters is shown as a function of the applied dose. It is remarkable that, although most parameters show some shifts as a function of the dose, almost no parameter, except IZH, drifted out of specification. Usually, during total dose radiation testing, the first parameter that fails is the (stand-by) power supply current, specifically if the parts are biased during irradiation, as was also observed for the SEEQ-parts. For the HITACHI parts, neither the active nor the standby supply current shifted out of specification (see Figs. 2.5 and 2.6), although its specification was lower than for the SEEQ-parts. Also the input leakage current IIH shifts as a function of total dose (Fig. 2.4), but not above the specified value (2µA) upto 350 krad. Except for the devices that showed problems with the output buffers, the values of VOH and VOL had only minor shifts (Fig. 2.2 and 2.3). If the VOH and VOL-values are out of specification, they are completely failing (e.g. VOL>5V or VOH < 100mV), which does not point to a parametric shift due to some change in MOS-threshold voltage or current drive capability, but rather a catastrophic failure at the output stage.

4. Discussion

As already mentioned before, the results of this test for the HITACHI parts are somewhat surprising. Although one expects a better radiation tolerance for SNOS-technologies, radiation tolerances upto **350 krad** are beyond any expectation. The failures that were discovered nearly all point to a defect output stage, due to the fact that some of the output lines could not reach their level any longer, combined with the strongly increased tri-state output currents in some cases. Only device 11 seems to be an exception, where no problems with the output lines were observed, but where the parts showed

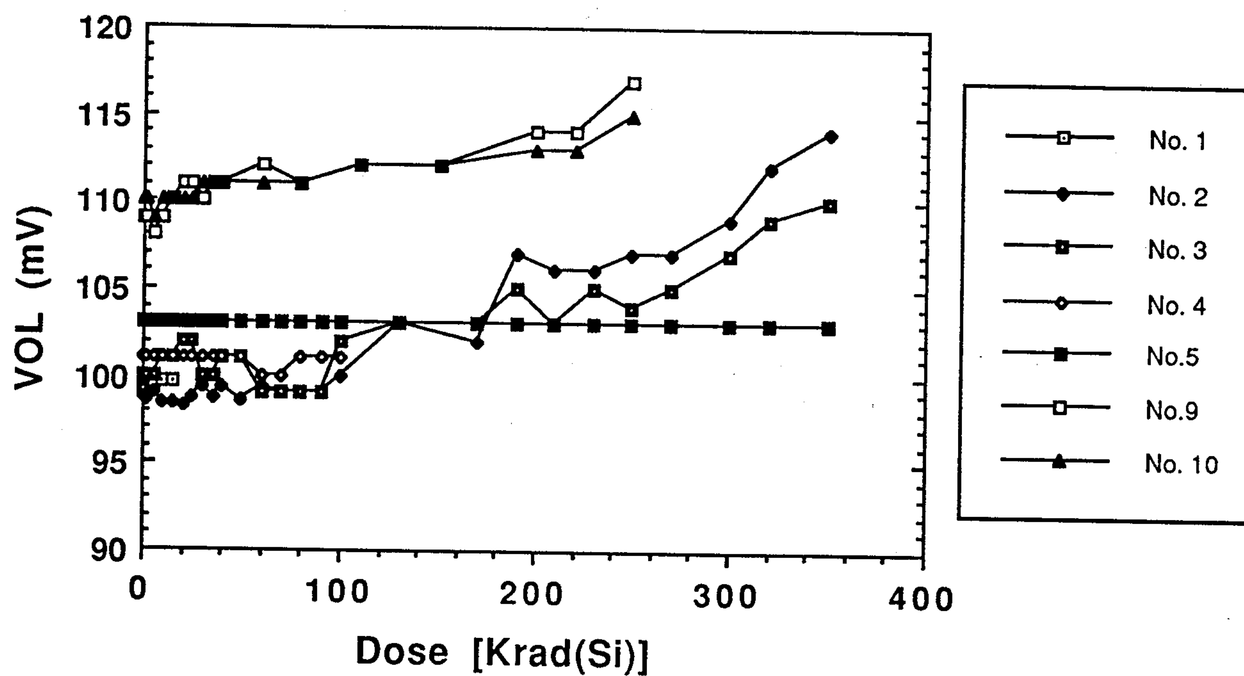

Fig. 2.2: VOL versus total dose

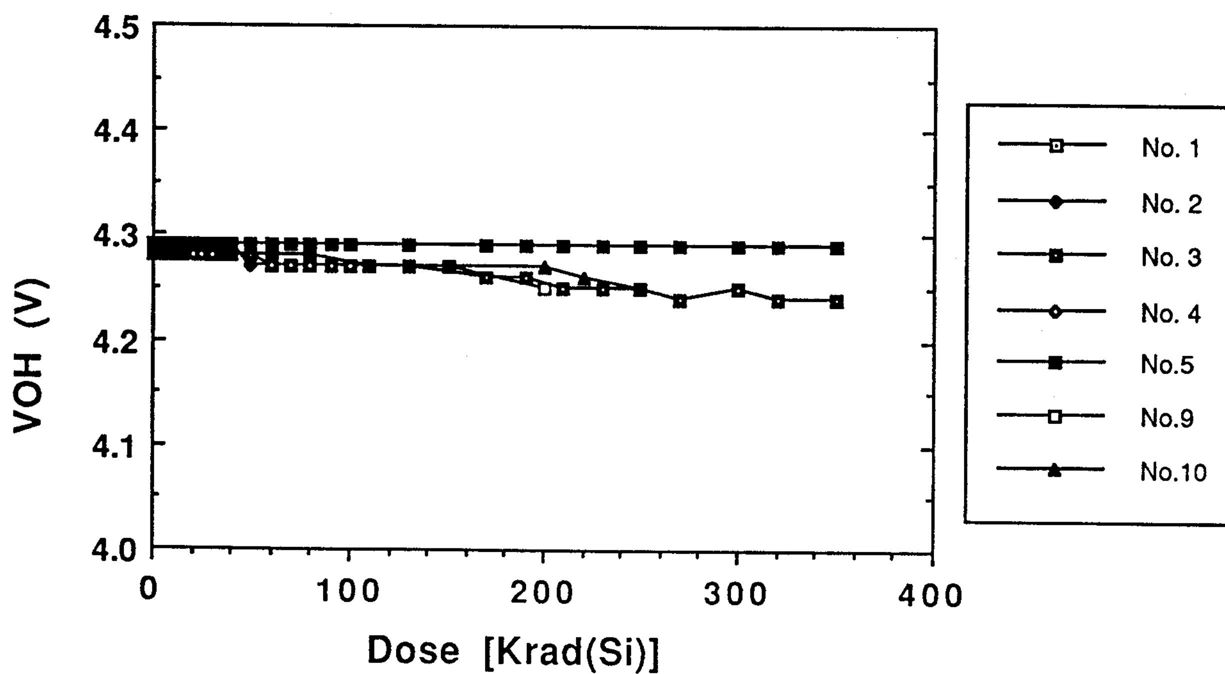

Fig. 2.3: VOH versus total dose

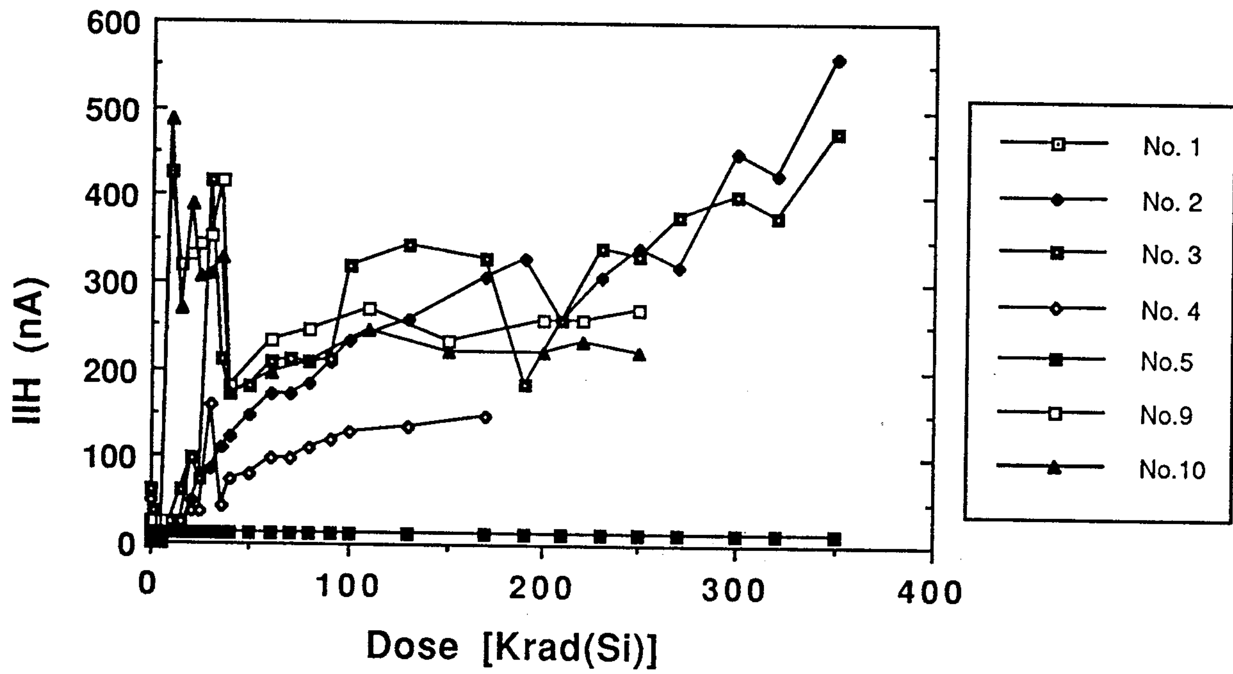

Fig. 2.4: IIH versus total dose

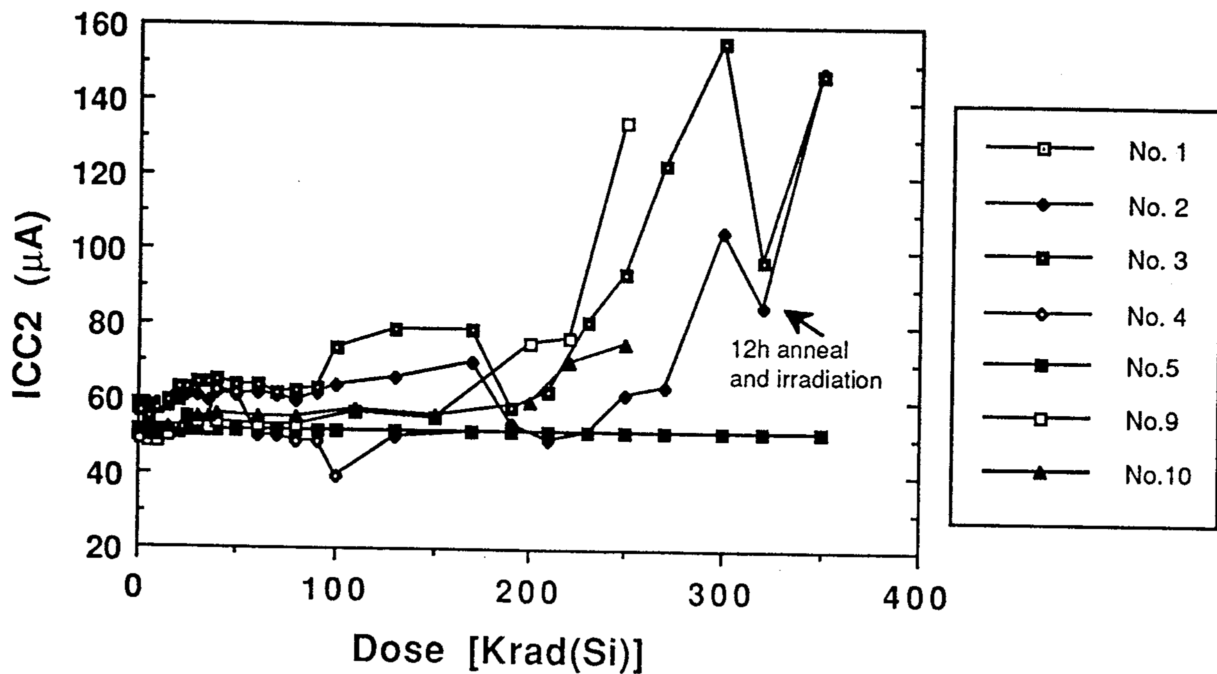

Fig. 2.5: Stand-by supply current ICC2 versus total dose

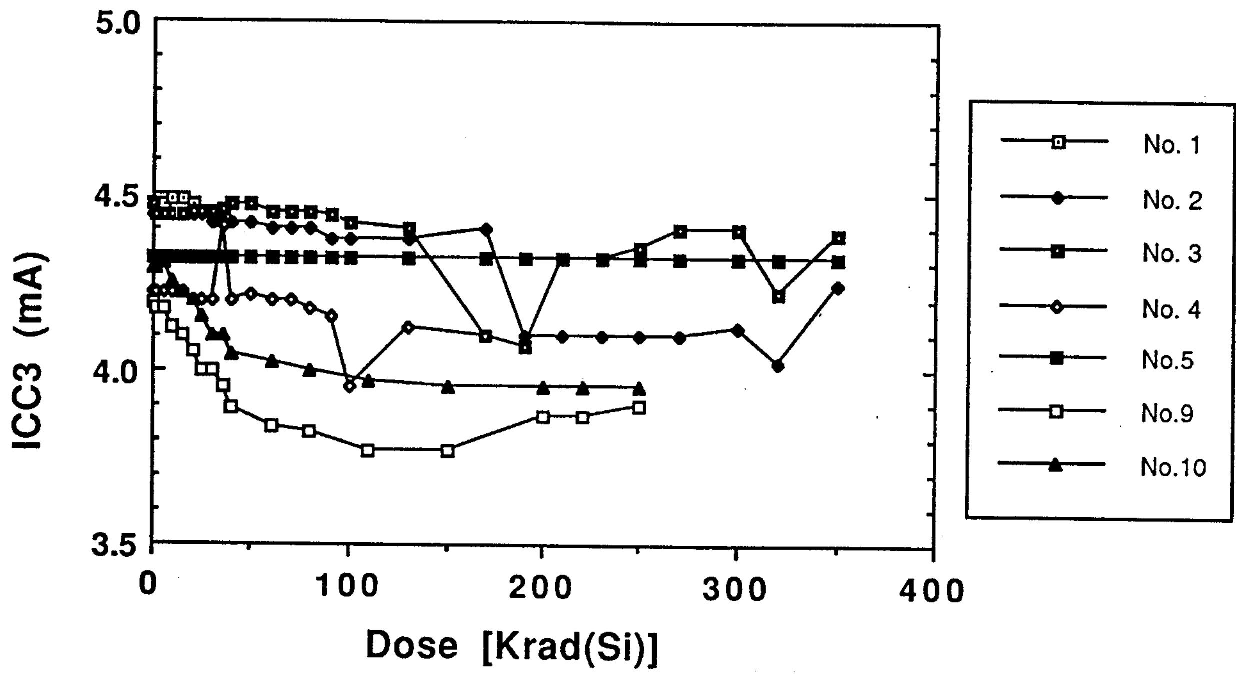

Fig. 2.6: Active supply current ICC3 versus total dose

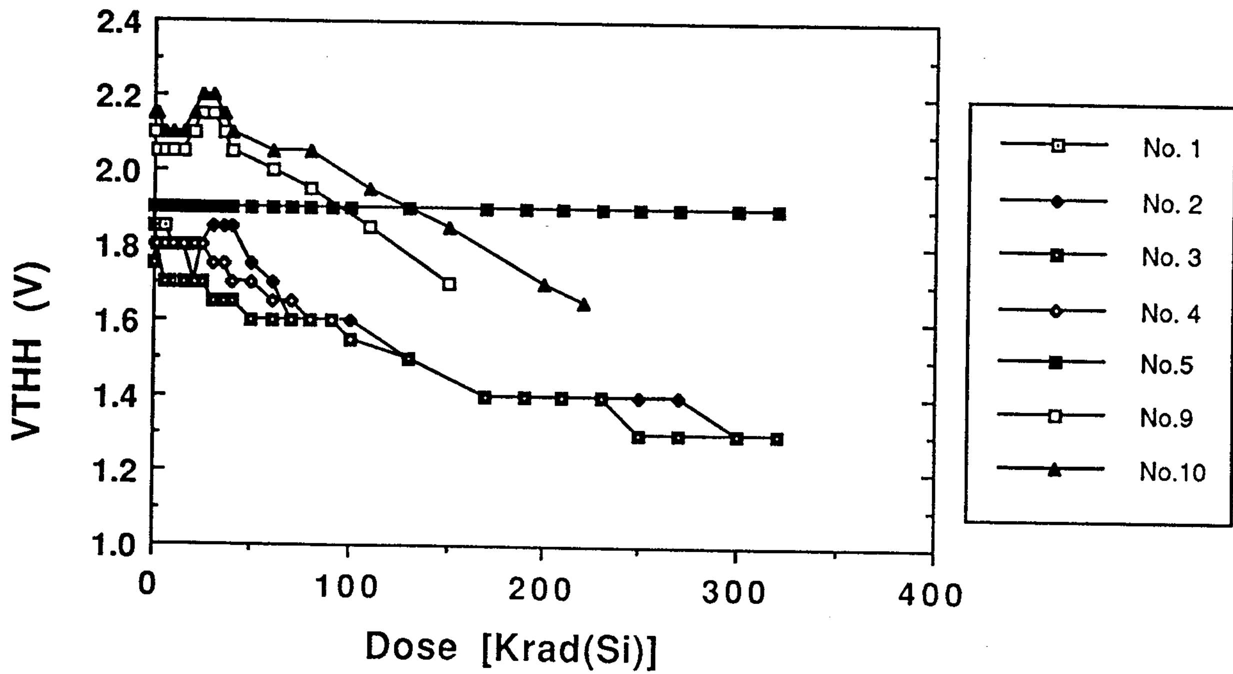

Fig. 2.7: Threshold high VTHH versus total dose

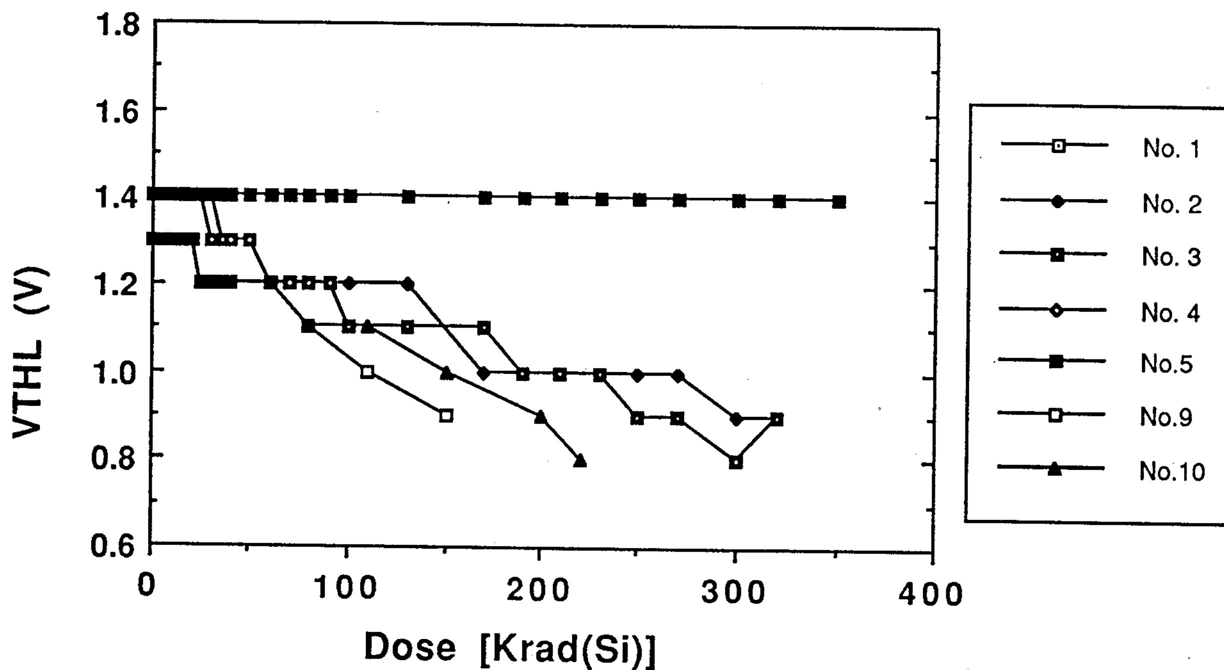

Fig. 2.8: Threshold voltage low VTHL versus total dose

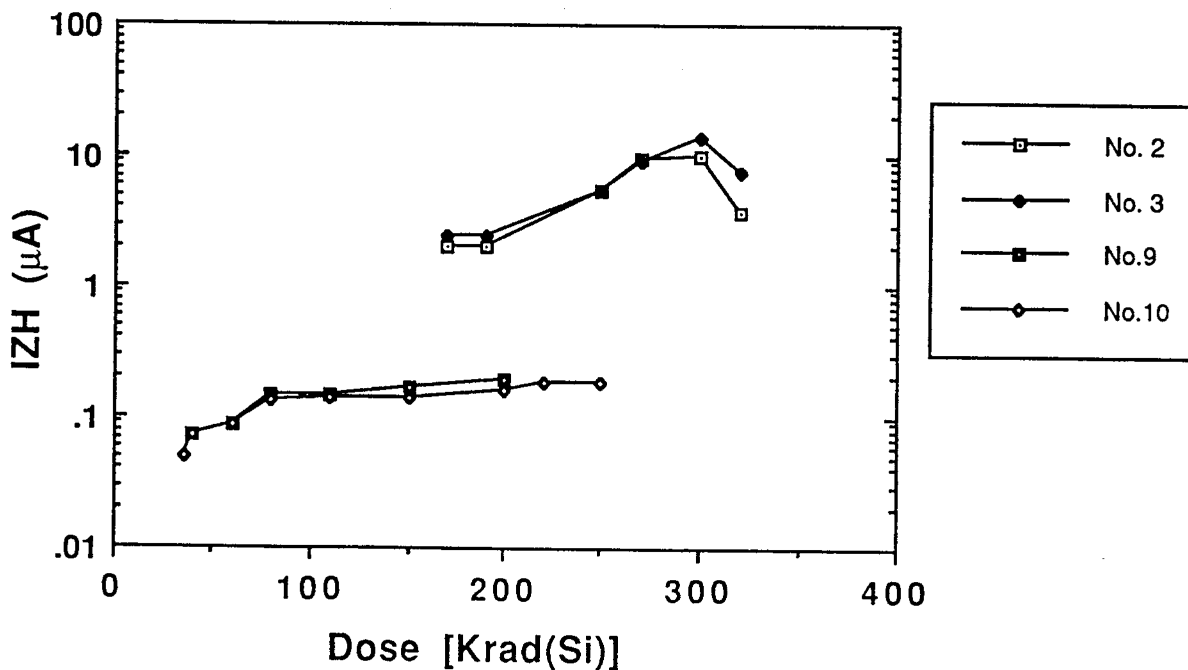

Fig. 2.9: Tri-state output current IZH versus total dose

more a retention problem. This retention problem occured after about 35 krad, and after reprogramming, again after 80 krad.

The fact that such high total dose tolerances are observed can only partly be ascribed to the weaker testconditions that were used for the HITACHI parts (only static bias during irradiation) - although even the unbiased SEEQ-parts all failed after 18krad - and the limited set of parameters that were evaluated. Also, the functional test which was done at the intermediate evaluation points was only a reading test to check if the pattern that was written at the beginning of the test was still in the memory. No reprogramming test was performed at these intermediate evaluations, in contrast to the SEEQ-evaluation, where such a reprogramming indeed was performed. Most SEEQ-parts failed the reprogramming test, although 2 devices also failed the read-test after 5 krad and 2 more after 18krad.

The reason for such unexpected high total dose tolerances is therefore not very clear. Although it is commonly known that MNOS-type memory cells, which are used in the HITACHI parts, are much more tolerant against radiation, it still is expected that the peripheral devices, which are built in a conventional CMOS-technology, would show nearly the same total dose tolerance than any other CMOS-technology. At least the power supply current should exceed its specification after some tens of krad.

5. Conclusion

The conclusion of this very limited test on the HITACHI parts therefore is that the results are considered to be unexpectedly promising, but certainly need confirmation by more extensive and detailed testing, where the full list of parameters is tested and also a full DC, AC and functional test, including reprogramming, is performed.

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