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EUROPEAN SPACE AGENCY
CONTRACT REPORT

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Title

MT4LC4M4B1DJ-6, 16 MBIT DRAM FROM MICRON

TOTAL IONISING DOSE CHARACTERIZATION TEST REPORT

ESA/ESTEC Contract No. 11755/95/NL/NB-WO1/CO1

	Name and Function	Date	Signature
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Document type	Nb WBS	Summary : Low voltage memories were tested under total ionising dose irradiation to study the effect of supply voltage on the radiation sensitivity. This report presents the results obtained on 16 Mbit Micron DRAMs.

SUMMARY OF RESULTS

Test sample characteristics :

Part Name :	MT4LC4M4B1DJ-6	**Function :**	4 M x 4 DRAM
Technology :	CMOS, 0.5 µm	**Package :**	24/26-pin plastic SOJ
Manufacturer :	Micron	**Location :**	USA
Sample size :	3 (4.5 V), 3 (3.3 V)	**Date Code :**	9640

TID test results

Functional test

The following table summarises the failure doses at the first error and at the 100th error:

S/N	V_{CC} V	Dose at 1st error krad(Si)	Error mode	Dose at 100th error krad(Si)	% of 0→1
15	**4.5**	59.8	1→0	>61.6	-
16	**4.5**	47.0	1→0	53.0	75
17	**4.5**	46.4	0→1	53.0	74
33	**3.3**	49.0	0→1	58.1	61
34	**3.3**	53.1	1→0	>59.9	-
35	**3.3**	58.4	0→1	>59.9	-

No device recovered functionally in the high temperature annealing of 168 h at 85°C.

Functional test conclusion

The results of these experiments demonstrate that on the average 16 Mbit DRAM MT4LC4M4B1DJ-6 (60ns) from Micron, when biased at 4.5 V, is more sensitive to ionising radiation than biased at 3.3 V in terms of the first error detected. This correlates with the average dose at 100th error: biased at 3.3 V the better radiation tolerance is reached compared to the 4.5 V biasing mode.

Parametric test

The following table summarises the average dose levels for both bias at which sensitive parameters have drifted **20%**:

Parameter	**Dose Level** V_{CC} **= 4.5 V**	**Dose Level** V_{CC} **= 3.3 V**
Standby supply current	35 krad(Si)	40 krad(Si)
Operating supply current	>60 krad(Si)	>60 krad(Si)

Parametric test conclusion

The results of these experiments demonstrate that 16 Mbit DRAM MT4LC4M4B1DJ-6 (60ns) from Micron biased at 4.5 V is more sensitive to ionising radiation than at 3.3 V bias.

DOCUMENT CHANGE LOG

Issue/ Revision	Date	Modification Nb	Modified pages	Observations
1	20/10/97			Original Edition

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Issue of this document comprises the following pages at the issue shown

Page	Issue/ Revision	Page	Issue/ Revision	Page	Issue/ Revision	Page	Issue/ Revision	Page	Issue/ Revision	Page	Issue/ Revision
All	1										

DISTRIBUTION LIST

		Overall document		Summary
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TABLE OF CONTENTS

1. INTRODUCTION

The aim of this work is to investigate radiation effects in low voltage technologies. The study is focused on memory devices, which require lower voltage to achieve higher integration. Parts selected consists of SRAMs (1 Mbit, 2 types), DRAMs (16 Mbit, 2 types), and FLASH memories (8 Mbit, 2 types).

The object of this document is to describe the irradiations performed on the Micron 16 Mbit MT4LC4M4B1DJ-6 (60ns), in order to measure the influence of two different supply voltage levels on the total ionising dose sensitivity.

Irradiations were performed in March 1997 (10^{th}-17^{th}) according to the procedures referenced in the following paragraph.

This work was performed in the frame of the WO1/CO1 for ESTEC Contract n°11755/95/NL/NB.

2. REFERENCE DOCUMENTS

[1] ESA/SCC 22900-4 ESA Basic Specification for Total Dose Steady-State Irradiation

[2] Micron Manufacturer Data Sheet

[3] Description of the VTT memory tester, AUT/PRO/76/96 (in Finnish)

[4] "Radiation effects in 5V and advanced lower voltage DRAMs" D.C. Shaw, IEEE Trans. On Nucl. Sci., Dec. 94, No6, p2452.

3. PART DETAILS

3.1. DEVICE IDENTIFICATION

3.1.1. References

Type	:	MT4LC4M4B1DJ-6
Manufacturer	:	Micron
Place	:	USA
Packaging	:	24/26-pin plastic SOJ

3.1.2. Function

4 M x 4 bit DRAM (60 ns)

3.1.3. Technology

CMOS (See next page for further details)

3.1.4. Part Procurement

Origin	:	VTT Automation, Finland
Level	:	Standard Level
Temperature range	:	-25°C, +85°C (Industrial)
Date code	:	9640
Screening	:	/
Sample size	:	3 (biased at 4.5 V), 3 (biased at 3.3 V)
Manufacturer Marking	:	MT4LC4M4B1DJ-6 9640 F USA CR67
Detailed specifications	:	Manufacturer Data sheet

3.1.5. Previous TID details/history

No radiation data on this device. Another 16 Mbit version from Micron was proviously tested, and exhibited a lower Total Dose tolerance (functional failure at 30 krad), but the tests were performed at high dose rate (>72 krad/h) [4].

3.2. TECHNICAL INFORMATION

The 16 Mbit MT4LC4M4B1DJ-6 DRAM from Micron is a device that can be operated at 3.3V or at 4.5V.

The functionality and the parametric integrity of the devices were examined prior to irradiation. No screening nor burn-in were carried out during this study.

General information

Name	Micron MT4LC4M4B1DJ-6
Package Marking	MT4LC4M4B1DJ-6 9640 F USA CR67
Access time/ns at 4.5V	60
Temperature range/°C	-25, +85
Organisation	4 M x 4
Supply Voltage/V	3.0 - 4.6

Technology

Name	Micron MT4LC4M4B1DJ-6
CMOS	yes
Mask	D28
Epitaxial layer	No (bulk)
Design rules	0.35 µ
Die size	5.6 mm x 10.2 mm
Cell size	0.875 µm x 1.75 µm

* The missing information was unsuccessfully required from the manufacturer.

* Two other versions followed the D28 version: D42 and D52 (0.3 µm). The D28 version is no longer commercialized.

4. TEST DESCRIPTION

4.1. IRRADIATION FACILITY

Name MMS Cobalt 60-source, model Shepherd 484

Location Matra Marconi Space France
37, avenue Louis Bréguet
78146 VELIZY-VILLACOUBLAY Cedex
France

Activity < 8.9 curies.

Calibration 10/03/97.

4.2. TID TEST SET-UP

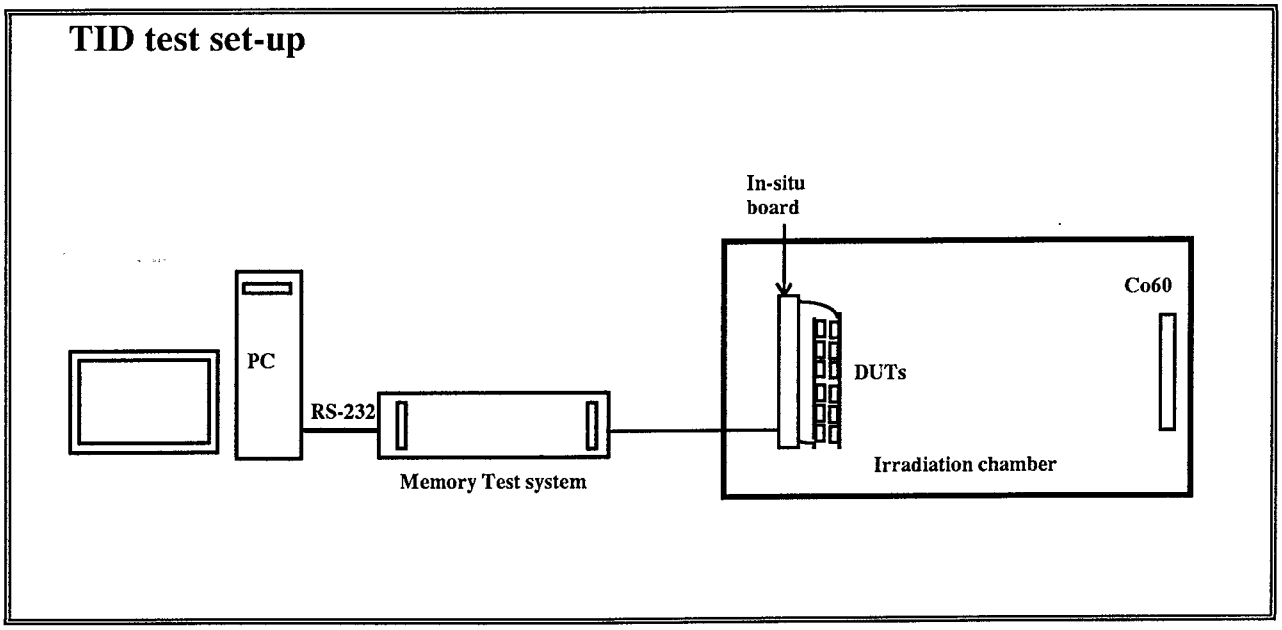

Fig 4.1. Description of the TID test set-up.

The DUTs were soldered on small PCB's with pin headers. They were mounted on the two large PCB's that were biased at 4.5 V and 3.3 V. The distance between 4.5 V and 3.3 V devices were 2 mm from package to package. The difference in dose rates was taken into account when computing the doses received by the devices.

The device under test was selected by a chip select logic located in the In-situ board. The supply voltage was provided by the memory tester. A complete description of the memory tester is given in [3].

The test flow chart is given in fig. 4.2.

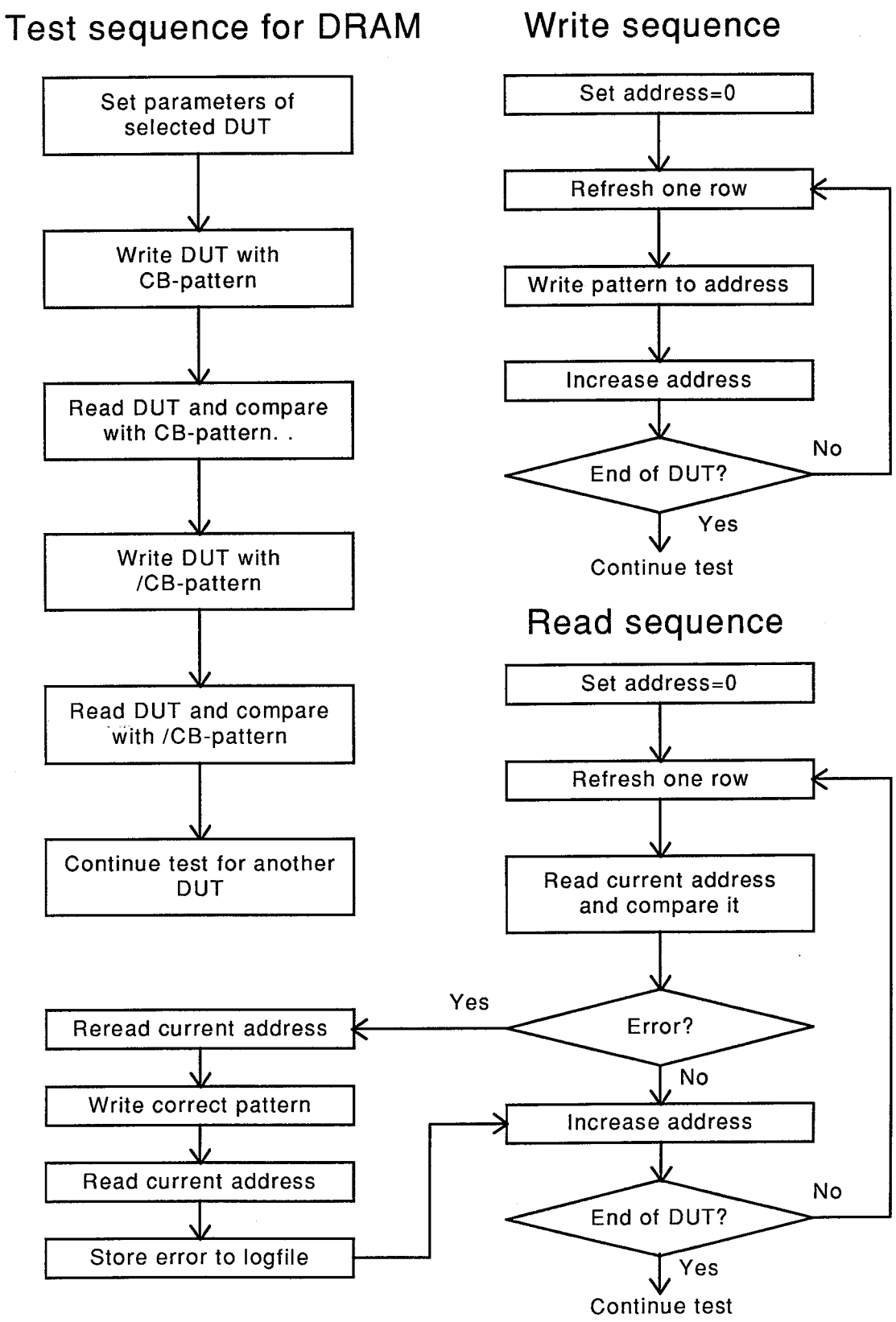

Fig. 4.2. The test flow chart of an individual device with write and read sequencies.

The write and read cycles during functional test were as follows:

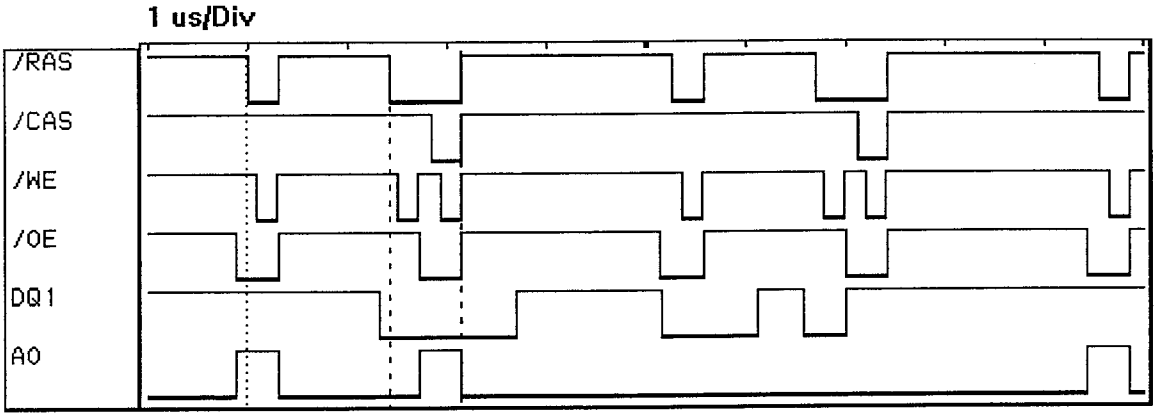

Fig. 4.3. Write Cycle of MICRON DRAM during functional test.

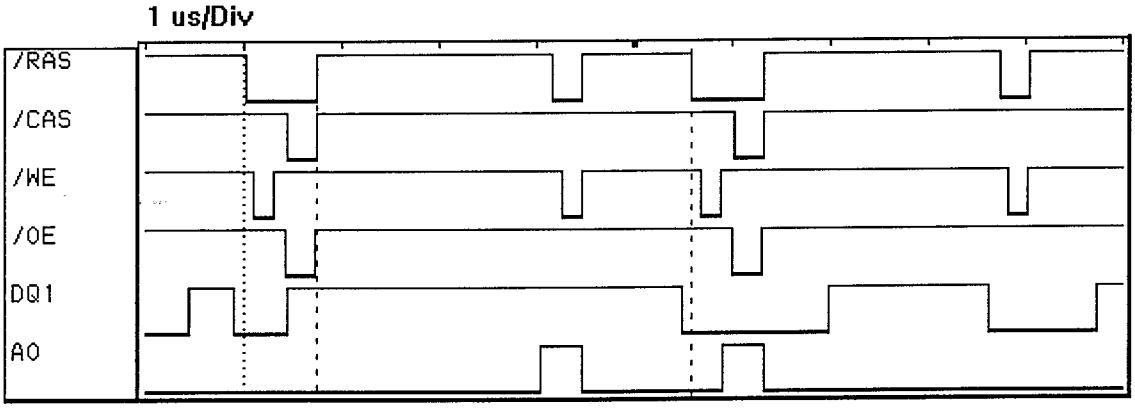

Fig. 4.4. Read Cycle of MICRON DRAM during functional test.

5. TOTAL IONISING DOSE EXPERIMENTAL RESULTS

5.1. TID IRRADIATION TEST SEQUENCE

During irradiations all the devices were functionally tested 3 times per hour automatically in the exposure chamber, and the results were stored on a hard disk of the measuring computer. The memory test started with the write of a CB (checkerboard) pattern to the memory device. Thereafter the memory contents of the device was read and it was compared to the original pattern. After this the memory was tested with a complementaly CB pattern in an identical way. During the irradiation, the memory contents was the complementaly CB pattern. Therefore, this represents the worst case testing.

If errors were encountered, the corrupted data was immediately reread and rewritten with the original pattern. The write operation was verified with another read. In this way peripheral circuitry errors, memory cell errors, write errors and stuck bits can be indicated. Due to the limitation of the measuring computer, the maximum number of recorded corrupted bytes was set to 100. TTL levels were applied in control, address and data signals. 4.5 V bias was applied to devices s/n 15-17 and 3.3 V bias was applied to devices s/n 33-35.

In the time between the irradiations, the parameters were measured remotely at the end of each step within two hours with the VTT parametric tester in another room. Except the measurement, the devices were unbiased during this time. The resolution of the voltage measurements was 1.2 mV. The irradiation was accomplished in seven steps. The average dose rates were 420 rad(Si)/h and 410 rad(Si)/h for 4.5 V and 3.3 V devices, correspondingly. The dose rates and cumulative doses with durations of each irradiation are given in table 5.1.

Table 5.1. Dose rates, durations and cumulative doses for 4.5 V and 3.3 V Micron DRAMs.

Step	Dose rate 4.5 V rad(Si)/h	Dose rate 3.3 V rad(Si)/h	Duration h	Total Dose 4.5 V krad(Si)	Total Dose 3.3 V krad(Si)
1	262.0	258.1	20.00	5.2	5.1
2	327.5	317.3	19.00	11.5	11.2
3	471.6	458.1	8.00	15.2	14.8
4	471.6	458.1	12.00	20.9	20.4
5	471.6	458.1	19.17	29.9	29.1
6	471.6	458.1	7.18	33.3	32.4
7	471.6	458.1	60.00	61.6	59.9

After the last irradiation step and parametric measurement, the devices were put into a heat chamber for an annealing period of 168 h at 85°C. The devices were functionally tested 3 times per hour. The test set-up for the Micron DRAMs was the same one as during irradiation.

5.1.1. Problems encountered/Discussion

No specific problem was encountered during irradiations.

5.2. TID TEST RESULTS

Functional test

The following table summarises the failure doses in the functional test:

Table 5.2. Failure doses at first and 100th errors with error modes.

S/N	V_{cc} V	Dose at 1 error krad(Si)	Error mode	Dose at 100th error krad(Si)	% of 0→1	Annealing	Remarks
15	4.5	59.8	1→0	>61.6		No functional recovery	1 error: 1→0
16	4.5	47.0	1→0	53.0	75	No functional recovery	
17	4.5	46.4	0→1	53.0	74	No functional recovery	
33	3.3	49.0	0→1	58.1	61	No functional recovery	
34	3.3	53.1	1→0	>59.9		No functional recovery	6 errors; 5: 0→1
35	3.3	58.4	0→1	>59.9		No functional recovery	21 errors; 14: 0→1

The average first error dose was 53.5 krad(Si) for 3.3 V bias and 51.1 krad(Si) for 4.5 V bias. One device of 4.5 V bias and two devices of 3.3 V bias did not fail within the maximum dose. The lower bias tends to increase to dose tolerance at both error level.

At 4.5 V bias the first error mode was the transition 1→0 in two devices. At 3.3 V bias the first error mode was the transition 0→1 in two devices.

All devices failed in the parametric test after the last irradiation step. No device recovered functionally in the high temperature annealing of 168 h at 85°C.

Detailed functional test results are given in appendices 1 and 2.

Functional test conclusion

The results of these experiments demonstrate that on the average 16 Mbit DRAM MT4LC4M4B1DJ-6 (60ns) from Micron, when biased at 4.5 V, is more sensitive to ionising radiation than biased at 3.3 V in terms of the first error detected. This correlates with the average dose at 100th error: biased at 3.3 V the better radiation tolerance is reached compared to the 4.5 V biasing mode.

Parametric test

The table 5.3 summarises the average dose levels at which parameters have drifted 20% and the average relative recovered values after 168 h at 85°C annealing for both bias. The average relative recovery indicates the recovered value after annealing divided by the preirradiated value.

Table 5.3. Average dose levels at 20% drift and relative recovery after annealing.

Symbol	Parameter	Dose Level/krad(Si)		Parametric recovery	
		V_{CC} = 4.5 V	V_{CC} = 3.3 V	V_{CC} = 4.5 V	V_{CC} = 3.3 V
I_{CCSB}	Standby Supply Current	35	40	0.2	0.5
I_{CCOP}	Operating Supply Current	>60	>60	1.0	1.0
I_{IL}	Input Current Low Level	>60	>60	0.9	1.0
I_{IH}	Input Current High Level	>60	>60	1.0	1.0
I_{OZL}	Output Leakage Current High Impedance Low level Applied	>60	>60	0.9	0.9
I_{OZH}	Output Leakage Current High Impedance High Level Applied	>60	>60	1.0	1.0
V_{OL}	Output Voltage Low Level	>60	>60	1.0	1.0
V_{OH}	Output Voltage High Level	>60	>60	1.0	1.0
T_{AOE}	Output Enable Access Time	>60	>60	1.0	1.0
T_{ACS}	Chip Select Access Time	>60	>60	1.0	1.0

The parameters were very stable to 30 krad at both bias modes. Except I_{CCSB} , the parameters are almost insensitive to total dose up to the maximum dose. 3.3 V bias slightly increases the tolerance compared to the higher one.

After annealing, I_{CCSB} recovered to a value less than the preirradiated one at both bias modes.

Parametric test results are given as graphs in appendix 3.

Parametric test conclusion

The results of these experiments demonstrate that 16 Mbit DRAM MT4LC4M4B1DJ-6 (60ns) from Micron DRAM biased at 4.5 V is more sensitive to ionising radiation than when biased at 3.3 V.

6. CONCLUSION

Ionising dose tests were performed on the 16 Mbit DRAM MT4LC4M4B1DJ-6 from Micron with 3.3 V and 4.5 V bias. The dose tolerance of the device is good.

The results of the functional tests demonstrate that MT4LC4M4B1DJ-6, when biased at 4.5 V, is more sensitive to ionising radiation than biased at 3.3 V in terms of the first error detected. The results of the parametric tests indicate that MT4LC4M4B1DJ-6, when biased at 4.5 V, is more sensitive to ionising radiation than biased at 3.3 V in terms of the parametric drifts.

APPENDIX 1. Functional test results for 4.5 V Micron devices.

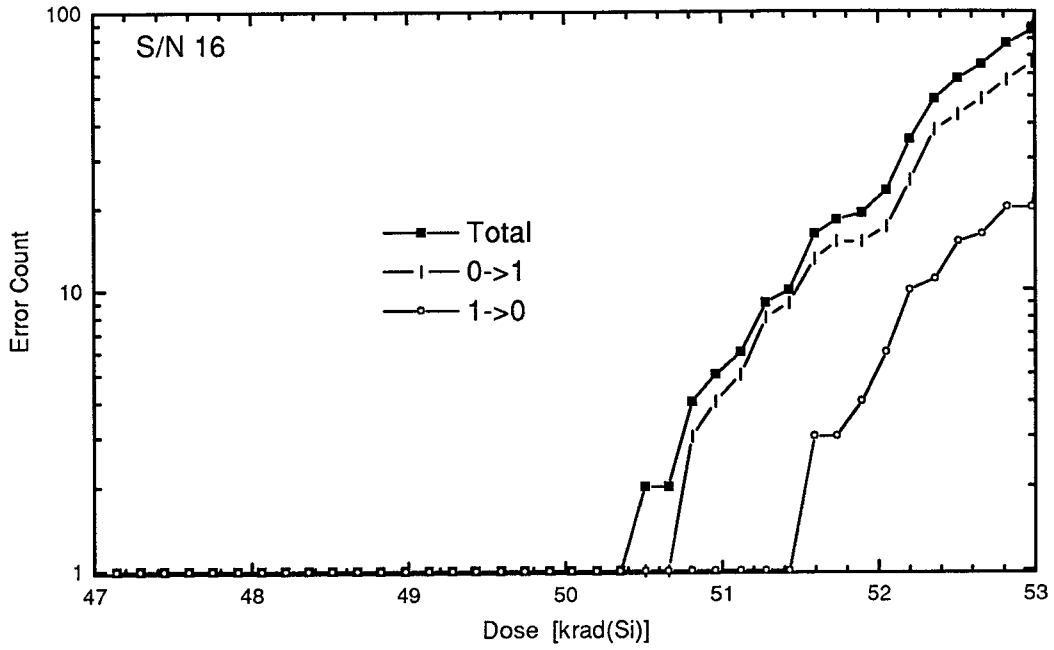

Fig. 1. Error count with modes 0→1 and 1→0 versus dose in 4.5 V Micron DRAM s/n 16.

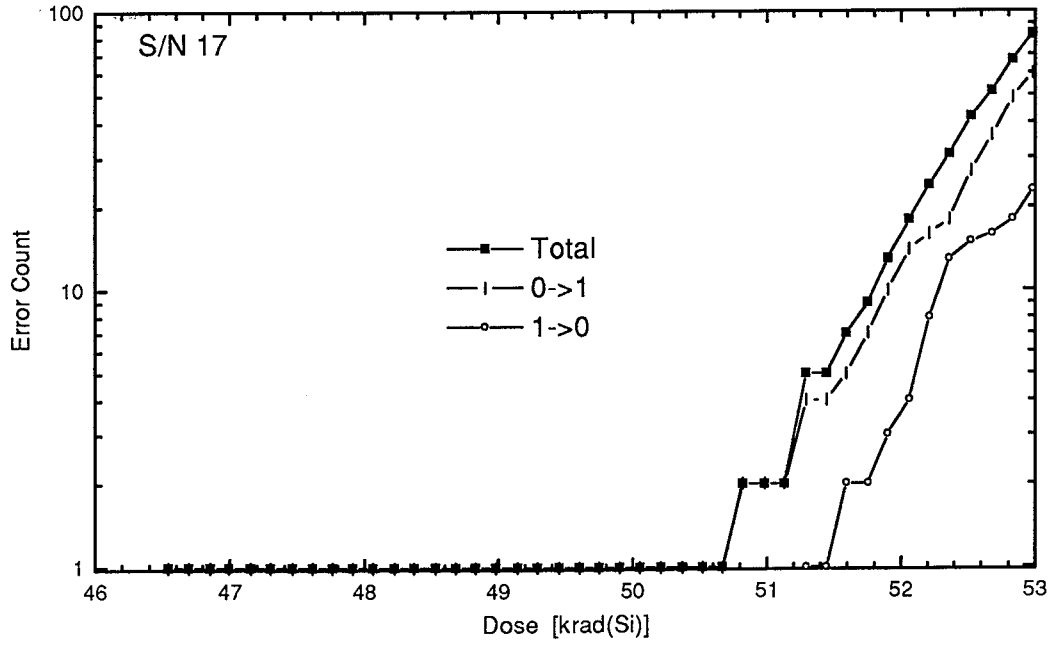

Fig. 2. Error count with modes 0→1 and 1→0 versus dose in 4.5 V Micron DRAM s/n 17.

APPENDIX 2. Functional test results for Micron 3.3 V devices.

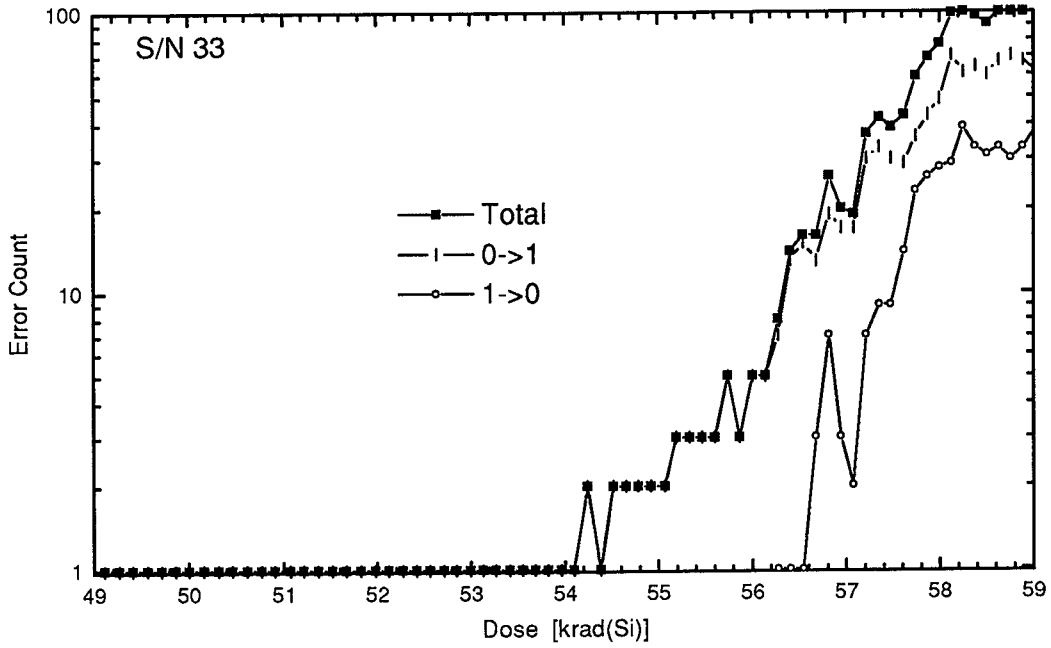

Fig. 1. Error count with modes 0→1 and 1→0 versus dose in 3.3 V Micron DRAM s/n 33.

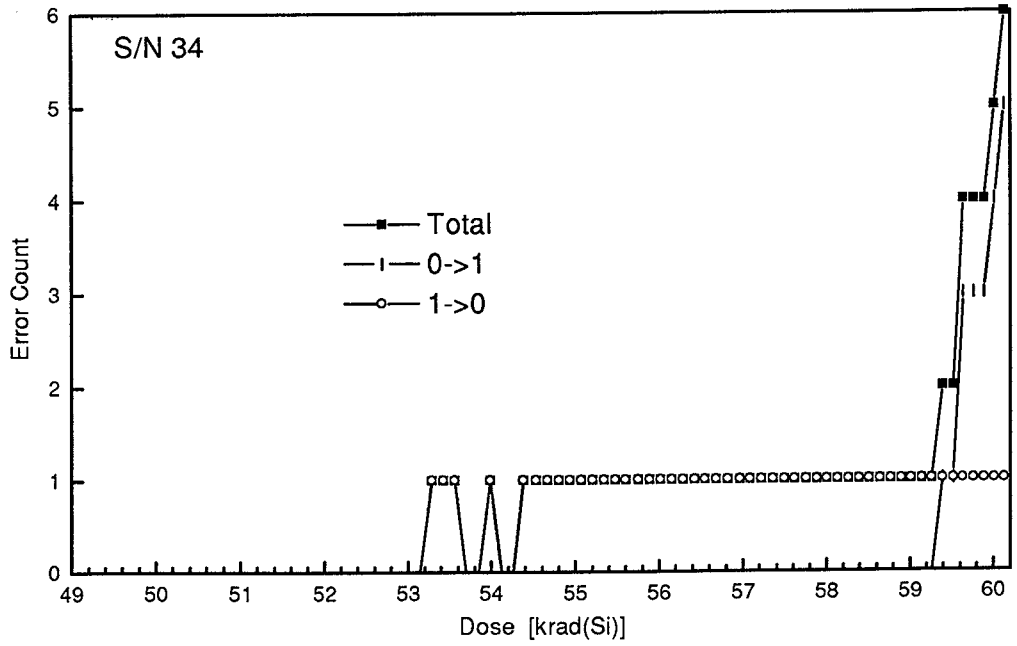

Fig. 2. Error count with modes 0→1 and 1→0 versus dose in 3.3 V Micron DRAM s/n 34.

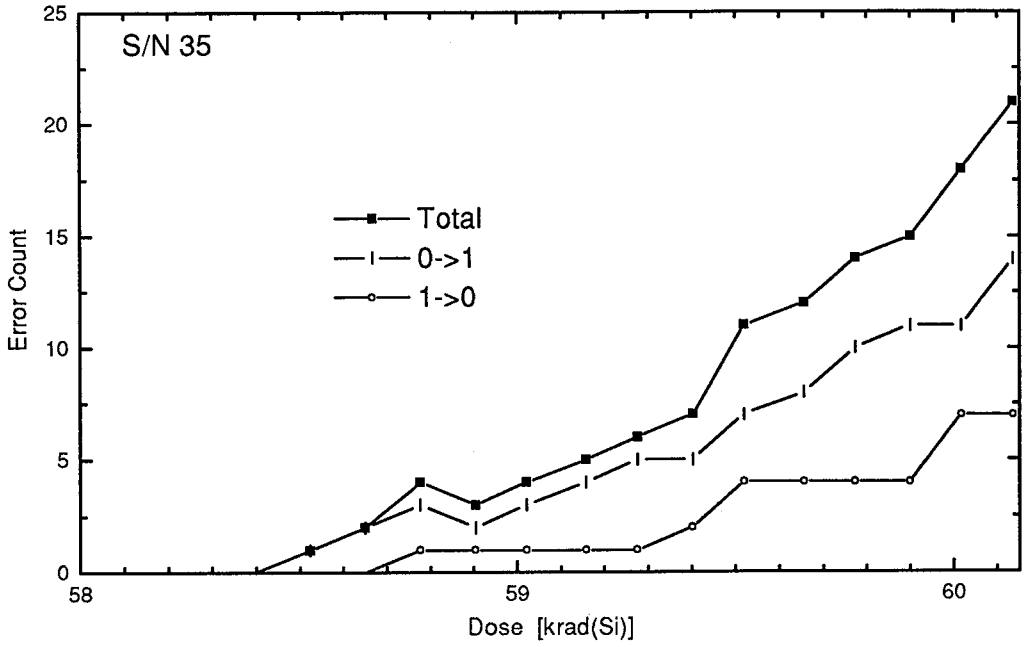

Fig. 3. Error count with modes 0→1 and 1→0 versus dose in 3.3 V Micron DRAM s/n 35.

APPENDIX 3. Parametric test results for Micron DRAM devices.

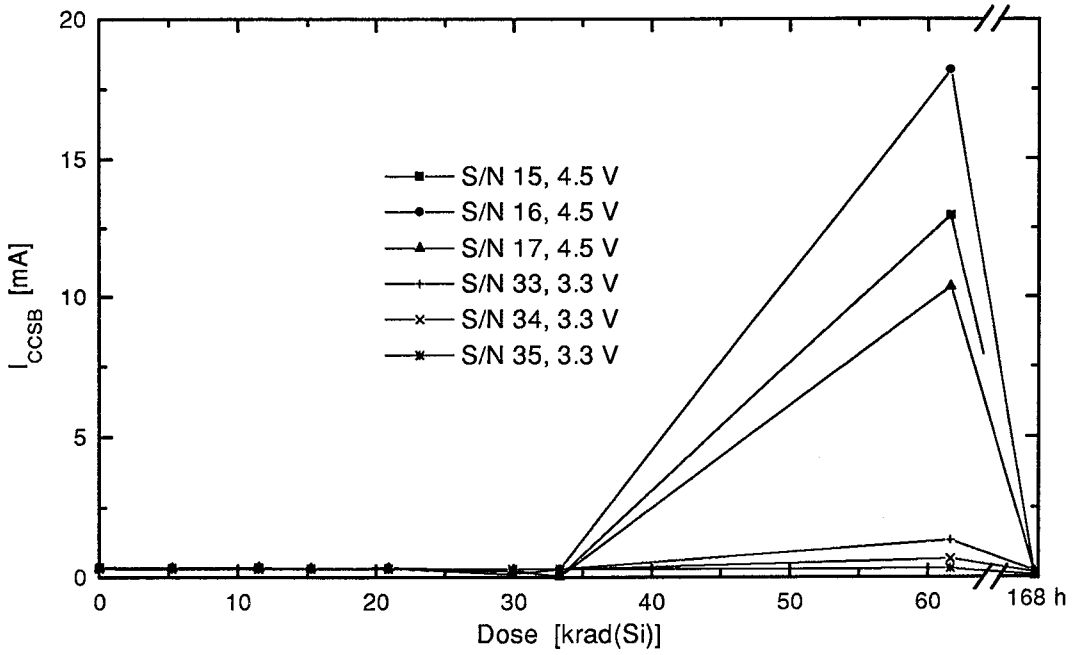

Fig. 1. Standby supply current versus dose and after annealing for Micron DRAMs.

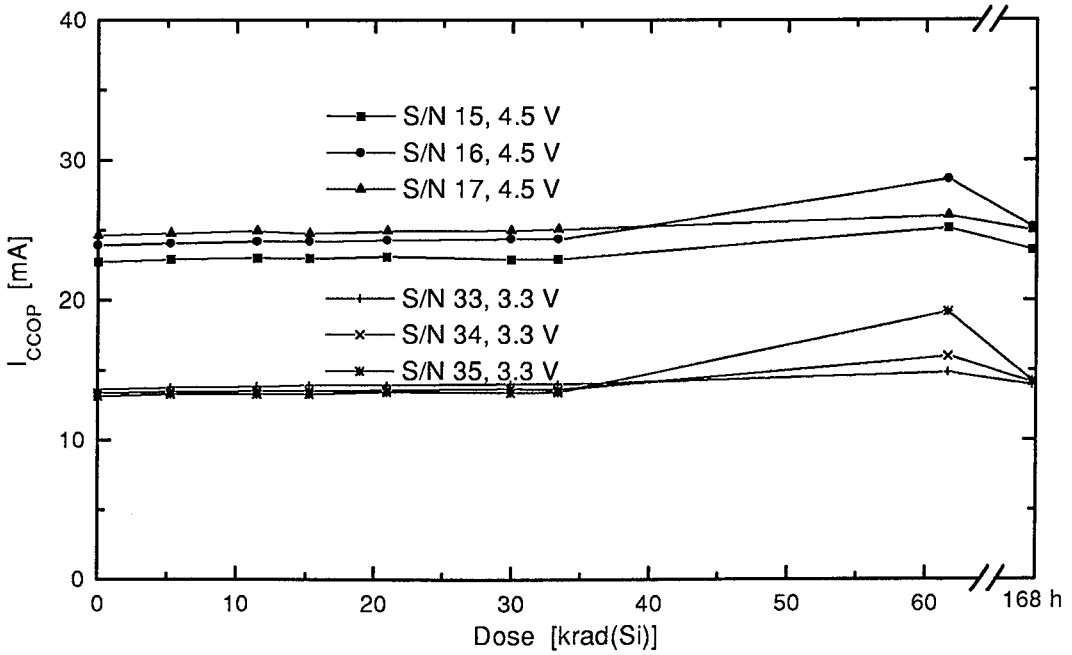

Fig. 2. Operating supply current versus dose and after annealing for Micron DRAMs.

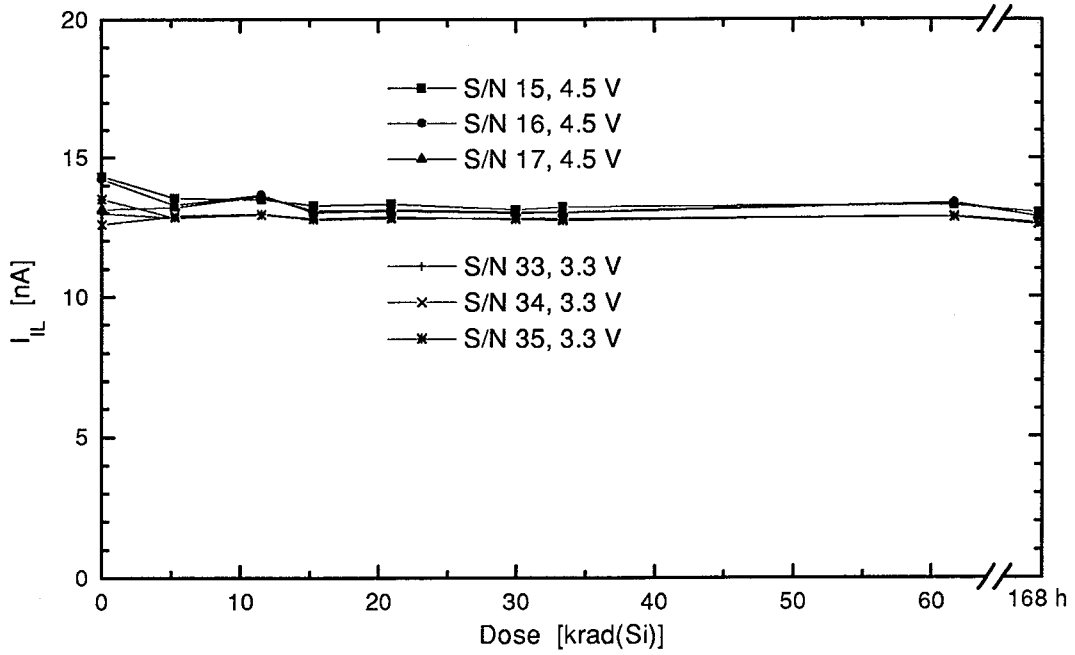

Fig. 3. Input current low level versus dose and after annealing for Micron DRAMs.

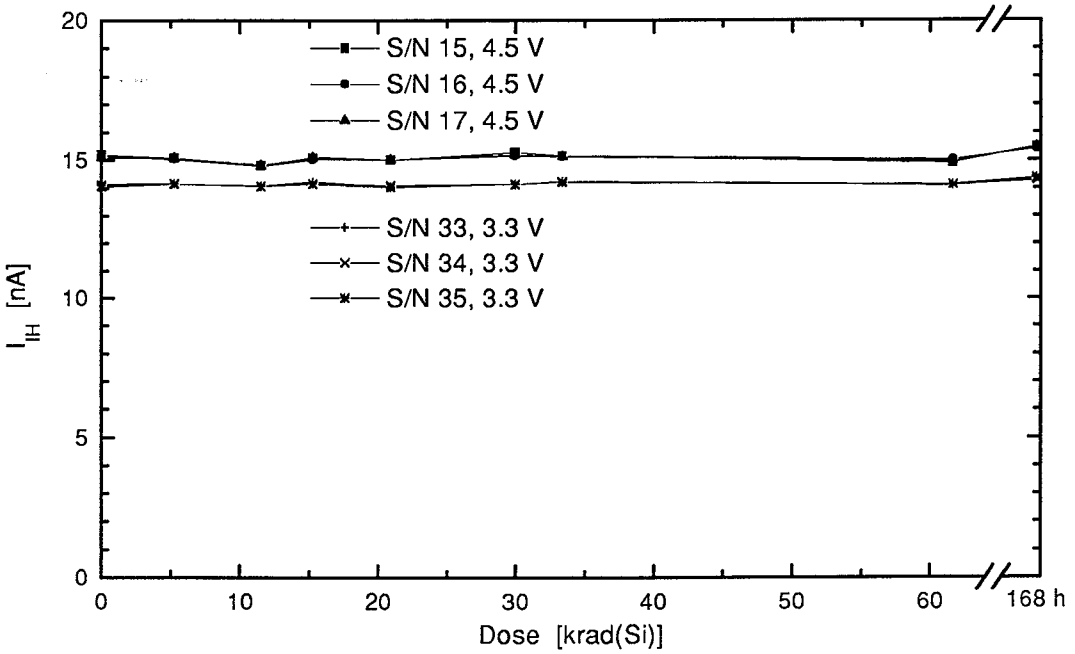

Fig. 4. Input current high level versus dose and after annealing for Micron DRAMs.

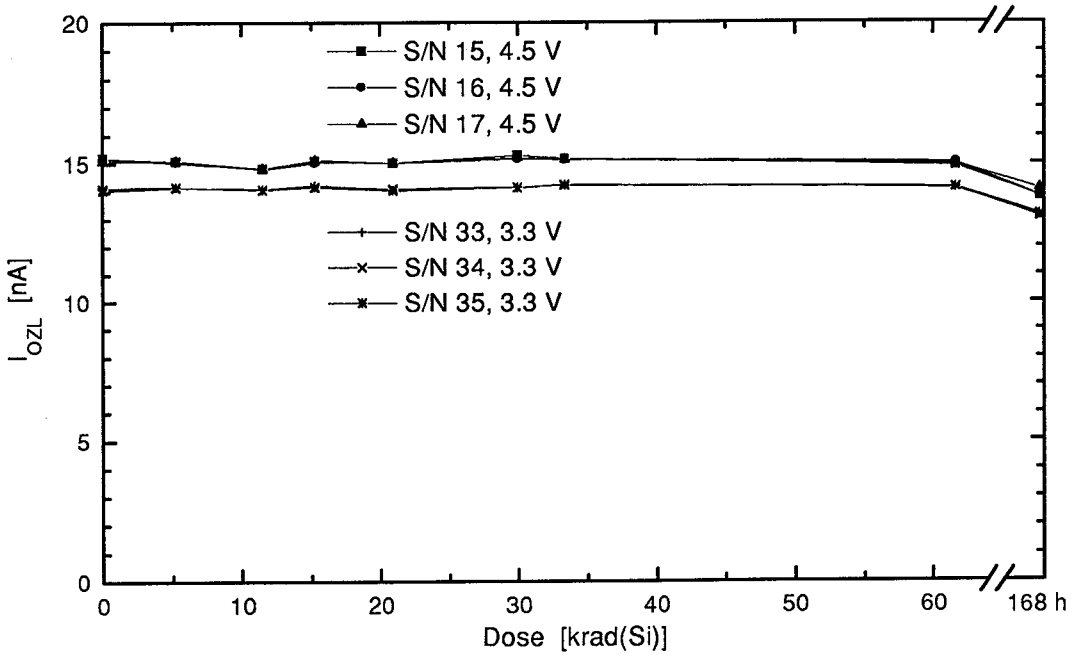

Fig. 5. Output leakage current third state low level applied versus dose and after annealing for Micron DRAMs.

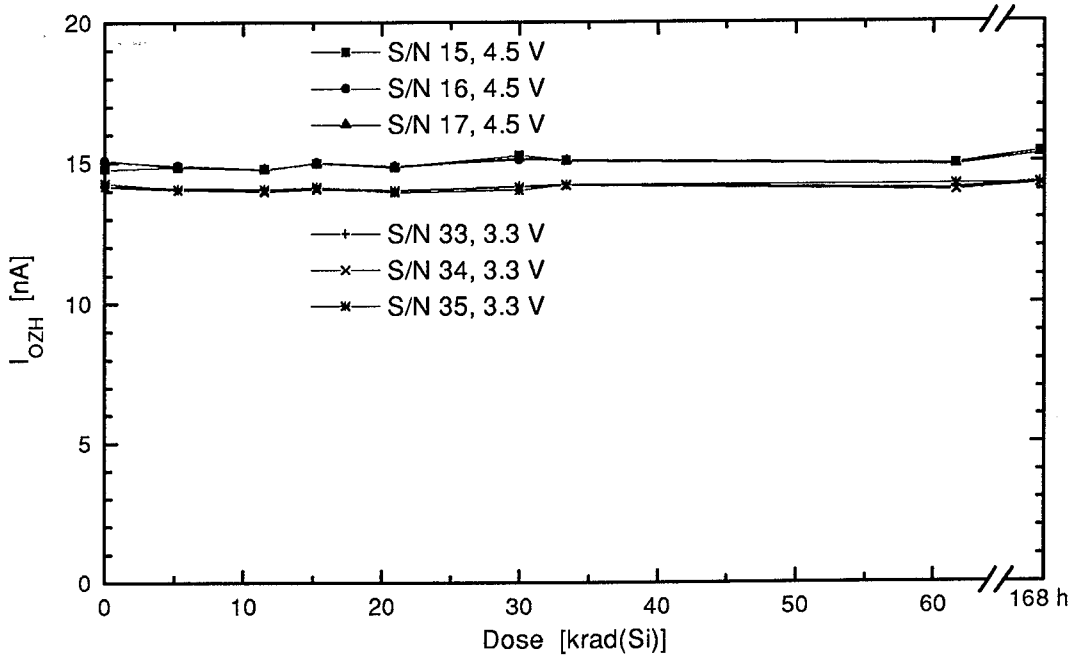

Fig. 6. Output leakage current third state high level applied versus dose and after annealing for Micron DRAMs.

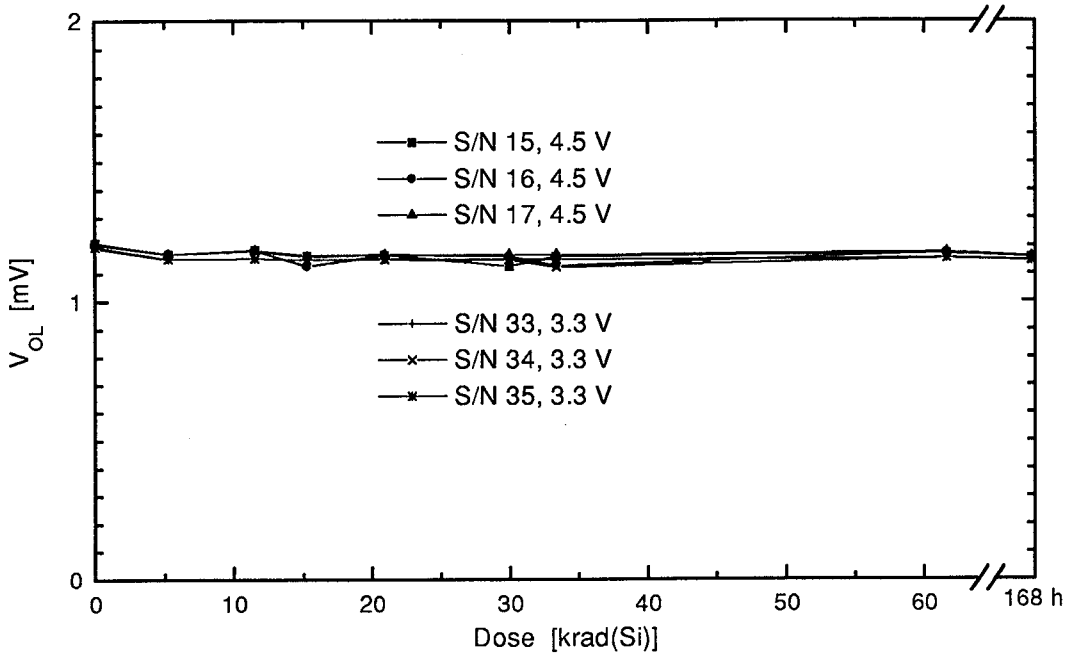

Fig. 7. Output voltage low level versus dose and after annealing for Micron DRAMs.

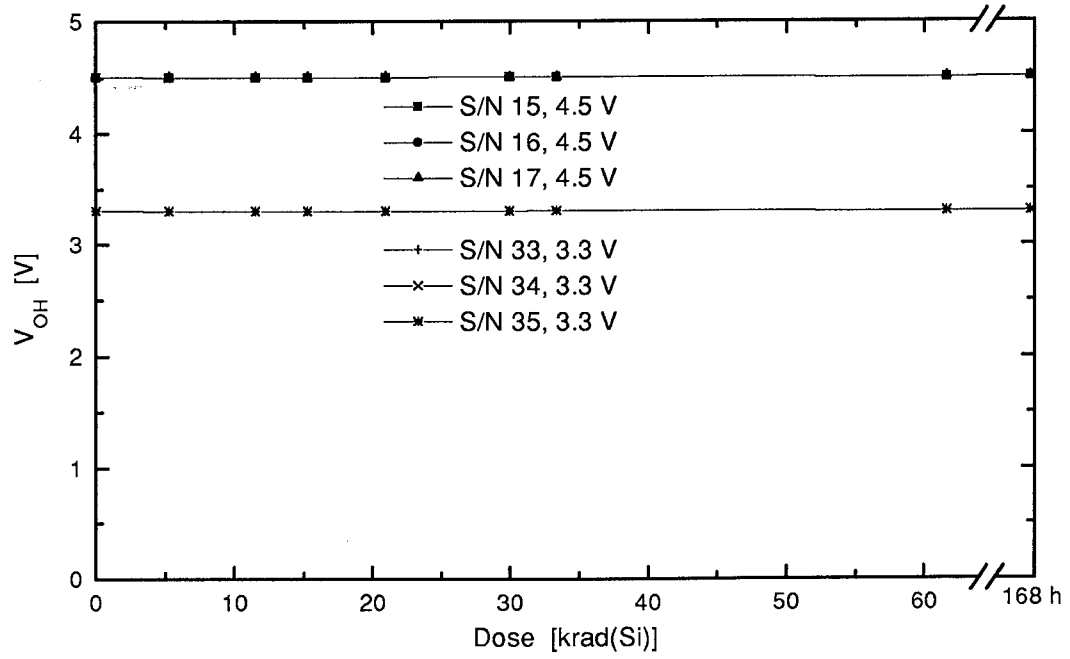

Fig. 8. Output voltage high level versus dose and after annealing for Micron DRAMs.

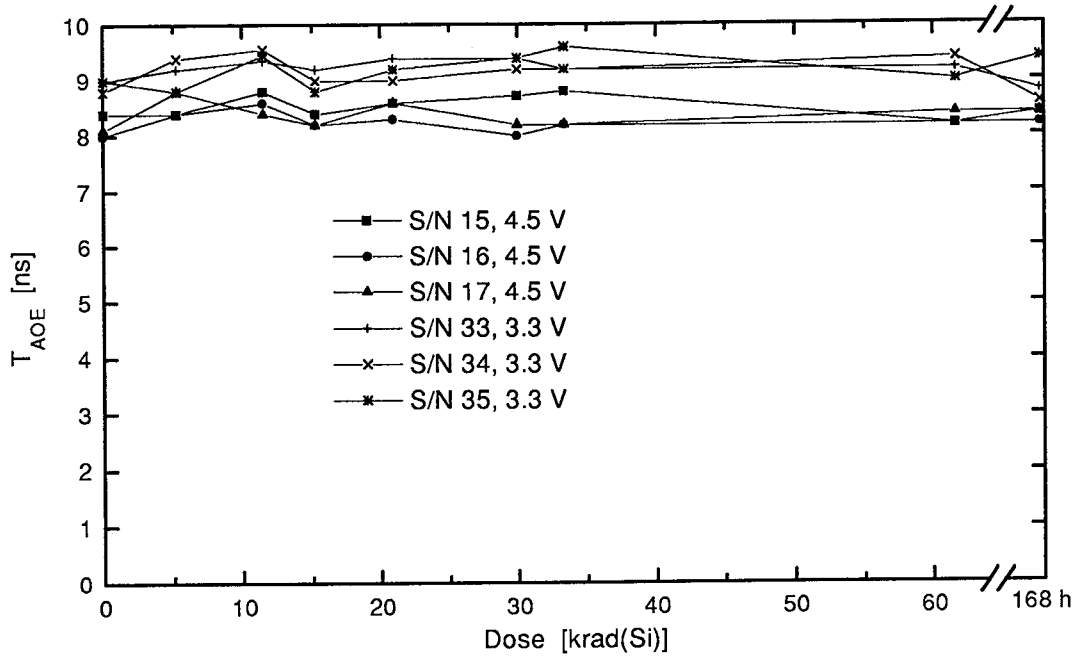

Fig. 9. Output enable access time versus dose and after annealing for Micron DRAMs.

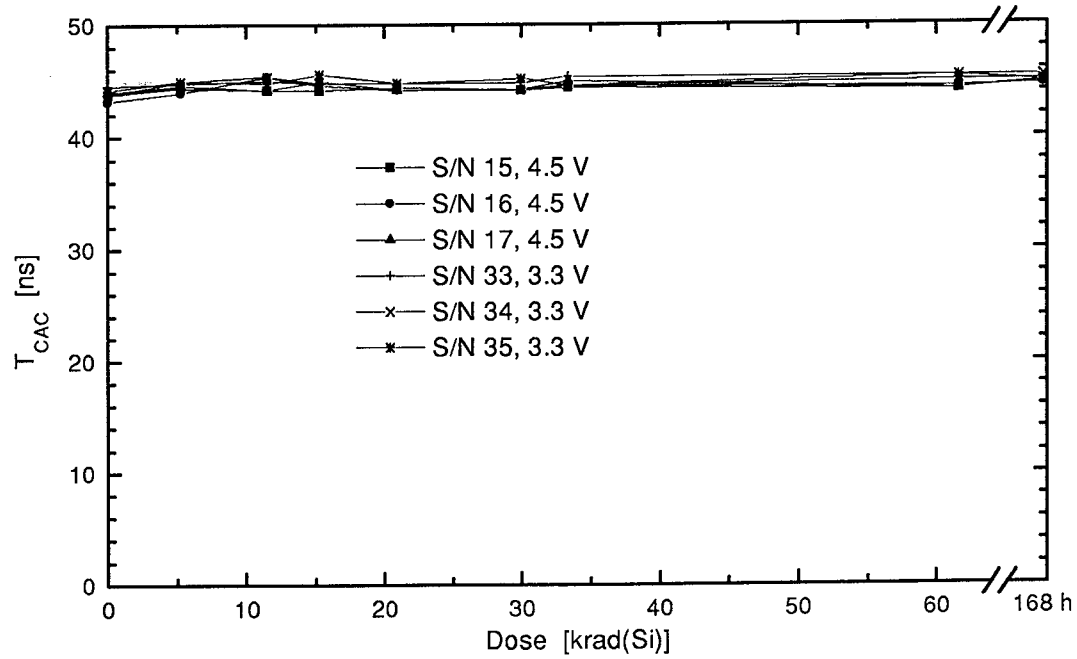

Fig. 10. CAS access time versus dose and after annealing for Micron DRAMs.