HEAVY ION SINGLE EVENT EFFECTS
RADIATION TEST REPORT

Part Type : NPSE-TC9 chip

1M-bit SRAM Cut 1 - 6T SRAM cell.

1M-bit SRAM Cut 2 - 6T2Cdram rSRAM cell.

Manufacturer : STMicroelectronics

STMicroelectronics Purchase order No PD 4000083535 dated 13/01/04

STMicroelectronics Technical Officer: Hervé DUPERRAY

STMicroelectronics
3 r Suisse
35200 Rennes

Hirex reference :	HRX/SEE/0103	Issue : 01	Date :	February 23, 2004
Prepared by :	Hirex		Date :	February 23, 2004
Checked by :	F.X Guerre		Date :	February 23, 2004
Approved by :	J. F. Mounes		Date :	February 23, 2004

Heavy ion SEE characterization of NPSE-TC9 chip Cut 1 & 2

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1 INTRODUCTION

This report presents the results of a Single Event Effects (SEE) test program carried out on two memory cuts, Cut 1 and Cut 2 of NPSE-TC9 chip, from STMicroelectronics.
This device was used for heavy ion test at the Brookhaven National Laboratory (BNL) facility, at Long Island, New York, USA – January 17/18, 2004.
This work was performed for STMicroelectronics under STMicroelectronics Purchase order No PD 4000083535 dated 13/01/04.

2 REFERENCE DOCUMENTS

RD1. RD-1. NPSETC9_1 testchip, Version 1.4, Central R&D Crolles, 26 August 2003
RD2. RD-2. 7/28/2003 – Netlist, NPSE testchip, NPSEin5PM03255_Rev3.txt
RD3. RD-3. SUBSTRATE PBGA 27X27-256+16 BALLS PAD 10.25X10.25MM, 7186129 Rev B, 16–DEC–2002
RD4. RD-4. RAPIDOV2, version 2.0, Testchip&Tools Team, 8 November 2001
RD5. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100
RD6. Brookhaven National Laboratory, SEU Test Facility, User Guide, revised January, 1997

3 DEVICE INFORMATION

3.1 NPSE-TC9 chip

1M-bit SRAM Cut 1 - 6T SRAM cell with deep buried layer (NISO).
1M-bit SRAM Cut 2 - 6T2Cdram rSRAM (LIL strap) cell with deep buried layer (NISO).

Each cut is organized as 1 Bank of 32768 words of 32 bits (mux 32) of 1024 rows and 1024 columns
Address size is 15bits

3.2 Sample preparation

The samples were delidded mechanically.

4 Test Definition

4.1 Test Set-up

Hirex test equipment is composed of a modular rack coupled with a generic memory test board :

This modular rack is derived from Hirex BILT modular instrumentation system and present 8 slots for modular instruments.
Dedicated to the test of memories, the generic test board is based on a 12 MIPs on-board processor which controls the test sequence and the communication with the rack.
The board include programmable logic circuits with a total capacity of 30000 cells and 960 macrocells. This logic circuitry can work at high speed (up to 100 MHz) while being compatible with thermal requirements imposed by vacuum environment.
Today, the board has a capacity of 80 pin-drivers , using transceivers able to interface memory devices with voltage supply requirements between 1 and 7 volts. The DUT can have two different power supplies.

4.2 Test Configuration

The two memory cuts have been tested in sequence.
The DUT was tested in static conditions, which consist in the following cycle, repeated continuously.

Test cycle period was set to 5s (iteration).

- Write the entire memory (cut1 then cut2)
- Expose the memory for a given time period
- Read the memory (cut1 then cut2).

Test pattern consists in a repetitive pattern shown in Table 1. An offset is applied in the pattern at each cycle which allows to check that every word has been effectively rewritten with new data.

The table here below provides, for each group of 4 bits, the 14 words repetitive pattern.

	It k	It k+1	It k+2	It k+3	It k+4	It k+5	It k+6	It k+7	It k+8	It k+9	It k+10	It k+11	It k+12	It k+13	It k+14
address n	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000
address n+1	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010
address n+2	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101
address n+3	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111
address n+4	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001
address n+5	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110
address n+6	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101
address n+7	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000
address n+8	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010
address n+9	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101
address n+10	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111
address n+11	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001
address n+12	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110
address n+13	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010
address n+14	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000

Table 1 – Test pattern

It is also possible to select a All0 or a All1 pattern.

Errors which can be detected and counted are the following :

- Any single error in the memory block with identification of the transition (up : 0->1 or down : 1->0)
- Any word with at least one bit flip with the identification of the word address

DUT power supply module is monitored and each time the current consumption exceeds a programmable threshold, a power reset cycle is done and latch-up error counter is incremented.
In addition the use of a fast latch-up detection with a high speed comparator avoid the counting of SEU errors which could be induced by the latch-up condition.

4.3 Device Test Conditions

VDD value was set to the nominal voltage (1V2) for all the runs as mentioned in Table 3.

5 BNL TEST FACILITY

Test at the Tandem Van de Graaff accelerator was performed at Brookhaven National Lab, Upton, New York (USA) under HIREX Engineering responsibility.

RD6 document provides a description of this facility.

5.1 Dosimetry

The current BNL Tandem dosimetry system and procedures were used.

5.2 Used ions

Ion	**Energy** MeV	**LET(Si)** Mev/(mg/cm²)	**Range (Si)** µm
C-12	98.7	1.445	183.6
F-19	140	3.38	120.4
Si-28	181	7.993	73.6
Cl-35	199	11.73	59.41
Ni-58	265	26.58	42.2
I-127	220	57.95	23.7
Au-197	333	81.44	27.53

Table 2 – BNL ions selection

5.3 Beam set-up

The use of a tilt angle allows for additional effective LET values.
For each run, the following information is given in the detailed results table provided in the next paragraph (paragraph 6):

- Run Number
- Device ID
- Ion type
- Energy
- Range
- LET
- Tilt angle
- Test Duration
- Fluence
- SEU
- Cross-section

6 RESULTS

Detailed results per run are presented in Table 3 and the corresponding SEU error cross-sections are plotted in Figure 1 for Cut1 (standard cell) and in Figure 2 for Cut2 (robust cell).

No SEL were detected up to a LET of 81 MeV/(mg/cm²) with a fluence of 1 E7 #/cm².

No Large error (LE), either row or column error, have been detected for both memory cuts.

Table 4 for Cut1, respectively Table 5 for Cut2 provide a more in-depth analysis of the recorded SEE errors:

- In these tables, data presented in the two columns, Bit errors and Word errors, show that most of the word errors are single bit errors.
- However using the physical descrambling information, it is found that a very significant number of MBUs (involving several words) occurred. This number of MBUs even become preponderant versus SEUs number when the LET value is increased.

Then, from these data, Event (MBUs and SEUs) error cross-section can be plotted versus LET and are shown in Figure 3 for Cut1 and in Figure 4 for Cut2.

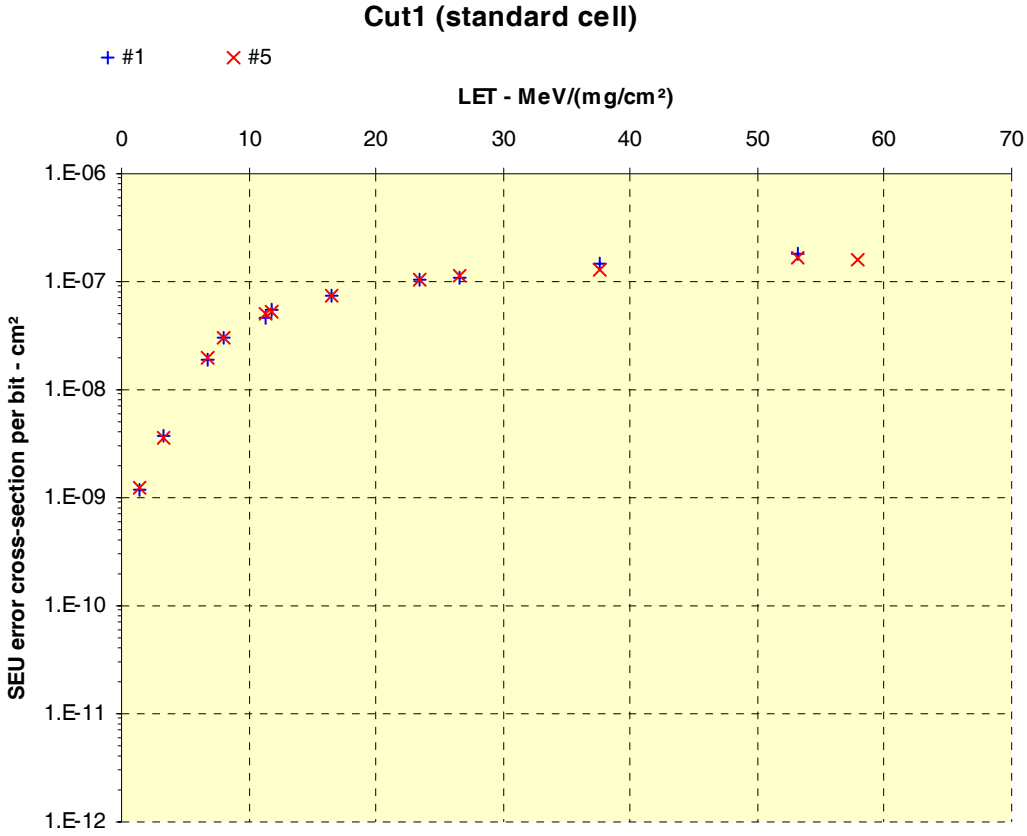

Figure 1 – Cut1, SEU error cross-section per bit vs. Effective LET

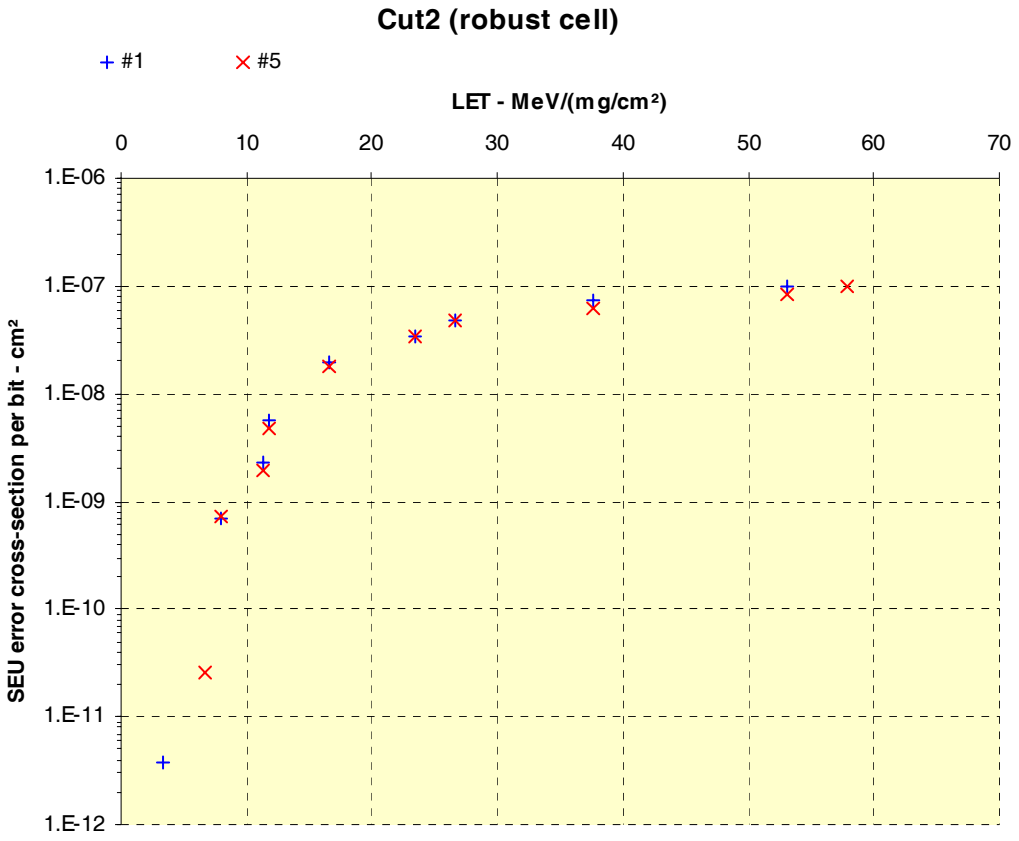

Figure 2 – Cut2, SEU error cross-section per bit vs. Effective LET

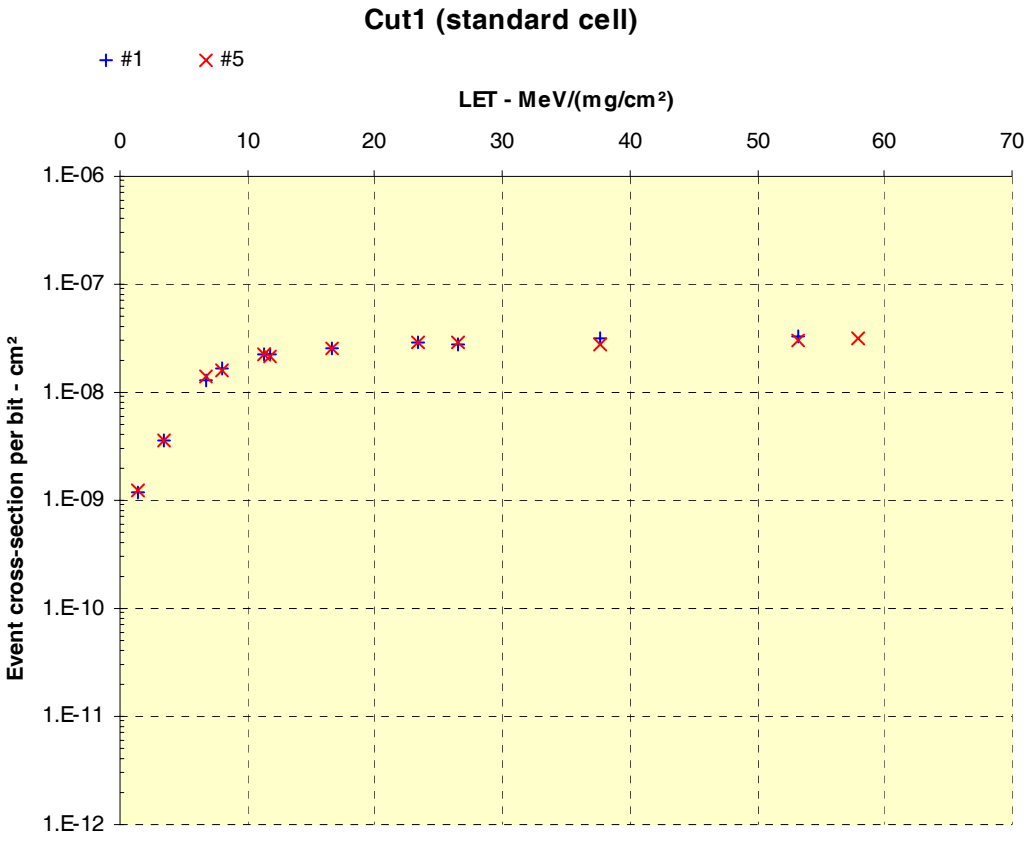

Figure 3 – Cut1, Events error cross-section per bit vs. Effective LET

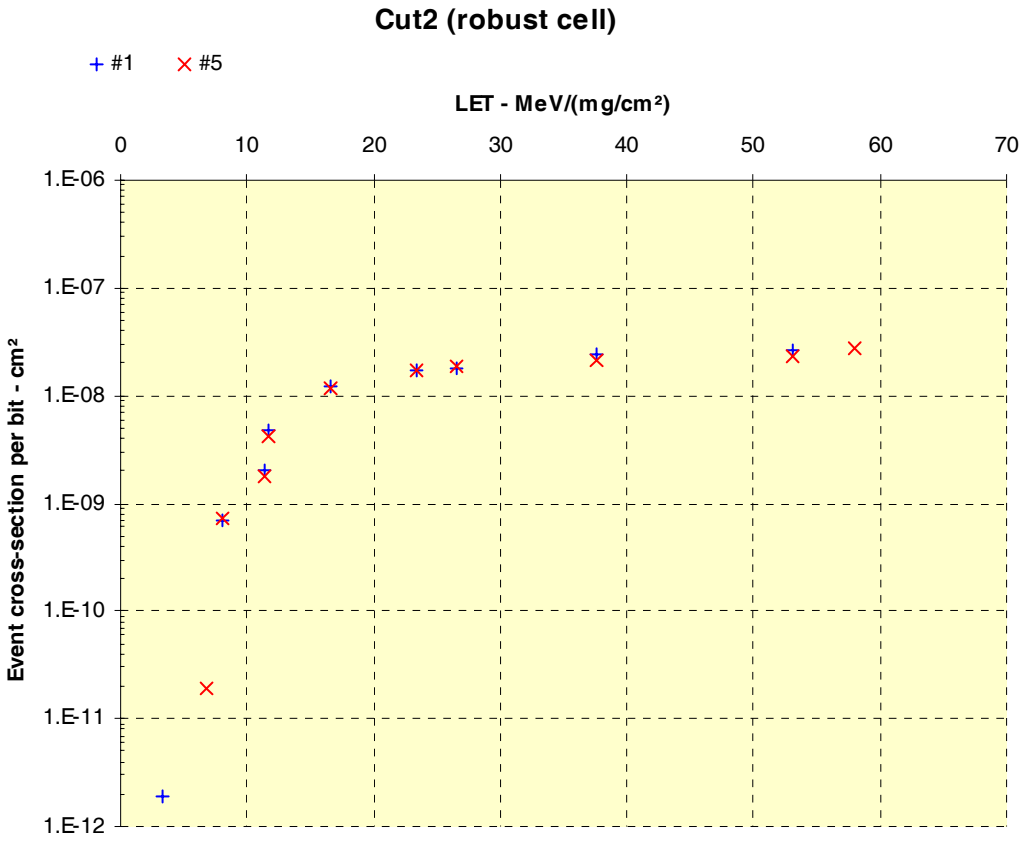

Figure 4 – Cut2, Events error cross-section per bit vs. Effective LET

NPSE1			BEAM						SEU (bit) errors		LE errors		SEL errors	SEU error cross-section per bit (cm²)	
Run #	S/N	DUT voltage (V)	Ion	LET MeV/(mg/cm²)	Tilt (deg.)	Eff LET MeV/(mg/cm²)	Beam time (s)	Fluence (# / cm².s)	Cut1	Cut2	Cut1	Cut2	DUT	Cut1	Cut2
17	5	1.2	Ni	26.58	60	53.16	61.80	2.18E+04	3795	1884	0	0	0	1.66E-07	8.26E-08
18	5	1.2	Ni	26.58	45	37.59	64.00	3.15E+04	4281	2083	0	0	0	1.30E-07	6.30E-08
19	5	1.2	Ni	26.58	0	26.58	52.50	3.68E+04	4332	1821	0	0	0	1.12E-07	4.72E-08
20	1	1.2	Ni	26.58	0	26.58	43.00	3.21E+04	3602	1582	0	0	0	1.07E-07	4.71E-08
21	1	1.2	Ni	26.58	45	37.59	46.00	2.20E+04	3362	1691	0	0	0	1.46E-07	7.32E-08
22	1	1.2	Ni	26.58	60	53.16	47.70	1.63E+04	3037	1711	0	0	0	1.78E-07	1.00E-07
23	1	1.2	F	3.38	60	6.76	258.50	3.32E+05	6486	0	0	0	0	1.86E-08	
24	1	1.2	F	3.38	0	3.38	222.80	5.01E+05	1941	2	0	0	0	3.69E-09	3.80E-12
25	5	1.2	F	3.38	0	3.38	127.80	2.70E+05	1038	0	0	0	0	3.67E-09	
26	5	1.2	F	3.38	60	6.76	135.60	1.50E+05	3184	4	0	0	0	2.02E-08	2.54E-11
27	5	1.2	Si	7.993	0	7.99	93.80	1.56E+05	4886	120	0	0	0	3.00E-08	7.36E-10
28	5	1.2	Si	7.993	45	11.30	76.10	9.18E+04	4792	184	0	0	0	4.98E-08	1.91E-09
29	1	1.2	Si	7.993	45	11.30	82.70	1.04E+05	5174	247	0	0	0	4.74E-08	2.26E-09
30	1	1.2	Si	7.993	0	7.99	100.60	1.76E+05	5561	127	0	0	0	3.01E-08	6.87E-10
31	1	1.2	Cl	11.73	0	11.73	52.00	9.10E+04	5202	535	0	0	0	5.45E-08	5.61E-09
32	1	1.2	Cl	11.73	45	16.59	37.90	4.73E+04	3639	955	0	0	0	7.33E-08	1.92E-08
33	1	1.2	Cl	11.73	60	23.46	37.40	3.26E+04	3530	1171	0	0	0	1.03E-07	3.43E-08
34	5	1.2	Cl	11.73	60	23.46	47.20	4.19E+04	4574	1468	0	0	0	1.04E-07	3.35E-08
35	5	1.2	Cl	11.73	45	16.59	49.70	6.43E+04	4988	1233	0	0	0	7.40E-08	1.83E-08
36	5	1.2	Cl	11.73	0	11.73	56.00	1.01E+05	5532	508	0	0	0	5.25E-08	4.82E-09
37	5	1.2	I	57.95	0	57.95	48.70	2.16E+04	3557	2277	0	0	0	1.57E-07	1.01E-07
39	1	1.2	C	1.445	0	1.45	148.20	9.93E+05	1227	0	0	0	0	1.18E-09	
40	5	1.2	C	1.445	0	1.45	166.50	1.00E+06	1285	0	0	0	0	1.22E-09	
41	5	1.2	Au	81.44	0	81.44	24.80	1.02E+07	-	-	-	-	0	-	-
42	1	1.2	Au	81.44	0	81.44	27.90	1.01E+07	-	-	-	-	0	-	-

Table 3 - Heavy ion detailed results per run

S/N #	Run #	Tilt angle Deg.	Effective LET MeV/(mg/cm²)	Fluence #/cm²	SEU (1 bit)	MBU2	MBU3	MBU4	MBU5	MBU6	MBU7	MBU8	MBU9	MBU10	MBU11	MBU12	MBU13	MBU14	Events No	Bit errors No	Word errors No	Event cross-section cm²
1	39	0	1.45	9.93E+05	1221	3													1224	1227	1227	1.18E-09
1	24	0	3.38	5.01E+05	1869	36													1905	1941	1940	3.62E-09
1	23	60	6.76	3.32E+05	2968	1321	206	62	2										4559	6486	6482	1.31E-08
1	30	0	7.99	1.76E+05	1479	988	404	186	20	6	2								3085	5561	5537	1.67E-08
1	29	45	11.30	1.04E+05	843	795	444	240	63	21		1							2407	5174	5146	2.21E-08
1	31	0	11.73	9.10E+04	575	632	473	296	107	29	5	2							2119	5202	5153	2.22E-08
1	32	45	16.59	4.73E+04	236	350	335	221	111	32	5	4							1294	3639	3619	2.61E-08
1	33	60	23.46	3.26E+04	99	188	212	215	150	80	37	4	3		1				989	3530	3510	2.90E-08
1	20	0	26.58	3.21E+04	75	133	180	205	164	108	38	14	5	1					923	3602	3593	2.75E-08
1	21	45	37.59	2.20E+04	48	64	105	140	135	120	75	34	11	2					734	3362	3328	3.18E-08
1	22	60	53.16	1.63E+04	29	33	57	86	74	80	79	60	34	18	4			1	555	3037	3023	3.26E-08
5	40	0	1.45	1.00E+06	1274	3			1										1278	1285	1284	1.22E-09
5	25	0	3.38	2.70E+05	1002	18													1020	1038	1036	3.61E-09
5	26	60	6.76	1.50E+05	1374	639	103	53	1	1									2171	3184	3182	1.38E-08
5	27	0	7.99	1.56E+05	1277	791	380	179	24	6	1	1							2659	4886	4862	1.63E-08
5	28	45	11.30	9.18E+04	720	708	432	217	68	19	4			1					2169	4792	4767	2.25E-08
5	36	0	11.73	1.01E+05	685	651	438	332	123	32	6	2	2	2					2273	5532	5493	2.16E-08
5	35	45	16.59	6.43E+04	330	447	438	304	152	60	6	9							1746	4988	4941	2.59E-08
5	34	60	23.46	4.19E+04	120	228	299	266	206	110	33	10	4						1276	4574	4529	2.91E-08
5	19	0	26.58	3.68E+04	91	159	221	252	203	123	36	23	7						1115	4332	4303	2.89E-08
5	18	45	37.59	3.15E+04	44	88	109	191	175	137	99	48	16	3	2				912	4281	4265	2.76E-08
5	17	60	53.16	2.18E+04	30	55	71	96	89	121	94	72	41	18	5	3	1		696	3795	3781	3.05E-08
5	37	0	57.95	2.16E+04	33	65	82	119	135	123	81	56	13	7	3	2			719	3557	3511	3.18E-08

MBUx = x bits in errors (Δ row $\leq$5 and Δ column $\leq$5) during a test cycle iteration (5s)

Table 4 – Cut1 (standard cell) , error distribution and Event cross-section per run

S/N #	Run #	Tilt angle Deg.	Effective LET MeV/(mg/cm²)	Fluence #/cm²	SEU	MBU2	MBU3	MBU4	MBU5	MBU6	MBU7	MBU8	MBU9	MBU10	MBU11	MBU12	MBU13	MBU14	Events No	Bit errors No	Word errors No	Event cross-section cm²
1	39	0	1.45	9.93E+05															0	0	0	
1	24	0	3.38	5.01E+05		1													1	2	2	1.90E-12
1	23	60	6.76	3.32E+05															0	0	0	
1	30	0	7.99	1.76E+05	127														127	127	127	6.87E-10
1	29	45	11.30	1.04E+05	199	24													223	247	247	2.04E-09
1	31	0	11.73	9.10E+04	396	65	3												464	535	534	4.86E-09
1	32	45	16.59	4.73E+04	373	163	49	26	1										612	955	954	1.23E-08
1	33	60	23.46	3.26E+04	225	192	95	55	9	2									578	1171	1168	1.69E-08
1	20	0	26.58	3.21E+04	162	163	131	99	30	18	2	3	1						609	1582	1580	1.81E-08
1	21	45	37.59	2.20E+04	98	134	125	102	51	31	11	3							555	1691	1688	2.40E-08
1	22	60	53.16	1.63E+04	49	78	77	94	80	40	22	8	3					1	452	1711	1710	2.65E-08
5	40	0	1.45	1.00E+06															0	0	0	
5	25	0	3.38	2.70E+05															0	0	0	
5	26	60	6.76	1.50E+05	2	1													3	4	4	1.90E-11
5	27	0	7.99	1.56E+05	120														120	120	120	7.36E-10
5	28	45	11.30	9.18E+04	166	9													175	184	184	1.82E-09
5	36	0	11.73	1.01E+05	390	57		1											448	508	508	4.25E-09
5	35	45	16.59	6.43E+04	473	214	65	33	1										786	1233	1229	1.17E-08
5	34	60	23.46	4.19E+04	320	238	125	57	9	4									753	1468	1465	1.72E-08
5	19	0	26.58	3.68E+04	209	194	147	92	52	16	5	3							718	1821	1807	1.86E-08
5	18	45	37.59	3.15E+04	126	176	182	130	64	26	9								713	2083	2075	2.16E-08
5	17	60	53.16	2.18E+04	69	87	101	133	66	44	15	10	3						528	1884	1879	2.32E-08
5	37	0	57.95	2.16E+04	55	108	138	134	110	52	16	8	2						623	2277	2261	2.76E-08

MBUx = x bits in errors (Δ row ≤5 and Δ column ≤5) during a test cycle iteration (5s)

Table 5 – Cut2 (robust cell) , error distribution and Event cross-section per run

7 CONCLUSION

Heavy ion tests were conducted on two samples of NPSE-TC9 chip from STMicroelectronics to evaluate the sensitivity to SEUs of both 1 M-bit standard cell SRAM (Cut1) and 1M-bit robust cell SRAM (Cut2), using the heavy ions available at the Tandem Accelerator facility at Brookhaven National Lab (BNL), Long Island, New York, USA.

SEU error cross-section versus LET could be plotted for both cuts over an LET range of 1.5 to 58 MeV/(mg/cm²) and the main outcomes are summarized in the table hereafter.

	LET Threshold (MeV/(mg/cm²°	Asymptotic cross-section per bit (cm²)
Standard cell (Cut1)	< 1.45	1.6 E-7
Robust cell (Cut2)	3.4	1 E-7

No row or column error could be detected for both memory cuts.
Analysis of the recorded SEE errors data show that most of the errors are single bit word errors.
However, MBUs errors (several single bit word errors induced by an ion strike) could occur and even these MBUs become preponderant versus SEUs when the LET value is increased.

Lastly, NPSE-TC9 chip was not found to be sensitive to SEL when tested to an LET of 81.5 MeV/(mg/cm²) and with a fluence of 1 E+7 ions/cm².