Micro Electro Mechanical Systems

LTCC-Packaged Single Pole Double Through (SPDT) Switch in MEMS technology for high reliability application

Presented by Francesco Vitulli – Alenia Spazio, Rome Italy

Contents:

Alenia interest in field of MEMS

- As a Company dedicated to space equipment for telecom, our main interest is toward those MEMS promising good RF performance, like Cavity Resonators, Varactors, RF Switches.
- RF Switches have been studied for several years; many Electrostatically actuated SPST (Single Pole Single Through) Switches have been realized in IC technology.
- RF Switches offer good performance in respect of: linearity, power consumption, mass.
- RF Switches are of interest if, in addition to electrical performance, they can achieve a high level of reliability and competitive cost.
- A SPDT (Single Pole Double Through) RF Switch is being developed by Alenia in the frame of contract NR. 14628/NL/CK with ESTEC.

Work organization for the development of a SPDT RF Switch

- Alenia Spazio S.p.A. (ALS): prime contractor, also in charge of package assembly
- Technische Universität München (TUM), Istitüt für Hochfrequenztechnik: switch and switch matrix design, wafer layers design
- Università di Perugia (UNI-PG), Department of Electronics: electromagnetic simulation and design support
- Istituto di Ricerca Scientifica e Tecnologica del Trentino (IRST), Microsystem Division: fabrication process development, foundry service, mechanical simulation
- Consiglio Nazionale delle Ricerche (CNR), Microwave and Microsystem Laboratory : electrical testing and design support

Technical requirement for the SPDT RF Switch

- Frequency range : 1 to 30 GHz
- Input RF power : 10 W minimum
- Insertion loss : 0.4 dB maximum
- Isolation : 50 dB minimum
- Return loss : 20 dB minimum
- Actuation voltage : 50 V maximum
- Temperature range : -25°C to 75°C
- Switching time, power consumption : to be minimized

Quality Requirements for the SPDT RF Switch

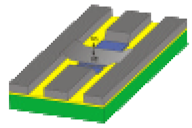
- Number of cycles : 10^6 minimum
- Lifetime by design : 10 years minimum
- Sine vibration : 20Hz -2000Hz at 20g, 3-axis, 4 minutes each axis
- Random Vibration :
  - 20-100Hz +3dB/octave
  - 100-200Hz 1 g^2/Hz
  - 200-2000Hz -4dB/octave
  - Duration : 2.5 minutes
- Mechanical Shock : n. 5, 1500 g, 0.5 ms, y1 axis
- Thermal Vacuum : 7 cycles, below 1.3x10^{-6}hPa (PSS-01-802)
- Radiation tolerance : up to 100 krads (target)

Design aspects:

- The SPDT design must take into account the present technology availability, in order to have a final product which can be manufactured without critical and costly processes. We have avoided to choose “state of the art” technology.
- While SPST Switches have been already demonstrated to be realized as single devices, SPDT Switches are much more difficult to be made as single devices.
- Our choice has been to obtain SPDT Switch as a combination of SPST Switches but still in a monolithic form.
- Therefore the first step was to design and characterize SPST cells, within the technology domain and the layout rules offered by the foundry IRST.

1) Parallel, classical SPST Switch:

- This Switch has a metallic membrane shaped like a bridge, which is placed above the central conductor and connects both ground electrodes. The membrane can be attracted to the central (underpass) conductor if a DC voltage is applied between the central conductor and the membrane itself (ground). The underpass conductor is covered by a thin passivation layer (capacitor dielectric) to avoid the sticking of the electrodes.

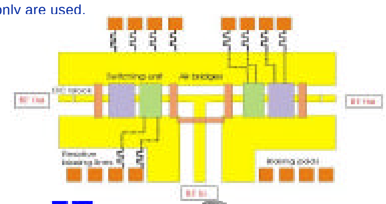


2) Series SPST Switch:

- The central conductor is interrupted, the gap will be closed by the metal bridge when the switch is actuated. The contact is ohmic with a low resistance value; this will insure a low insertion loss when the switch is actuated.
- To avoid sticking problems the center conductor is not used as an actuation pad. Separate (two) pads are added instead.
- The same approach of having separate pads from the center conductor is used for the parallel switch.
- Care has to be taken to achieve a good isolation of the RF signal path from the DC actuation pads and biasing lines. To this scope the biasing lines are made of polysilicon (230Ω/).

SPDT RF Switch:

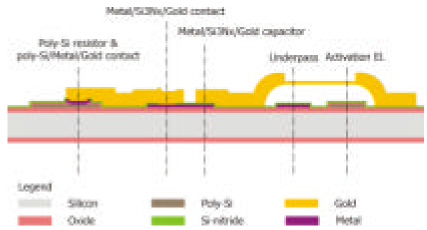
- None of the above described switches can meet the technical requirements, in particular RF isolation between input and output port in “off” condition, therefore a concatenation of series and shunt switches is needed for each branch. To reduce the insertion loss one series and one parallel switch only are used.



Fabrication process requirements

- Electrical specification:
  - Actuation voltage < 50V
  - Max input RF power >10W
- Structural requirements:
  - HF sections: Air Bridges, CPW lines
  - LF sections: 50kohm resistors, DC block capacitors, connection lines for actuation signals

Basic device structures of the RF-switch process



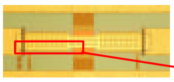
4th Round Table on M/NT – ESTEC Noordwijk 20/5/2003

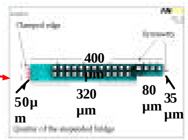
Mechanical Design

The pull-in voltage $V_p = \sqrt{\frac{8kg_0^3}{27e_0 A}}$

k = spring constant
g_0 = air-gap
ε_0 = permittivity of vacuum
A = area of the actuation pad

k calculated by FEM simulation program ANSYS.





Bridge Stress [MPa]	$Pressure_{pull-in}$ [MPa]	x_{max} [µm]	$V_{pull-in}$ [V]
53	$1.3*10^{-3}$	1.023	34.3
53+9	$1.5*10^{-3}$	1.016	36.8
53-9	$1.1*10^{-3}$	1.033	31.5

4th Round Table on M/NT – ESTEC Noordwijk 20/5/2003

Fabrication Process 1

1) 1000 nm isolation oxide growth, 300 nm polysilicon deposition, Boron implantation, poly definition, Boron diffusion 925 °C, 300 nm TEOS oxide and contact holes opening.

2) Ti/TiNAl/Ti/TiN 60/200/400/60/100 nm deposition and definition (underpass)

Silicon Oxide Poly-Si

4th Round Table on M/NT – ESTEC Noordwijk 20/5/2003

Fabrication Process 2

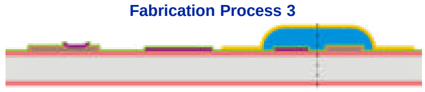
3) 100 nm LPCVD oxide (or PECVD nitride) and Via definition

4) 3 µm Resist Spacer deposition and definition

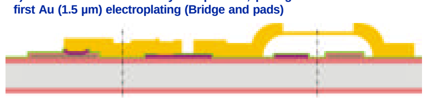
Silicon Oxide Poly-Si TiN

4th Round Table on M/NT – ESTEC Noordwijk 20/5/2003

Fabrication Process 3



5) Cr/Au 10/150 nm seed layer deposition, plating mould definition and first Au (1.5 µm) electroplating (Bridge and pads)



6) Second Au (3.5 µm) electroplating (CPW lines), seed layer removal, and final release

Silicon Oxide Poly-Si
TiN Si-nitride Resist Spacer

4th Round Table on M/NT – ESTEC Noordwijk 20/5/2003

Fabrication Process 4

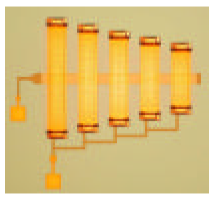
Process statistics
7 mask-layers
~ 130 process steps
20 product wafers (4") per run
9 weeks cycle time

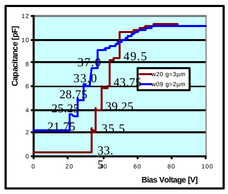
Advantages
No need for planarization steps
High isolation of the actuation electrodes
High C_{on} – C_{off} ratio, mostly break-down independent

Next improvements
Polysilicon and underpass multilayer of same height

4th Round Table on M/NT – ESTEC Noordwijk 20/5/2003

Actuation test results

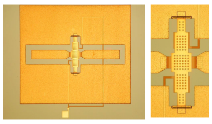




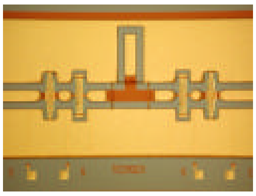
W=150 µm
L= 850, 750, 650, 550, 450 µm

g_0= 3 µm ΔC=2.1pF
g_0= 2 µm ΔC=1.4pF

Finished devices



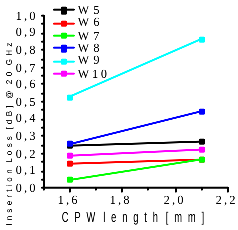
Classical shunt switch



SPDT prototype

CPW lines Insertion Loss

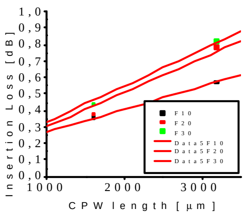
- Presently, an acceptable figure of merit for the CPW losses is 0.1 dB/mm at 30 GHz and ≤0.2 dB/mm at 40 GHz
- The measured insertion loss is in the order of 0.17 to 0.27 dB for a CPW having a length of 2.1 mm, i.e. 0.11 dB/mm
- In order to improve the insertion loss of the Shunt Switch a triple layer: TiN-Al-TiN has been used for the underpass of shunt switches



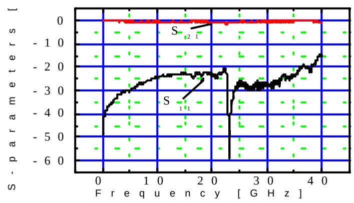
Insertion Loss due to biasing lines and actuation pads

- CPW lines with biasing lines and actuation pads have been manufactured to determine their contribution
- The effect on the I.L. is in the order of 0.1 dB @ 30 GHz, by using polysilicon actuation lines and pads

	I.L. @ 10 GHz [dB]	I.L. @ 20 GHz [dB]	I.L. @ 30 GHz [dB]
Line loss [dB/mm]	0.14	0.20	0.22



Shunt Switch Response (ON state)



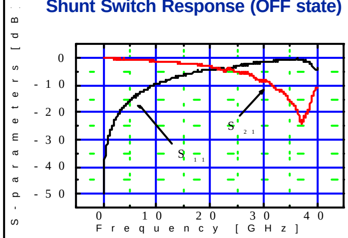
- The return loss is better than 20 dB up to more than 35 GHz. Losses are 0.28 @ 10 GHz, 0.43 @ 20 GHz and 0.58 @ 30 GHz. The line is included (1.5mm), so the switch alone is expected to contribute no more than 0.25dB @30 GHz

Shunt Switch Response (ON state)

Wafer #	Inserion Loss [dB]		
	10 GHz	20 GHz	30 GHz
1	-0.31	-0.58	-0.60
2	-1.25	-1.48	-1.30
6	-0.33	-0.58	-0.53
11	-0.28	-0.43	-0.58

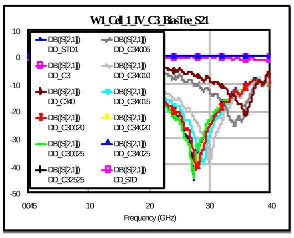
- Wafer #1, 6, 11 have been realized by using the multilayer for the underpass conductor: TiN/Al/TiN; while wafer #2 is TiN.
- The triple layer has been demonstrated suitable for this application

Shunt Switch Response (OFF state)



- The actuation voltage is about 50V. Note that a voltage between 10 to 20% higher is necessary after the first actuation to switch
- The peak in the isolation does not match with the simulation prediction (6Ghz vs 36.5Ghz measured!). This is likely caused by the bridge position which is not flat on the bottom electrode of the underpass, as the bottom electrode is not in the same plane as the actuation pads
- This explanation is confirmed by the test shown in the following chart.

Shunt Switch Response (OFF state)



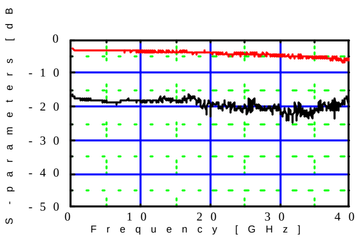
- In addition to the actuation voltage, an extra voltage has been applied between the central conductor of the CPW and the mobile bridge by using a bias tee
- The result is the increasing of the capacitance in Off state and, consequently, the reduction in frequency of the isolation peak, in the direction of the simulated behavior
- Comparison between the red curve (only 20V through the bias tee) and the yellow one (20V-bias teen plus 40V-actuation pads), shows that the voltage given by the bias tee in much more effective (the curves are practically superimposed)

Shunt Switch Response (OFF state)

Wafer #	d [µm]	εr	Fres [GHz]	I.L. [dB]	F'res [GHz]	I.L.' [dB]
1	100	3.94	11.2	-37	35.7	-26
2	100	3.94	10	-32.7	28.9	-30
6	30	3.94	6	-46	36.4	-25
11	200	7	14.5	-40	34.34	-27

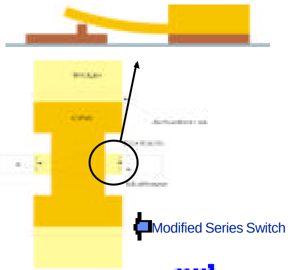
- Comparison between the insertion loss peak (IL) and frequency (Fres) of actuated by design switches with IL' and F'res of voltage actuated swithes over different wafers. d is the thickness of the dielectric.

Series Switch Response (ON state)



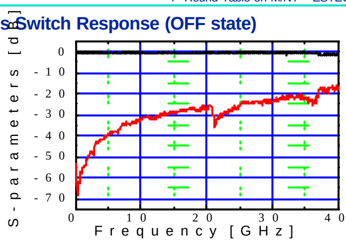
- The insertion loss is in the order of 3.5 to 4 dB. This is due to the poor ohmic contact of the bridge with underpass conductor.
- The formation of a chromium oxide layer in the bottom part of the bridge is likely the root cause.
- This layer must be broken when the bridge goes down to ensure a good electrical contact

Series Switch Response (ON state)



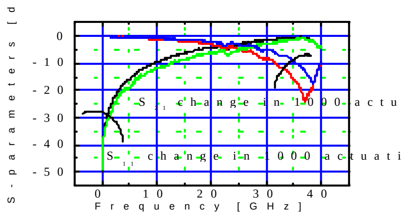
- Improvement of the electrical contact:
- The idea is to grow a array of dimples (by using the polysilicon layer) in the underpass area of contact with the mobile bridge
- The size of such dimples is to be minimized to get higher pressure
- An higher contact force is also preferable
- The beam must flex only in one plane to allow for a larger contact area

Series Switch Response (OFF state)



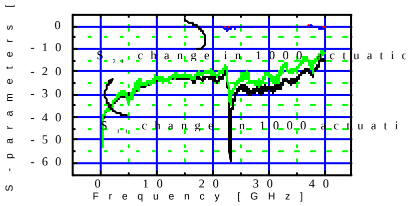
- The OFF behavior is satisfactory, better at low frequency as expected. An isolation of 20dB is obtained up to 35 GHz.

Shunt switch performance after 1000 ON/OFF cycles



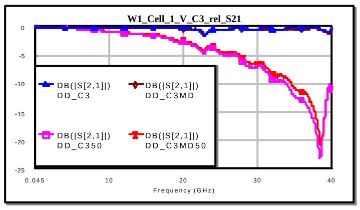
- OFF state performance (wafer 6)

Shunt switch performance after 1000 ON/OFF cycles



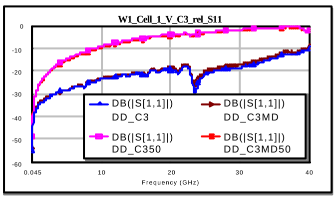
- ON state performance (wafer 6)

Shunt switch performance after 1500 ON/OFF cycles



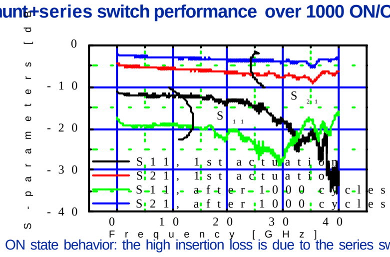
- ON/OFF state performance (wafer 1)

Shunt switch performance after 1500 ON/OFF cycles



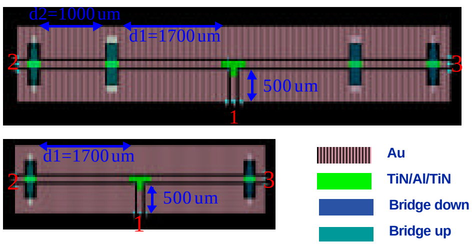
- ON/OFF state performance (wafer 1)

Shunt+series switch performance over 1000 ON/OFF cycles

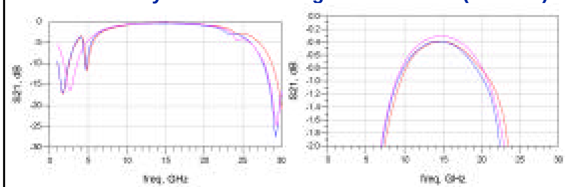


- ON state behavior: the high insertion loss is due to the series switch. Note the incremental reduction of the insertion loss over cycling, corresponding to the improvement of the mechanical contact between bridge and underpass

Next foundry run – SPDT design: shunt-shunt



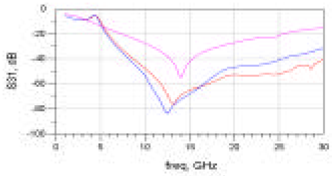
Next foundry run – SPDT design: shunt-shunt (On state)



- SPDT 1
- SPDT 2
- SPST

- Narrow band design: the transmission frequency depends on D1
- Simulation: ADS Momentum; the underpass triple layer has been simulated as a unique layer, the actuation pads an biasing lines are proved to be not influent and therefore not considered in the simulation.

Next foundry run – SPDT design: shunt-shunt (Off state)



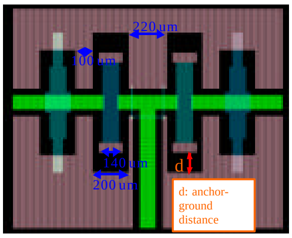
SPDT 1

SPDT 2

SPST

- The isolation behavior depends on the resonant frequency of the switch. The mobile bridge has been assumed flat on the bottom electrode (actuation pads having the same height as the bottom electrode). An additional layer of chromium oxide has been considered (5um) plus 10um of air to account for the roughness of the metals in contact.

Next foundry run – SPDT design: series-shunt



- The series and shunt switches are closer together, resulting in a large band behavior in comparison to the shunt-shunt switch
- The T-junction is made of underpass, so no blocking capacitors are necessary
- The contact resistance of the bridge with the underpass is the critical point.

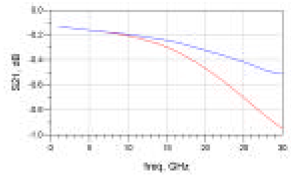
Au

TiN/Al/TiN

Bridge down

Bridge up

Next foundry run – SPDT design: shunt-series (On state)



D=50um

D=130um

- Simulation has been carried out by using Sonnet
- The On behavior still needs some optimization at high frequency

Next foundry run – SPDT design: shunt-series (Off state)

D=50um

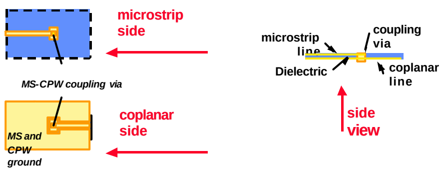
D=130um

- The Off behavior still requires further optimization at high frequency

LTCC 3D Micropackage

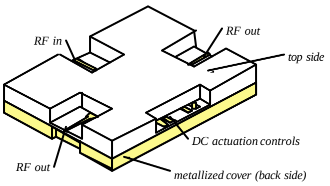
- The need for packaging comes from several reasons:
  - The SPDT Switch, as contains mobile parts, requires to be protected by particles and pollution to ensure good reliability
  - The CPW is better to be transformed to microstrip line to interface with other circuits
- Advantages of the LTCC technology:
  - Alenia Spazio have this technology in house
  - The LTCC package is inherently low cost
  - The CPW to MS transition is embedded in the package itself
  - The control circuitry can be embedded in the package as long as the control lines and pads

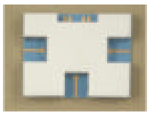
Microstrip to CPW transition



4[th] Round Table on M/NT – ESTEC Noordwijk 20/5/2003

Micropackage - Assembly

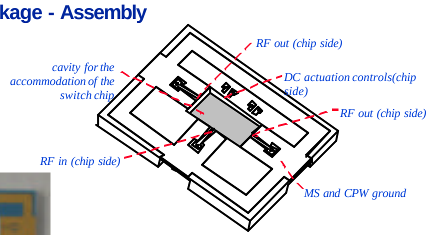


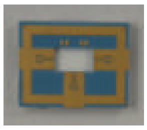


topside view

4[th] Round Table on M/NT – ESTEC Noordwijk 20/5/2003

Micropackage - Assembly

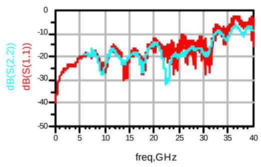


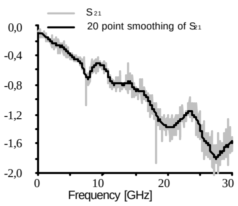


backside view

4[th] Round Table on M/NT – ESTEC Noordwijk 20/5/2003

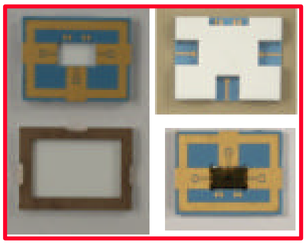
Micropackage – Electrical behaviour

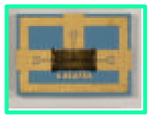




4[th] Round Table on M/NT – ESTEC Noordwijk 20/5/2003

Micropackage – Assembly components





4[th] Round Table on M/NT – ESTEC Noordwijk 20/5/2003

Conclusion:

- The achieved results on the insertion loss of the shunt switch gives good confidence the requirements can be encountered; the third design and foundry iteration, now underway, is needed to verify if the switch resonance (Off state) can be predicted, proving that the fabrication process and simulation match together
- The series switch is also expected to improve its insertion loss performance by using polysilicon dimples to help in obtaining a good electrical contact
- The LTCC micropackage shows satisfactory performance
- The SPDT Switch will be finally assembled in the package and subjected to a qualification program to assess the robustness of the design and developed technology