Quality assurance in complex microsystem development

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Abstract:

Quality assurance (QA) is absolutely necessary for the success of any complex microsystem development. However, there is no widely accepted manner in which to implement an efficient quality assurance programme in microsystems research. This paper aims at bridging this gap.

The development of complex microsystems differs in a number of ways from traditional space manufacture or related industrial sectors, e.g. the microelectronics industry. The foremost problem is the complexity of manufacture and integration, considering the yield and compatibility of processes. In order to use the full potential of miniaturization by microsystems technology, the systems need to be integrated at the microsystem level, eliminating packages and conventional interfaces.

This paper describes the implementation of QA programmes in the development of microsystems, with examples primary from a highly integrated micropropulsion system made from micromachined and bonded silicon wafers. The implementation ranges from process research, over device proof-of-concepts and integration issues, to the delivery of flight hardware. The discussion highlights the distinguishing character of a QA programme for complex microsystems, and details the use of test structures, documentation, process compatibility, reliability and space environment issues, and failure mode evaluation and analysis.

In particular, test structures are used to monitor process performance, to demonstrate microsystem functions, and to aid in failure analysis. All development work are carefully planned and formally documented, necessary for reliable manufacture.

The main conclusion is that the traditional development hierarchy of engineering models, qualification models, and flight models should be abandoned in favour of a pertinent QA implementation with continuous testing of microsystem features throughout the microsystem development. In this way, the development starts from a microsystem concept and ends in flight hardware, without incurring unnecessary development delays and costs while proving engineering and qualification systems that must be completely redesigned due to integration issues in the final microsystem version.

Introduction:

The remarkable constraints on autonomy, data-handling and data-transmission capability, power requirements, operational reliability, available space, and mass allowance involved in enabling space missions have always invited massive research and engineering efforts in order to succeed. However, in any engineering or research project of this magnitude, there is risk present: risk threatening the schedule, the technical performance, the project budget, the life and health of those involved, or the scientific, strategic, or commercial output of the mission [1].

Moreover, the space endeavor requires vast resources. Hence, the space community keeps a sharp lookout for possible ways of saving cost, improving performance, or increasing the return of space missions. In these efforts, miniaturization of spacecraft and their subsystems have long been recognized as a vital part. With the advent of microsystems technology, the extreme miniaturization schemes imagined identified this as a key technology in future space missions [2].

The launch cost, a major part of any mission, is directly dependent on the launched mass. Furthermore, the microsystems may also enable missions that would otherwise be impossible. For example, the precision configurations of satellites or deep-space platforms intended for future space research missions require the use of micropropulsion [3] which in turn calls for microsystem technology [4]. In general, any mission that need a multitude of spacecraft, cheap access to space, or a distributed risk will become feasible.

The disposable spacecraft concept has suggested robust nanosatellite swarm networks with distributed functions. High-risk nanoprobes for planetary exploration can also be allowed provided they do not infringe too much on the mass budget of the mother spacecraft. Furthermore, surveillance nanosatellites for military or other purposes may be rapidly launched on demand from fighter jets.

The microsystem approaches described above share the characteristics of being highly integrated, complex but versatile high-performance systems. Indeed, there are two separate possibilities to incorporate microsystems in space. First, you can use reliable, simple devices, developed for terrestrial applications. By proper design, you will end up with an affordable miniature spacecraft that will be in demand in the cheap-access-to-space business. On the other hand, you may deliver highly complex microsystems that increase spacecraft performance, dramatically reduces mass, or enables completely new missions. This road is the one pursued at the ÅSTC.

Extreme integration of microsystems

Six levels of packaging are recognised in the classical integrated circuit (IC) hierarchy, L0–L5 [e.g. 5]. These are IC features (L0), IC chip (L1), chip or multichip package (L2), chip package mounting board, e.g. printed wiring boards (L3), chassis, box, or harness (L4), and the entire system, e.g. a computer (L5). Each level routinely adds interconnects and packages requiring reliable mounting, extra mass, and extra space. Any integration of these levels brings miniaturisation, but in order to truly impact the total mass the integration of at least L0–L4 are required.

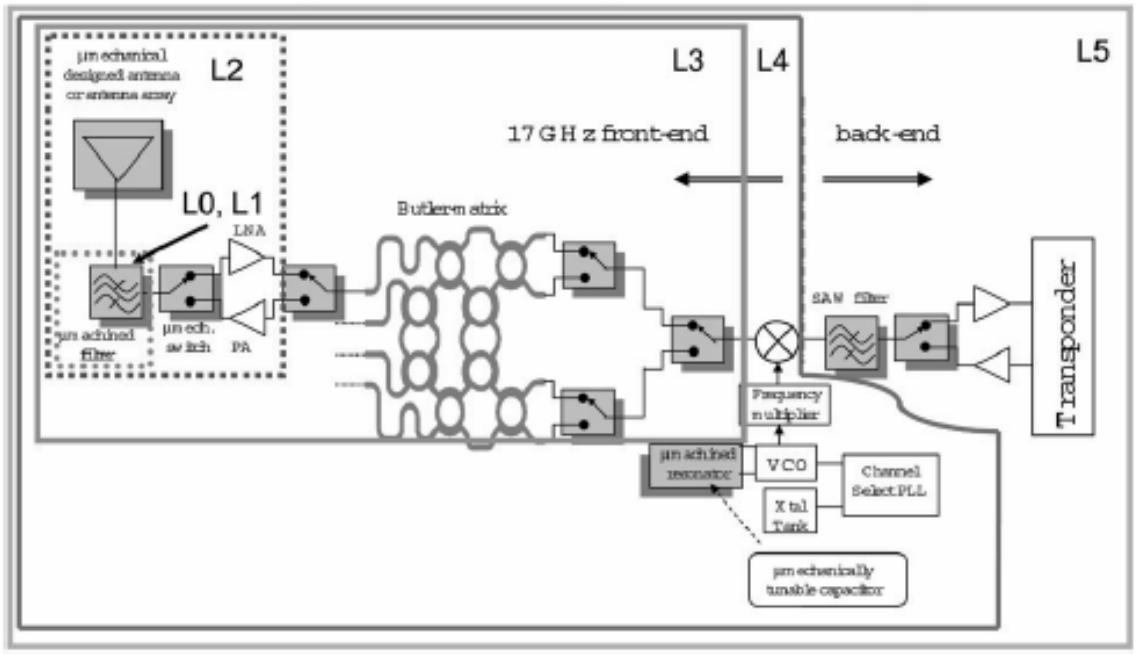

Figure 1: The illustration of integration levels in a typical system, here a 17 GHz rf telemetry link. L0 and L1 is the micromachined filters, L2 the chip integration of antenna, switches, and filters, L3 includes the beam-steering network (Butler matrix) and additional switches, L4 comprises the complete front-end, and L5 the entire telemetry link system.

In the ÅSTC approach the goal is to integrate all levels, possibly barring L5 (the spacecraft). The completed microsystem will be ready for direct mounting, or already be integrated in the spacecraft structure. The high level of integration efficiently reduces the mass and size of interconnections and eliminates intermediate packages.

One major challenge in the all-level integration is the tremendous demands on silicon microfabrication process compatibility and reproducibility. In order to meet this challenge, the ÅSTC has initiated a quality assurance program for space microsystems design and manufacture. This program document

micromachining processes, design for the space environment, address the space industry's concerns on microsystem use, and test the performance and robustness of the microsystems.

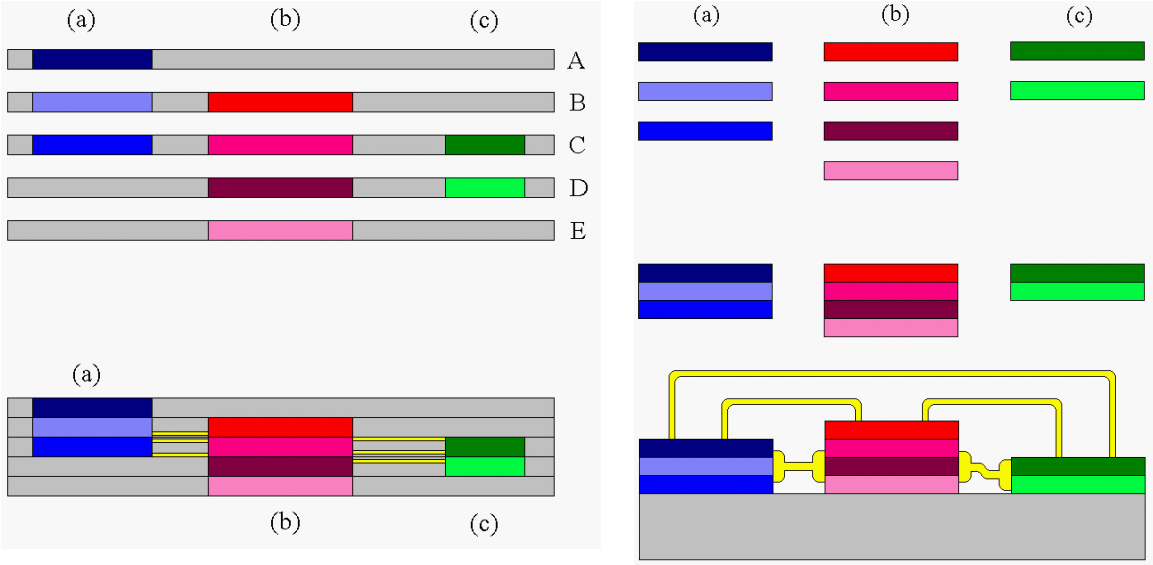

Figure 2: Integration of system functions in multiwafer structures.

For instance, using this high level of integration, the robustness of the system functions can be significantly increased. The number of interconnects and package-induced failures naturally decrease. Furthermore, the microsystems technology makes the systems spacious at the feature level, thereby enabling reliability management by introducing multiple redundancy.

Figure 2 illustrates the interface elimination idea, and some issues in this endeavour. The multiwafer integrated design of three system functions (colour-coded) that are processed in parallel in several wafers which, in turn, are subsequently bonded together. The separate functions are not testable before integration, and some cannot be reached by probing as integration is completed. On the other hand, a hybrid approach uses testable system components which are integrated and interconnected by more conventional technology. These interconnections and packages normally add magnitudes of mass an volume.

Microsystem manufacture process sequence

The successful delivery of a single working silicon microsystem forms the natural starting point for a general evaluation of the fabrication process. In order to benefit fully from the promises of massive integration, reliable manufacture of microsystems must be achieved. Here, the process time, fabrication yield, and microsystem cost must be considered. The resources necessary for development must be correctly assessed and valued. In this context, the detailed characteristics of the complete line of processing must be evaluated as a whole, in order to determine which alternate line uses the available resources most efficiently.

The process yield of the described fabrication sequence is a major issue for any microsystem manufacture. For IC manufacture, yield models are used with respect to substrate area, line width, routing density, feature size, typical defect size, process cleanliness, and number of process steps [6, 7]. These models are used mainly to estimate the economics of production, relying on large batches of identical devices [8].

In the current state of multifunctional silicon microsystem manufacture, on the other hand, the perspective is primarily technical – what is a feasible line of processing? The complex sequence of a multitude of advanced microfabrication techniques easily results in an overall low yield, suggesting a shaky reliability to the casual observer. However, the development of multifunctional microsystems is still in its infancy. The inherent yield losses are often associated with specific procedures, non-uniformity problems, or random

misfortunes. Such occurrences should be identified and evaluated in order to advise on efficient microsystem manufacture and process-risk mitigation.

Here, the efficiency of the manufacturing may be substantially influenced by the chosen design of the individual wafers in a multiwafer stack. By proper integration of structures on the wafer level, the number of necessary processes can be minimised. In this manner, the requirements on process compatibility can be relaxed. The wide variety of silicon microfabrication processes will still be available through the bonding of differently processed wafers. In other words, the peak performance of the fabrication process sequence will not be obtained by wafer-scale integration.

The production cost is also of prime interest when considering the microsystem manufacture. The feasibility of microsystem fabrication by a certain process should always be weighed against the cost of using that process. Naturally, the cheapest feasible processes are preferred. Furthermore, the total manufacture time will also be an item for optimisation, as a shorter manufacture turnover is desirable from a logistic point-of-view.

If an adequate total cost model is desired as a basis for pricing of the microsystems, the costs of documentation, goods, design, mask manufacture, and verification testing should also be included. Naturally, this can be done, but falls outside of the present discussion. When a precise price is requested, the manufacture would normally already be mastered. For research-intensive development projects this may not be true. The development of manufacturing processes will make the process choice, process duration, and process yield items of recurrent optimisation.

However, the three main issues – yield loss, process cost, and process duration – are not themselves de-coupled, independent quantities ready for optimisation. In mature IC production, management decides the priority of the separate optimisation of each item from a purely profit-based point of view [7]. Currently, the technology for fabrication of highly complicated silicon microsystems is still in a development phase, implying that yield is comparably low, large-scale production is rare and require hefty investments, and the market is small or slumbering. In other words, the production of multifunctional microsystems (for space) is rarely economic [9, 10]. Using yield modelling terms, the systematic yield can be suspected to be low, although perhaps easily amended if identified [6]. The microsystems technology has yet to gain acceptance and maturity in order to attract the sponsors necessary to overcome these issues. Until then, manufacturers have to work within these limits, perhaps eventually bringing about the desired change.

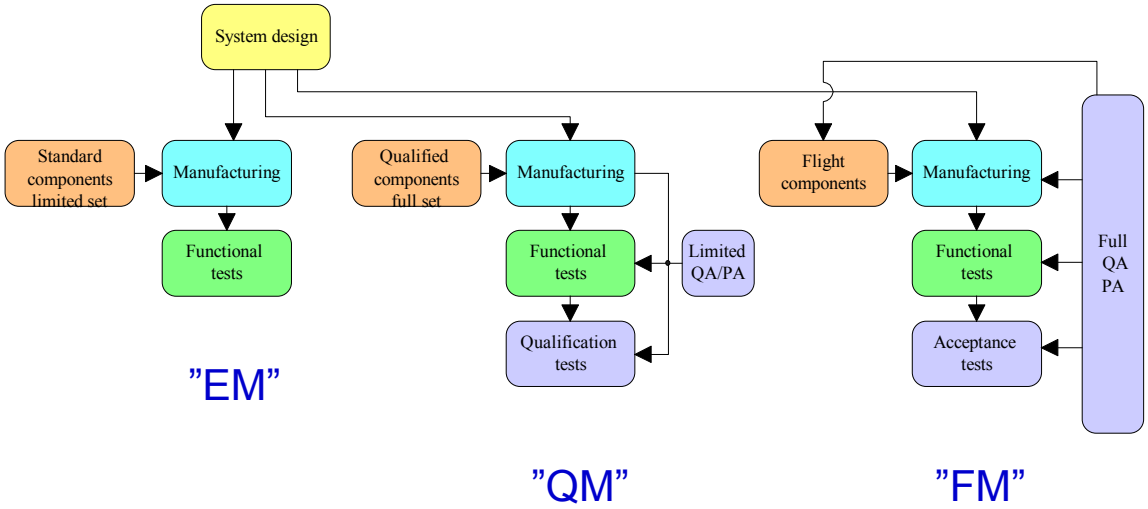

Figure 3: Standard development procedure. The development undergoes an increasingly more rigorous quality assurance programme during the sequential development of an engineering model, a qualification model, and finally the flight model.

System development procedure

The industrial commercialization of microsystems for space on mere device level has not been affordable. Space industry typically requires very small series of devices, far from any break-even point of device development [9]. The market for microsystem manufacture can rather be found in the microsystems that enable new mission concepts. These are complete, highly-integrated, and self-contained subsystems to the spacecraft. They can be successfully commercialized as they are mission-critical items, and priced accordingly.

In the traditional development approach, the progress follows a standard hierarchy through engineering model demonstration, qualification model delivery, and flight model manufacture (Figure 3). This roughly corresponds to proof-of-concept (bread-boarding), limited quality assurance implementation (space-qualified components), and full QA implementation (final design and flight components). In normal cases, this approach entails secure manufacture, albeit the administration and documentation can be overwhelming at times.

For highly integrated microsystems development, the traditional development approach becomes inefficient, time-consuming, and overpriced. This follows from the integration of all levels described above. Here, the integration of all system functions in a process sequence with reasonable yield is the main effort. This means that the design, component choice, and manufacture processes cannot be altered without starting the development completely from scratch all over again.

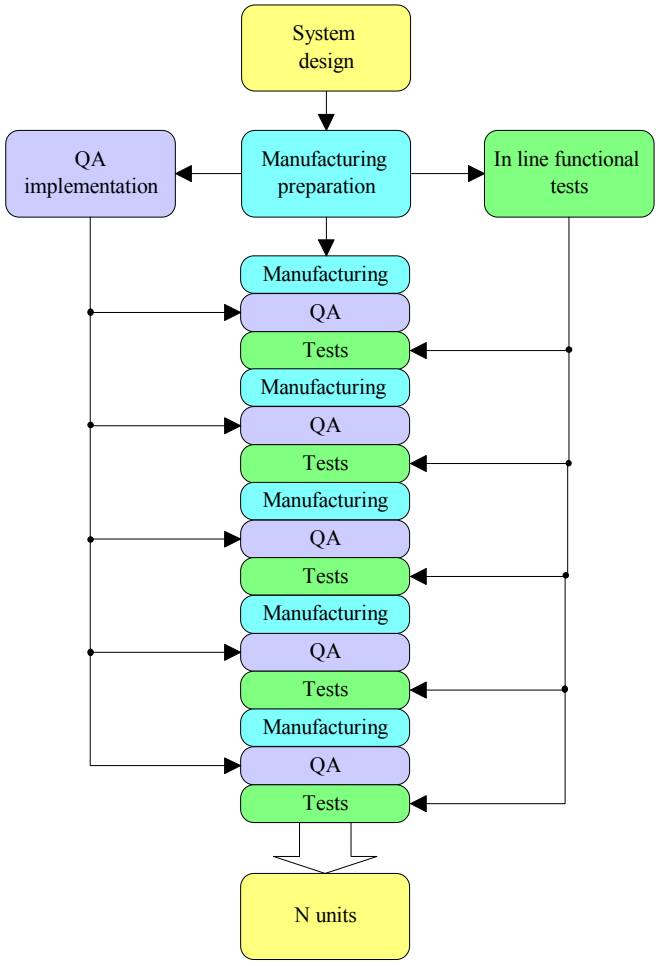

Figure 4: Suggested microsystem development procedure, enabling efficient development of highly integrated microsystems for flight demonstration and operation in orbit. The first unit is named EM and subjected to system level tests. Then, the EM is renamed the QM and put through qualification tests. The remaining N-1 units are put through the acceptance test and used as flight models.

Instead, an integrated microsystem development approach is suggested, where full QA is used and evaluated throughout the development, on the appropriate design, using a complete set of processes (Figure 4). Ideally, the first unit is named EM and subjected to system level tests. Then, the EM is renamed the QM and put through qualification tests. The remaining N-1 units are put through the acceptance test and used as flight models. This approach requires a detailed and professional planning and design prior to all manufacture and proof-of-concepts. However, the overall gain in speed (not doing the same thing repeatedly for any purpose) and testing cost (qualification and functional verification on system level instead of device level), defend these efforts.

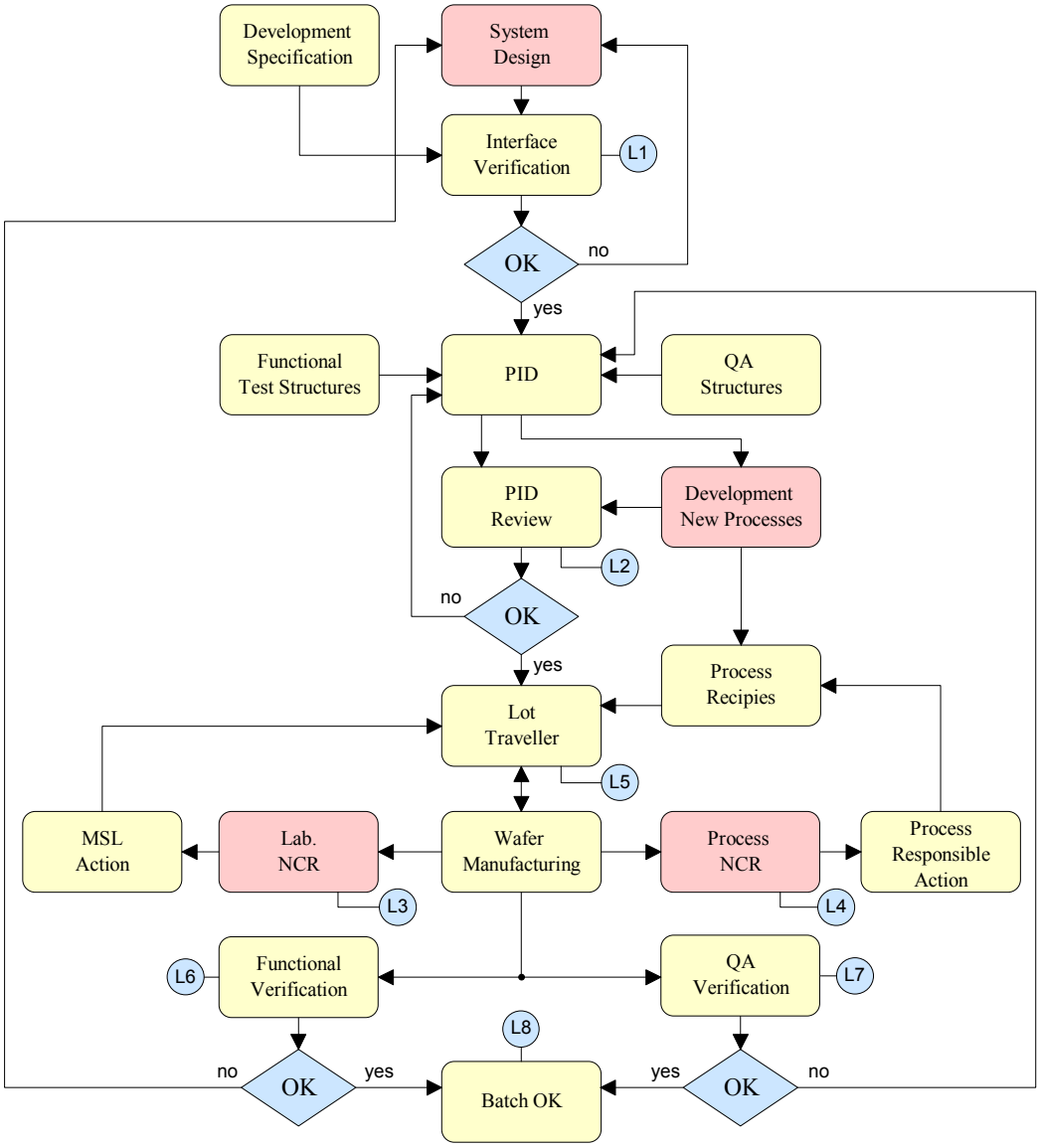

Figure 5: Methodology and documentation system for wafer level manufacture of highly integrated microsystems. This diagram illustrates the careful planning and meticulous documentation necessary in complex microsystems development. All L#-circles are logged documentation of various stages in the process. From the top, it runs from system design and verification of specifications, to the detailed process sequence design. This is compiled in the Process Identification Document (PID). This document translates into a full process description by compilation of reliable process recipes. Hereafter, the wafer manufacturing commences. Any problems in manufacture are reported in non-conformance reports (NCR), either to the laboratory responsible or the process responsible. The QA verification and functional verification finally approves the batch. Feedback to future processing is constantly extracted.

The detailed methodology adopted for highly integrated microsystem manufacture is outlined in figure 5. This diagram illustrates the careful planning and meticulous documentation necessary in complex microsystems development. All L#-circles are logged documentation of various stages in the process. From the top, it runs from system design and verification of specifications, to the detailed process sequence design. This is compiled in the Process Identification Document (PID). This document translates into a full process description by compilation of reliable process recipes. Hereafter, the wafer manufacturing commences. Any problems in manufacture are reported in non-conformance reports (NCR), either to the laboratory responsible or the process responsible. The QA verification and functional verification finally approves the batch. Feedback to future processing is constantly extracted, and implemented in the development of new processes, or simply logged to give the performance of the process sequence.

The quality assurance is implemented by the use of dedicated patterns and structures adjacent to the functional microsystem parts. These can either be evaluated in the line of processing, or stored for future reference, evaluation, or failure analysis.

A selection of quality assurance structures

This section gives four examples of quality assurance structures and results. The test samples described in this document fall into two distinct categories: the verification samples and the reference samples. The verification samples are used in the line of processing, often for immediate process verification. The results are logged in the Lot Travelers. The reference samples are stored for future reference in case of necessary failure analyses or other issues concerning the process performance.

Naturally, all structures cannot crowd every microsystem wafer. The selection of test structures for the wafers will be made according to relevance. Process yield issues commonly allows for plenty of room for the test structures in the wide perimeter of each wafer (typically a ring of inner diameter 45 mm and outer limit at diameter 90 mm on a 100 mm wafer.

Mask pattern precision verification

When structures need to be located with high precision on the wafer is it advisable to verify the mask pattern precision in advance. A set of alignment marks on the mask outside the four-inch wafer area can be used. The mask production time can be practically unaffected if the marks are located inside the corners of a four inch square. The mask is manually rotated 90° ccw in the mask generator and the test marks are exposed again onto the mask (Figure 6).

The lithographic mask precision verification structures are implemented in the standard pattern generator process, by using a new jobfile that add the relevant patterns to the mask being generated together with the current lithographic pattern being used for the subsequent lithography.

The verification is completed by an additional exposure in the mask generator, writing the second set of patterns after the manual 90° rotation of the mask.

Values are read from all eight scales, two in each corner of the mask. The orthogonality error is calculated from

$$\frac{1}{16}\left(\xi_1 - \eta_1 - \xi_2 + \eta_2 + \xi_3 - \eta_3 - \xi_4 + \eta_4\right) = \tan\Theta \tag{1}$$

using normalized coordinates. Typical global error is around 1 mrad

Figure 6: Mask pattern precision verification. Left: One mark of two possible readouts consists of a scale (above right) an indicator line (below left) and a verification circle. Right: After the manual rotation and double exposure, a new scale, a new indicator line, and a verification circle is developed across the first patterns. Eight different readouts of lateral deviation is then obtained (insert).

These marks comprise a scale for direct deviation readout, a perpendicular indicator line, and a pair of proof circles. The double exposure of the circles leaves a proof on the mask, to verify that the mismatch test was performed correctly. The indicator lines cross the scales for straightforward readout. This version of verification marks allows for a wide range of absolute deviations due to the manual rotation.

In the complex microsystem assembly, the structures of one wafer often need to be precisely aligned to the structures of another wafer, for example while bonding. The obtainable precision of such an alignment depend on the equipment used, the lateral extension of the structures, and the pattern errors (especially rotation errors) of the lithographic masks. If these errors are not eliminated at the mask manufacture, valuable work efforts will (and have been) wasted due to eventual structure mismatch.

Bond alignment assessment

Two bond alignment assessment methods can be used, one using cross-sectional inspection, and one requiring IR inspection, suitable for immediate investigation. Both make use of vernier patterned grooves, at widely spaced locations that give the lateral mismatch at that location.

Cross-sectional inspection: These alignment assessment structures simply comprise four symmetrically placed radial trenches in the periphery of each bonded wafer. Perfect bond alignment would thus entail perfect matching of the alignment assessment structures of one wafer to the trenches of the other. By inspecting cross-sections of these trenches after bonding, the bonding misalignment and rotation can be readily derived. The use of vernier-patterned grooves improves the accuracy of the readout. An ordinary single cross-sectional inspection would have an accuracy of ±3 µm at the best due to chipping at the edges of the groove, perhaps worse as the mismatch approach zero. The vernier-patterned grooves have their to accuracy improved to ±1 µm at a single cross-section observation. Inspection in IR gives an accuracy of ±2 µm, and is non-destructive. The total bond misalignment can be calculated in the same way as mask pattern precision above.

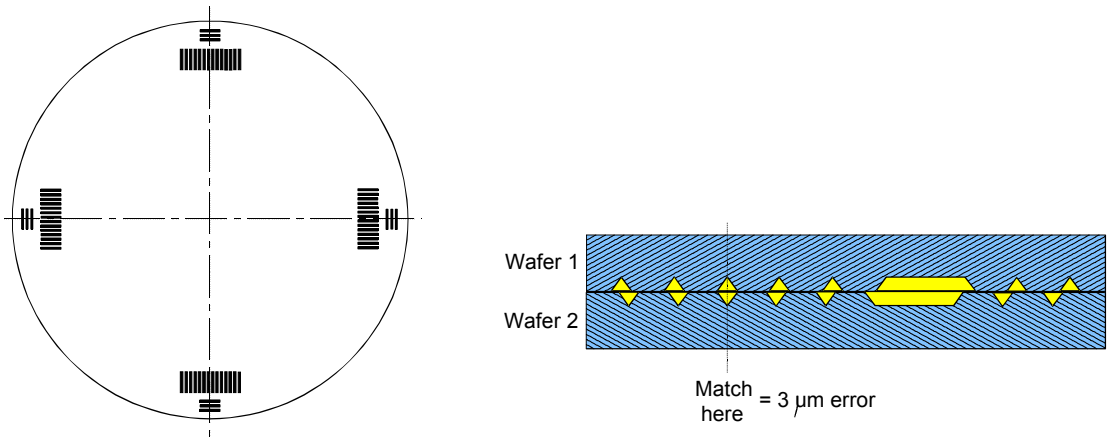

Figure 7: Bond alignment assessment. These structures should be placed as far as possible from each other in order to improve the accuracy of the rotational misalignment readout. The vernier pattern grooves give the mismatch with an accuracy of 1 µm in cross-sectional inspection and 2 µm in IR inspection.

Fluidic reference

A reference structure for fluidic performance verification can easily be implemented in any wafer stack already containing channels. This reference channel should be of specified length and cross-sectional dimensions in order to yield always comparable results for easy deviation detection, and would be used to verify that the process of making the fluidic conveyors has not introduced any unpredicted flow restrictions, due to e. g. surface roughness or other boundary effects such as turbulence or stagnant fluid layers (Figure 8).

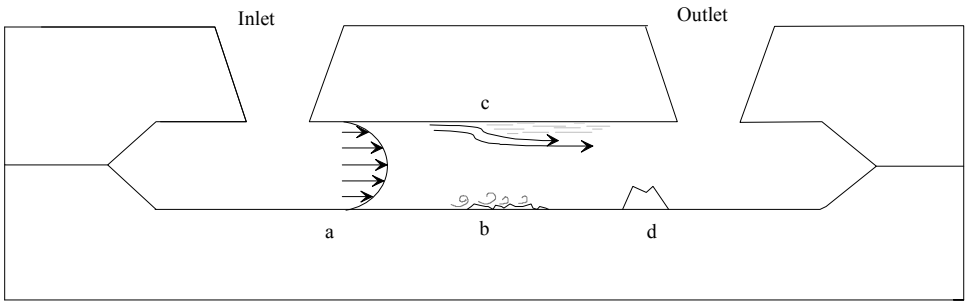

Figure 8: Fluidic device reference principle. a) Fully developed flow velocity profile, ideal case, b)Turbulence due to microroughness, c)Stagnant boundary layer formation, d) Etch defect flow obstruction.

The fluidic device reference can be implemented in any wafer stack containing gas conveyors of any kind, provided that these possess inlets and outlets through the top or bottom surfaces of the stack.

Bond quality and reliability

The harsh environment in space and while going to space put substantial requirements on the endurance of space systems. In silicon microsystems the weak links of the bonded wafers interfaces are a prime concern. Here, the greatest stresses are induced at the potentially the most defect-populated areas.

Spaceflight requires these microsystems to remain reliable during launch and in space. This includes trials like extensive vibration, thermal variations (abrupt and long-term), charged-particle impingements (e.g. solar protons, trapped electrons of the van Allen belts, and cosmic ray heavy nuclei), prevalent γ-irradiation, and micrometeoroid impacts [11, 12].

In e.g. a cold gas micropropulsion system [13], the major loads on the bonded microsystems are induced by internal gas pressure. A burst test would thus suit the quality assessment of the bonds in this application. Here, the burst pressures of test samples containing a specified cavity at the bond between two wafers are recorded, both for a reference series and for series subjected to spaceflight environment ground tests. These data series are then compared using statistical rank sum diagnostics in order to assess the significance of the fracture behaviour variation

A clear example of the effects of spaceflight environment on the bond quality is the test performed for γ-irradiation [14]. Here, the bond strength first degrades at dose 6 krad, then actually increases at 22 krad, and has finally degraded again at 100 krad (Figure 9). All these changes were found to be significant.

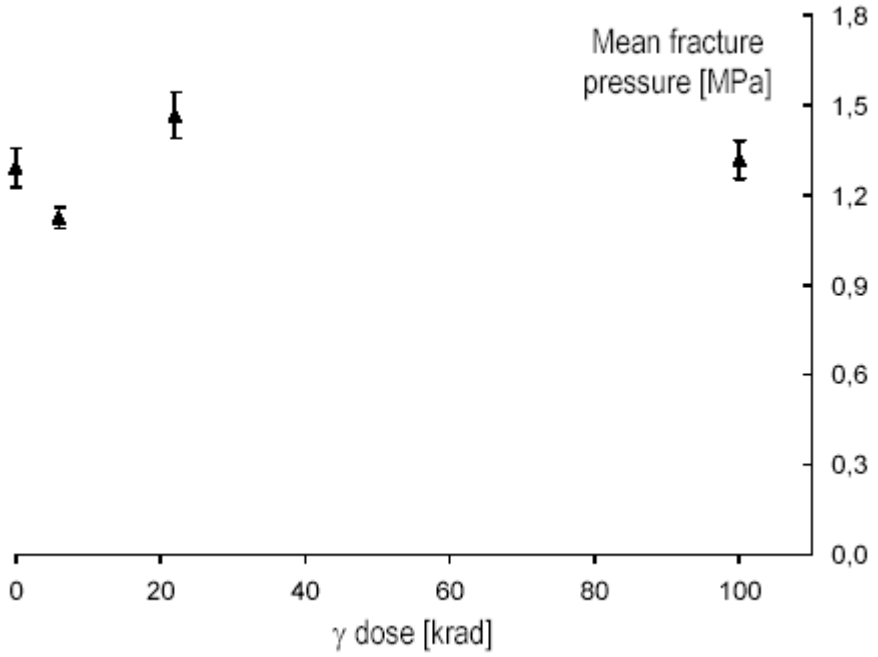

Figure 9: Bond quality variation in gamma ray exposure. The changing bond strength due to γ-irradiation of silicon-silicon samples annealed at 700°C. The 95%-confidence intervals are given. All changes due to increasing dose have been diagnosed significant.

Conclusion

The main conclusion is that the traditional development hierarchy of engineering models, qualification models, and flight models should be abandoned in favour of a pertinent QA implementation with continuous testing of microsystem features throughout the microsystem development. In this way, the development starts from a microsystem concept and ends in flight hardware, without incurring unnecessary development delays and costs while proving engineering and qualification systems that must be completely redesigned due to integration issues in the final microsystem version.

Acknowledgement

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