Low losses Microsystems Technology for mm and sub-mm wave applications

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Outline

Motivation

Losses in coplanar circuits

Membrane supported circuits

Demonstrators (millimetric and sub-millimetric)

Chalmers University

MEMSCAP

MOTIVATION

Telecommunication 20-30 GHz ; 40-50 GHz ; 60 GHz		Astronomical remote sensing 300 GHz - 3THz
***	low cost (low volume to mass production)	*
***	low size and weight	***
***	high integration	***
***	low losses	***
**	low noise	***
***	low consumption	**
***	high linearity	**

BREAK WITH CONVENTIONNAL HIGH FREQUENCY ELECTRICAL SYSTEM

Microtechnologies : well-known in sensors applications (1970)
for mm and sub-mm wave : Michigan Univ. (1991)

MOTIVATION

SILICON TECHNOLOGY WILL FIT PERFECTLY

Si for passive components — **Micro-machining opportunities**

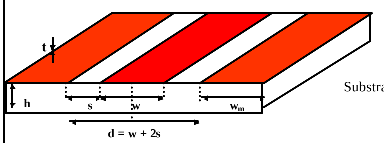
Si-Ge for active components — **Well established (up to 100 GHz)**

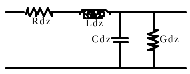
Bulk micro-machining → Low loss circuits

MEMSWAVES

Surface micro-machining → New behaviors : MEMS

LOSSES IN COPLANAR CIRCUIT





Substrate : C, G - Conductors : R, L

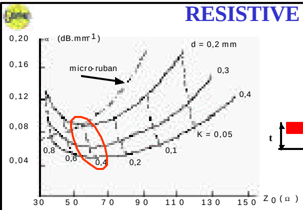
Low losses (R<<Lω ; G<<Cω)

$$\alpha = \alpha_c + \alpha_d \approx 1/2\left(\frac{R}{Z_o} + \frac{G}{Z_o}\right) \qquad Z_o \approx \sqrt{\frac{L}{C}} \approx 120\pi\,\varepsilon_o \frac{\sqrt{\varepsilon_{eff}}}{C} \approx 120\pi\,\varepsilon_o \frac{1}{C_a\sqrt{\varepsilon_{eff}}}$$

$$\varepsilon_{eff} \approx \frac{\varepsilon_r + 1}{2}$$

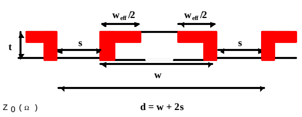
Quasi static approximation

RESISTIVE LOSSES



$$\alpha_c \approx \frac{R}{2Z_o} \approx \frac{\rho_c}{2\delta\, W_{eff}\ Z_o}$$

δ : skin depth



α_{cmin} : $\frac{w}{d}$ ≈ 0.4 → Zo ≈ 60 Ω

Si ($\varepsilon_r \approx 11.6$; $\varepsilon_{reff} \approx 6.3$) : Zo ≈ 60 Ω
Air ($\varepsilon_{reff} \approx 1$) : Zo ≈ 150 Ω ($Zo \approx \sqrt{\varepsilon_{eff}}$)

R.W. Jackson ; Coplanar waveguide vs. microstrip for millimeter wave integrated circuit. IEEE MTT-S Digest ; p. 699-702, 1986. pp. 16, 24
GaAs : ε_r = 12,8 ; f = 60 GHz ; h = 0,1 mm ; t = 3 µm ; tg∆ = 6.10^-4

Thickness effect : $\alpha_{c\ min}$: t ≈ 3 δ

☞ t >> 3 δ : W_{eff} æ
(concentration of EM field between conductors)

$$\delta = \sqrt{\frac{\rho_c}{\pi\,\mu_o\, f}}$$

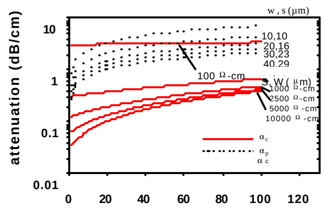
Gold
δ ≈ 0.55 µm @ 20 GHz (t > 1.65 µm)
δ ≈ 0.45 µm @ 30 GHz (t > 1.35 µm)
δ ≈ 0.32 µm @ 60 GHz (t > 1 µm)

DIELECTRIC LOSSES

$$\alpha_d = \left(\frac{\varepsilon_{eff}(f) - 1}{\sqrt{\varepsilon_{eff}(f)}}\right)\left[A\,.\,tg\,\delta\,.\,f + \frac{B}{\rho}\right]$$

Polarization (α_p) + Ohmic losses (α_c)

A, B : ctes (geometrical parameters)



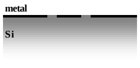
ρ > 2500 - 5000 Ω.cm

➔ $\alpha_p >> \alpha_c$

G.E. Pontchak, RF Transmission lines and passive circuits elements on silicon substrate 29th European Microwave Conference, Munich 1999, pp 158,161

MINIMIZATION OF DIELECTRIC LOSSES

Si HRS

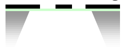


• Not compatible with active devices

Thickorganic between passive circuits and Si

• Higher losses

Bulk Si Micromachining



• Not always possible

Surface micromachining

Sacrificial layer

Overlay CPW line

• Lower design flexibility

Si etching

Wet

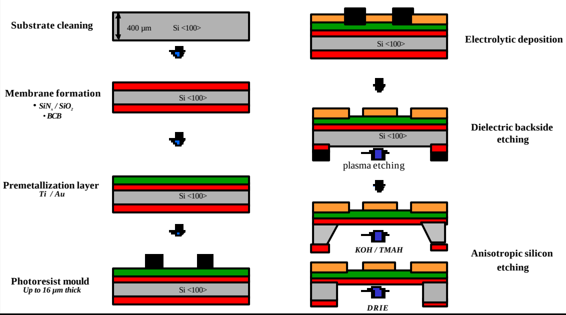
Dry

LOSSES IN COPLANAR CIRCUIT

Topology	Dielectric	Losses @ 30 GHz dB/cm
HRS	SiO2(1150°C)/SiNx (0.8/0.6µm)	5.1 (H_2SO_4/H_2O_2) 1.1 (RCA)
LRS	BCB (10µm) BCB (20µm) BCB (30µm)	6.5 (RCA) 4.6 (RCA) 3.3 (RCA)
LRS	BCB (10µm) + Si etched 10µm	4.2 (RCA) (≅ BCB 20 µm)
membrane	SiO2(1150°C) / SiNx (0.8 / 0.6µm) BCB (10-30 µm)	0.56 (resistive losses)

Metal : Ti/Au (1000A / 2.5µm)

TECHNOLOGICAL PROCESS FLOW for MEMBRANE SUPPORTED CIRCUITS



MINERAL DIELECTRIC MEMBRANE

Thermal oxide : $Si + O_2 \dashrightarrow SiO_2$: compressive stress (thermal stress)

☞ σ = -300 MPa (T = 1150°C) ; thickness = 0.8 µm

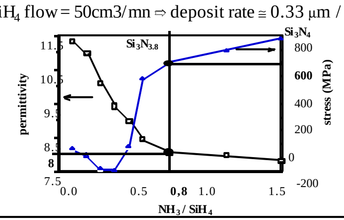
☞ dielectric constant ≅ 4

LPCVD nitride : $3SiH_4 + 4NH_3 \dashrightarrow Si_3N_4 + 12H_2$

T = 750°C; P = 300 mtorr; SiH_4 flow = 50cm3/mn ⇨ deposit rate ≅ 0.33 µm / h
thickness = 0.6 µm

Composite membrane

* thickness = 1.4 µm
* stress = 100 MPa



MINERAL MEMBRANE UNIFORMITY

$\lambda \sim (\varepsilon_{eff})^{1/2}$ ☞ ε_{eff} ~ dielectric membrane (ε_r , t)

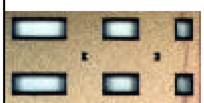
	Permittivity ε_r	Uniformity ε_r (run)	Thickness t	Uniformity t (wafer)	Uniformity t (run)
SiO_2	4	< ± 0.5 % 25 wafers	0.8 µm	< ± 1.5 %	< ± 5 % 25 wafers
$Si_{3.2}N_4$ (SiH_4)	8.1	< ± 0.9 % 25 wafers	0.6 µm	< ± 3 %	< ± 10 % 6 wafers
$Si_{3.4}N_4$ (SiH_2Cl_2)	8.3	< ± 0.6 % 25 wafers	0.6 µm	< ± 1.5 %	< ± 5 % 25 wafers

SiH_2Cl_2 : T = 800-830°C; P = 500 mtorr; $NH_3 / SiH_2Cl_2 = 0.24$

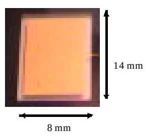
☞ Stress ≅ 520 MPa ± 7 %

☞ Deposition rate ≅ 0.4 µm / h

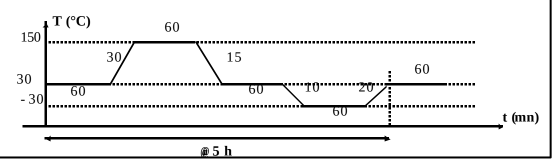
MINERAL MEMBRANE STRENGTH

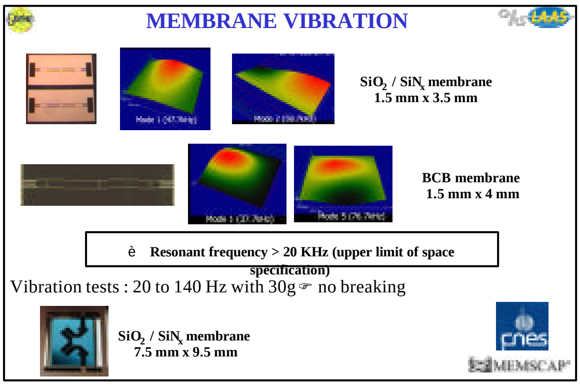


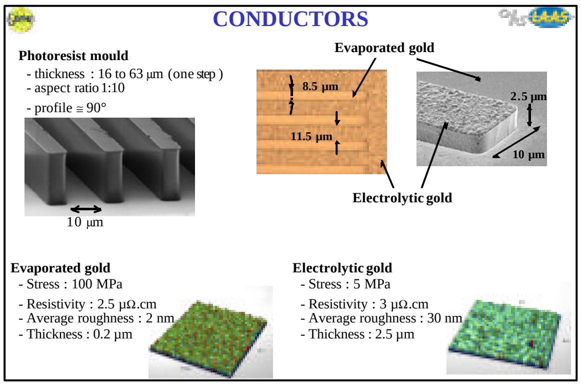
Area (mm²)	4 x 5	5 x 10
Breaking pressure (bars)	0.67	0.53

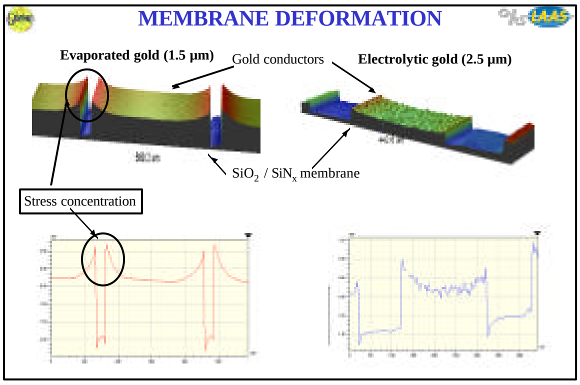


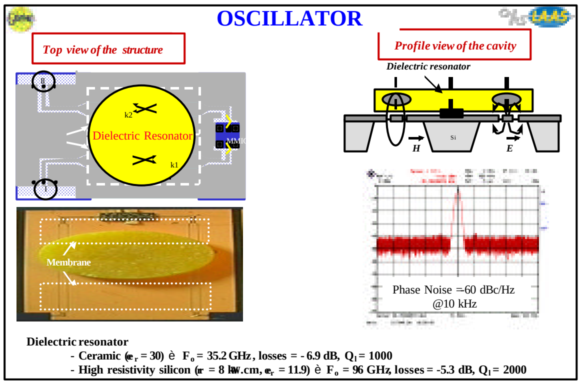
è Temperature cycles (2mm x 10 mm) : 250 ☞ no breaking

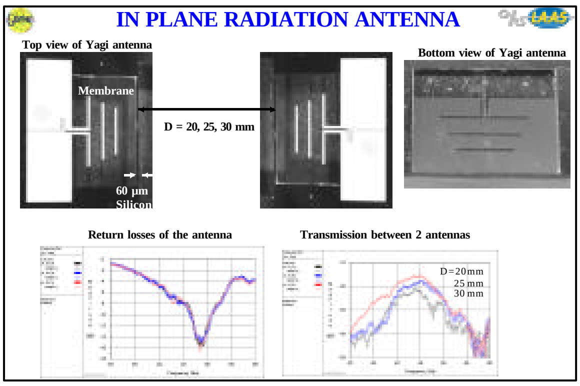


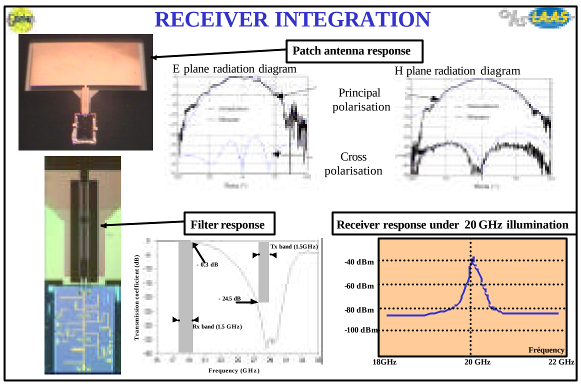

MEMBRANE VIBRATION
SiO_2 / SiN_x membrane
1.5 mm x 3.5 mm
BCB membrane
1.5 mm x 4 mm
è Resonant frequency > 20 KHz (upper limit of space specification)
Vibration tests : 20 to 140 Hz with 30g ☞ no breaking
SiO_2 / SiN_x membrane
7.5 mm x 9.5 mm
cnes
MEMSCAP

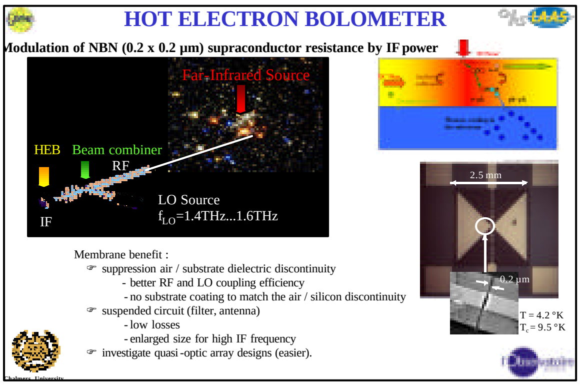

CONDUCTORS
Photoresist mould
- thickness : 16 to 63 µm (one step)
- aspect ratio 1:10
- profile ≅ 90°
10 µm
Evaporated gold
8.5 µm
11.5 µm
2.5 µm
10 µm
Electrolytic gold
Evaporated gold
- Stress : 100 MPa
- Resistivity : 2.5 µΩ.cm
- Average roughness : 2 nm
- Thickness : 0.2 µm
Electrolytic gold
- Stress : 5 MPa
- Resistivity : 3 µΩ.cm
- Average roughness : 30 nm
- Thickness : 2.5 µm

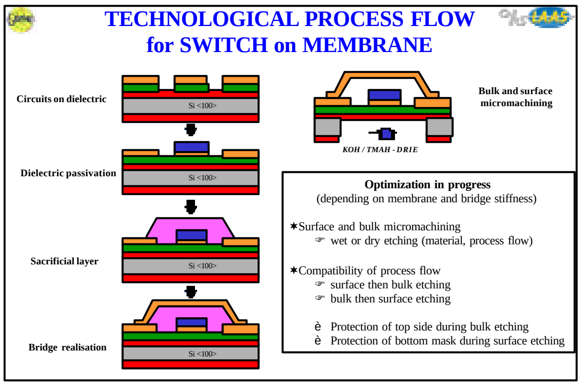

MEMBRANE DEFORMATION
Evaporated gold (1.5 µm)
Gold conductors
Electrolytic gold (2.5 µm)
SiO_2 / SiN_x membrane
Stress concentration

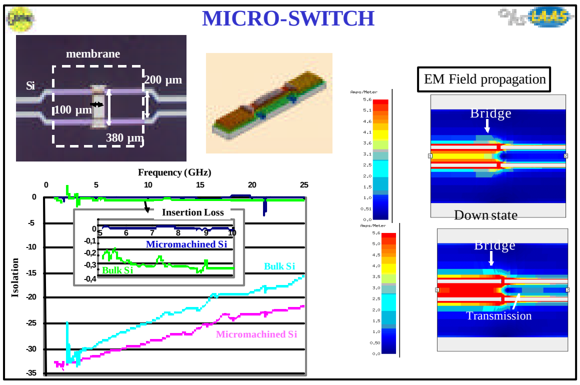

OSCILLATOR
Top view of the structure
Profile view of the cavity
Dielectric resonator
Dielectric Resonator
Membrane
H
E
Phase Noise =60 dBc/Hz
@10 kHz
Dielectric resonator
- Ceramic (ε_r = 30) è F_o = 35.2 GHz, losses = - 6.9 dB, Q_l = 1000
- High resistivity silicon (ρ = 8 kΩ.cm, ε_r = 11.9) è F_o = 96 GHz, losses = -5.3 dB, Q_l = 2000

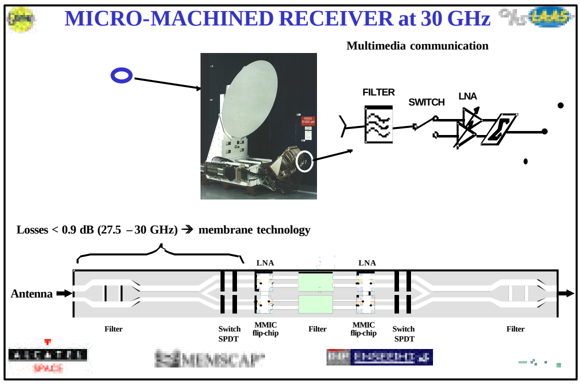

IN PLANE RADIATION ANTENNA
Top view of Yagi antenna
Membrane
D = 20, 25, 30 mm
60 µm
Silicon
Bottom view of Yagi antenna
Return losses of the antenna
Transmission between 2 antennas
D = 20 mm
25 mm
30 mm

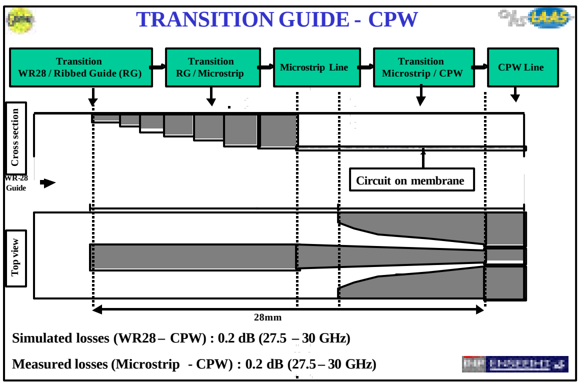

RECEIVER INTEGRATION
Patch antenna response
E plane radiation diagram
H plane radiation diagram
Principal polarisation
Cross polarisation
Filter response
Receiver response under 20 GHz illumination
-40 dBm
-60 dBm
-80 dBm
-100 dBm
18GHz
20 GHz
22 GHz
Frequency
Frequency (GHz)

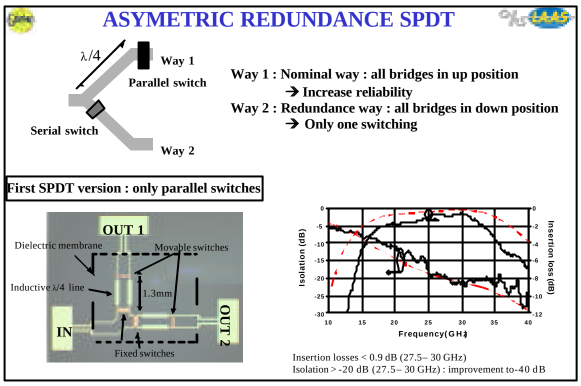

HOT ELECTRON BOLOMETER
Modulation of NBN (0.2 x 0.2 µm) supraconductor resistance by IF power
Far Infrared Source
HEB
Beam combiner
RF
LO Source
f_{LO}=1.4THz...1.6THz
IF
2.5 mm
0.2 µm
T = 4.2 °K
T_c = 9.5 °K
Membrane benefit :
suppression air / substrate dielectric discontinuity
- better RF and LO coupling efficiency
- no substrate coating to match the air / silicon discontinuity
suspended circuit (filter, antenna)
- low losses
- enlarged size for high IF frequency
investigate quasi-optic array designs (easier).

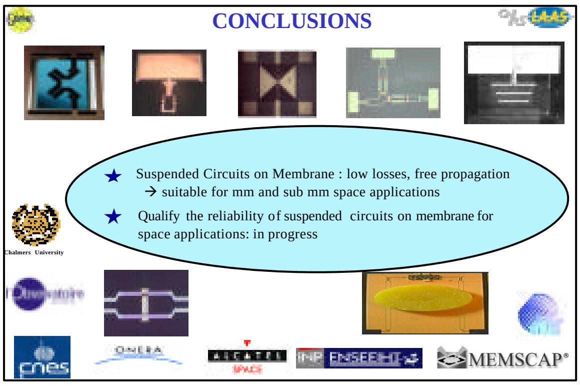

TECHNOLOGICAL PROCESS FLOW
for SWITCH on MEMBRANE
Circuits on dielectric
Si <100>
Dielectric passivation
Si <100>
Sacrificial layer
Si <100>
Bridge realisation
Si <100>
Bulk and surface
micromachining
KOH / TMAH - DRIE
Optimization in progress
(depending on membrane and bridge stiffness)
Surface and bulk micromachining
wet or dry etching (material, process flow)
Compatibility of process flow
surface then bulk etching
bulk then surface etching
Protection of top side during bulk etching
Protection of bottom mask during surface etching


MICRO-SWITCH
membrane
Si
200 µm
100 µm
380 µm
Frequency (GHz)
Isolation
Insertion Loss
Micromachined Si
Bulk Si
Bulk Si
Micromachined Si
EM Field propagation
Bridge
Down state
Bridge
Transmission


MICRO-MACHINED RECEIVER at 30 GHz
Multimedia communication
FILTER
SWITCH
LNA
Losses < 0.9 dB (27.5 – 30 GHz) → membrane technology
Antenna
LNA
LNA
Filter
Switch SPDT
MMIC flip-chip
Filter
MMIC flip-chip
Switch SPDT
Filter
MEMSCAP


TRANSITION GUIDE - CPW
Transition WR28 / Ribbed Guide (RG)
Transition RG / Microstrip
Microstrip Line
Transition Microstrip / CPW
CPW Line
Cross section
WR-28 Guide
Circuit on membrane
Top view
28mm
Simulated losses (WR28 – CPW) : 0.2 dB (27.5 – 30 GHz)
Measured losses (Microstrip - CPW) : 0.2 dB (27.5 – 30 GHz)


ASYMETRIC REDUNDANCE SPDT
λ/4
Way 1
Parallel switch
Serial switch
Way 2
Way 1 : Nominal way : all bridges in up position
→ Increase reliability
Way 2 : Redundance way : all bridges in down position
→ Only one switching
First SPDT version : only parallel switches
OUT 1
Dielectric membrane
Movable switches
Inductive λ/4 line
1.3mm
IN
OUT 2
Fixed switches
Isolation (dB)
Insertion loss (dB)
Frequency(GHz)
Insertion losses < 0.9 dB (27.5 – 30 GHz)
Isolation > -20 dB (27.5 – 30 GHz) : improvement to -40 dB


CONCLUSIONS
LAAS
Suspended Circuits on Membrane : low losses, free propagation
→ suitable for mm and sub mm space applications
Qualify the reliability of suspended circuits on membrane for space applications: in progress
Chalmers University
cnes
ONERA
ALCATEL
SPACE
INP ENSEEIHT
MEMSCAP®