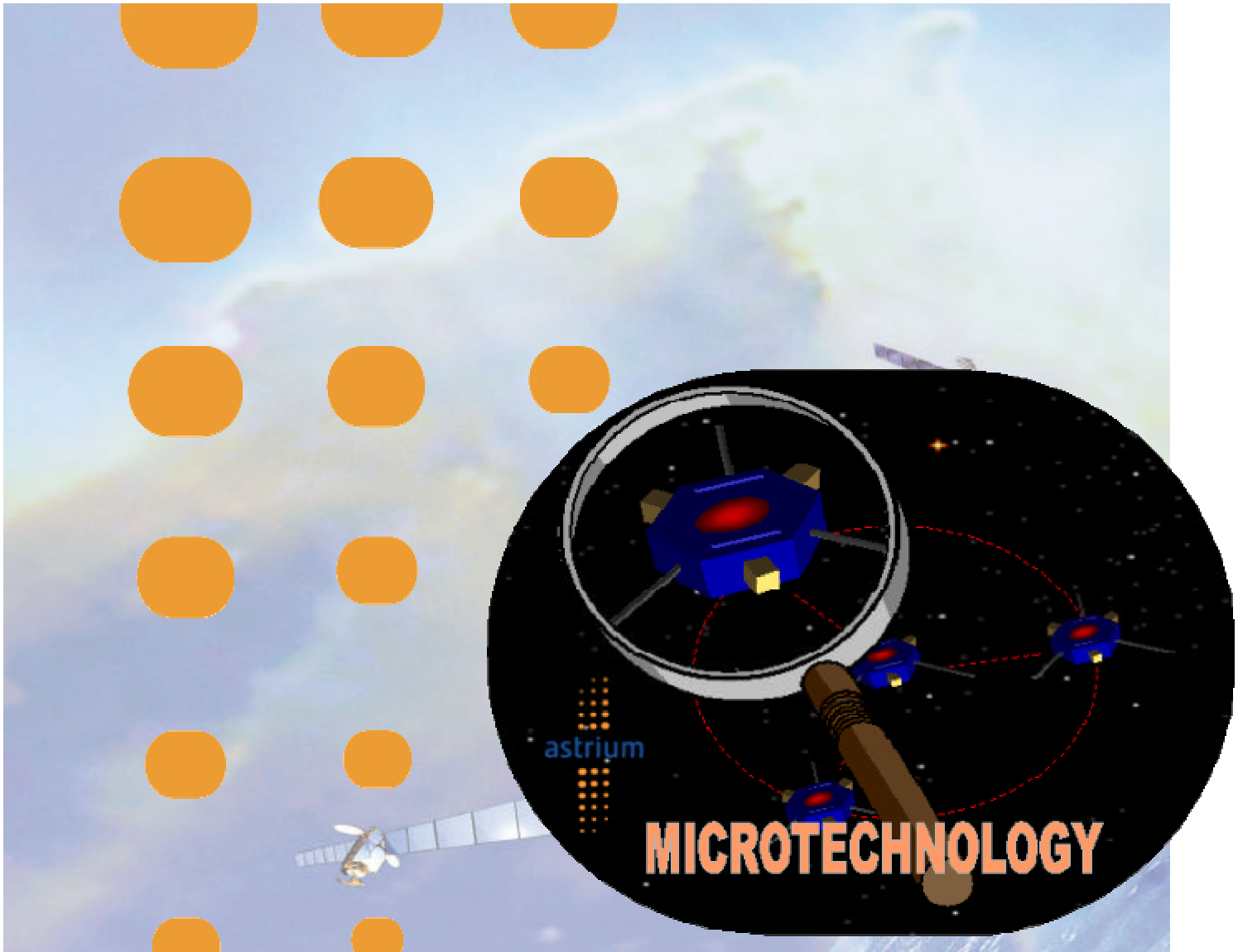

astrium

MICRO-SYSTEM-MODULES

An industrial Roadmap for Space MST Integration

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OUTLINE

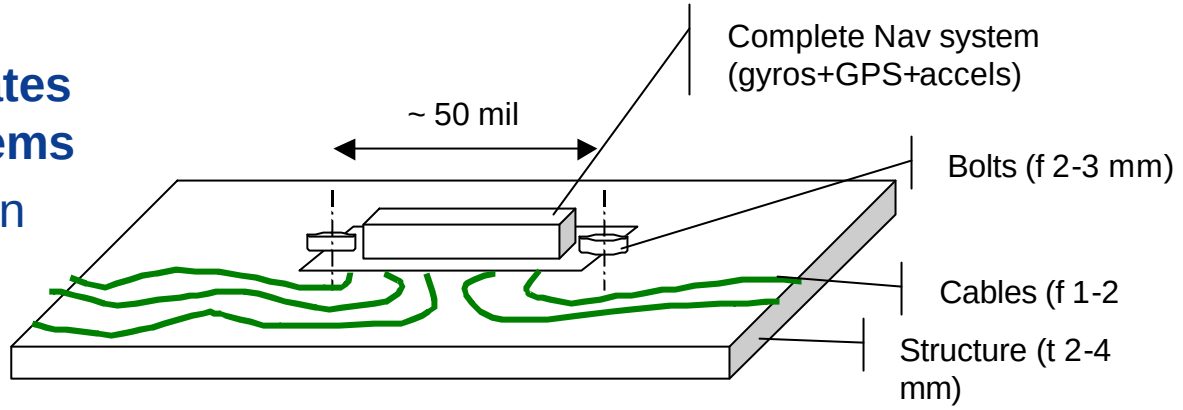
INTRODUCTION

- **BNSC ATS STUDY for MST integration in 2001-2002**
- **THANKS A LOT TO:**
  - Jean-Claude TUAL, Astrium SAS, Velizy
  - Jean Simonne, LAAS Toulouse, F (now out of it!)
- **THANKS ALSO TO:**
  - Carles Ferrer, CNR Barcelona, S
  - Paul Kirby, Cranfield Uni., UK

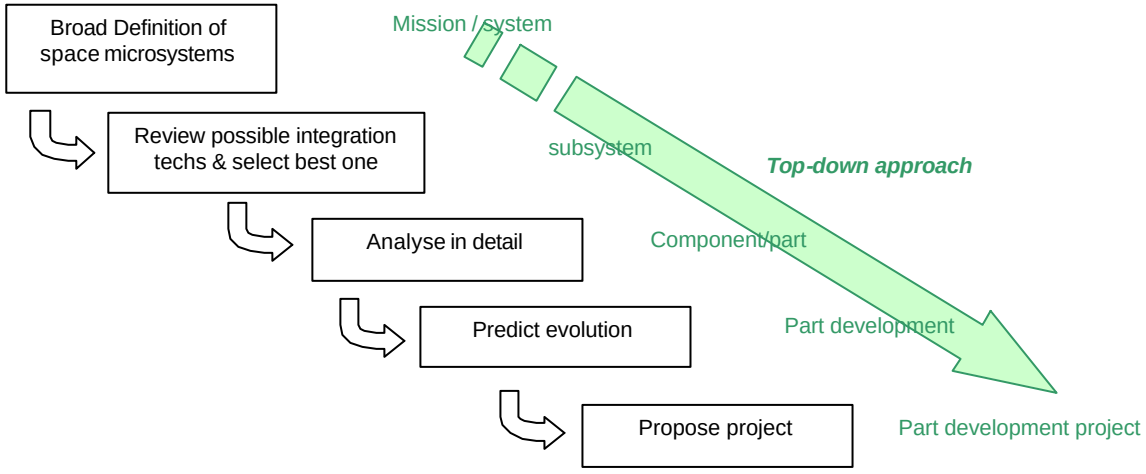
- **ADDRESS INDUSTRIALISATION OF SPACE MST**
  - Everyone recognises MST is vital for Space
  - But the industrialisation and qualification problems prove much harder than expected
  - To accelerate and prepare for the change a review / design of integration technologies is useful

BACKGROUND

- **The “advent” of MST creates system integration problems**
  - Single sensor integration
  - Electronics integration



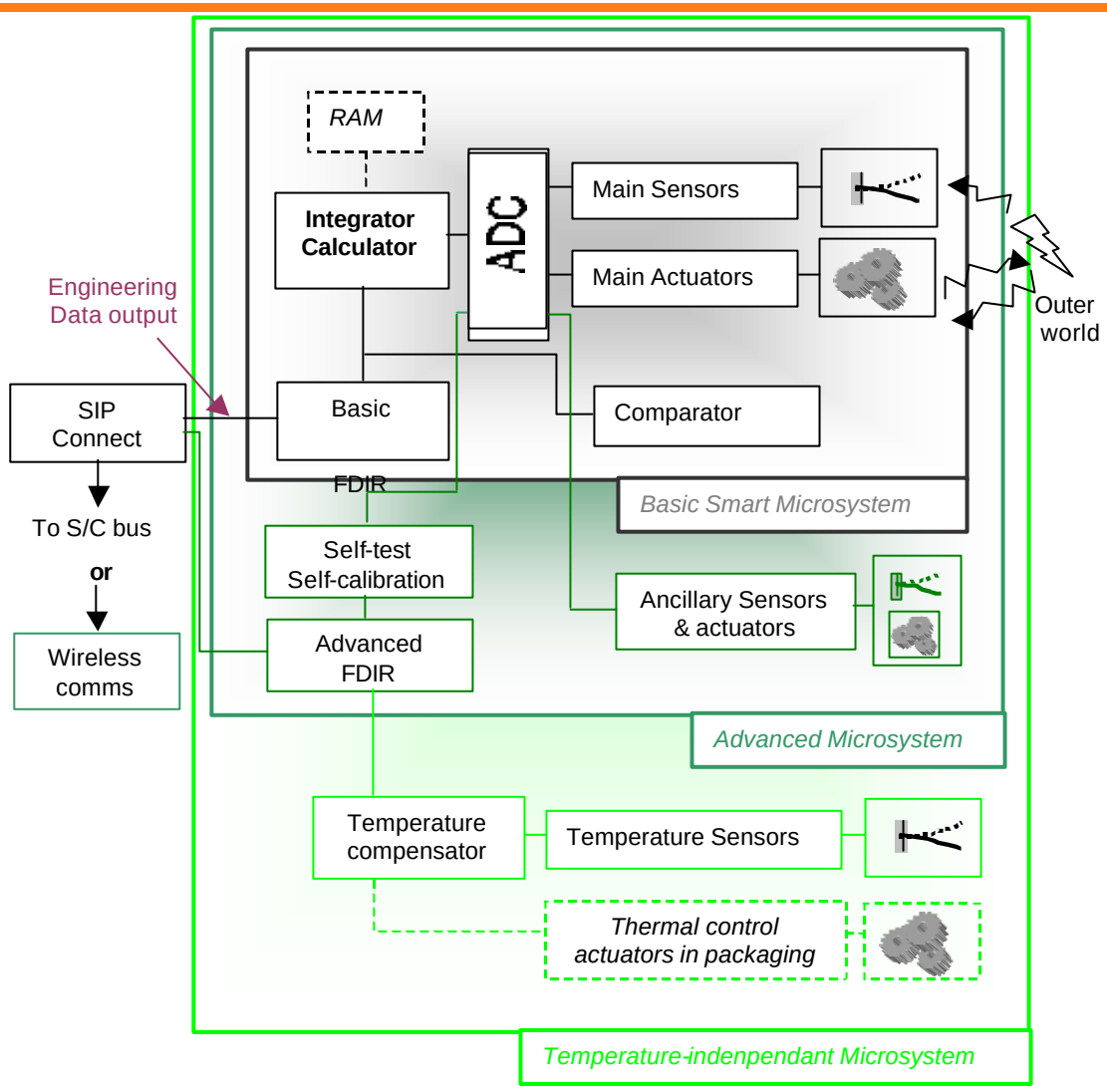
- **Necessary to define new AIV processes, technologies & skills:**
  - Qualification of devices
  - Micro-system design
  - *Systems Industrialisation*:
    - Integration
    - Procurement



“SMART MICROSYSTEMS”

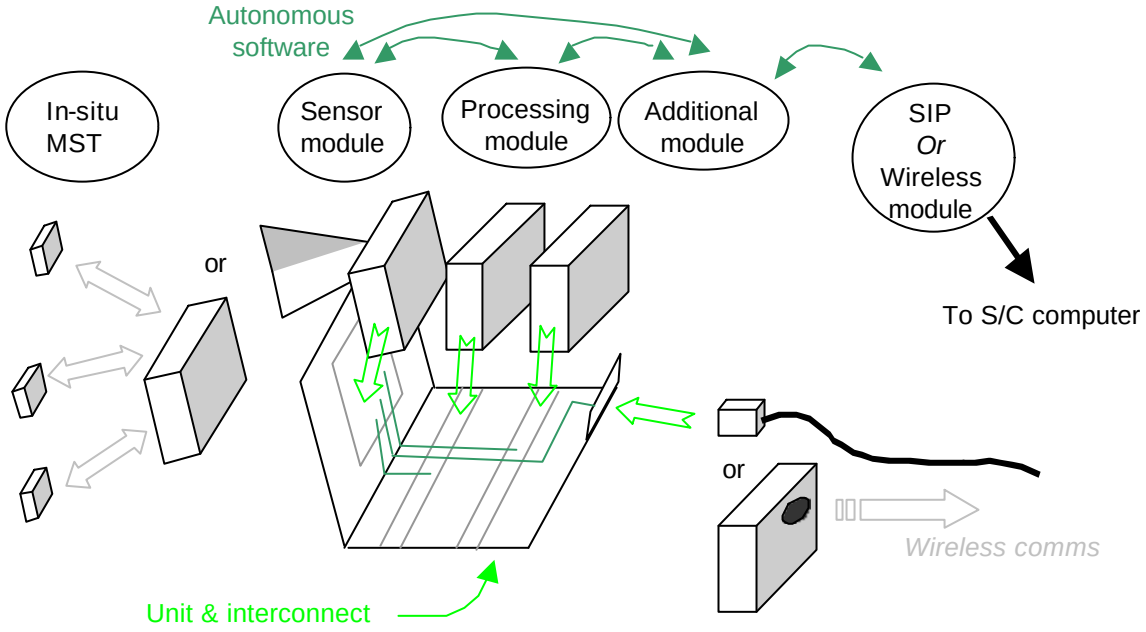
- **Highly integrated multi-sensor components**
  - Different levels of “smartness”
  - Suitable for micro-explorers
  - High-level output

- **Advanced functions**
  - Interface to SIP (ESA R&D)
  - Interface to Wireless
  - Temperature compensated
  - Can include FDIR



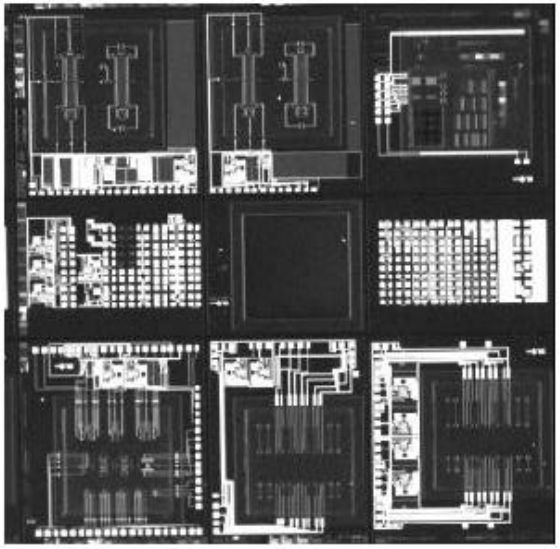
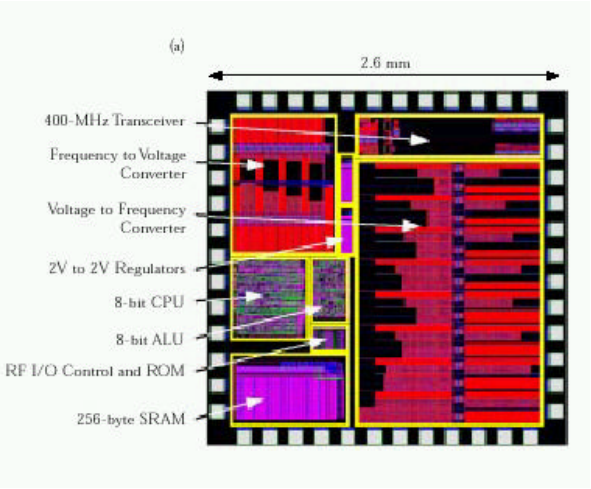
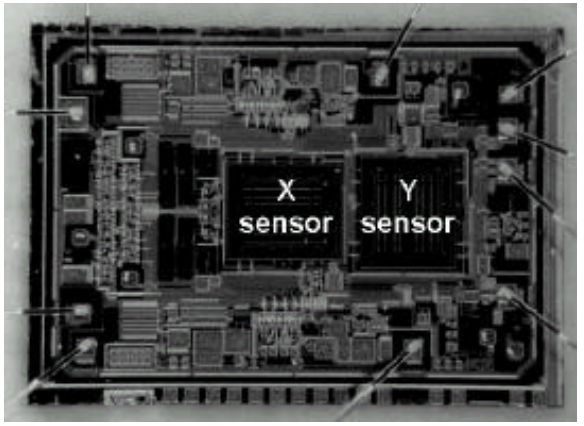
“SMART MICROSYSTEMS” IMPLEMENTATION

- **Composed of modular systems**
- **Used for intra-satellite remote sensing as well**
- **Three integration/implementation possibilities for components:**
  - System-on-a-chip
  - MCM-bas approach
  - Hybrids



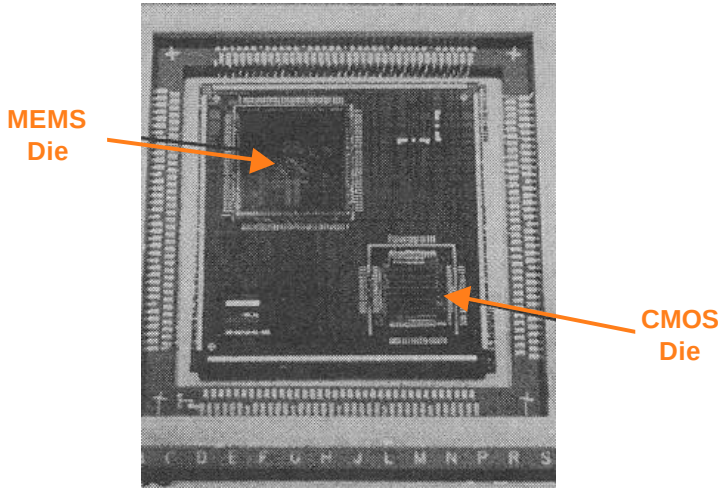
INTEGRATION TECHNOLOGY - SOAC

- Ultra high integration and system effectiveness
- No European effort for Space as of yet

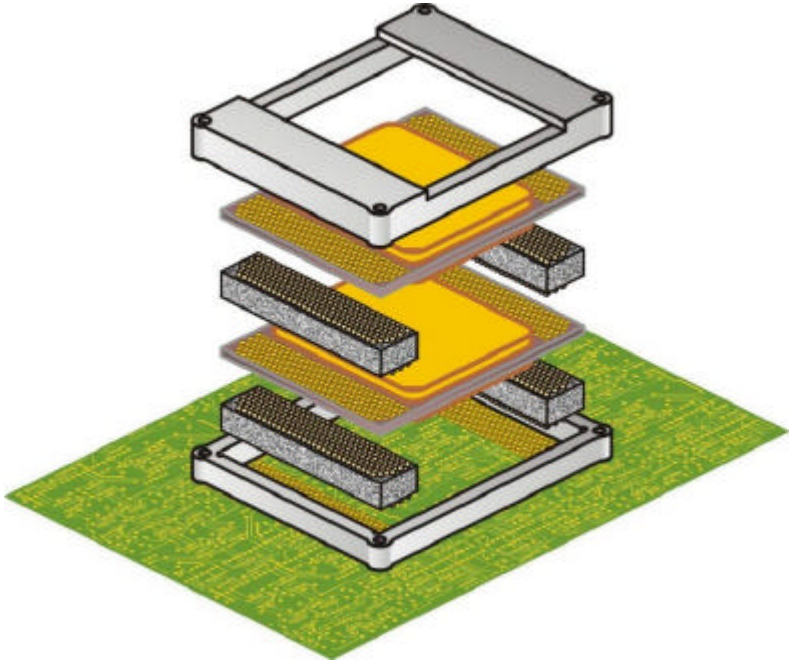
SANDIA LABS SUMMIT V	JPL CISM 0.35 µm SOI (Honeywell Process)	OTHER COMMERCIAL (Analog Devices)
		
Courtesy of Sandia National Laboratories	*Courtesy of Honeywell & NASA JPL*	*Courtesy of Analog Devices*

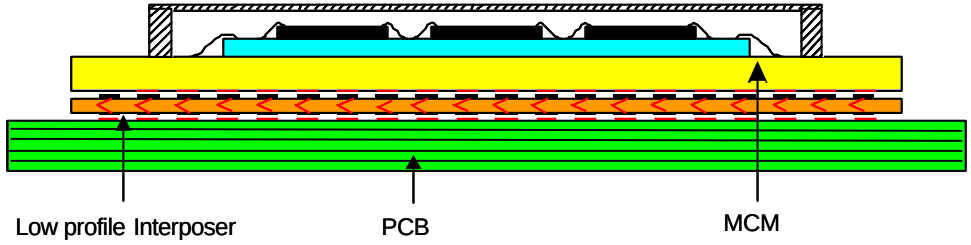
INTEGRATION TECHNOLOGY – MCM-BASED

- **Available in Space Industry**
- **Proprietary technologies**
- **Need significant adaptation**
- **Package influences design**



Courtesy of NASA GSFC

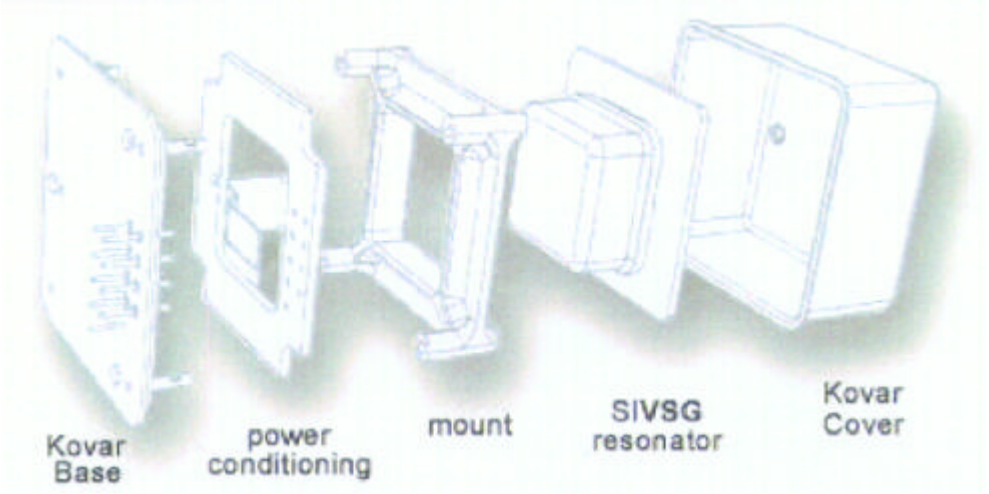




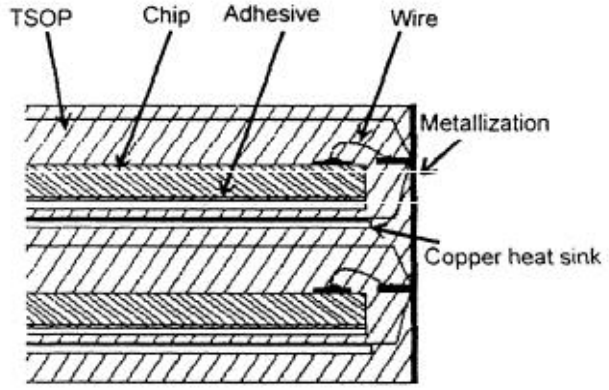
Courtesy of Astrium SAS

INTEGRATION TECHNOLOGY - HYBRIDS

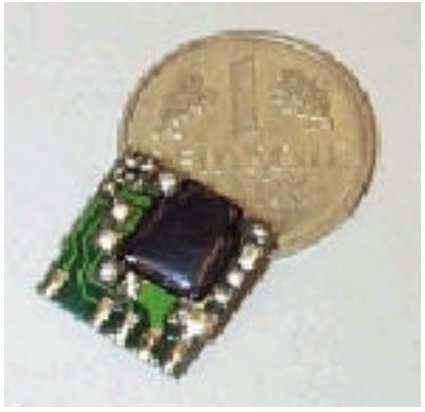
- **Available commercially**
- **Good turn-around**
- **Poor repeatability**
- **Plastic packaging maybe**

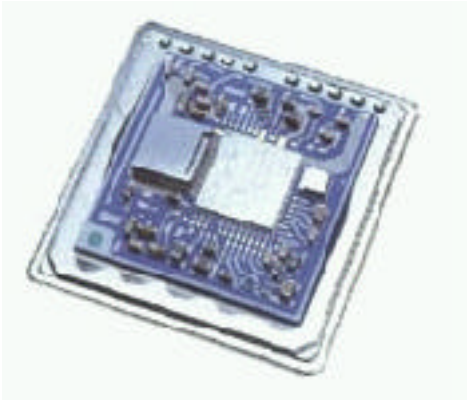


Courtesy of BAe Systems



Courtesy of 3D+



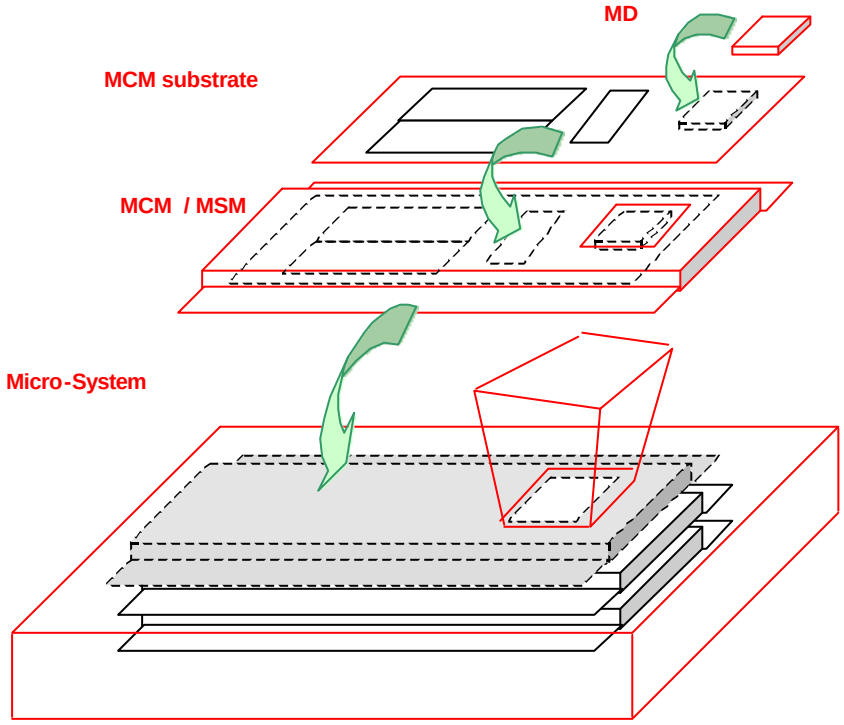


Courtesy of Astrium Gmbh

INTEGRATION TECHNOLOGY – TRADE-OFF

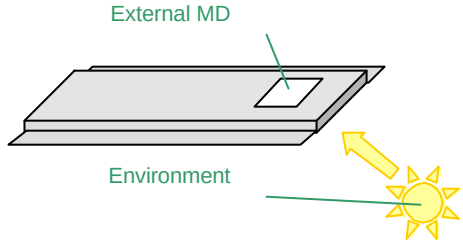
Technology	SOAC	MST-MCM	Hybrids
Integration levels	High Highest with current technologies	Medium Much better than current levels	Low Only the miniaturisation
Technology readiness	Development No working prototype	Prototype Some similar products	Product Flight proven
Technical hard points	Integrated design Complex project	Process compatibility	None
Industrial readiness	Europe industry does not have capacity	MCM capacity Adaptation possible	Ready except for device procurement
Industrial hard points	Very large infrastructure required	Modification of MCM process & culture	None
Est. Develpt cost	> 1 M£	~ 500 k£	~ 200 k£
UK Space industry	Not accessible	Accessible in Astrium UK & F	Accessible in SMEs & labs
UK SMEs	Not researched for space	Not researched for space	Accessible
Time to market	10 years	7 years	3 years
General pros	Ultimate in microtechnology, most efficient system	Good compromise Gives much better integration wrt current systems anyway	Rapid development Easily integrated into current spacecraft
General cons	Very technical and still many hard points	Some development necessary	Not efficient Not easily industrialised

MICRO-SYSTEM MODULE: COMPATIBILITY

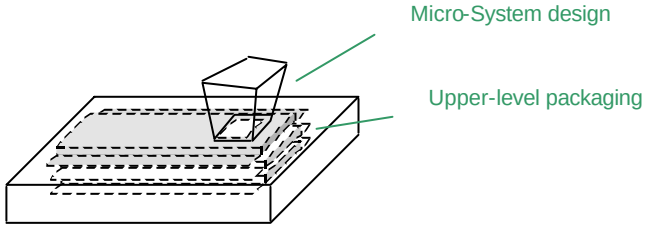


Internal compatibility

External compatibility



System-level design



INTERNAL COMPATIBILITY

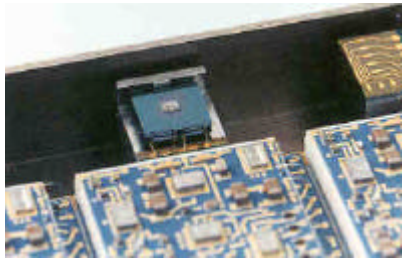
CONSTRUCTION

- Plastic maybe difficult (outgassing)
- P < 500 mW is OK
- No EMC problems for DC devices

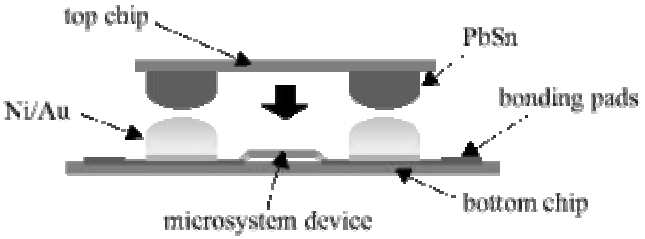
Gas	Density g/l	Viscosity mPa
Air	1.29	18.6
Nitrogen	1.25	17.9
Difference	3%	4%

CONFIGURATION

- May use m-brackets
- May use device packaging
- Height Maxi ~ 3.5 mm



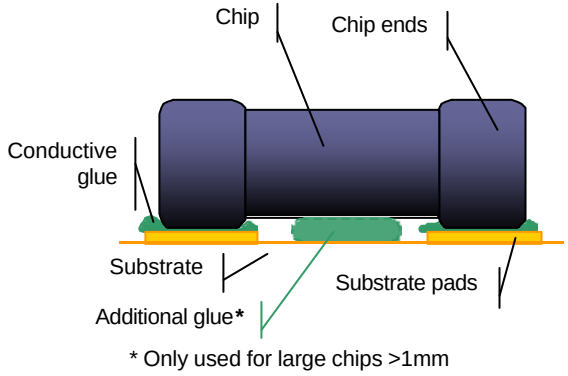
Courtesy of Litef Gmbh



Courtesy of IMEC

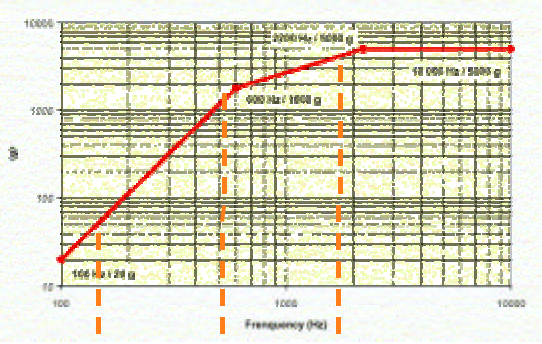
ATTACHMENT

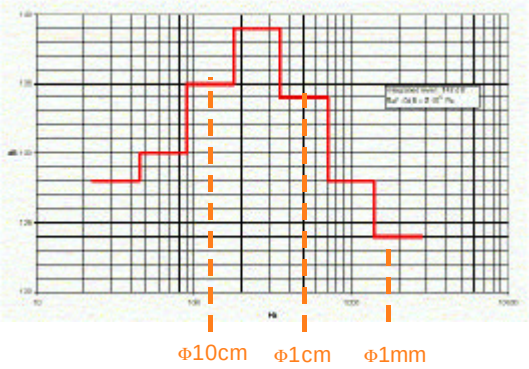
- Tolerance angle < 1mrad
- Al2O3 substrates
- AbleBond 84 adhesive



EXTERNAL COMPATIBILITY

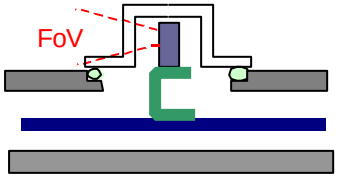
SPACE ENVIRONMENT

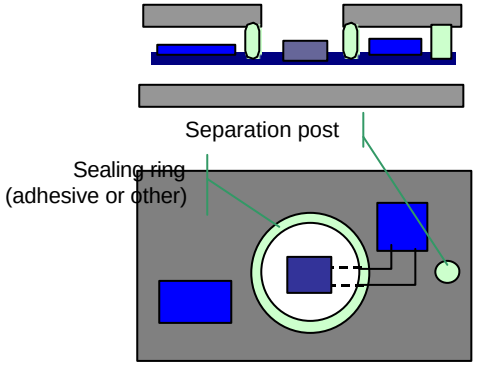


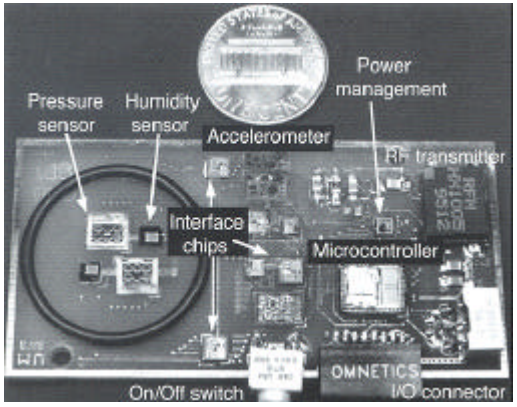


Comparative Temperature	S/C –40 C	S/C + 40 C
Flat chip	- 33.3	43.4
“I” profile	- 24.8	33.7

VIEWING EXTERNAL ENVIRONMENT







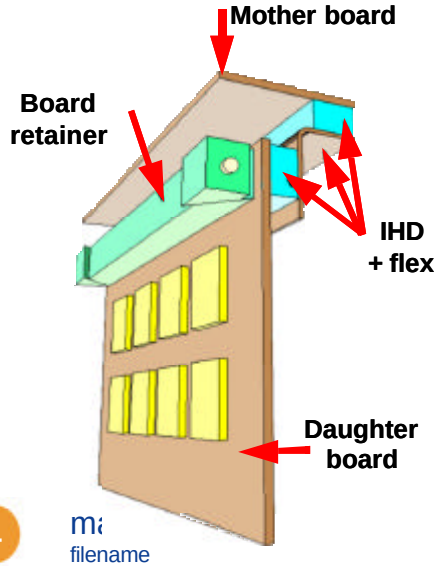
Courtesy of Aerospace Corporation

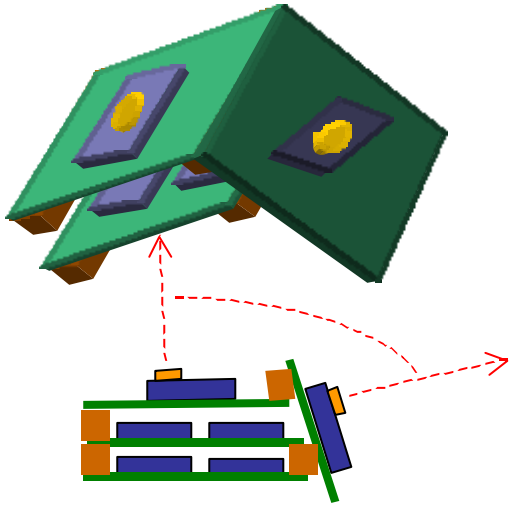
SYSTEM DESIGN COMPATIBILITY

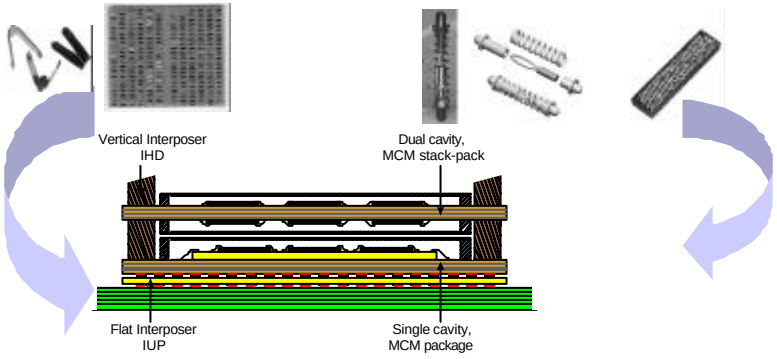
MICRO-SYSTEM INDUSTRIAL DESIGN

SYSTEM DESIGN	MICROSYSTEM DESIGN	DEVICE DESIGN	PROCESS & LAYOUT DESIGN	AIV PLANNING
MATLAB	*?*	*VHDL / SPICE*	*AutoCAD*	*MS Project*

SYSTEM-LEVEL PACKAGING







Courtesy of Astrium SAS

RESULTS

- **ROADMAPS for each implementation**
  - Technology tree
  - “Passive” and “Active” Roadmaps

MSM “Device Requirements documents”
  - Draft list of requirements
  - To be considered by device developers
  - Used primarily as a basis for discussion

- **PROJECT PROPOSALS**

- **CONCLUSIONS:**
  - In parallel to device reliability and qualification, industrialisation is necessary
  - Necessary to use integration technologies available in European industry
  - Design cycle impacted, adaptation of tools necessary
  - Is technically feasible, but needs to be addressed

ROADMAP (CONTROLLED)