IRIS3: A CMOS APS SINGLE-CHIP RADIATION-TOLERANT IMAGING SYSTEM

C.Van Hoof, T.Torfs*, T.Cronje**, W.Ogiers***, G.Meynants***, J.Bogaerts***, S.Habinc****, R.Weigand******

** IMEC vzw, Leuven, Belgium*
*** SunSpace, Stellenbosch, South Africa (formerly with IMEC)*
**** FillFactory nv, Mechelen, Belgium*
***** Gaisler Research, Goteborg, Sweden (formerly with ESA)*
****** ESA-ESTEC, Noordwijk, the Netherlands*

Abstract

The IRIS3 is a single-chip camera for visual monitoring from spacecraft in flight. This 1024 x 768 pixel imager has all interface and control logic on-chip, and is capable of directly addressing up to 64 megawords of off-chip memory for image storage. The sensor can use the CCSDS telecommand/telemetry packet format for its communication with the spacecraft.

Implemented in a commercial 5ì CMOS process, large parts of the chip were designed using proven radiation-hardening layout techniques.

This paper discusses the IRIS3's architecture and functionality, the characterisation results of its first silicon, and finally addresses some issues for future similar devices.

1 Introduction

Several missions in the recent past, notably TeamSat (1997), XMM (1999), and Cluster II (2000) have demonstrated on-board cameras for visual feedback of spacecraft-launcher separation or antenna deployment.

figure 1 VMC camera

Each of these camera examples were ad-hoc designs, using off-the-shelf components, typically industrial vision CMOS active pixel sensors and fairly small rad-tolerant FPGAs. In addition to their one-off nature, these cameras were somewhat restrained in operation by the S/C's OBDH system or the interface thereto.

The VTS camera on TeamSat lacked image memory and thus the S/C computer had to directly read out the pixel array. Even with a tailored RS422 serial data interface of 3.125Mb/s this limited the system frame rate to just one image per second.

figure 2 VMC image of XMM solar panel in flight

The VMC cameras on XMM and Cluster II offered spacecraft interface compatibility through their TTC-B-01 serial links running at 100kb/s or less. The XMM cameras had internal storage for one image, the Cluster camera had an external add-on memory box, the XMXU, offering in-line storage for about 10 images. In both cases the acquisition time for one image was 200ms.

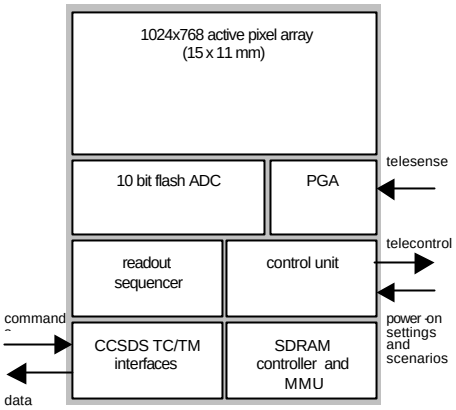
The subject of this paper, the IRIS3 single-chip camera, aims to overcome some of the limitations of older systems, offering more functionality and portability, higher electro-optical performance and yet lower impact on existing S/C architectures.
Moreover, it combines sensor and control/interfacing logic onto one silicon die, allowing for smaller cameras to be built.

figure 3 VMC/XMXU image of Cluster II separation (part of a movie sequence)

The development of this sensor, part of ESTEC contract 13716/99/NL/FM, was started in 1999 at IMEC's image sensor group, but got delayed somewhat when in 2000 this group spun off from IMEC to create FillFactory. Since then the development the chip has been a joint effort of both organisations, FillFactory being responsible for the architectural design and the analogue pixel array, IMEC for the logic design and device characterisation.

IRIS3 follows IRIS1, a VGA-resolution 8 bit sensor without any logic on-chip (used in the VMC camera), and IRIS2, which was an IRIS1 with on-chip logic for control and CCSDS-compatible interfacing (ESTEC contract 11970/96/NL/FM).

2 Camera chip architecture



The analogue core of the IRIS3 chip comprises of a line- and column-addressable pixel array with associated column amplifiers performing double sampling on the signal, a programmable gain amplifier (PGA), and an analogue to digital converter (ADC). The output of the ADC feeds the cell-logic based digital part of the sensor, which takes about 30% of the die's area. The logic takes care of generating the driving pulses for the pixel array, amplifiers and ADC. It receives commands from a set of serial and parallel input interfaces, and sends output data to a set of parallel and serial output interfaces.
Telecommands and telemetry data can be in the ESA/CCSDS packetised format.

figure 4 IRIS3 sensor chip block diagram

An important feature of the IRIS3 is its on-chip SDRAM memory interface and manager. The sensor can use this memory, up to 64 megawords large, for the storage of tens of images. It can also use this memory for passing information and data to and from an external processor, like an image compression chip. Such a processor can return the images after compression to the shared SDRAM, after which these data are accessible by the S/C for download through IRIS3's telemetry link.

Additional interfaces are an analogue input to the ADC, for recording telesense data of external sensors. These data can be associated with an image at acquisition time and then stored in the SDRAM for future download. There are also six digital telecontrol outputs, useful for switching external signals such as cover controls, lighting, etc.

3 Configurations

3.1 Stand-alone

The smallest camera consists of just the sensor and its biasing components. As there is no local image storage, all acquisition data is sent to the host system in real time.

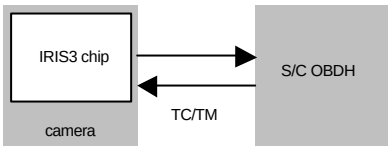


figure 5 Single-chip camera

3.2 With memory

Using one, two, or four industry-standard 256 megabit SDRAM chips the sensor has local storage for up to 60 full-size images (or more smaller-size images) at 8 bit resolution, or at 10 bit resolution with the added benefit that part of the memory is used for corrective EDAC. Images can be captured at high speed, buffered in the memory, and later on downloaded at leisure.

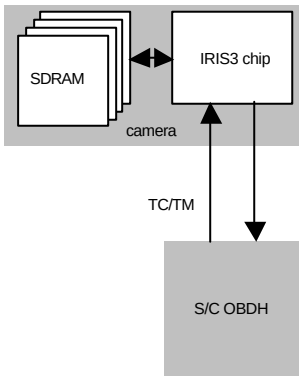


figure 6 Camera with image memory

3.3 With memory and processor

An external processor interfaces to the system through the SDRAM's lower pages. In these pages resides a command and parameter passing area, allowing IRIS (and the end-user) to instruct the processor, and a shared datastructure that describes the images and attached telemetry data in the memory.

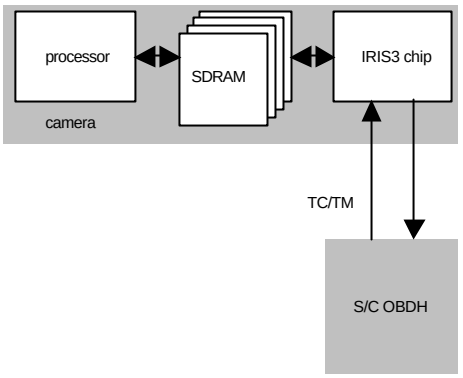


figure 7 Camera with image memory and processor

4 Functionality

4.1 Operating modes

The envisaged method of operating IRIS3 is sending it telecommand packets containing settings (such as exposure time, window size and position, PGA gain, ...) and the action to be undertaken (typically the capture of up to 127 images, spaced apart 0 to 32 seconds, and delayed with up to 18 hours). One can also directly access the off-chip memory, for instance for sending commands to a processor through the shared data area.
If needed IRIS generates the requests for image processing/compression to the external processor, using a predefined set of commands that the processor has to recognize.

Although IRIS3 is meant to be operated under control of a local intelligence, the system provides for a limited autonomy after power-on. Several straps can be used to define the chip's post-reset settings, as well as an operating scenario that makes the sensor take a defined number of images with a defined period of time between them, and either store these in memory or present them directly on the telemetry interface of choice.

This scenario can be triggered by a chip reset, or by a trigger signal fed to the chip, coming e.g. from a strap relief connected between S/C and launcher.

The triggered action can be executed immediately, or after a programmed delay time of up to 128 seconds.

4.2 TC/TM packetising

The telecommand and telemetry data interfaces of IRIS are compliant with CCSDS packetising with grouping, ESA-CCSDS packetising with segmentation, or could be used in unpacketised, raw mode. The payload area in the packets or segments can be sized up to 256, 512, 1024, or 2048 bytes.

4.3 Spacecraft interfaces

Several telecommand and telemetry data interfaces are available for connection to the spacecraft or other devices.

-asynchronous serial, 115.2kbps up to 25Mbps
-synchronous serial, up to 25Mbps
-TTC-B-01, 8 bit version, up to 4Mbps
-TTC-B-01, 16 bit version, up to 4Mbps
-synchronous parallel, up to 12.5Mwords/s

The asynchronous interface is similar to RS422/485 and offers compatibility with standard UARTs when used at its lower datarates.

4.4 Memory interface

The memory interface is compatible with industry-standard 256 megabit 32Mx8 organisation SDRAMs that allow for burst lengths of 1024 reads or writes. Examples of such chips are:

-Hitachi HM5225805B
-NEC mPD45256841
-Micron MT48LC32M8A2
-Samsung K4S560832A

The interface supports configurations of 1, 2, or 4 chips, offering 32 or 64 megawords of storage. Word lengths of 8 bit and 16 bit can be used. In the former case, only the 8 upper bits of pixel data are stored. In the 16 bit case, all 10 bits of pixel data are stored, alongside 4 standard EDAC bits (Hamming code over a full word), allowing for the detection and correction of one bit error per word.

4.5 Processor interface

All communication to the processor is through the memory, with the exception of two status lines, indicating the processor's status with respect to the memory, and IRIS3's request for access to it.

The memory is split into several parts, each storing a specific type of data structure:

command passing zone	a mailbox allowing predefined commands to be passed from IRIS to processor, and status information in both directions.
processor parameter area	500 kilobytes of space not used by IRIS itself, but available to the end user to upload e.g. program code to the processor.
Image data location table	a shared datastructure detailing the whereabouts and status of every raw or compressed image residing in the memory.
scratch area	2 megawords of area for the processor to use while operating on images.
image buffer	the raw and/or processed image storage space proper.

Typical scenarios are to have the processor compress all images after capture, or to have it compress and rewrite images when they become available. During these proceedings the memory is always available to the external processor, with two exceptions: IRIS3 needing access for writing images and updating the associated datastructure, and IRIS3 performing a refresh operation.

In all cases all interfacing to the S/C is handled by IRIS3, making the addition of memory and processor entirely transparent. And as IRIS3 totally controls the SDRAM, the processor need not be concerned with SDRAM configuration and refresh sequences.

4.6 Image acquisition

When the memory is used, image acquisition occurs at a pixel rate of 12.5MHz, resulting in 12 full frames per second. Restricting the frame size by windowing and/or subsampling yields proportionally higher frame rates, appr. 40 frames/s at 512x512 pixels, and 120 frames/s at 256x256 pixels.

When the image is directly downloaded on the output interface, i.e. without memory buffering, the acquisition rate is obviously limited by the transmission rate of that interface.

The sensor employs a rolling-blade electronic shutter, allowing for exposure times ranging from 0.1ms to 77ms and beyond.

An automatic shutter control loop is present too, but this only works on streaming images, i.e. when more than 10 images are requested.

5 Electro-optical specification

The analogue sensor core and ADC of IRIS3 were essentially lifted from the one megapixel STAR1000 sensor ([1]), and reduced to 1024 x 768 pixels to allow for fitting in the on-chip logic. (The similarity went so far that during development most of the IRIS3 could be prototyped using a STAR1000 and a Xilinx Virtex 600 FPGA.)

format	1024x768 pixels
pixel size	15µm x 15µm
ADC	10 bit
pixel rate	12.5MHz
frame rate	12 full frames/s
	40 quarter frames/s etc.

This specification compares favourably with the 640x480 pixel resolution at 8 bits per pixel of earlier cameras. In addition the IRIS3 can be operated in standard linear transfer mode, as well as with a bi-linear transfer curve which enhances the optical dynamic range by compressing brightly-illuminated parts of the scene.

6 Rad-hard implementation

The design was implemented using FillFactory's megarad-tolerant layout techniques ([2]), in the commercial AMIs .5µm CMOS process (formerly Alcatel Micro-Electronics, Oudenaarde, Belgium).

The logic cells were not rad-hardened, but were selected from a commercial library with low leakage current as criterion. With these measures the chip is expected to withstand total doses in the range of 50-100krads with negligible performance deterioration.

All long-term settings registers as well as the more important state machines are SEU-protected by tripling them up with regenerative voting feedback in each clock cycle.

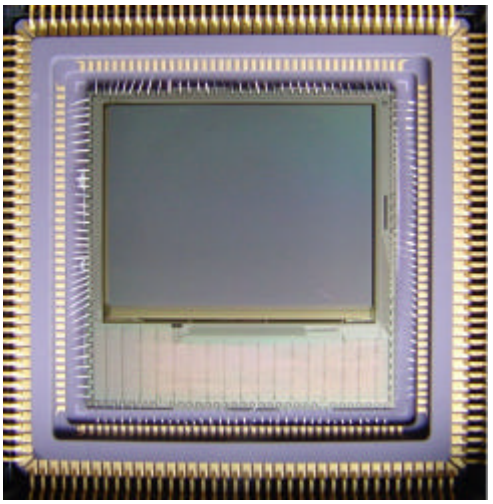


figure 8 IRIS3 camera chip in its QFP package

The resulting chip measures 17 x 17 mm, has about 3.5 million transistors, and has 144 IO pins. It comes in ceramic PGA240 and QFP160 packages.

7 Test results

After processing and first tests the chip was found to be fully functional. Several devices were subject to electro-optical characterisation.

voltage conversion factor	10.4µV/e-
quantum efficiency	25% (including fill factor effects)
saturation charge	120000e-
linear region	85000e-
fixed pattern offset	<0.09% of full-scale (local)
	<0.57% (global)

pixel response non-uniformity	<0.57% of FS (local)
	<3.48% (global)
readout noise	52e-
	550ì V
signal swing	1.3V
dynamic range	67dB
dark signal	2200e-/s
	23mV/s
	56 bit counts/s
	155p A/cm^2
power	600mW

The performance known of the STAR1000 analogue-only sensor was largely repeated, indicating that the inclusion of large amounts of logic was not detrimental to the noise behaviour.

figure 9 Sample raw output image

8 On-going work

The project is not finished yet. In the near future IRIS3 will be tested for total dose irradiation as well as single event upsets and latch-up.

IMEC will design and deposit a Bayer-pattern RGB colour mosaic, yielding a colour sensor. However, as mosaic-pattern-to-RGB colour interpolation is not part of the chip's functions, this interpolation still has to be done in an external processor or on the ground.

Lastly, IMEC together with DSS-OIP (Oudenaarde, Belgium) are developing flight-worthy demonstration cameras, including a full complement of SDRAM in the shape of 3D-Plus's stacked memory module.

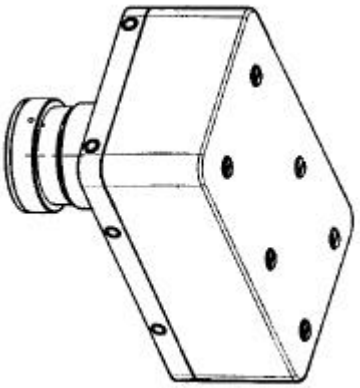


figure 10 Impression of the flight camera under development

9 Where in the future?

Even with IRIS3 being quite a versatile component, a number of features are still missing. Future image sensors could benefit from the following additions that seem feasible at this time, provided .25ì m or .18ì m CMOS processes are used for the implementation:

SpaceWire (IEEE1355.2) high-speed serial interface: there is a move towards SpaceWire as standard chip-to-chip and instrument interface ([3]). With expected arrival of an ESA-funded portable IP core for SpaceWire ([4]), the inclusion on image sensors should be fairly straightforward.

RGB colour mosaic with on-chip colour interpolation. Advanced interpolation techniques require on-chip SRAM memory in the order of 100kbits for a 1024 pixel per line imager.

Automatic exposure control loop with industry-class levels of performance.

Video mode: generation of video streams compatible with e.g. ITU.R BT601 digital video, for use in real-time on manned flights.

Programmable processor core: for sensor control and overall execution of pre-programmed timelines.

10 Conclusions

The latest in a series of ESA-funded CMOS active pixel image sensors for space use, IRIS3 is the first to combine rad-hard design techniques and system-level integration of functionality onto a single chip, allowing for smaller and simpler, yet more powerful visual monitoring cameras.

It is expected that IRIS3 will be commercialised by FillFactory as part of the STAR series of rad-hard sensors.

A first opportunity for in-flight demonstration will probably be the next-generation Amsat P3-E mission, in early 2005.

11 References

[1] F.Boldrini et al, “Applications of APS Detectors to GNC Sensors”, 5th ESA International Conference of Spacecraft Guidance, Navigation, and Control Systems, October 2002

[2] J.Bogaerts et al, "Total Dose and Displacement Damage Effects in a Radiation-Hardened CMOS APS", IEEE Trans. on Electron Devices, vol.50, January 2003

[3] S.Parkes, “SpaceWire: The Standard”, DASIA 99, May 1999

[4] http://www.estec.esa.nl/microelectronics/core/corepage.html