Aspects of Future Memory Module Architecture

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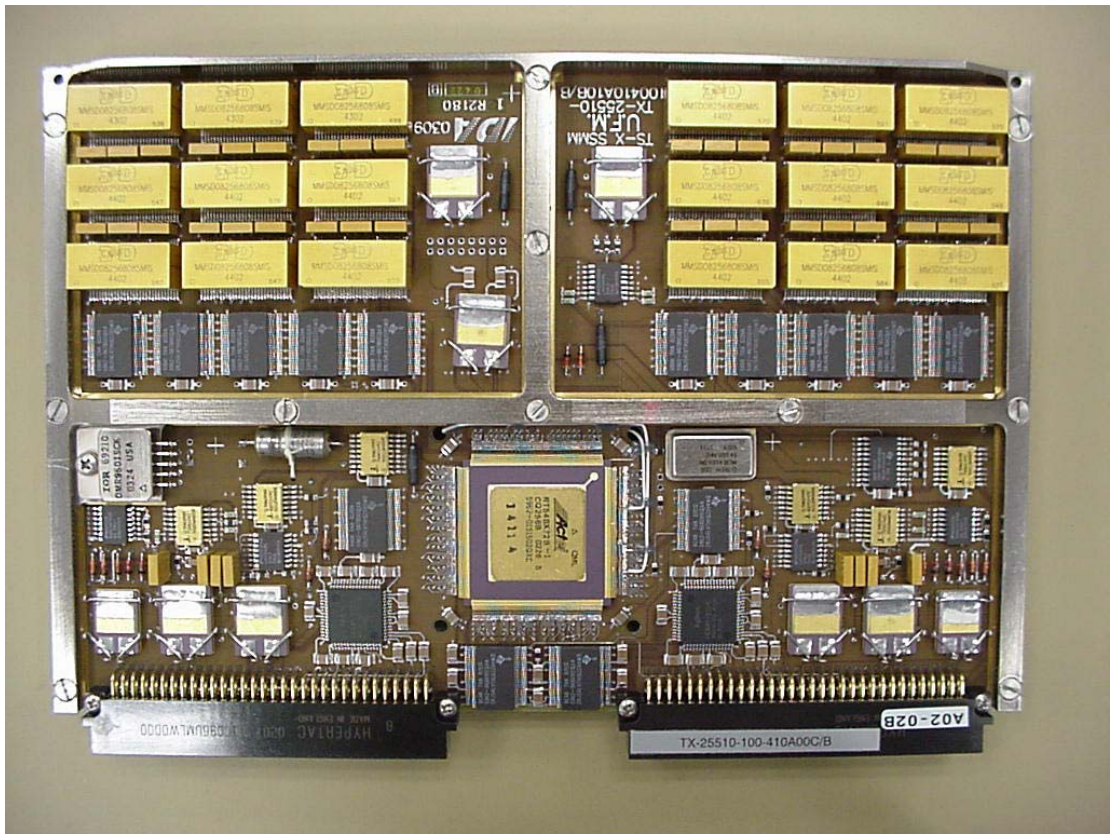
Background and Heritage

- Characteristics of current Module Designs
  - HCMM (used in MEX; VEX; Cryosat 1&2; ISSR; Rapid Eye)
    - Up to 128/256 Gbit/Board with stacked SDR-SDRAMs in 2&4 Gbit cubes
    - Module overall data rate <= 250 Mbit/s
    - Interfaces: SpaceWire and parallel link for data
  - UFM (TerraSAR-X; Tandem X)
    - Up to 64/128 Gbit/Board with stacked SDR-SDRAMs in 2&4 Gbit cubes
    - Module overall data rate <= 2 Gbit/s
    - Interfaces: Gigalink and parallel link for data
  - HCMM and UFM
    - Power Consumption <12 W
    - Flow-through RS Error Detection and Correction on word (128 bit) basis, capable to correct single symbol errors

Example: TerraSar-X SSMM Module (UFM)



High Speed (up to 2 Gbit/s) and High Capacity (64/128 Gbit),

- G-Link serial input interfaces and parallel output interface
- 64/128 Gbit/Board (256/512 Mbit SDR-SDRAM devices)
- appr. 1.6 Gbit/s input data rate
- appr. 300 Mbit/s output data rate
- appr. double Eurocard board size

Example: CryoSat 1&2-MMFU Module (HCMM)

Medium Speed (up to 250 Mbit/s) and High Capacity (128/256 Gbit) Memory Module

- 128/256 Gbit/board (256/512 Mbit SDR-SDRAM devices)
- 8 bit parallel data links (4)
- Serial command link
- appr. 160 Mbit/s input data rate
- appr. 80 Mbit/s output data rate
- Extended double Eurocard board size

Requirements for future Memory Modules

- Data Rate (in + out)
  - Science Missions: up to some 100 Mbit/s
  - EO Missions: up to some Gbit/s
- Capacity
  - Science Missions: typ. <0.5 Tbit
  - EO Missions: up to some Tbit
- Functional Requirements
  - Science Missions
    - Multiple Data Sources with large data rate range (low to high)
    - File system support
  - EO Missions
    - Very High Speed Streaming Data from a few sources
  - Both: high data integrity (handling of SEFI´s *and* SEU´s)

DRAM type comparison (e.g. SAMSUNG)

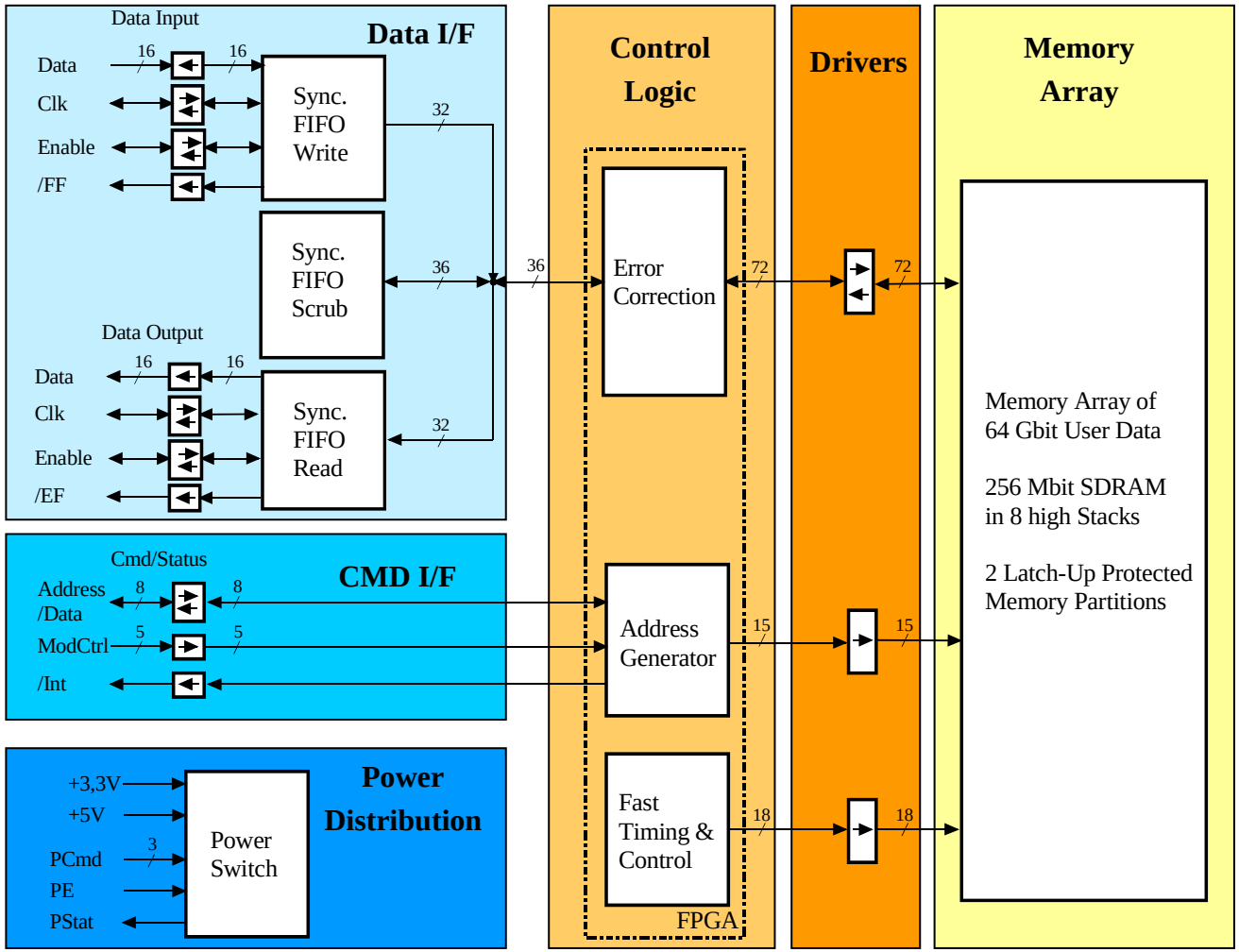
Type	SDR SDRAM	DDR SDRAM	DDR2 SDRAM
Device Capacity	≤ 512Mbit	≤ 1Gbit	≤ 1Gbit
Clock Frequency / Throughput	≤ 133MHz SDR	≤ 200MHz DDR	≤ 400MHz DDR
Packaging	TSOP	TSOP, FBGA	FBGA
Voltage	3.3V, LVTTL I/O	2.5V, SSTL_2 I/O	1.8V, SSTL_1.8 I/O
Typ. Power / device (64M8 devices @ 133MHz)	20mW standby 330mW burst (@ 1 GBps)	75mW standby 325mW burst (@ 2 GBps)	10mW standby [1)] 114mW burst (@ 2 GBps)

1) Low power active power-down mode with DLL disabled (only DDR2)

Module Design Drivers

	Impacts
• Device Packaging – Memory Device Types, Availability, Size – FPGA Type, Pin Count,	capacity, speed, on-module functions,
• Power Supply – Low voltage supply on-module board needed (conversion, distribution, switching)	capacity, speed, low voltage design
• Module Controller Implementation – SRAM based FPGA (XILINX) vs. Antifuse (ACTEL)	on-module functions, capacity, speed
• Interfaces – SpaceWire covers medium to high data rates – Very high data rates >1Gbit/s require new serial I/F technology	speed

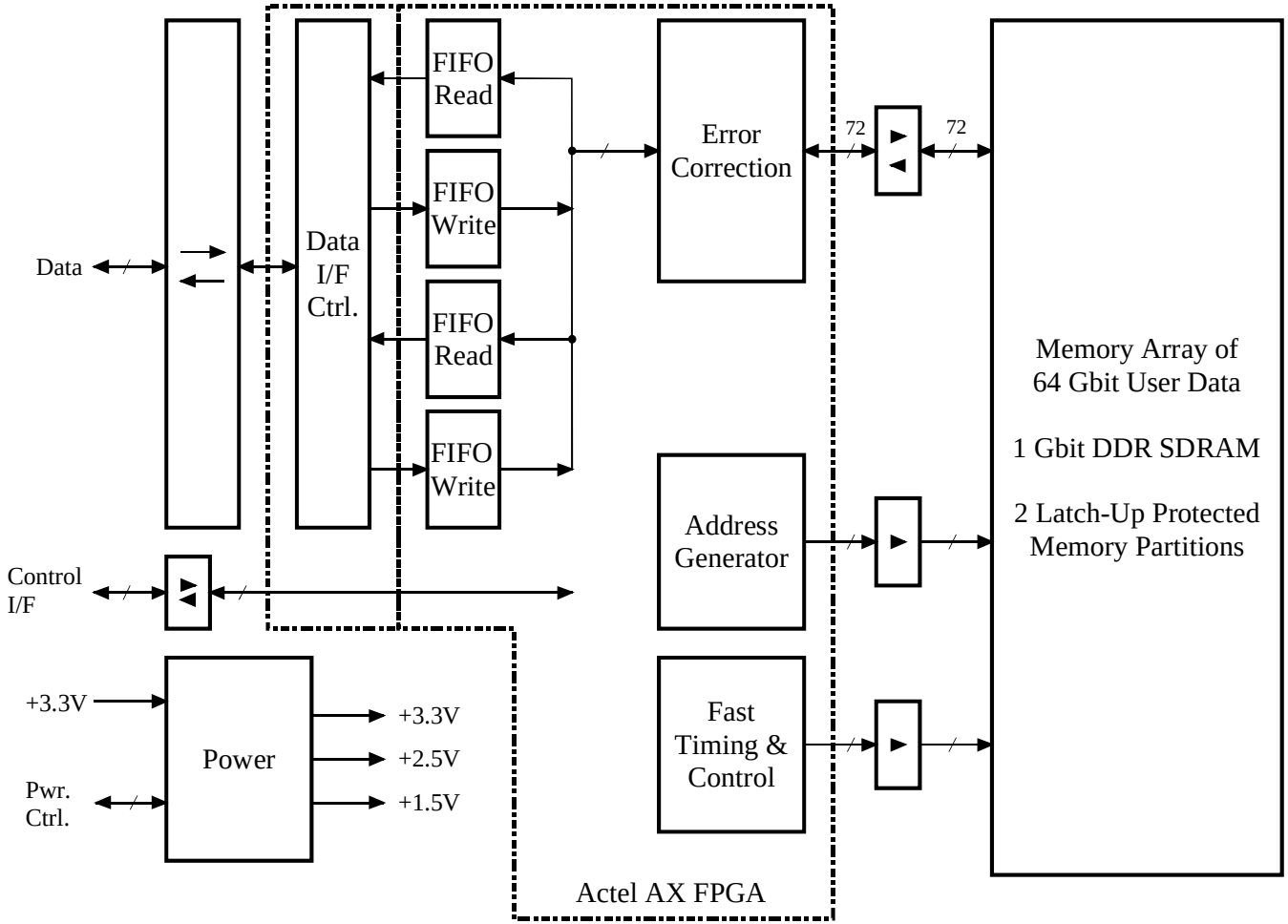
Memory Module functional groups (UFM design)



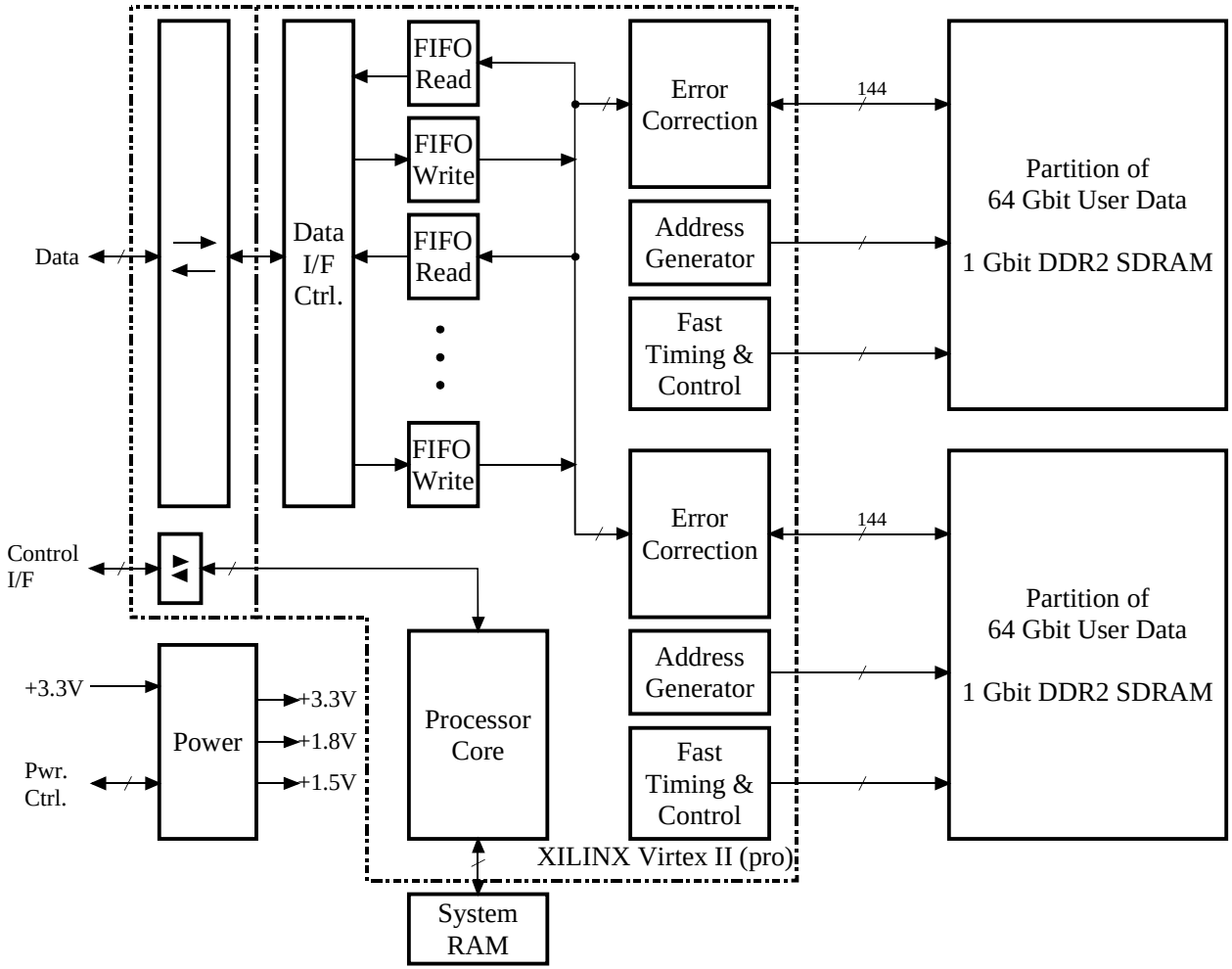
Conservative vs. Advanced Design

	Conservative Approach	Advanced Approach
Memory Type	DDR SDRAM	DDR2 SDRAM
Control Logic	Actel AX FPGA	XILINX Virtex II pro FPGA
Housing	TSOP / TQFP	BGA
Code Word Length	128 Bit net, 144 Bit gros	
Bus Width	72 Bit	144 Bit
Wordgroups	4 (2 per Partition)	8 (4 per Partition)
Capacity	64 GBit	128 GBit
Memory Channels	1	2 (1 per Partition)
Max. Internal Datarate	6 GBps	2 x 10 GBps
Max. DMA Channels	4 (2 write, 2 read)	8 (4 write, 4 read)
ext. I/F	partially configurable	configurable
File System Support	no	yes (Datarate < 4 GBit)

Block Diagram Conservative Design



Block Diagram Advanced Design



Recommendation

- **Conservative Design:**
  - may cover most near future applications on the cost of mission specific optimisation/adaptation
  - coverage period of future missions: 3 - 5 years from now
  - relies on conventional device packaging
- **Advanced Design:**
  - generic functionality and flexibility
  - supports wide range of applications with a single design:
    - up to very high data rates (several Gbit/s)
    - increased functionality (e.g. file system support on module)
  - coverage period of future missions: up to 5-8 years from now
  - needs qualification of BGA type packages

  => A module architecture study should investigate the features of an advanced design approach

Items to be studied (Example List)

- System Aspects:
  - Module functionality
  - Reliability
- Module Power:
  - Generation and Distribution of low voltage supply
  - Redesign of Power and Latch-Up Switches
- Data Interface:
  - Very High Data Rate Interfaces
  - Separate vs. integrated implementation (e.g. using XILINX Rocket I/O)
- Module Control:
  - Failure Tolerant Design within SRAM based FPGA
  - Implementation of File System Support functions

Components Radiation Testing

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Test coverage

- Test pattern & modes for the SEE tests are determined by device operation in application, i.e. the memory module
- We propose to focus on following aspects:

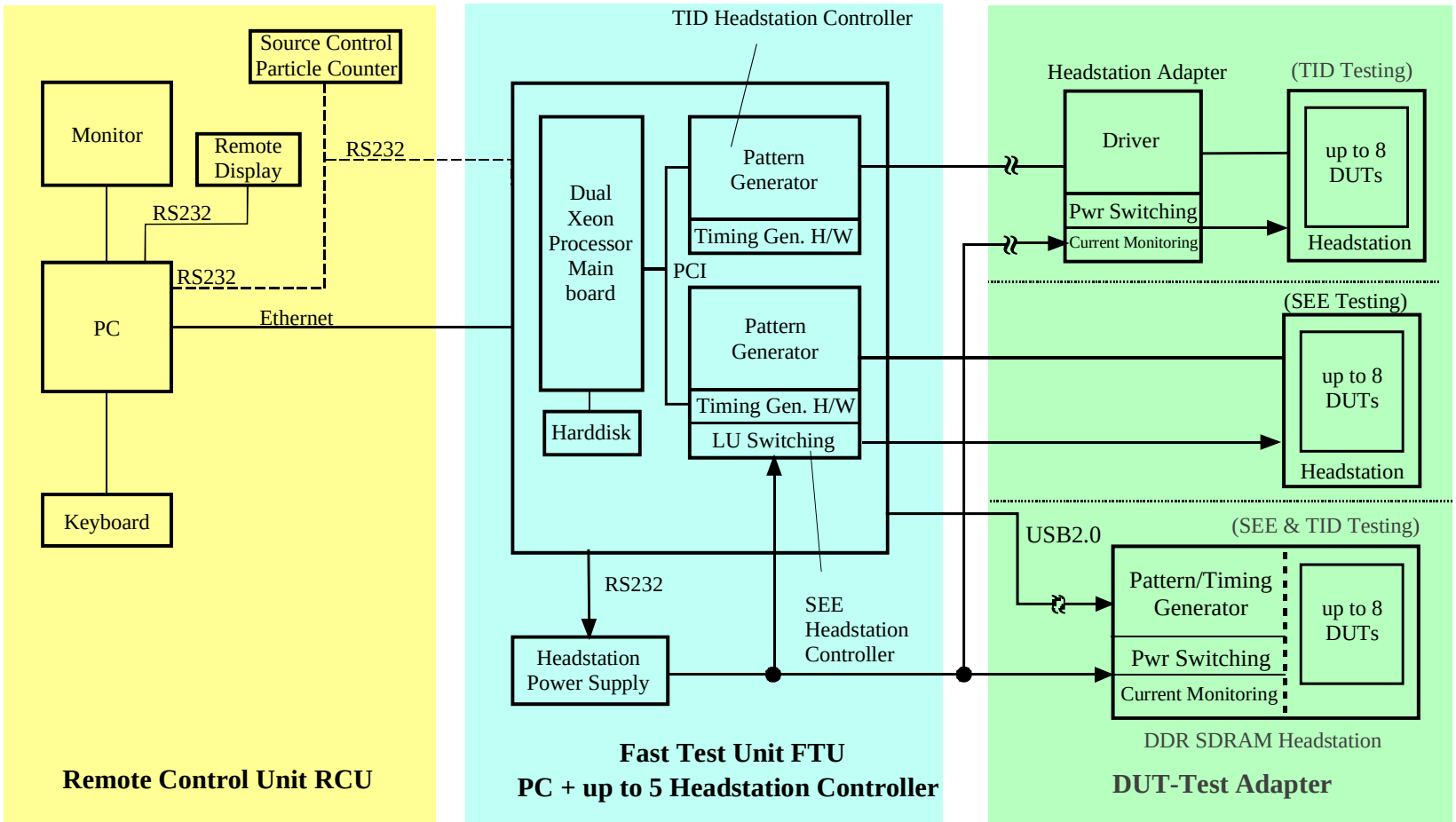
  - Test of Core Functions - Pattern: Marching covers
    - Bit Flips in Array
    - Address Errors

  - Test of Peripheral Functions
    - DLL Errors: covered by Read Background
    - Power up / down (covered by tbd.) (DDRII only)
    - Etc.

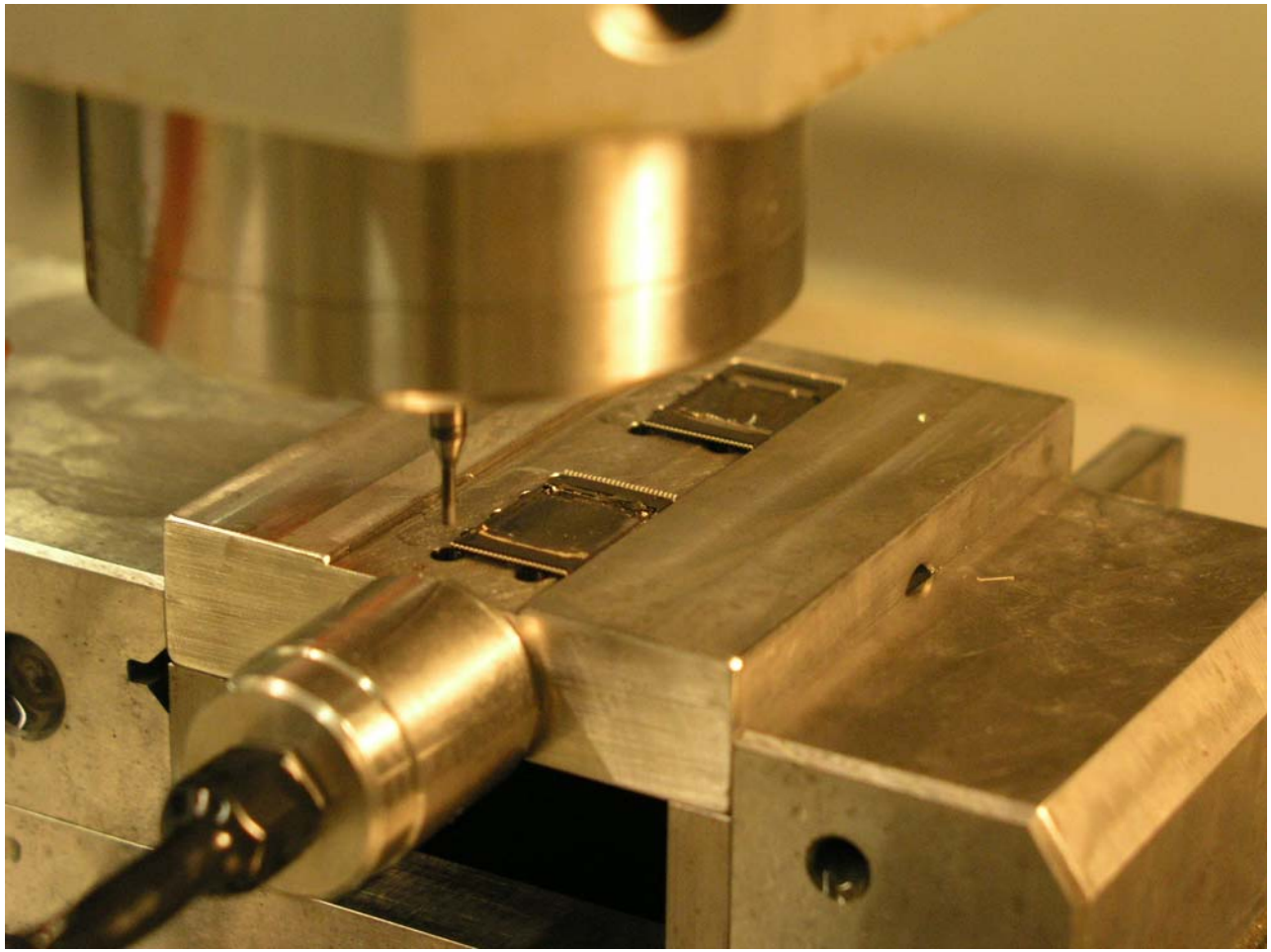
RTMC-3 Rad Test Bed

- Developed under ESTEC contract
- PC based system with special plug-in cards to implement real time functions (Fast Test Unit)
- Special Headstation for DDR SDRAM
- TID and SEE test capabilities and requirements achievable with the same basic equipment
- Adaptable device control and test patterns implemented in firmware within configurable high performance FPGA´s
- Remote control of in-situ tests supported via network
- Quick-Look data analysis to support in-situ tests

Block Diagram of In Situ Radiation Test Bed

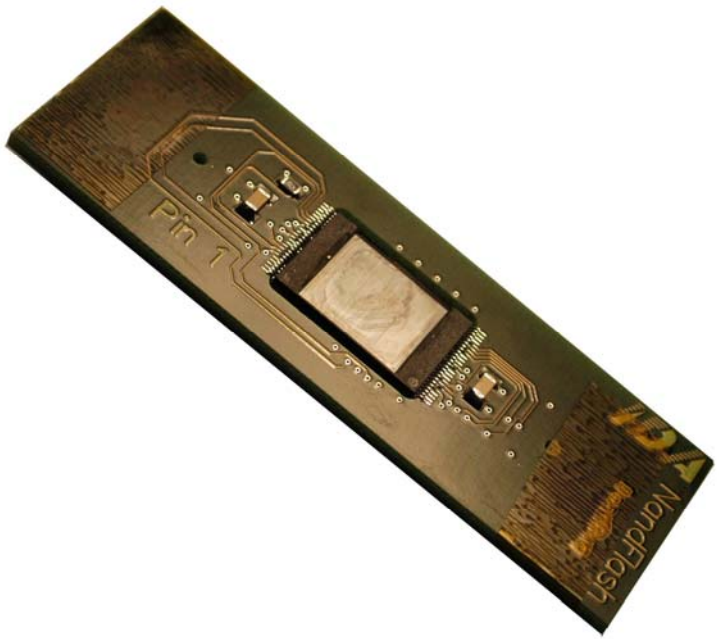


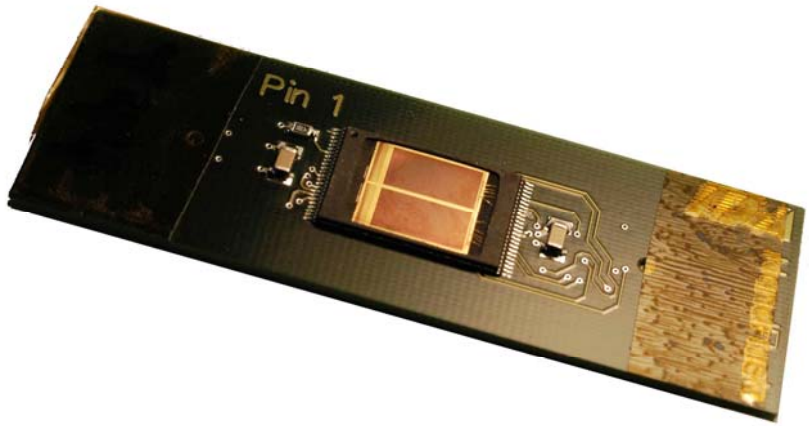
Backside opening



Open Devices

Backside Opened Device





Frontside Opened Device

Summary

- For a mid to long term coverage a new module architecture is needed:
  - Use of DDR2-SDRAM
  - SRAM based FPGA´s for control functions
  - File system support on module
  - Very high data rate serial interfaces
- A generic radiation test bed is available for device characterisation (Memory Devices DDR-1 and DDR-2, XILINX FPGA)