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ESTEC

13/03/06

Radiation Evaluation of DDR /DDR2 SDRAM Memories

# HIREX ENGINEERING

- Sample Preparation
- Memory Test System
- Radiation Testing (test conditions/bias/pattern/speed/temp

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G. Lewis

## Sample Preparation (1/16)

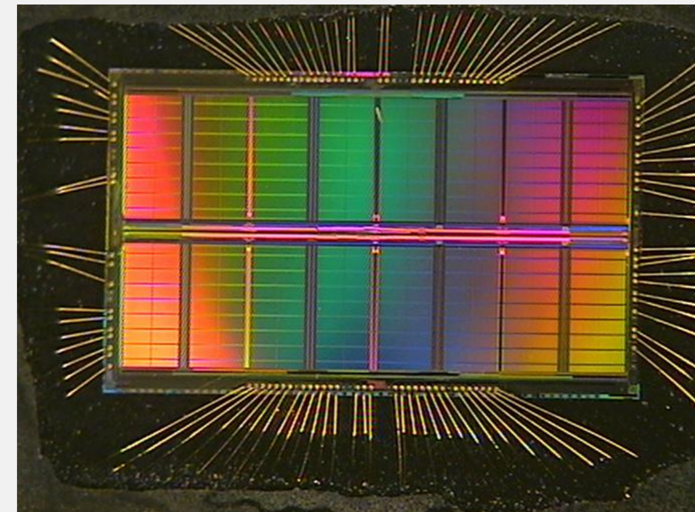


- Using Hirex Physical Analysis lab ressources (fully equipped for Construction Analysis, DPA, Failure analysis)
- Preparation of SDRAM memories for radiation testing:
  - Chemical etching (jet etcher)
  - Die thinning (ASAP1)
  - Third option: get the die out of the package and rebond it

# Sample Preparation

Jet etcher

Nitride and sulfuric acids



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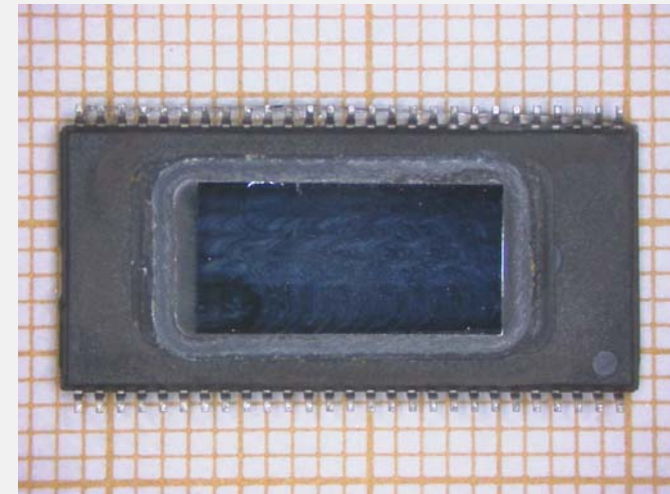
# Sample Preparation



ASAP-1

DIGIT CONCEPT



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# Sample Preparation

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# Sample Preparation





- Radiography
- Cross section to evaluate the die thickness
- Determine the dimensional parameters of the sample
- Set the sample in position on the Sample holder Plate
- Removing Material up to die attach exposure
- After removing die attach, measure the height of the silicon die (reference point) and adjust the tilt
- Stop silicon removal 25µm before the goal to integrate pre-polishing and polishing
- After optical polishing, control the final thickness of the die

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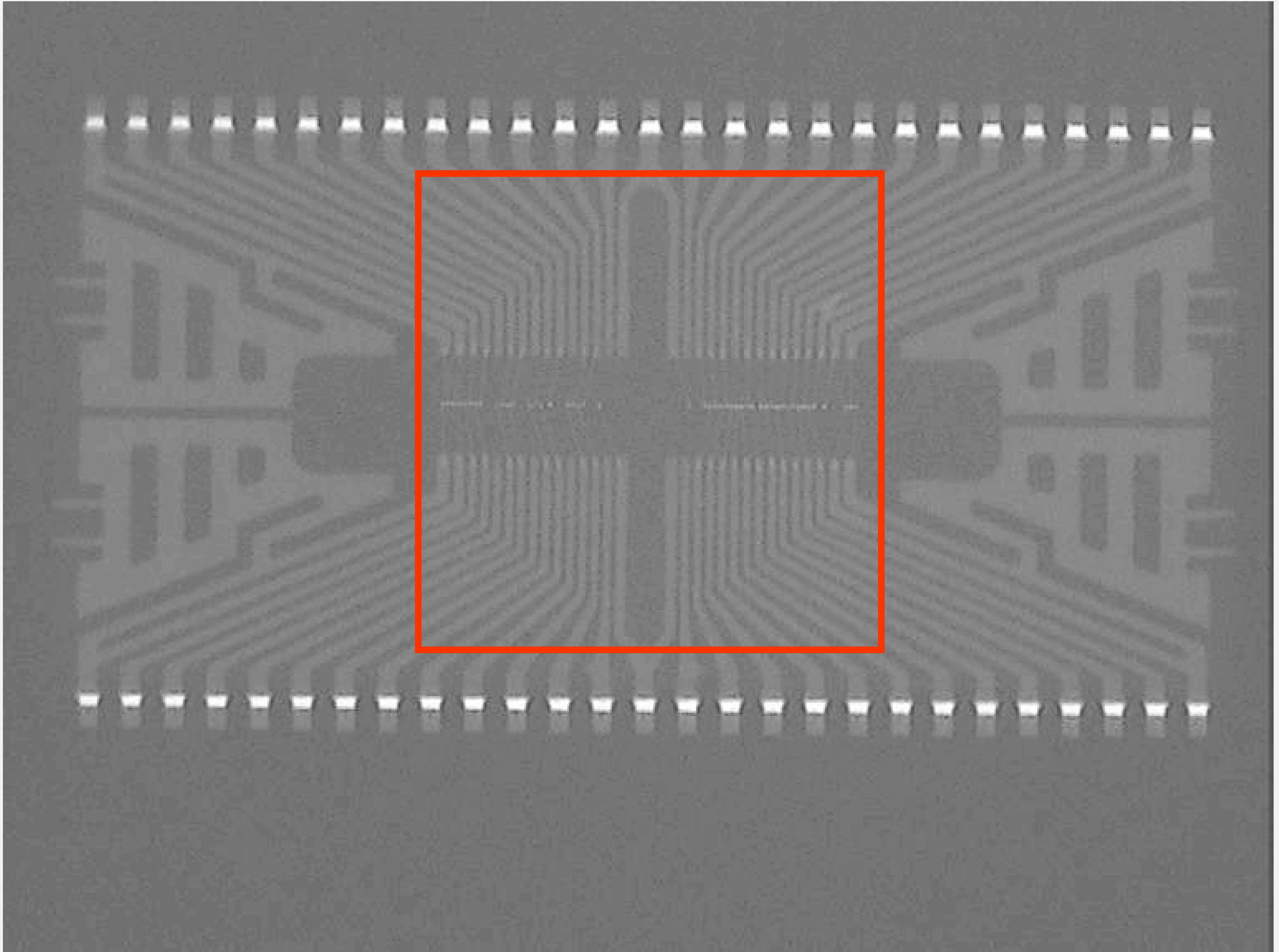
# Sample Preparation







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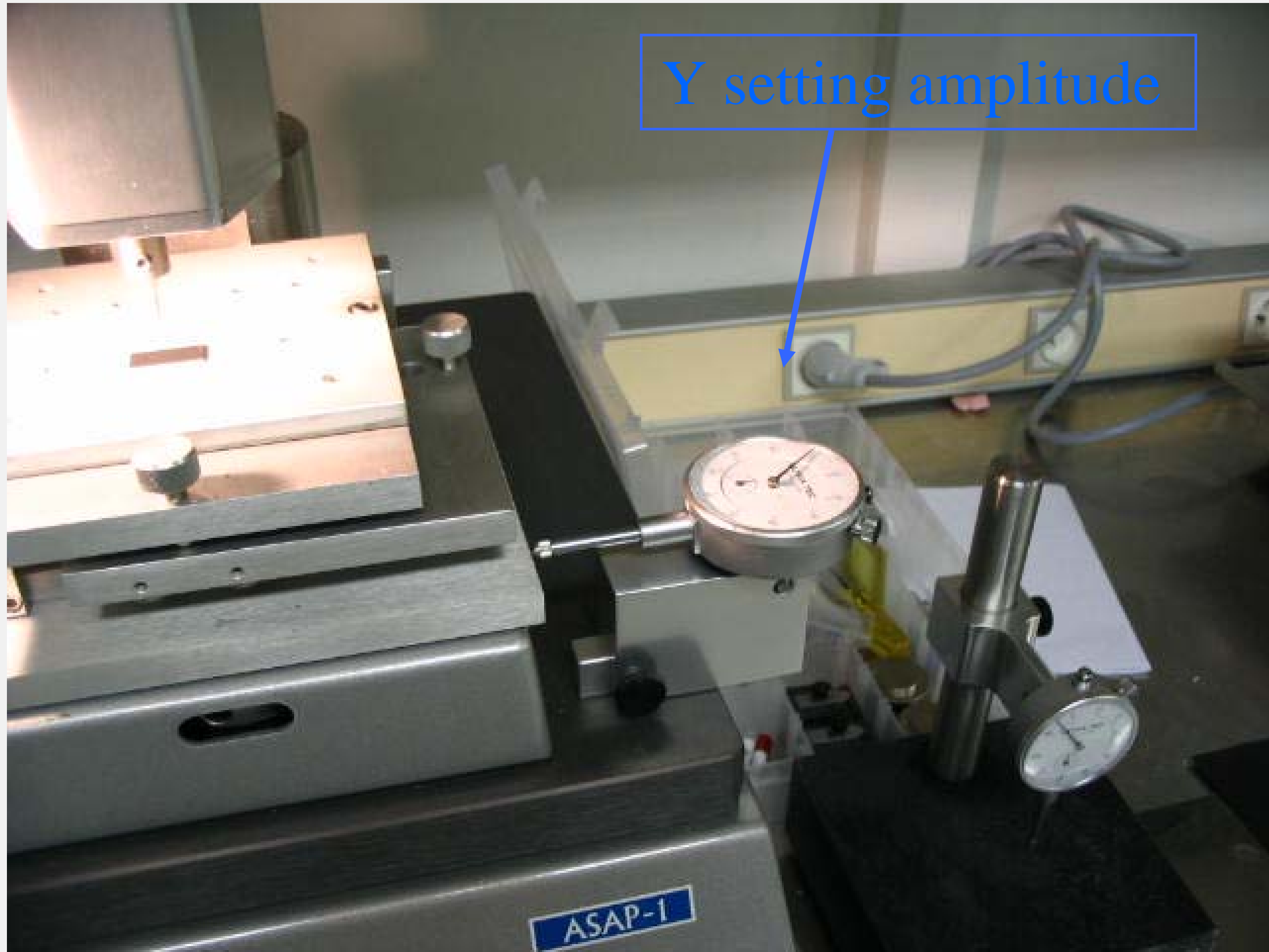
# Sample Preparation





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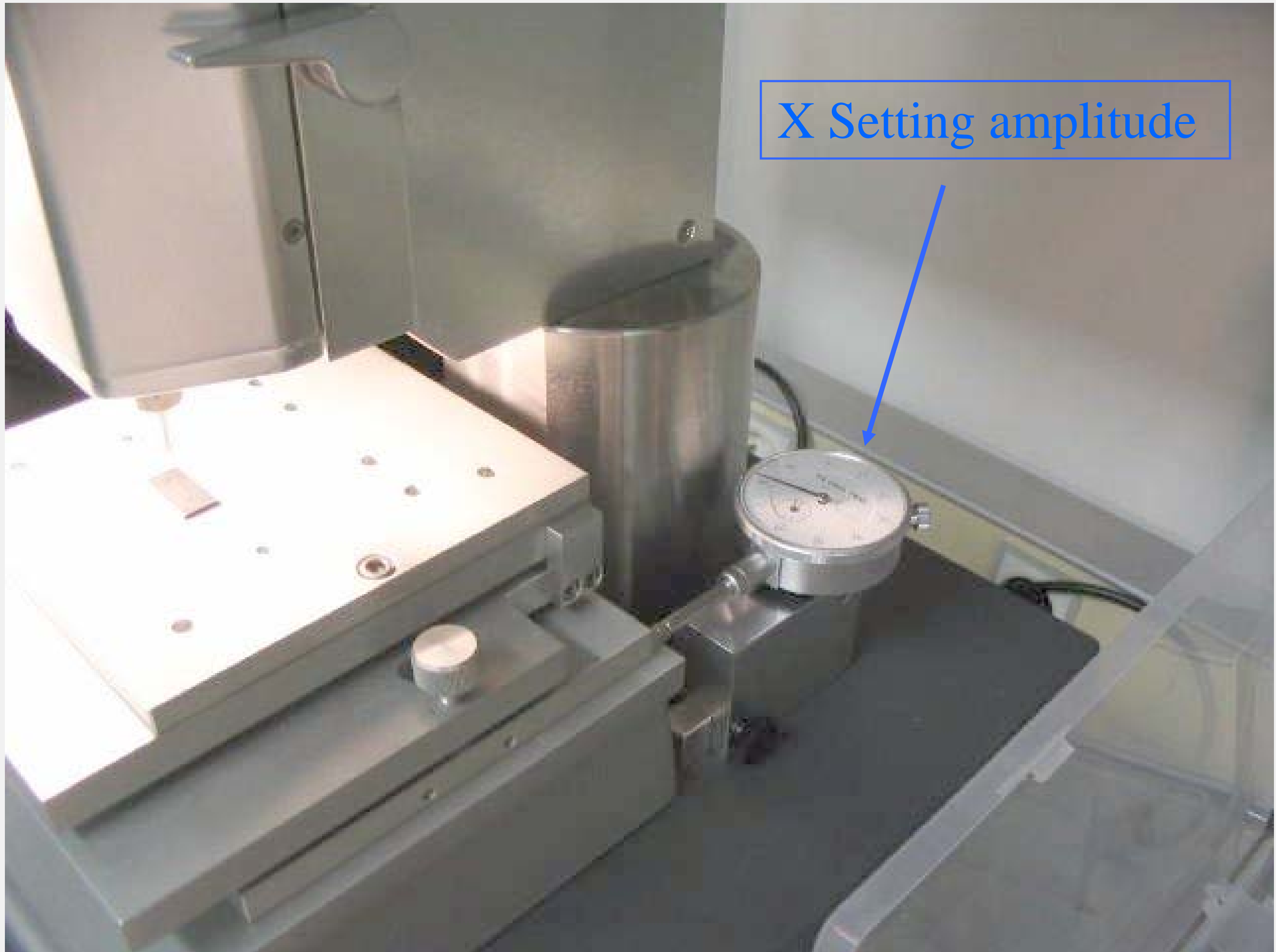
# Sample Preparation





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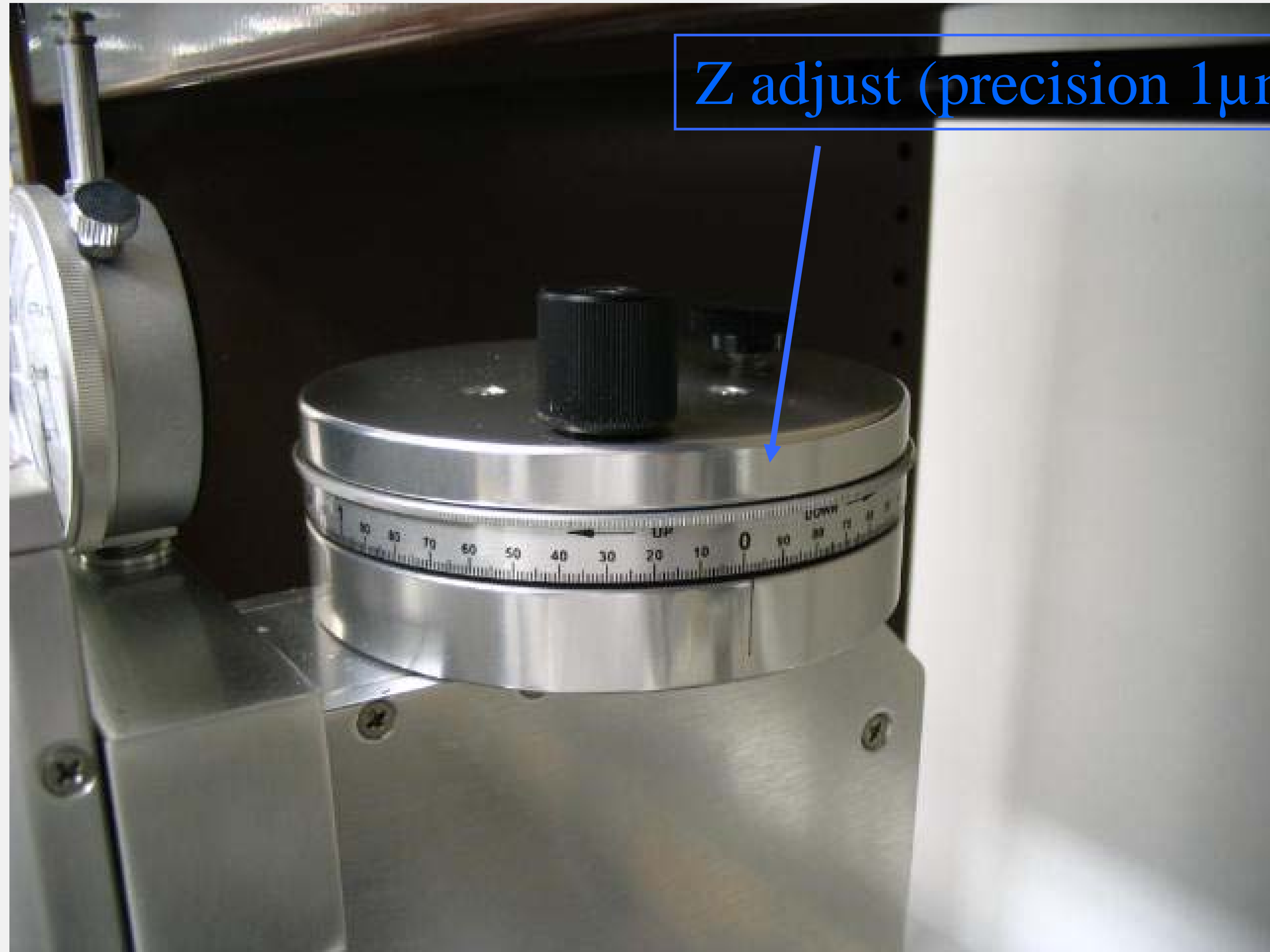
# Sample Preparation





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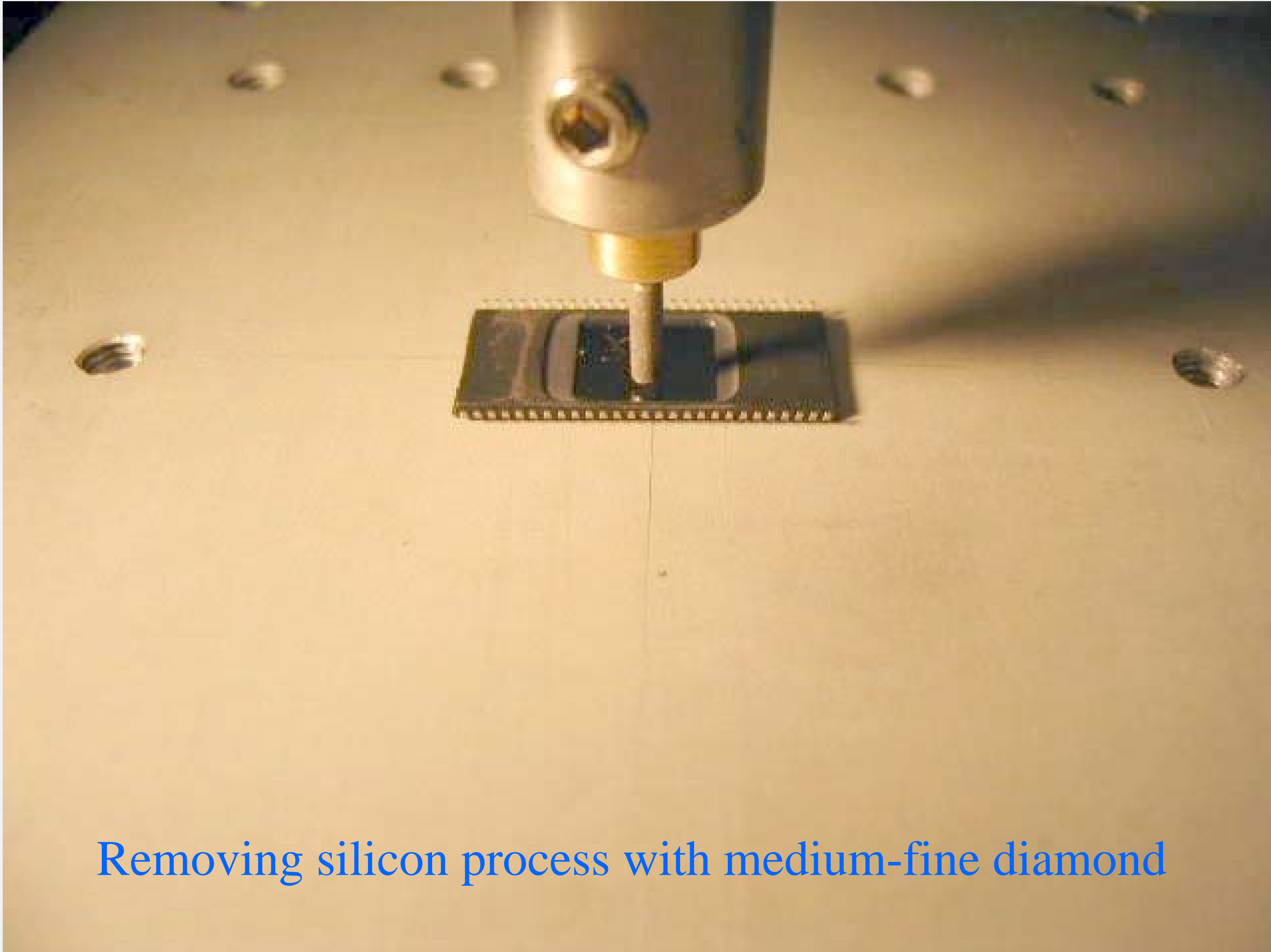
# Sample Preparation

Removal package process with coarse diamond tool

# Sample Preparation







Removing silicon process with medium-fine diamond

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# Sample Preparation

Pre-polishing with wood tool to remove scratches

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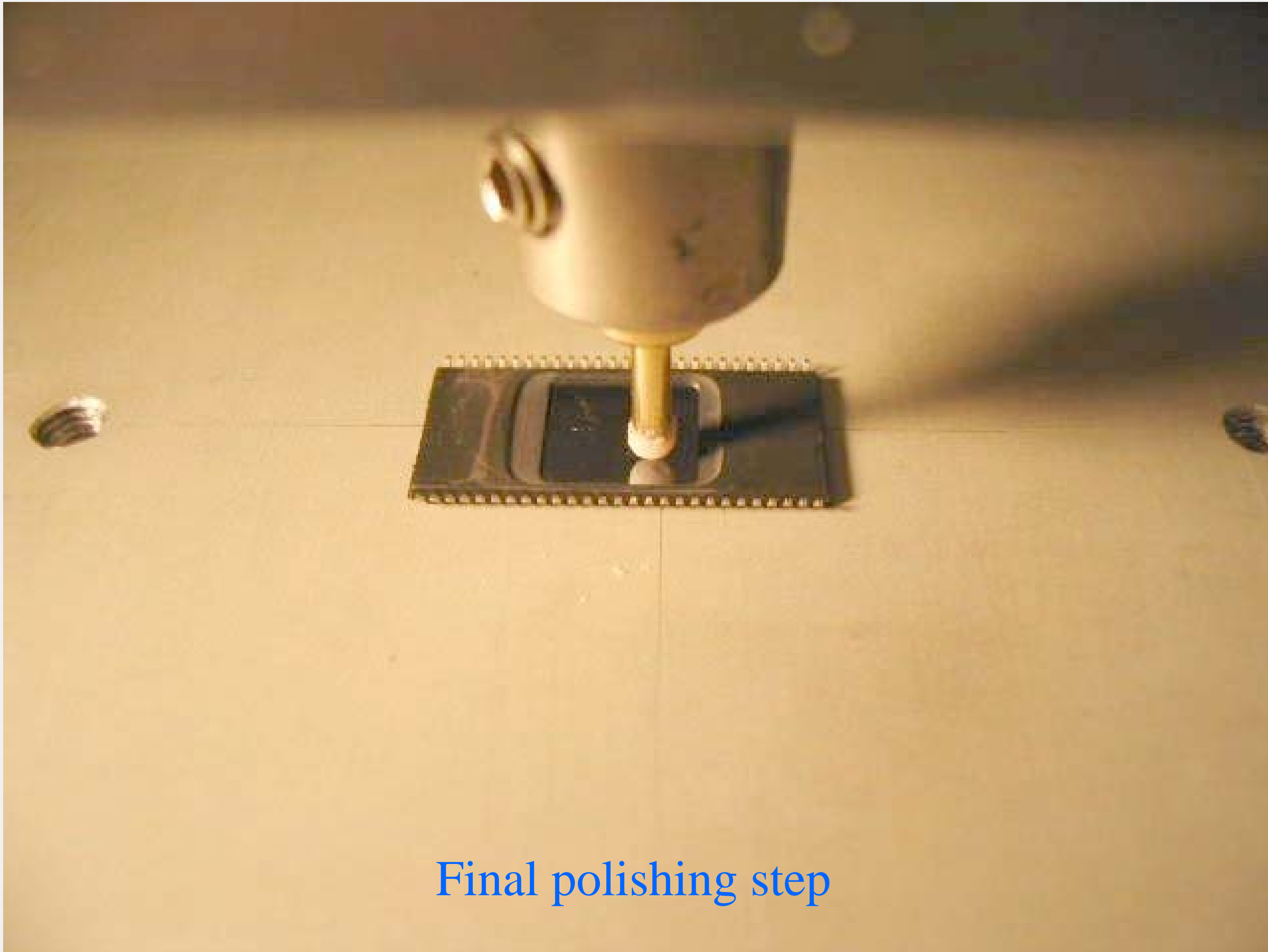
# Sample Preparation





Final polishing step

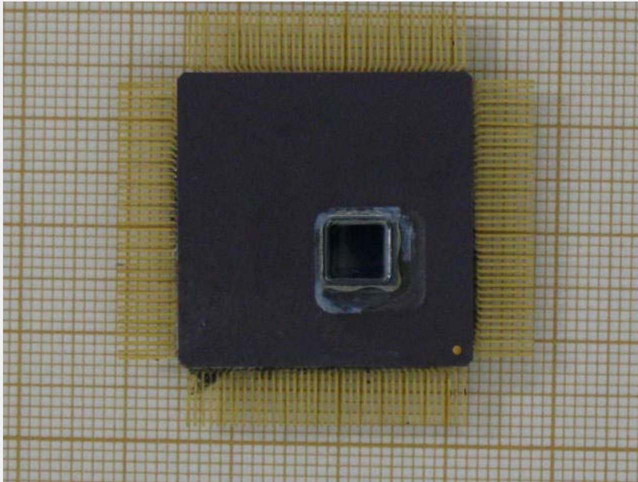
# Sample Preparation

Final control of die thickness

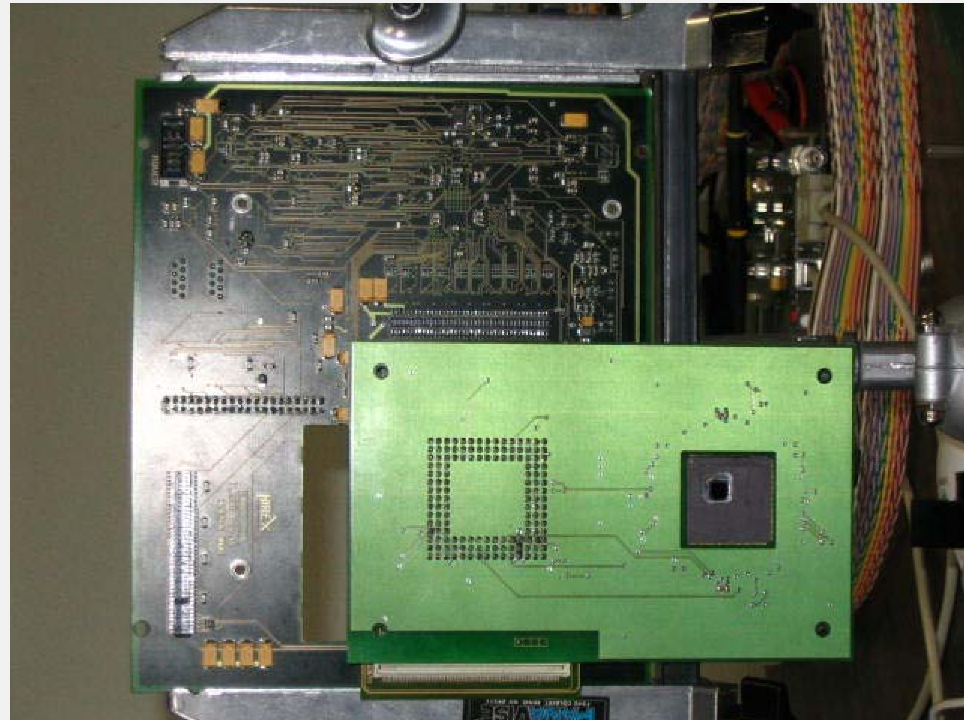
# Sample Preparation







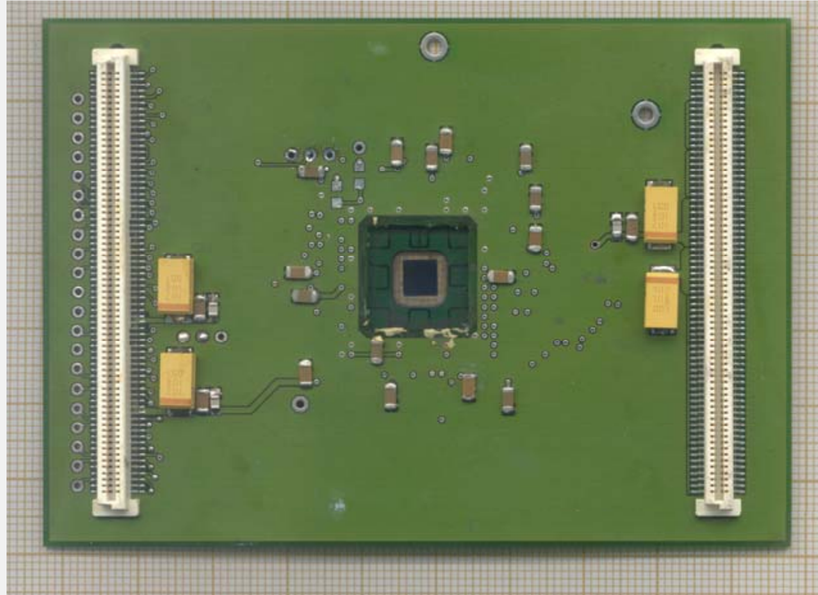
Partial die thinning (1/4 die) in a ceramic quad flat pack



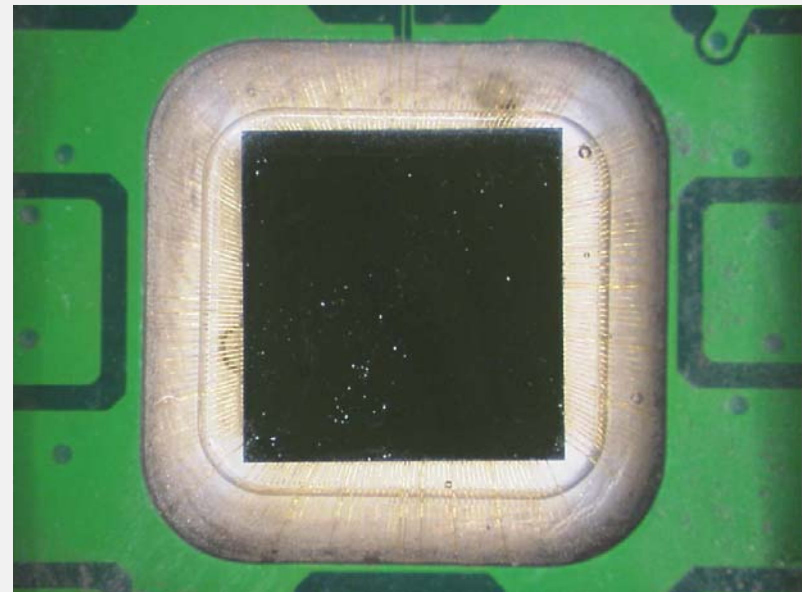
# Sample Preparation







Die thinning in a BGA package



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# Memory Test System





## SEE actual test system

- Compatible with most of the radiation test facilities (neutron, protons, heavy ions, alphas, laser)
- 120 I/Os up to 100MHz from 0.8V to 5V
- 4 supply up to ±5V/1A with latchup processing
- 16K SEU error records in memory (8M-bit RAM)
- Heating up to 125°C
- TCP/IP@10M network
- Robust hardware & software
- Fully remote configuration

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## TID actual test system

- Based on Digital Tester from Credence (Electra)
- Up to 200MHz Clock Frequency
- Will be used for SDRAM, DDR Functional & parametric testing
- Will be used in conjunction with SEE tester for DDR2 functional & parametric testing. Final configuration will be finalised depending upon performance of selected devices.

# Memory Test System



## SEE updated test system under development : 06/06

**Not a new test system, takes advantage of the modularity of Hirex existing memory test system**

- Basically, same architecture than the current version but incorporating a more powerful FPGA on beam test board
- Same test environment (board supervisor, data process and storage, Ethernet link with remote laptop,…)
- Improvements:
  - DDR2, QDR, RLDR interfaces blocks
  - operating frequency up to 267MHz for DDR2, 300MHz for QDR & RLDR
  - Increased number of DUT supplies with latchup processing

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## SEE H/W Configuration

1 SEE Test

- 1 Supervisor test board
- 1 SEE Beam test board
- 1 Device Interface Board
- 1 Laptop

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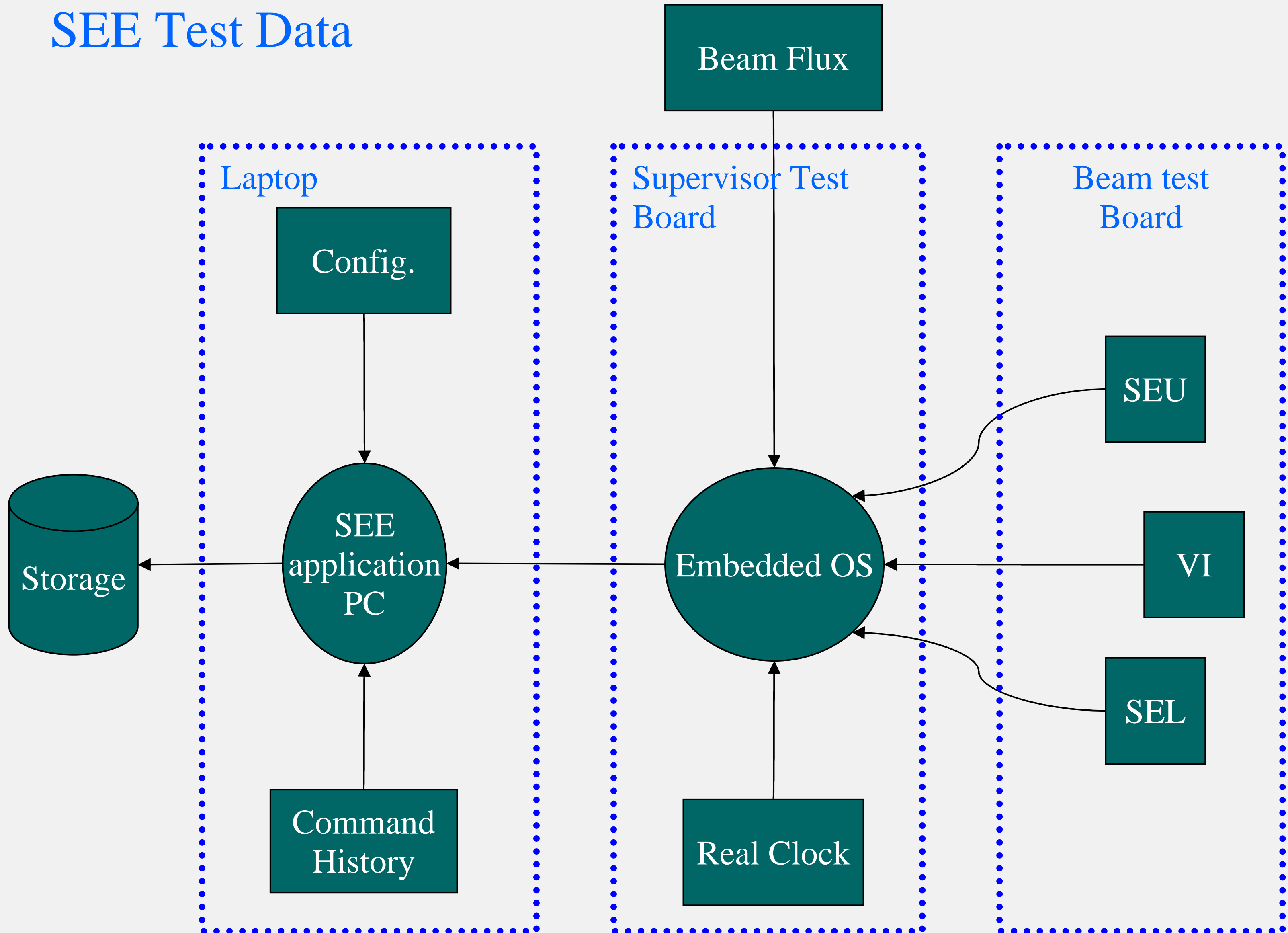
## SEE Test Data

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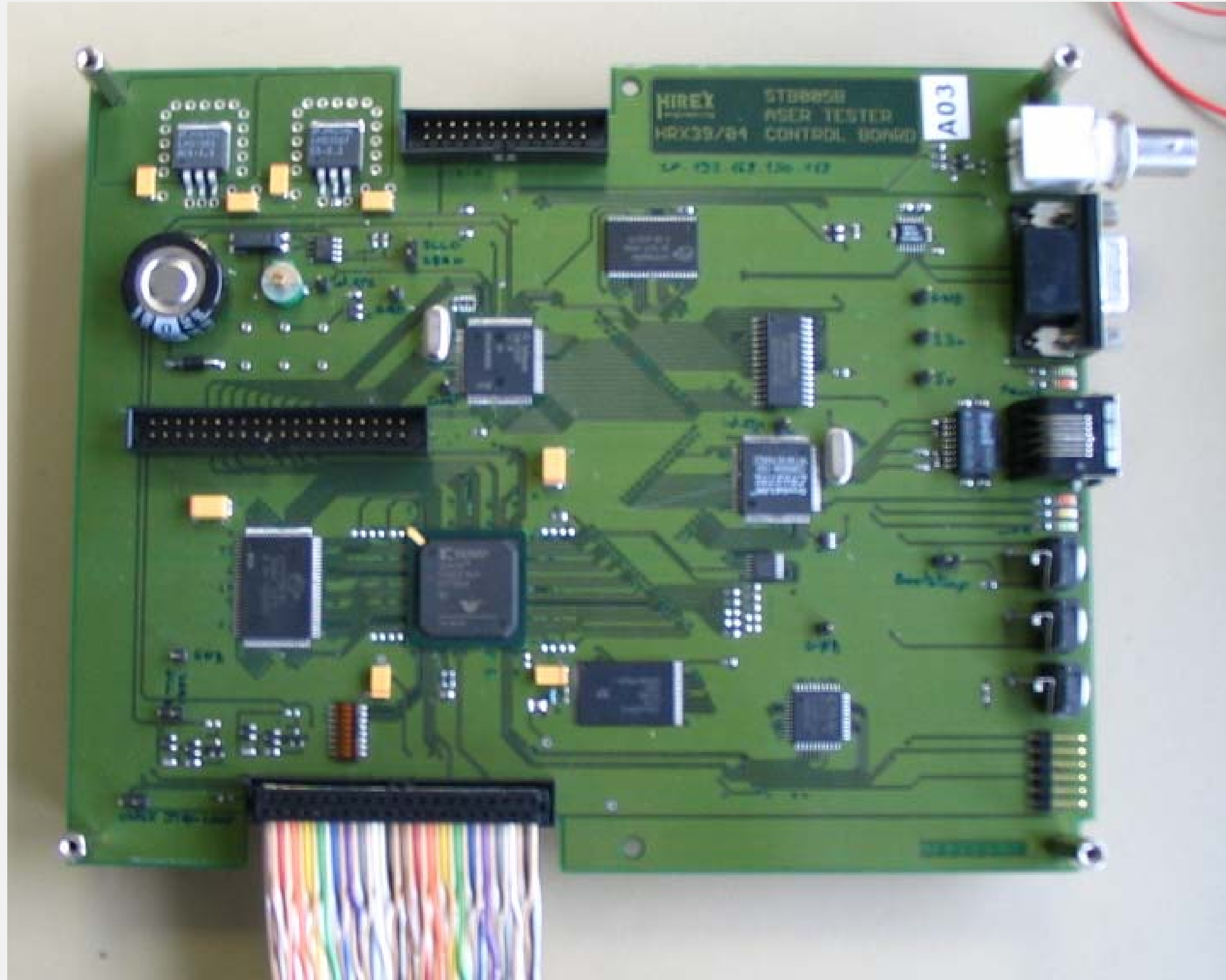
# Memory Test System





## SEE Supervisor Test Board

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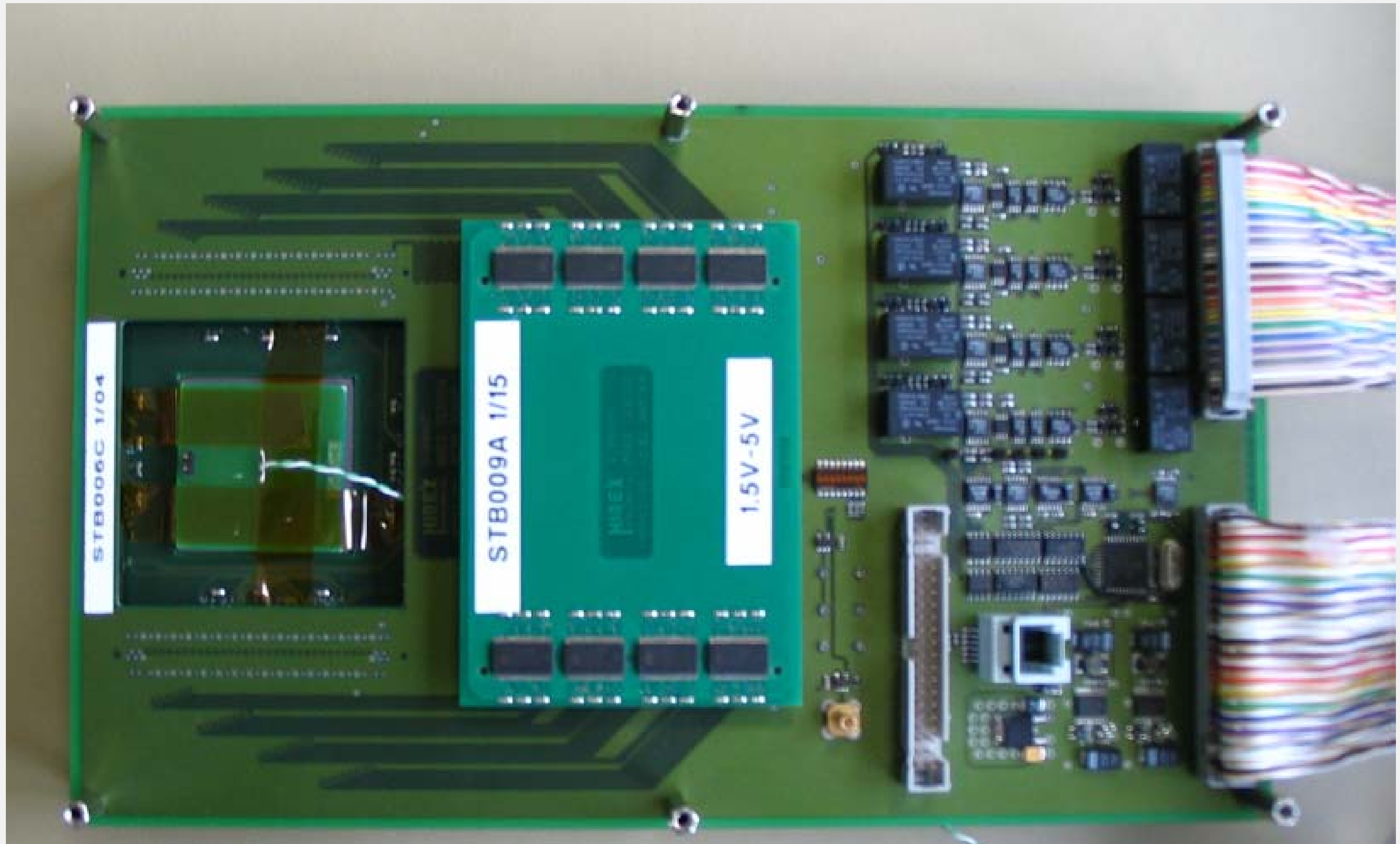
## SEE Beam test board

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## Proposed test configuration and planning

*SEE*

- SDRAM actual tester – development completed
- DDR actual tester – ready June 2006
- DDR2 updated tester – ready September 2006

*TID*

- SDRAM actual tester – currently ready
- DDR actual tester – ready June 2006
- DDR2 updated tester – ready September 2006

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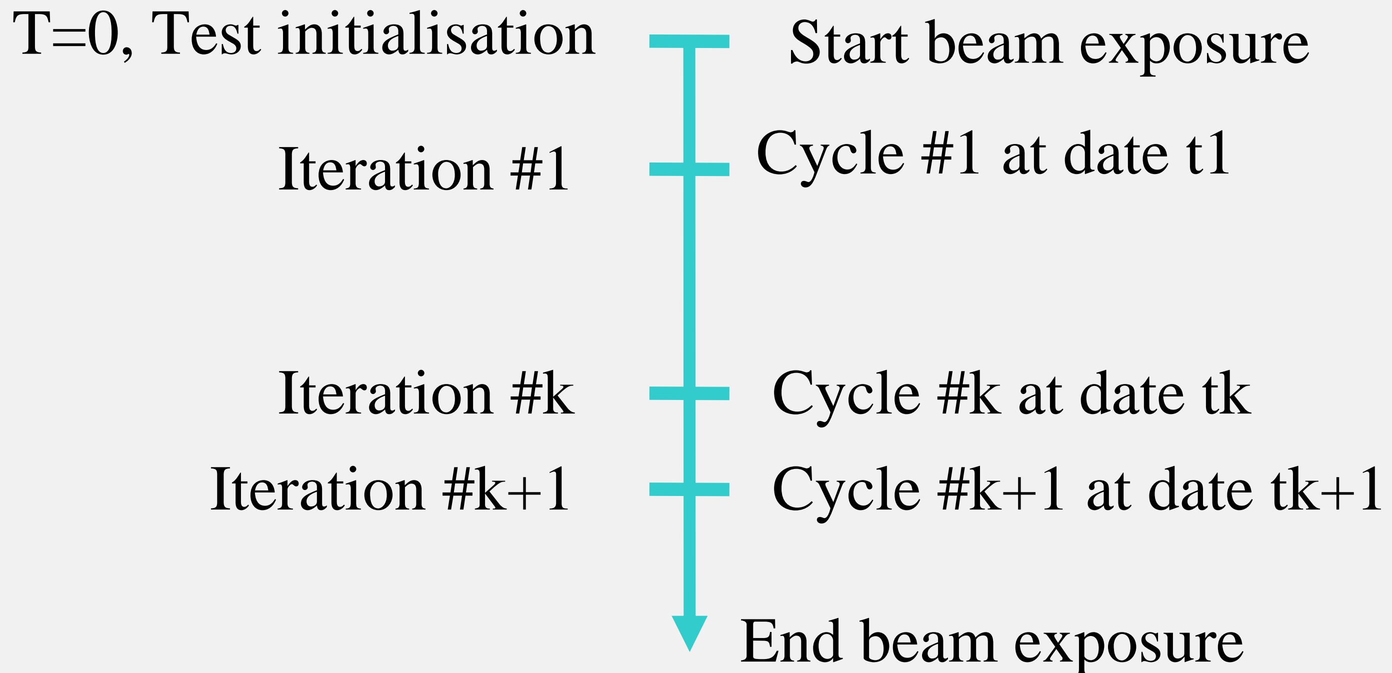
## What is a SEE test run ?

A run = 1 test configuration (DUT, Supply values, pattern, etc.)




Note: a common cycle is a write access, an iteration delay and a read/comparison access

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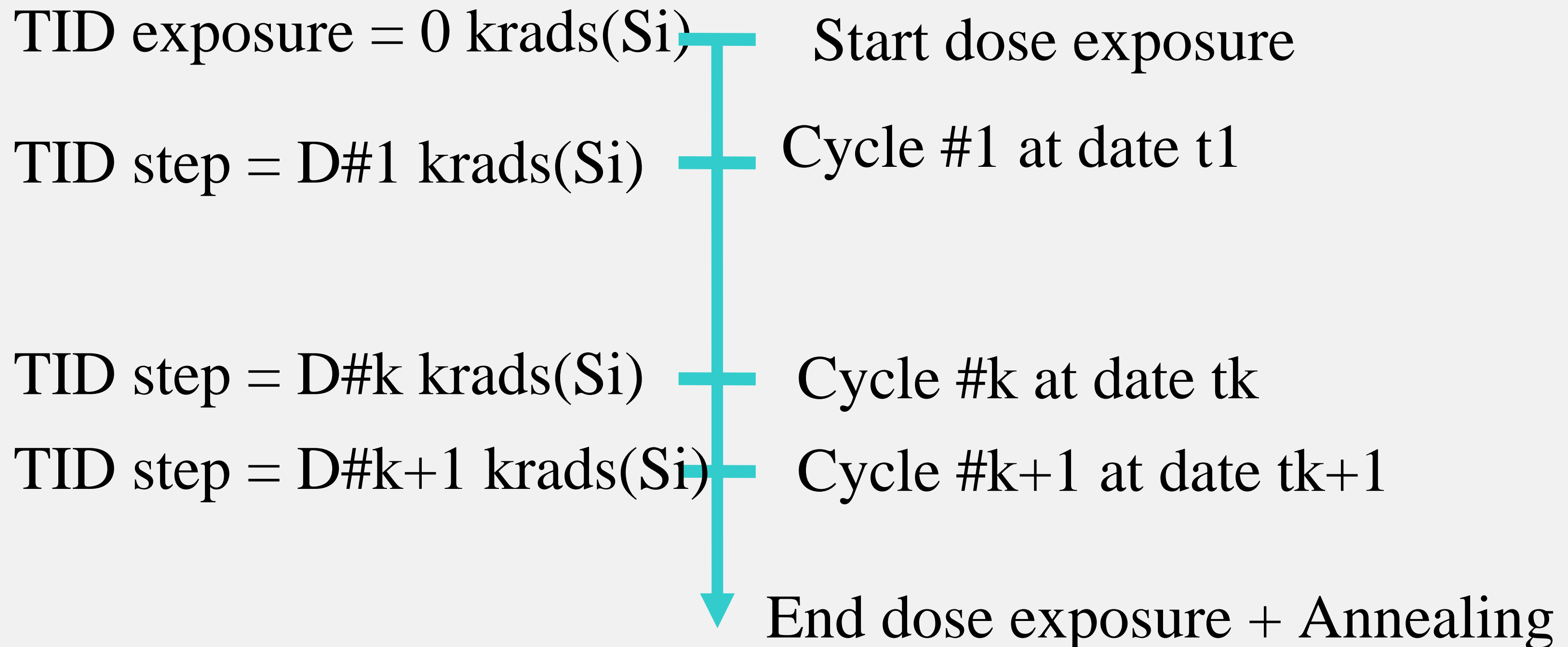
## What is a TID test campaign ?

A campaign = 1 test configuration (DUT, Supply values, bias during exposures and annealing, functionality & parameters to check, total dose and dose steps, etc.)




Note: a common cycle is a measurement of electrical parameters and functionality tests

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## Test conditions

- *SEE (Run Test Modes)*
  - Static (use of a shutter during write and read)

    Consecutive write from 1 to 4 banks

    Refreshing during iteration time (self or auto refresh)

    Consecutive read of selected banks

    Idem for the next iteration
  - Dynamic

    Consecutive Writes and Reads of a selected bank with a no iteration time
  - Others (according to customer needs)

    Read only, most of writes...

- *TID*
  - Self refresh during exposures and annealing

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## Potential Test Patterns

- *SEE*
  - ALL0
  - ALL1
  - Checkerboard, inverted Checkerboard each iteration and each burst access
  - Hirex "Moving" pattern
    - 14 sequential pattern values with the same weight of '0' and '1'
    - Enable to detect shifted data burst
- *TID*
  - ALL0
  - ALL1
  - Checkerboard, inverted Checkerboard

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## Functional Test Speed (Device Clock Frequency)

- *SEE*
  - SDRAM 25 MHz
  - DDR 85 MHz
  - DDR2 200MHz or 267MHz
- *TID*
  - SDRAM 100Mhz
  - DDR 100Mhz
  - DDR2 200MHz or 267MHz

*Note: Test frequency will be adjusted according to final selected devices.*

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## Test Bias

- *SEE*
  - Up to 4 independent DUT power supplies with dedicated SEL process
  - Record of the current and voltage values during the run for each supply channel.
  - DUT Power to the nominal voltages
  - If needed +/- 10%

- *TID*
  - Self refresh mode during exposures and annealing at nominal voltages.

## Temperature tests (Hirex common practice)

- *SEE*
  - Device Interface Board is designed with a hole below the DUT to adapt a small heating pad PCB
    - Use of a SMD resistor + a thermocouple probe
  - Temperature regulator (up to 125°C)
  - Not applicable on BGA packages

- *TID :* not applicable

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# Radiation Testing





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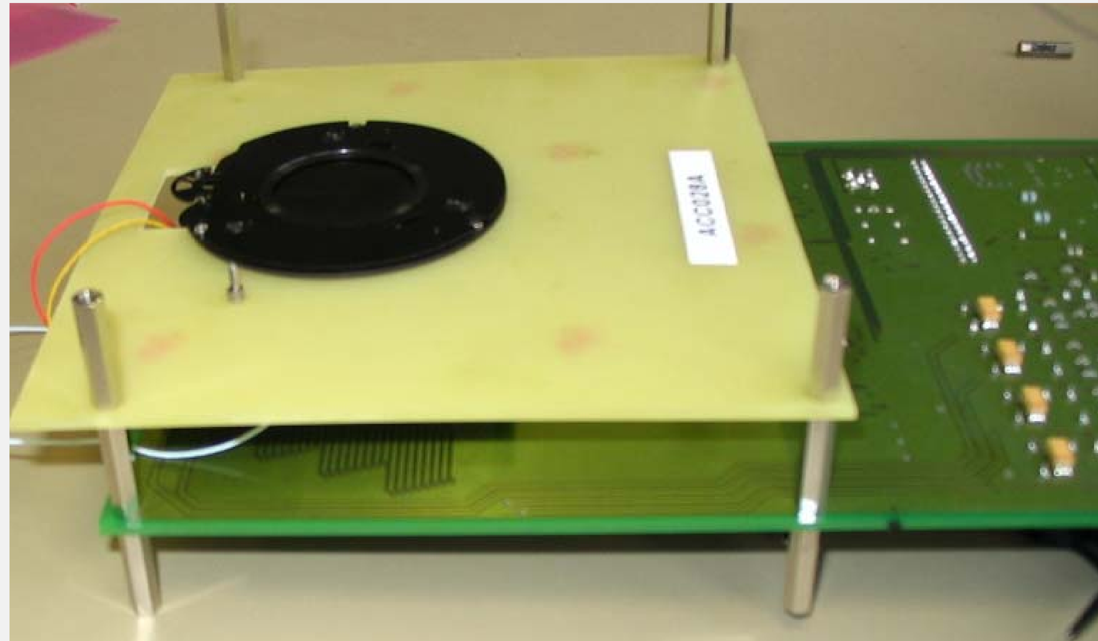
Protections against entering into an unknown state (only heavy ions)

- Use of a shutter for static tests during Write and Read (automatically controlled)



→ Physical protection

## Protections against entering into an unknown state (only SEE)

- Detection of unknown state during read
  - Reload of the registers
  - Reread of the memory without rewriting it
    - Count a Soft SEFI → if unknown state can be recovered by software
    - Or count a Hard SEFI → if unknown state can only be recovered by power off the DUT (automatic power OFF and re-power ON)

Note: If DDR devices are powered off, stored data will be lost.

→ Software protection

## Detected error types

- *SEE*
  - SEU: Single Bit error
  - MCU: Multi Cell Error (scrambling info needed)
  - Row/Column error
  - Burst Error
  - Read errors, Write errors, Cell errors
  - Soft SEFI (registers modification)
  - Hard SEFI (when power off is needed)
  - SEL
- *TID*
  - Parameters drift
  - Functionality error

# SEE real time data analysis

- Cumulated SEU errors count
- Cumulated SEFI (Hard and Soft) errors counts
- Cumulated SEL errors counts for each DUT supply
- Voltage and current graphs for each supply
- Error mapping (if descrambling is provided)

- SEU cross section graphs versus LET

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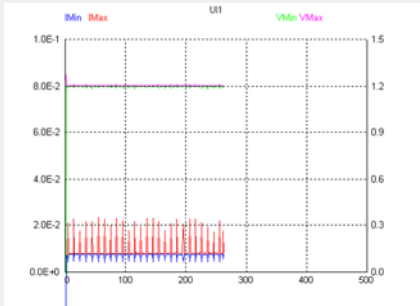
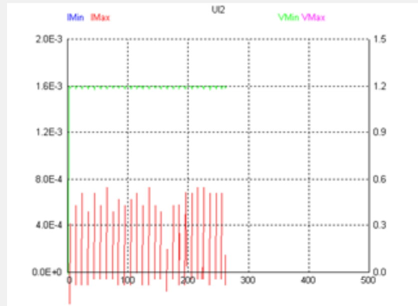
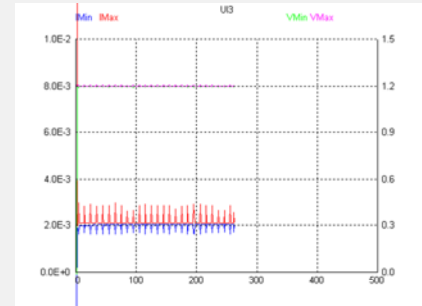
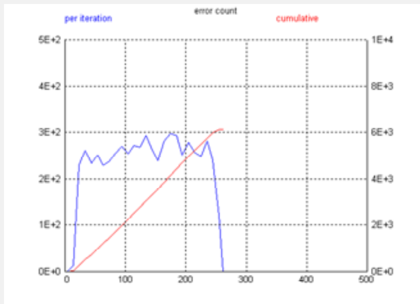
# Test Report

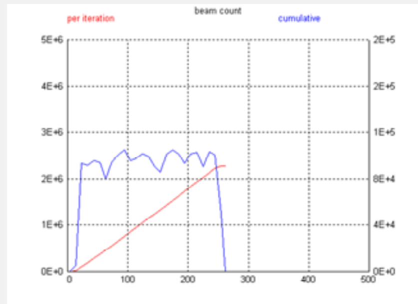
## •*SEE*

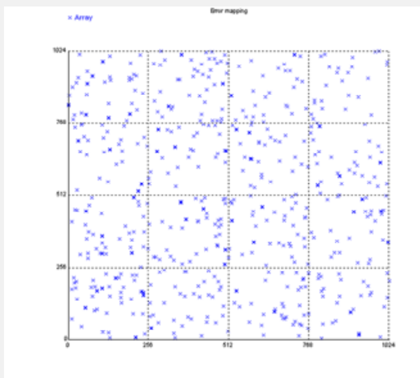


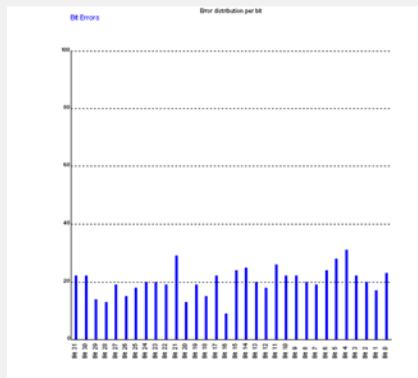



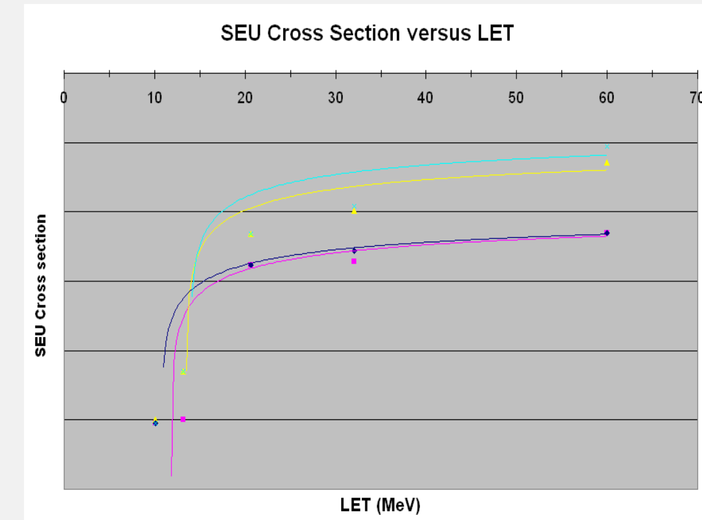








- Real-time analysis
- Results database

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