Non-Volatile Flash Memory Module SafeGuard Data Recorder

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Why Non-Volatile Mass Memories?

- **Benefits:**
  - Non-Volatile ⇨ Data immune against Power Breakdowns
    ⇨ Power Savings
    ⇨ SEFI / SEL recovery without data loss in contrast to SRAMs / DRAMs
  - Densest Mem. Techn. available ⇨ High Capacity (NAND)

- **This can be exploited to enhance and to optimize Missions with strong requirements with respect to**
  - Autonomy (Deep Space)
  - Complex Mission Modes (Operational Scenarios)
  - Long term or frequent Power Off Phases during the Mission
  - Low Power Requirements (Smart S/C, Outer Solar Systems)
  - Storage of Mission Critical Data, Emergency Commands, SW Patches
  - Sparse download / upload Capabilities
  - etc.

SafeGuard Data Recorder

- **Main Design Drivers:**
  - Non-Volatility combined with Robustness of semiconductor Storage Devices
  - Excellent Data Integrity after Long Term Storage

- **Tentative Technical Features:**
  - Pure NAND Flash Memory Core
  - Safe with Respect to Power-Outages
  - Multiple Orthogonal RS Error Correction grants high Data Integrity in harsh Radiation Environment
  - File Management including Management of Circular Buffers
  - Interfaces compliant to HICDS

  - Capacity: 4 GByte per Module
  - Write Performance: 6 MByte/s
  - Read Performance: 25 MByte/s
  - Data Integrity: < 1 Error / 1 MByte / 10 years without refresh

SGDR Non-Volatile Storage Technology

- **Preferred Technology: Flash EEPROM NAND Type**
  - (+) Widely used commercial Technology
  - (+) Intrinsic Non-Volatility by Technology
  - (+) Large Storage Density (up to 2 Gbit per Device)
  - (+) Heavy Ion SEE Tests of 1 Gbit Devices delivered encouraging Results
  - (+) Data Retention up to 10 Years, extendable by Refresh
  - (+) Performance tailored to a wide Spectrum of Applications

  - (-) Moderate Data Input Rate 1 MByte/s/dev
  - (-) Endurance limited to approximately 10^6 Write Cycles, can be extended by Wear Levelling

Failure Effects and Countermeasures

Error / Failure Modes:	Corrective Measures:
Distributed single Byte Errors in retrieved Page Data	Flow Through Orthogonal RS Error Correction (uninterrupted Data Flow)
Bulk Errors in retrieved Page Data, Write Verification Errors, Block Errors, SEFIs, Device Failures	Access Repetition, If Error persists: Device Interrupt and / or Power Cycling, If Error still persists: Move corrected Page to another uncontaminated Page, Write to another Page, etc.
Endurance	Wear Levelling
Data Retention	Scrubbing Move corrected Page / Block
Latch Up	Current Monitoring Power Cycling

All Errors / Failure Modes can be detected and coped by dedicated Countermeasures!
To minimize SEFIs the Flash Devices are powered only during Access Periods.

Device Level: Open Issues

- **Final Evaluation of the Heavy Ion SEE Test Results nearly completed.**
- **Preliminary Summary of the SEE Test Results available in SGDR Phase 1 Final Report (SGDR-RP-7001)**
- **Open Issues resulting from Phase 1 SEE Tests:**
  - Power cycling after erase is an effective countermeasure against (all?) persistent device failures and SEFIs. But this statement is based on only a few devices tested up to now. Therefore additional attention will be given to this topic in the next tests with new devices.
  - Discrepancy between the storage mode cross section values gained by low penetration beam tests and by high penetration beam tests. A repetition of the low penetration beam tests is regarded to be the next reasonable step for disclosing this discrepancy.
  - Data retention and endurance behaviour of Flash devices under radiation could not be investigated up to now.

SGDR Phase 1 Activities

- **Performed Tasks**
  - Storage Technology Evaluation
  - Heavy Ion SEE Tests
  - System Analysis
  - Data Integrity Analysis
  - Elaboration of Provisions to enhance Data Integrity
  - Requirement Specification
- **Results are summarized in SGDR Phase 1 Final Report (SGDR-RP-7001)**

SGDR Phase 2 Activities

- **Next Tasks**
  - Phase 2 Radiation Tests
    - Open Issues from SEE Phase 1 Tests
    - Proton Tests
    - TID Tests
  - Architectural SGDR Design
  - Operations and Functions
  - Detailed Module Design
  - MAIT of EM Module

- **Goal**
  - SGDR EM Memory Module available End of 2006