 HIREL EXPERTISE <b>HIREX</b> ENGINEERING a Tecnologica company	<b>COMPTE RENDU de REUNION</b>  <b>MINUTES of MEETING</b>		Ref. : <b>HRX/MOM/0087</b>		
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Objet / Purpose		Kick-off meeting, COO-019 radiation evaluation of DDR/DDRII SDRAM			
Place : ESTEC, Noordwijk, NL – Room Aj-021					
Participants Attendees	Société Company	Signature Signature	Participants Attendees	Société Company	Signature Signature
R. Harboe Sorensen	ESA/ESTEC		F. J. Rombeck	EADS Astrium	
P. Roos	ESA/ESTEC		M. Stähle	EADS Astrium	
T. Paulsen	ESA/ESTEC		H. Michalik	IDA	
S. Landstrom	ESA/ESTEC		T. Fichna	IDA	
F. Martinez Martin	ESA/ESTEC		F. Gliem	IDA	
A. Fernandez-Leon	ESA/ESTEC		M. Brüggemann	IDA	
L. Tunesi	ESA/ESTEC		F. X. Guerre	Hirex	
M. Suess	ESA/ESTEC		G. Lewis	Hirex	
Rédacteur / Written by :			F. X. Guerre		
Conclusion : Agenda see 1 <sup>st</sup> presentation.  Activity start : 13.03.2006  Progress meeting at ESTEC : mid September 2006  Meeting presentations: <a href="https://escies.org/public/radiation/esa/">https://escies.org/public/radiation/esa/</a>					
Actions Principales / Main Actions :					
Distribution :		Nom Name	Société Company	Nom Name	Société Company
Participants / Attendees +					

Welcome and introduction ESA/ESTEC

Mass Memory Products for Space applications EADS Astrium

Present status of Solid Mass Memories and near future needs

Twofold:

High speed 2 to 6 GBPS

High capacity 1.2 Terabytes (Terrasat)

Additional functions:

Data compression

Data encryption

See slides for the list of identified programmes

Advantage of DDR2 10mW in power down mode

Memory procurement aspects:

512Mbit SDRAM (stocks available at EADS to cover tbd programmes)

DDR production until 2006

DDR2 production until 2010/12

Aspects of future memory module architecture IDA (EADS Astrium contract)

Memory controller used in Terrasat modules: Antifuse ACTEL FPGA

Need to move to SRAM based FPGA (pin count and gate capacity)

Advanced module under development:

Xilinx VIRTEX2 PRO

144bit bus width

No drivers anymore (FPGA -> memories)

Radiation Test Bed (memory tester) and Radiation Testing IDA

DDR test head under development (for both TID and SEE), based around FPGA solution

Use of Marching test pattern

Should take care of DUT DLL errors

Main concern is SEFI, how to characterize and how to overcome

IDA states that they will perform the sample preparations for their needs

General discussion about power distribution for these memory units:


Which chip set

How to characterize to SEE environment

How to deal with SEL sensitive devices (up to now, policy was not to use them)

SEL protection (must react in microseconds and not milliseconds)

Impact on reliability

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<p><u>Hirex Engineering presentation</u>                      <u>see slides</u></p> <p>Sample preparations</p> <p>Memory Test System</p> <p>Radiation Testing</p>			
<p><u>Test facilities</u>    <u>ESA/ESTEC</u></p> <p>ESA will provide the necessary beam time at HIF, PIF and RADEF for both heavy ions and protons characterizations</p> <p>ESA makes available the CO60 ESTEC source facility.</p> <p>As an alternative, ESA fully accepts the use of ONERA CO60 source by Hirex.</p>			
<p><u>Test Samples/Test Conditions</u>                      <u>ESA/ESTEC</u></p> <p>EADS Astrium states that they have no contract for delivering test samples for this work</p> <p>EADS Astrium already procured 25 samples/lots, 2 years ago, of SDRAM/DDR and provided 5 samples per lot to Hirex for evaluating what was needed for sample preparation</p> <p>EADS Astrium reports that Infineon is willing to provide specific test samples compatible with heavy ion testing but this should have a cost.</p> <p>EADS Astrium agrees to approach Infineon to evaluate the conditions.</p> <p>It is proposed to start with the parts already delivered.</p> <p>However the concern is that these samples would be no more representative of what we could get now</p> <p>Action is then to identify what can be procured now</p>			
<p><u>Radiation Test Plan/Time Frame</u>                      <u>ESA/ESTEC</u></p> <p>See slides.</p> <p>Basically 1 year work program starting from 13/03/06 (Kick-off meeting)</p> <p>ESA requests a monthly progress report on this activity</p> <p>ESA foresees to organise a progress meeting in six months time</p>			
<p><u>Support Activities</u>    <u>ESA/ESTEC</u></p> <p>See slide</p>			
<p><u>Other Mass Memory related activities (Flash)</u>                      <u>EADS Astrium</u></p> <p>See slides</p> <p>Presentation of SGDR : Safe Guard Data Recorder</p> <p>Non volatile Flash memory</p> <p>4Gigabytes per module</p> <p>1error /Megabyte/10 years refresh</p> <p>1Mbyte/device/s</p>			



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Project Presentations

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General discussion about how to procure memory devices for a space program

Evaluate 1 die revision

Negotiate with manufacturer 1 lot (1 site, 1 diffusion lot,...)

Lot up-screening (temperature range)

Other:

CNES activity on DDR memories

information should be provided during radiation workgroup meeting (on 14/03/06 at ESTEC)