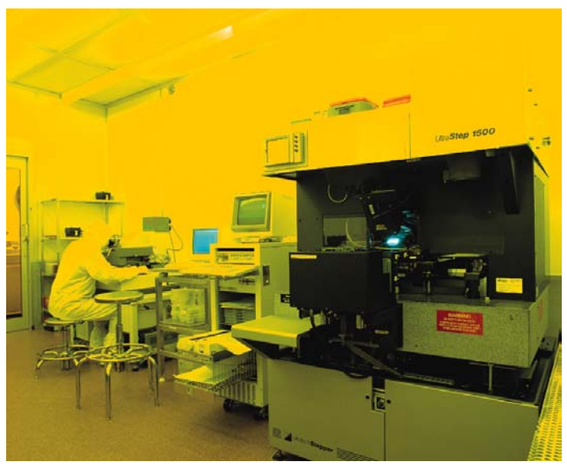
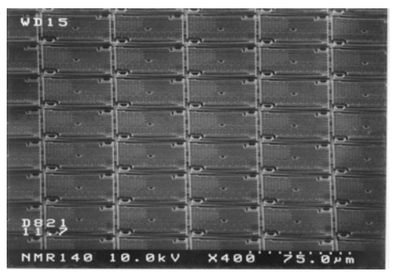
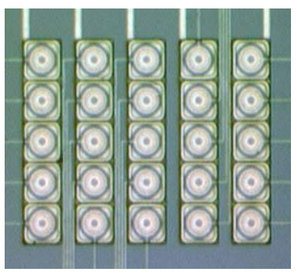
Comprehensive Fabrication Facilities at NMRC

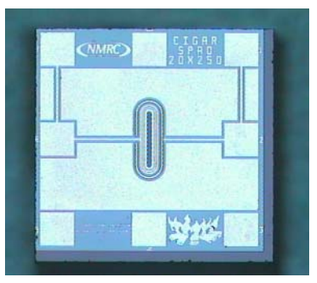
Silicon Fabrication

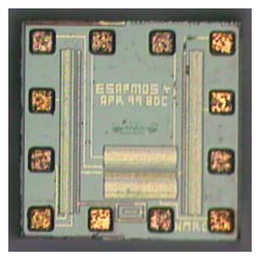


- Full CMOS Processing capability
- Flexible processing regime allows integration of novel components into standard processes
- Processes successfully transferred to commercial fabrication facilities
- Staffed by full time professional engineers and technicians

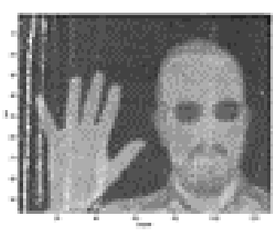








PMOS RADFETs For space and Medical applications



- Single IR Bolometer and Bolometer array integrated into 1.5µm CMOS Process
- Successfully transferred to commercial foundry
- 0.1k NETD in recent measurements

- Single photon detector integrated into a 1.0 µm SOI CMOS Process
- Breakdown voltage 14V
- Low dark count

Flexible substrate rolled with RADFETs for In-Vivo applications

Compound Semiconductor/Nanofabrication

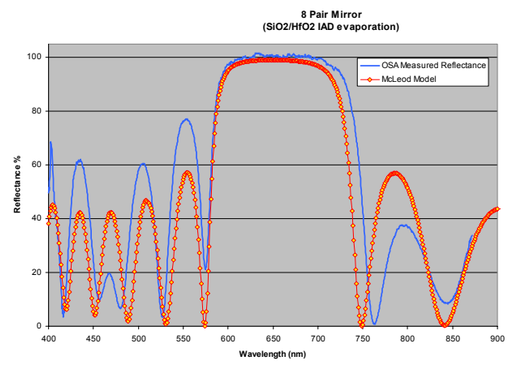
Optoelectronics ~ emitters - laser diodes, light emitting diodes, VCSELs, RCLEDs.

Nanotechnology ~ fabrication of structures for electrical characterisation of Nano-devices.

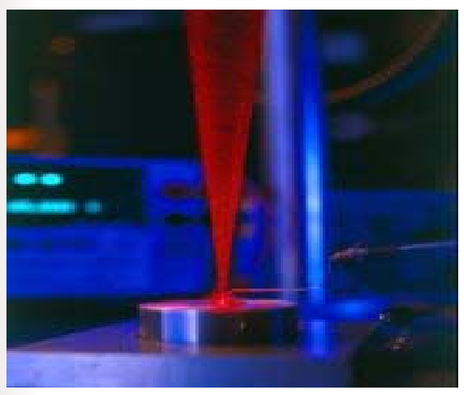
Sub-millimetre Wave Technology ~ Schottky diodes, Q-MMICs, Membrane structures

Jeol 6000FS Electron Beam Lithography system with 20nm resolution

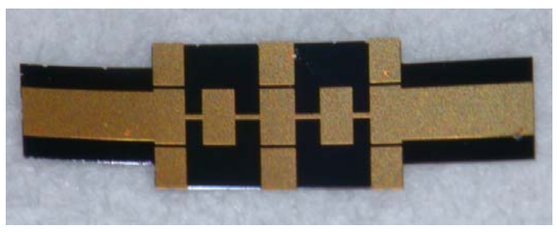
GaN RCLED emitting at 530nm for POF applications



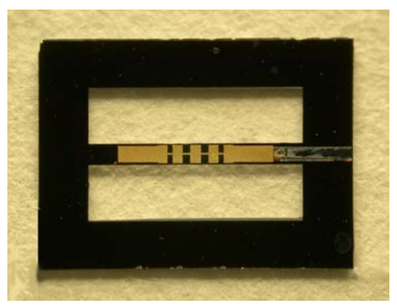
Simulated and measured performance of a SiO_2/HfO_2 eight pair mirror fabricated using a Leybold Lab 600 dielectric Deposition system



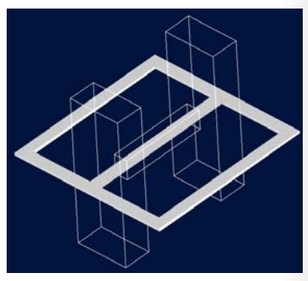
High brightness red VCSELs for plastic optical fibre (POF) communications



Filter structure (3.1 x 0.65mm) on 3um GaAs membrane



3um GaAs membrane filter structure supported in 180um GaAs frame



Schematic showing Framed membrane in channel between two waveguides.

Comprehensive Fabrication Facilities at NMRC

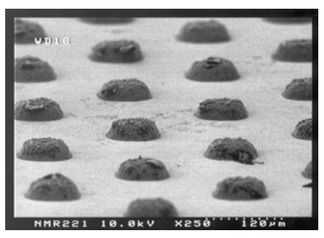
Plating Technology

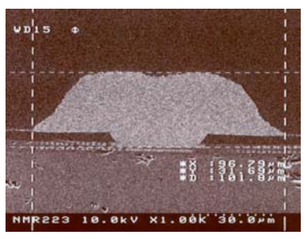
- Electroless Cu, Ni, Co/Fe, Co/Ni/Fe
- Electrolytic Cu, Ni, Au, Sn, Ni/Fe, Co/Ni/Fe

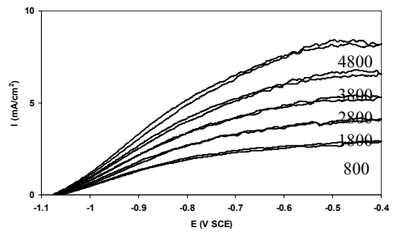
- High speed electroless copper for advanced packaging
- Electroless deposition for Interconnect
- Electroless magnetics for on chip integration
- Plating technologies for Micropower sources

High speed electroless copper for advanced packaging

Selective electroless Copper deposition for flip chip packaging



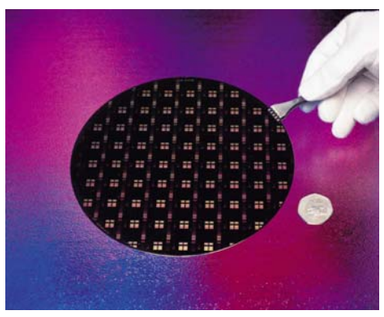


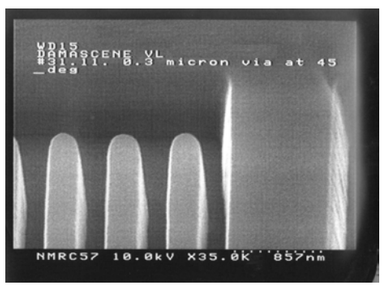


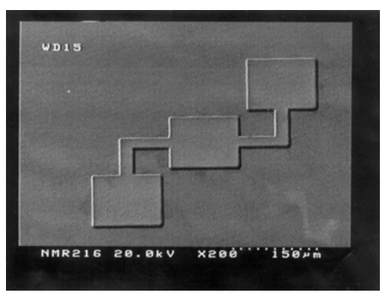
- 20 mm/hr on Cu bond pad
- Polyimide dielectric compatible
- Selective deposition
- Good adhesion ~30kg/mm^2
- Electrochemical data verification of high rate deposition

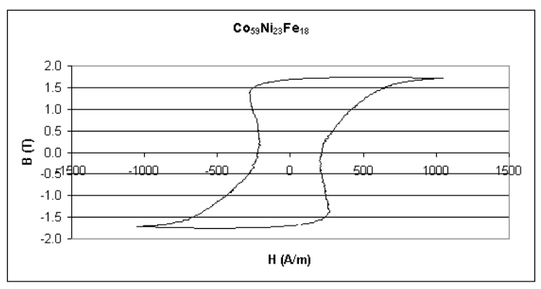
Electroless Copper for Damascene seed layer and interconnect deposition

50 nm seed layer for electrolytic build up deposit on TiN barrier layer materials
Conformal deposition in high aspect ratio features







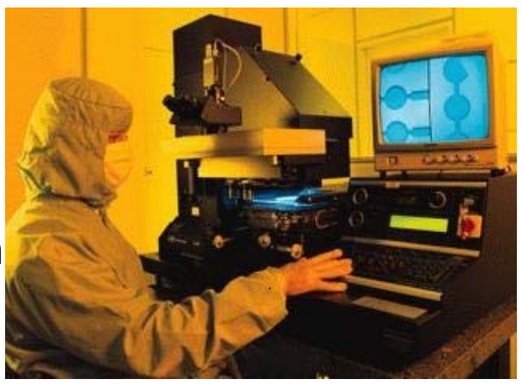


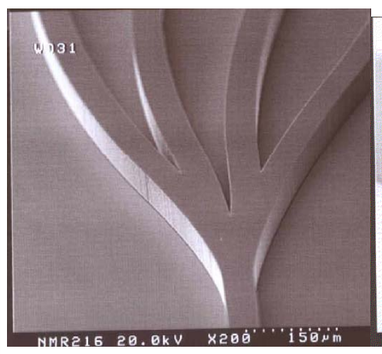
Selective electroless CoNiFe deposition for on chip magnetics integration

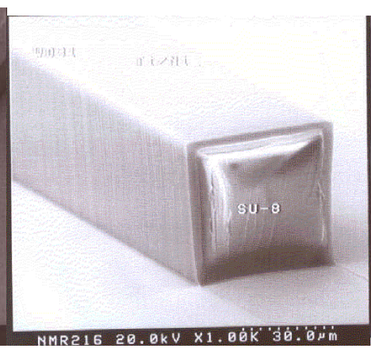
Ternary alloy deposition
Selective
Resist compatible
High saturation magnetisation (B_s)
Low coercivity

Microsystems Fabrication

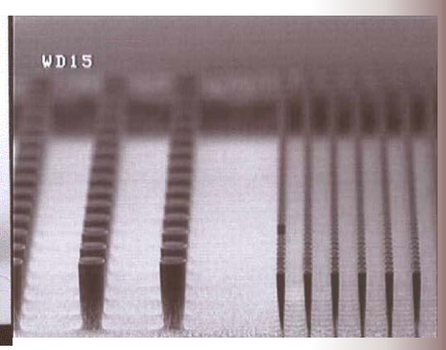
- Bulk and surface micromachining
- Wide range of polymer processes
- ASE/AOE DRIE
- Many MST process integrated with CMOS



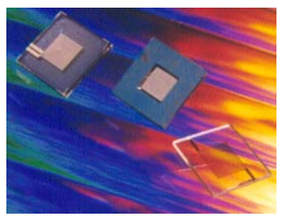




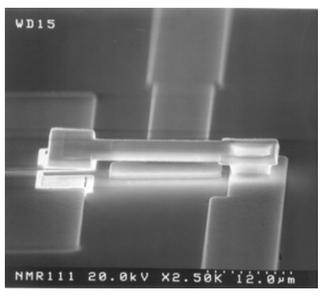
Waveguides fabricated in SU8 and capped with TiNi



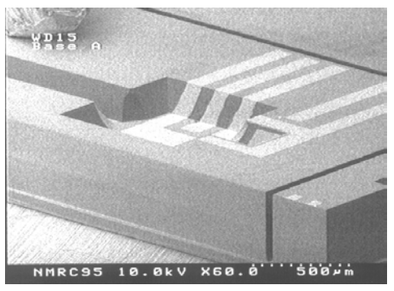
300µm Si pillars etched using STS ASE DRIE



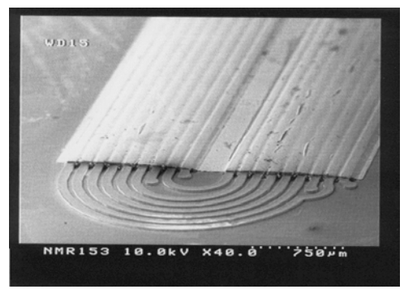
Miniaturised PCR chambers for DNA amplification



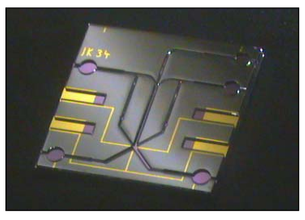
CMOS compatible surface machined switch



Bulk micromachined Silicon optical bench



Integrated Planar Magnetics
A transformer fabricated in copper and SU8 on a silicon substrate with NiFe core



Microfluidic chip fabricated in SU8 on silicon