european space agency
agence spatiale européenne

Pages 1 to 52

CHARGE COUPLED DEVICES, SILICON,

PHOTOSENSITIVE, AREA ARRAY, IMAGE SENSOR,

512 LINES × 512 PIXELS, FRONT ILLUMINATED,

FRAME TRANSFER, MULTI PINNED PHASES

BASED ON TYPE TH7890M

ESA/SCC Detail Specification No. 9610/002

space components
coordination group

Issue/Rev.	Date	Approved by	
		SCCG Chairman	ESA Director General or his Deputy
Issue 1	June 2002		

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE Reference Item	Approved DCR No.

TABLE OF CONTENTS

TABLES

FIGURES

APPENDICES (Applicable to specific Manufacturers only)
None.

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical, geometrical, electrical and electro-optical characteristics, test and inspection data for a silicon Photosensitive Area Array CCD Image Sensor, 512 Lines x 512 Pixels, Front illuminated, frame transfer, multi-pinned phases, based on Type TH7890M. It shall be read in conjunction with ESA/SCC Generic Specification No. 9020, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

A list of the type variants of the basic area array CCD image sensor specified herein, which are also covered by this specification, are given in "Table 1(a) - Type Variant Summary".

For each type variant, the full electro-optical, electrical and geometrical characteristics are given in individual "Tables 1(a) - Type Variant Detailed Information" at the end of this specification.

The contents of the individual Tables 1(a) shall be as shown in Table 1(c).

The specific characteristics shall be negotiated between the Manufacturer and the Orderer. The Manufacturer shall then apply to the ESA/SCC Secretariat for a type variant number for each individual basic area array CCD image sensor concerned, by sending a finalised Table 1(a) which shall also be copied to the Qualifying Space Agency (QSA).

For information concerning Variant 01, see ESA/SCC Generic Specification No. 9020, Para. 4.1.1.

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the components specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS AND GEOMETRICAL CHARACTERISTICS

The physical dimensions and geometrical characteristics of the components specified herein are shown in Figures 2(a) and 2(b).

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TIMING DIAGRAMS

As per Figure 3(b).

1.8 FUNCTIONAL DIAGRAM

As per Figure 3(c).

1.9 HANDLING PRECAUTIONS

The component is susceptible to damage by electro-static discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 with a Minimum Critical Path Failure Voltage of 400 Volts.

1.10 INPUT PROTECTION NETWORKS

Protection networks shall be incorporated into each input as shown in Figure 3(d).

TABLE 1(a) - TYPE VARIANT SUMMARY

VARIANT	REFERENCE TEMPERATURE (T_{ref} °C)	OPERATING TEMPERATURE RANGE (T_{op} °C)	TIMING DIAGRAM (FIGURE 3(b)) (TD)	SPECTRAL RANGE FOR WINDOW OPTICAL COATING WOC (nm)
01	+22 ± 3	−20 to +85	TD1	400 to 900
02	−20 ± 3	−40 to +85	TD1	400 to 900
03	−20 ± 3	−20 ± 3	TD1	400 to 900

NOTES

1. Full electrical and electro-optical characteristics are given in the individual Tables 1(a) at the end of this specification.

TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNITS	REMARKS
1	Range of applied voltages (vs VSS)	-	−0.3 to +17	V	Note 1
2	Range of applied voltages (vs VSS)	-	−16 to +16	V	Note 2
3	Range of applied voltages (vs VSS)	-	−0.3 to +18	V	Note 3
4	Range of applied voltages (vs VSS)	-	−0.3 to +20	V	Note 4
5	Input Current	I_{IN}	15	mA	Note 6
6	Device Dissipation		160	mW	Note 5
7	Storage Temperature Range	T_{stg}	−55 to +150	°C	
8	Operating Temperature Range	T_{op}	−40 to +85	°C	TBC
9	Soldering Temperature	T_{sol}	+260	°C	

NOTES

1. On ØR, VGS.
2. On $ØM_{4B}$, $ØM_{4A}$, $ØM_{1B}$, $ØM_{1A}$, $ØP_{2B}$, $ØL_1$, $ØL_2$, ØM, $ØM_{2B}$, $ØM_{2A}$, $ØM_{3B}$, $ØM_{3A}$, $ØP_{4B}$, $ØP_{2A}$, $ØP_{3B}$, $ØP_{3A}$, $ØP_{1A}$, $ØP_{1B}$, $ØP_{4A}$. Voltage difference between each pins should be below 17V. Maximum swing should be below 17V.
3. On VDR, VDP. Voltage difference between ØM and VDP should be below 20V.
4. On VDD.
5. Output amplifier only. Max output amplifier dissipation = 20V x IDD(Top)max = 160mW.
6. Output amplifier only. Shorting the video output to VSS or VDD, even temporarily, can permanently damage the output amplifier.

FIGURE 1 - PARAMETER DERATING INFORMATION

Not applicable.

TABLE 1(c) - FORMAT FOR INDIVIDUAL TABLES 1(a)

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION

TYPE VARIANT No.

No.	CHARACTERISTICS	SYMBOL	LIMITS		UNITS	REMARKS
			MIN.	MAX.		
1	Operating Temperature Range	T_{op}			°C	
2	Reference Temperature	T_{ref}			°C	
3	Flatness of Image Area	P			µm	
4	Spectral Range for Optical Coating on Window	WOC			nm	Note 1
5	Timing Diagram	TD			-	Note 2
6	Power Supply Current 1	I_{DD1}			mA	Note 3
7	Power Supply Current 2	I_{DD2}			mA	Note 3
8	Power Supply Current 2 over T_{op}	I_{DD2} (T_{op})			mA	Note 3
9	DC Output Level	V_{Ref}			V	
10	Output Impedance	Z_S			Ω	Note 4
11	Saturation Voltage for the Image Area	V_{SAT}			mV	
12	Vertical Charge Transfer Inefficiency	VCTI			%	Note 5
13	Horizontal Charge Transfer Inefficiency	HCTI			%	Note 5
14	Average Dark Signal	VDS			mV	Note 6
15	Average Dark Signal over T_{op}	VDS(T_{op})			mV	Note 6
16	Dark Signal Non-uniformity, standard deviation σ	DSNU(σ)			mV	Note 7
17	Number of Dark Signal Defects beyond a3 limit	Ndef3			-	Note 7
18	Number of Dark Signal Defects beyond a4 limit	Ndef4			-	Note 7

NOTES: See Page 10.

TABLE 1(c) - FORMAT FOR INDIVIDUAL TABLES 1(a) (CONTINUED)

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION (CONTINUED)

TYPE VARIANT No.

No.	CHARACTERISTICS	SYMBOL	LIMITS		UNITS	REMARKS
			MIN.	MAX.		
19	DSNU Limit for Ndef3	a3			mV	Note 7
20	DSNU Limit for Ndef4	a4			mV	Note 7
21	Responsivity	R			V/μJ/cm²	Note 8
22	Responsivity over T_{op}	$R(T_{op})$			V/μJ/cm²	Note 8
23	Photoresponse Non-uniformity, standard deviation σ	PRNU(σ)			%	Note 9
24	Number of PRNU Defects beyond a1 Limit	Ndef1			-	Note 9
25	Number of PRNU Defects beyond a2 Limit	Ndef2			-	Note 9
26	PRNU Limit for Ndef1	a1			%	Note 9
27	PRNU Limit for Ndef2	a2			%	Note 9
28	Spectral Responsivity in Optical Band B1	R(B1)			V/μJ/cm²	Note 10
29	Spectral Responsivity in Optical Band B2	R(B2)			V/μJ/cm²	Note 10
30	Spectral Responsivity in Optical Band B3	R(B3)			V/μJ/cm²	Note 10
31	Spectral Responsivity in Optical Band B4	R(B4)			V/μJ/cm²	Note 10
32	Spectral Responsivity in Optical Band B5	R(B5)			V/μJ/cm²	Note 10
33	Spectral Responsivity in Optical Band B6	R(B6)			V/μJ/cm²	Note 10
34	Spectral Responsivity in Optical Band B7	R(B7)			V/μJ/cm²	Note 10
35	Linearity Error	LE			%	Note 11

NOTES: See Page 10.

TABLE 1(c) - FORMAT FOR INDIVIDUAL TABLES 1(a) (CONTINUED)

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION (CONTINUED)

TYPE VARIANT No.

No.	CHARACTERISTICS	SYMBOL	LIMITS		UNITS	REMARKS
			MIN.	MAX.		
36	Temporal Noise	V_N			µV	Note 12
37	Offset Voltage	V_{Offset}			mV	
38	Amplitude of Reset Feedthrough	V_{Reset}			mV	
39	Reference Level Settling Time	$t_{D\text{-}Ref}$			ns	Note 13
40	Reference Level Duration	$t_{U\text{-}Ref}$			ns	Note 13
41	Reference Level Error Band	ΔU_{Ref}			mV	Note 13
42	Signal Level Settling Time	$t_{D\text{-}Signal}$			ns	Note 13
43	Signal Level Duration	$t_{U\text{-}Signal}$			ns	Note 13
44	Signal Level Error Band	ΔU_{Signal}			mV	Note 13
45	Electrode Capacitance	$C\phi P$			pF	
46	Electrode Capacitance	$C\phi M$			pF	
47	Electrode Capacitance	$C\phi L$			pF	
48	Electrode Capacitance	$C\phi R$			pF	
49	Charge to Voltage Conversion Factor	CVF			µV/e	Note 14

NOTES: See Page 10.

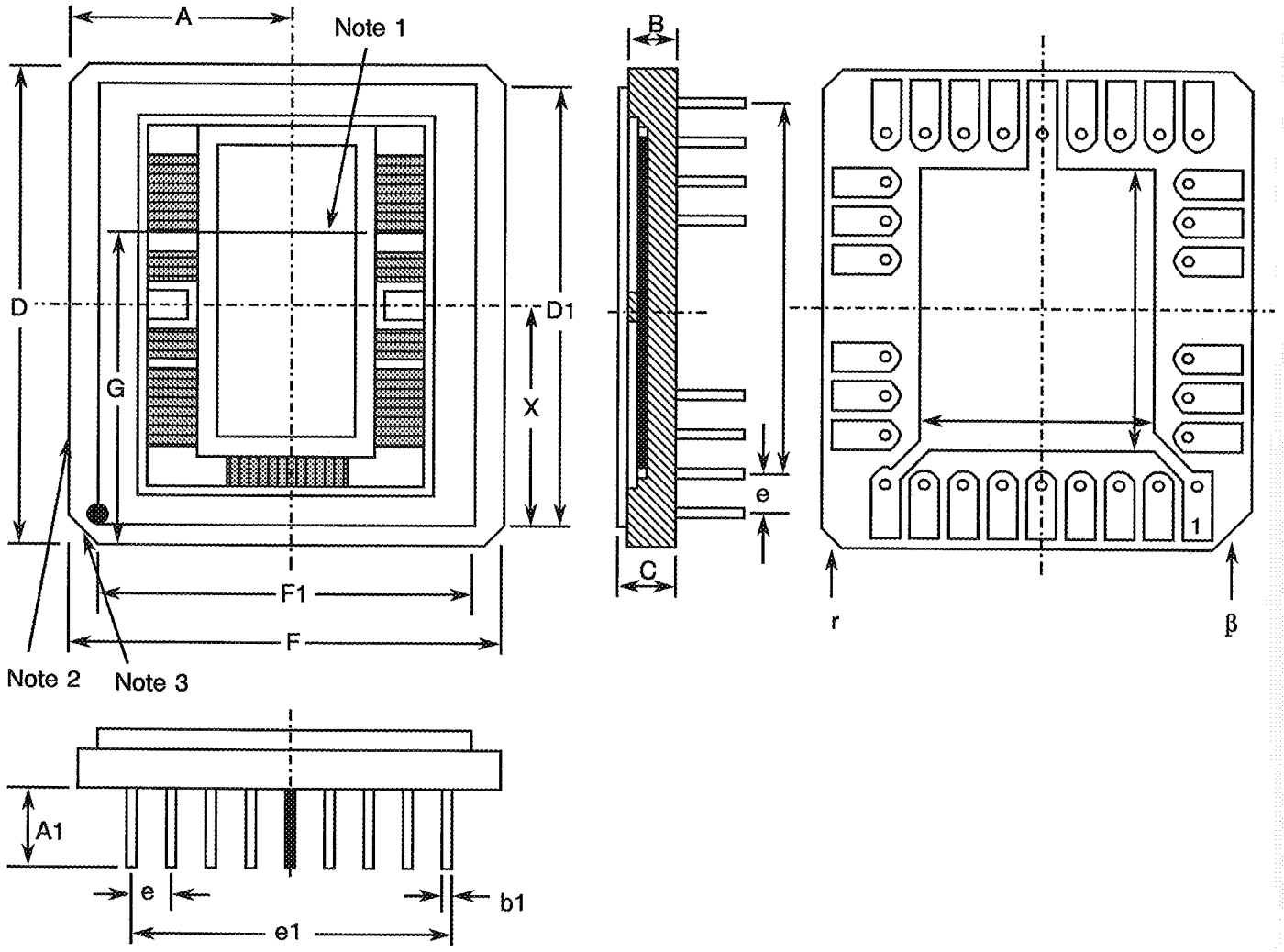
TABLE 1(c) - FORMAT FOR INDIVIDUAL TABLES 1(a) (CONTINUED)

NOTES

1. The reflectance for each side of the window shall be specified inside the spectral range for optical coating.
2. The timing diagram TD1 or TD2, as specified in Table 1(a), shall be used for all measurements.
3. I_{DD1} measurement shall be static, I_{DD2} measurement shall be dynamic, $I_{DD2(T_{op})}$ measurement shall be dynamic and all shall be specified in Table 1(a).
4. The values of R and C used for output impedance measurement shall be defined in Table 1(a).
5. The measurement is based on uniform illumination - ESA/SCC Basic Specification No. 25000, Para. 6.12.2(a).
6. VDS is measured on the last lines of the image area.
7. The slope effect included.
8. The responsivity is measured under uniform illumination with BG38 optical filter.
9. The PRNU is measured under uniform illumination with BG38 filter.
10. The optical bands shall be specified in terms of centre wavelength and bandwidth at 50% of transmission peak.
11. The measurement is made under uniform illumination with a BG38 optical filter. The output signal range used for linearity error calculation shall be defined in Table 1(a).
12. The measurement is based on two successive acquisitions of the same row.
13. For output signal waveform measurements, see Figure 4(h).
14. The CVF is measured by sampling on 5 devices per wafer lot, but not on deliverable devices.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - PHYSICAL DIMENSIONS

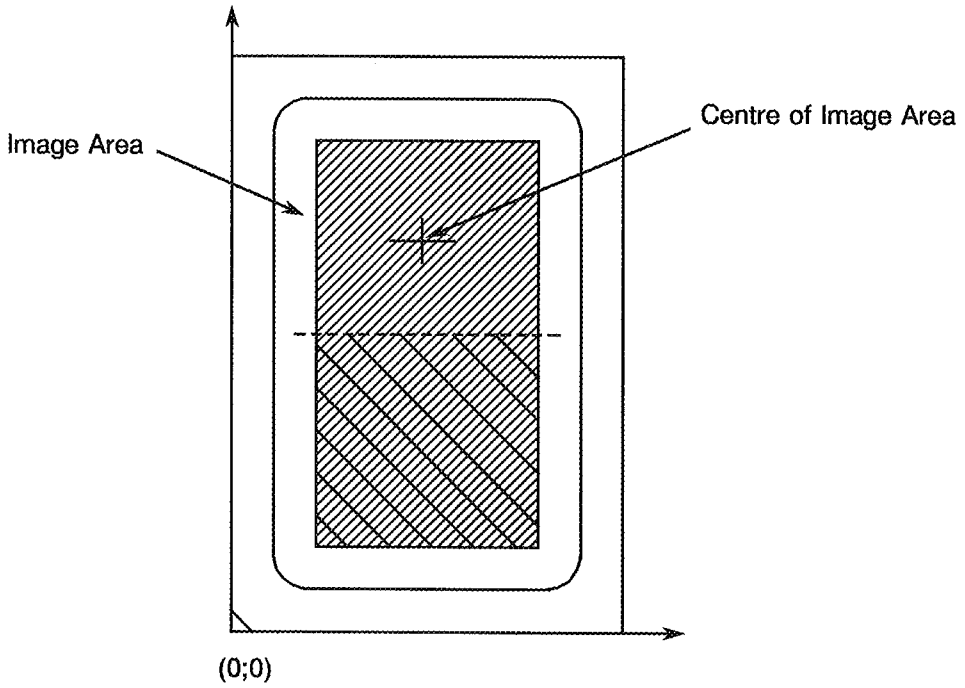


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	13.32	13.52	
A1	4.57 Typ.		
b1	0.46 Typ.		
B	2.97	3.63	
C	4.11	5.01	
D	31.25	31.85	
D1	29.50 Typ.		
e	2.54 Typ.		
e1	20.32 Typ.		
F	26.26	26.74	
F1	23 Typ.		
G	21.3	21.5	
X	16.50 Typ.		
r	0.5 x 0.5		
β	2.0 x 2.0		

NOTES: See Page 13.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - GEOMETRICAL CHARACTERISTICS



No.	CHARACTERISTIC	SYMBOL	LIMITS		UNIT	REMARKS
			MIN.	MAX.		
1	Flatness of Image Area	P		30	µm	Note 4
2 3	Position of the Centre of Image Area	X Y	13320 21300	13520 21500	µm	Note 5
4	Image Plane Orientation	θ	−0.5	+0.5	°	Note 6
5	Optical Distance between Image Plane and Window	Z	1.5	2.0	mm	Note 7
6	Parallelism between Image Plane and Window	TILT	−100	+100	µm	Note 8
7	Image Plane Dimensions	L W	8685 8685	8725 8725	µm	Note 9

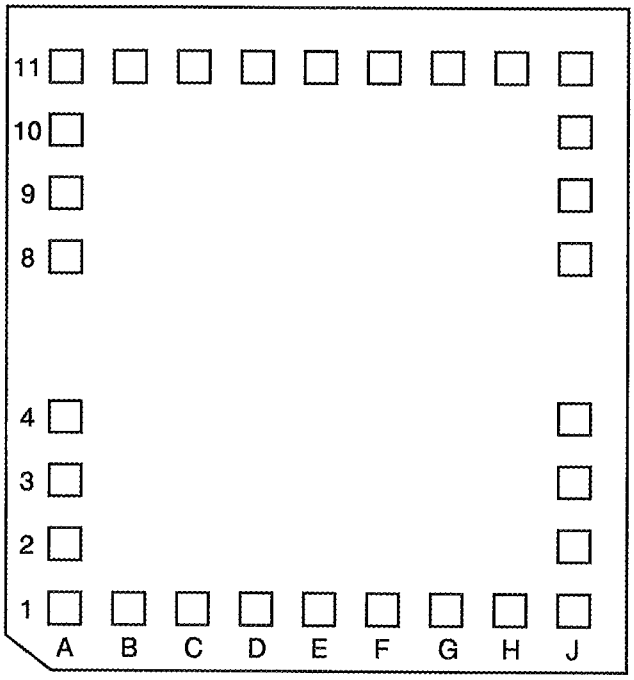
NOTES: See Page 13.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURES 2(a) AND 2(b)

1. Photosensitive Area Centre.
2. Mechanical references.
3. Index area: a large chamfer located adjacent to Pin A1 and the ESD symbol.
4. Measured on a 100% basis.
5. Measured on a 100% basis.
6. θ = site angle. Measured by sampling on 5 devices per lot.
7. Measured by sampling on 5 devices per lot.
8. Measured by sampling on 5 devices per lot.
9. Measured by sampling on 5 devices per lot. The pixels are square and the size of each pixel is equal to 17µm x 17µm.

FIGURE 3(a) - PIN ASSIGNMENT



PIN No.	SYMBOL	DESIGNATION
A1, E11, J1	V_{SS}	Substrate Bias, Ground
A2	ϕR	Reset Clock
A8, A9 J3, J4 J8, J9 A3, A4	ϕM1 ϕM2 ϕM3 ϕM4	Memory-Zone Clock
A10	V_{DP}	Protection Drain Bias
J10	V_{SSP}	ESD Protections Bias
J2	ϕM	Memory Zone to Shift Register Clock
F11, G11 A11, B11 C11, D11 H11, J11	ϕP1 ϕP2 ϕP3 ϕP4	Image-zone Clock
G1 H1	ϕL1 ϕL2	Readout Register Clock
F1	V_{GS}	Output Gate Bias
E1	V_{DR}	Reset Drain Supply
D1	V_S	Output Amplifier Substrate Bias
C1	V_{OS}	Video Output
B1	V_{DD}	Output Amplifier Drain Supply

FIGURE 3(b) - TIMING DIAGRAM

TD1

FRAME TIMING DIAGRAM

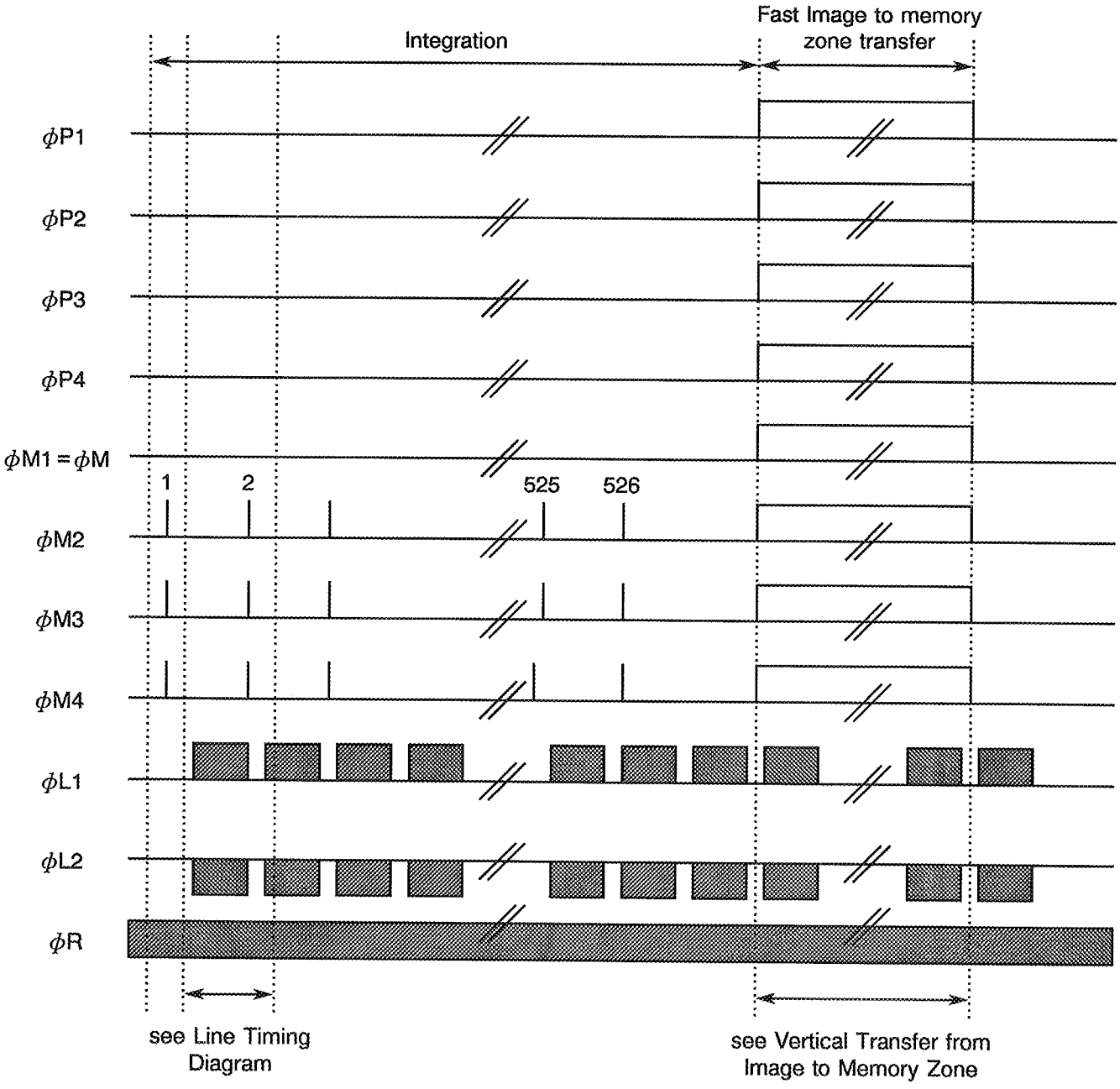
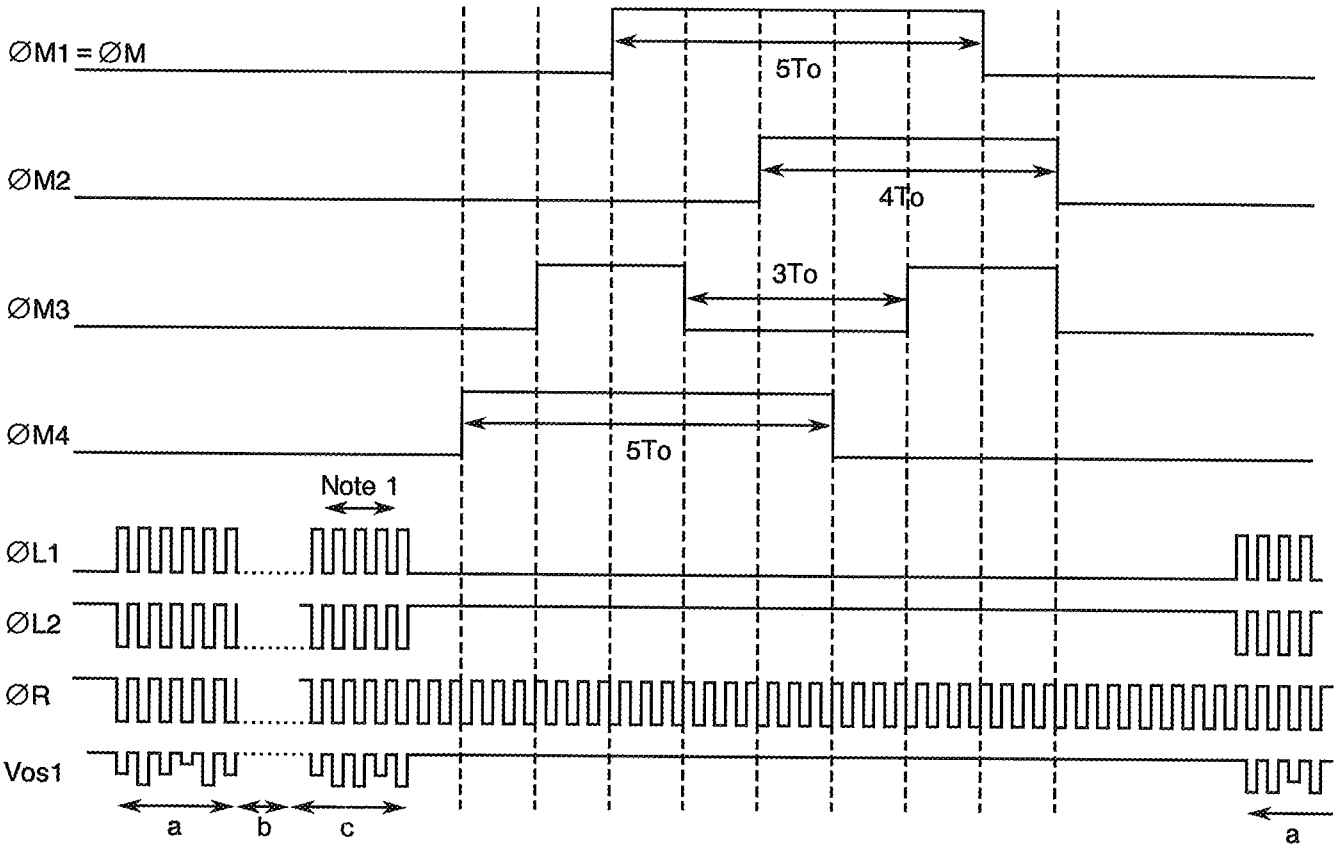


FIGURE 3(b) - TIMING DIAGRAM (CONTINUED)

LINE TIMING DIAGRAM



a: 16 prescan pixels
b: 20 isolation pixels
c: 512 useful pixels

NOTES

1. See output timing diagram for readout register and reset clock at 4MHz.

FIGURE 3(b) - TIMING DIAGRAM (CONTINUED)

VERTICAL TRANSFER (IMAGE TO MEMEORY ZONE TRANSFER)

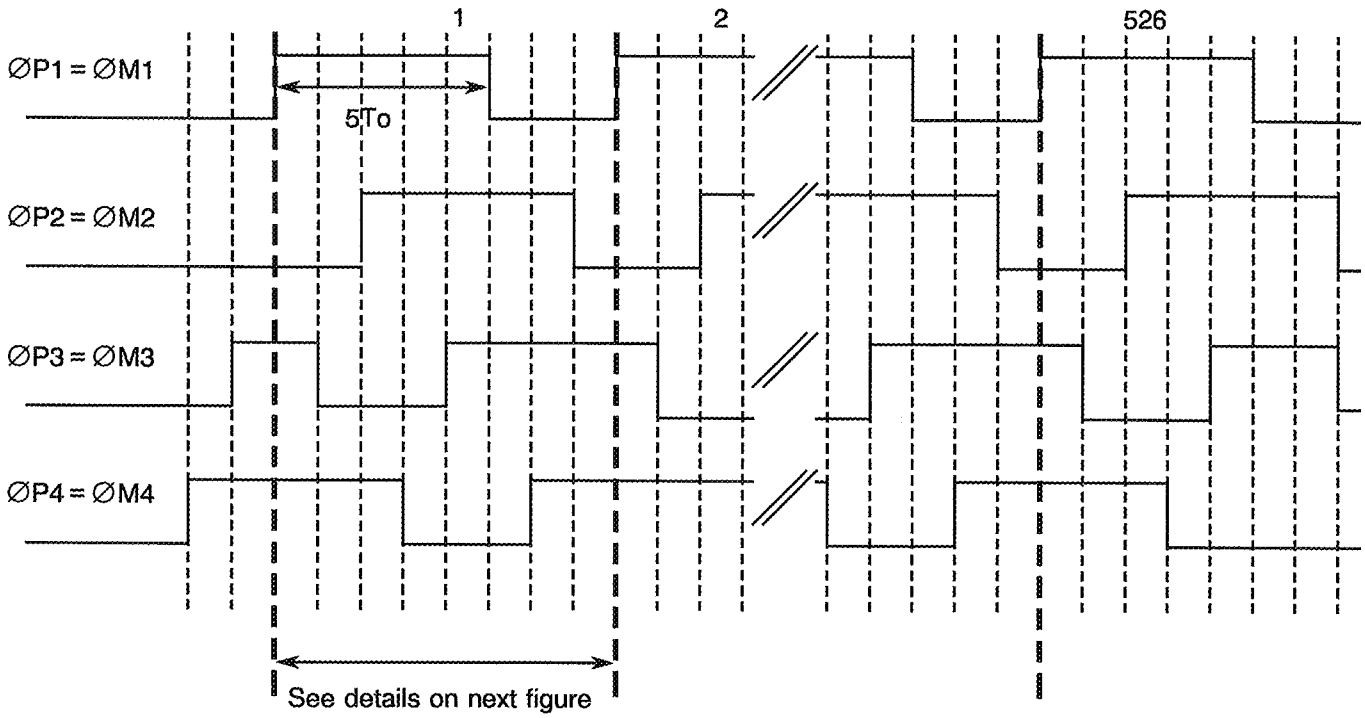
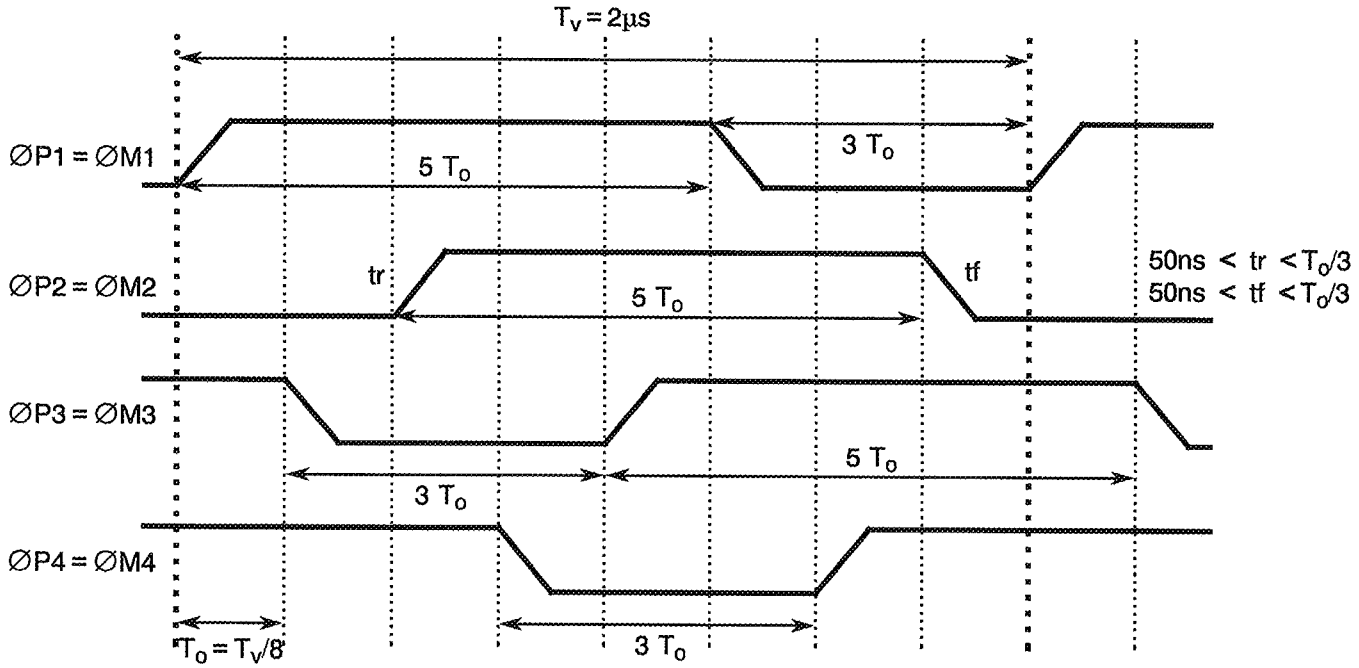
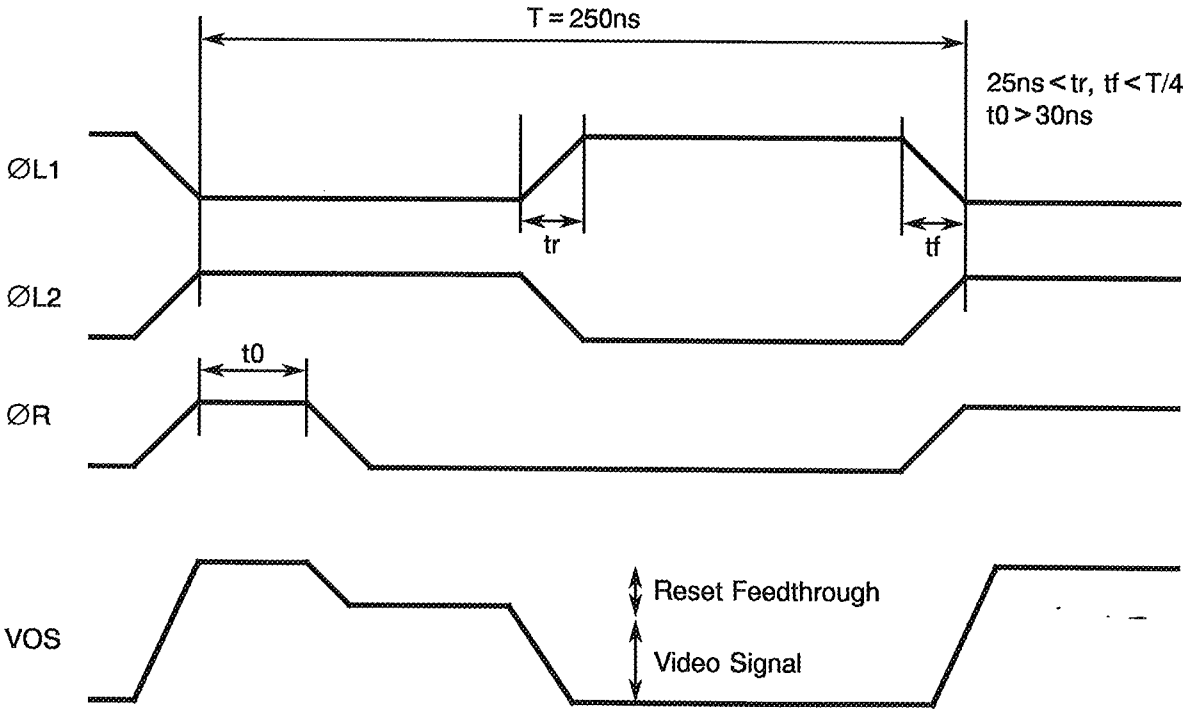


FIGURE 3(b) - TIMING DIAGRAM (CONTINUED)

IMAGE ZONE TO MEMORY VERTICAL TRANSFER (500kHz FREQUENCY)

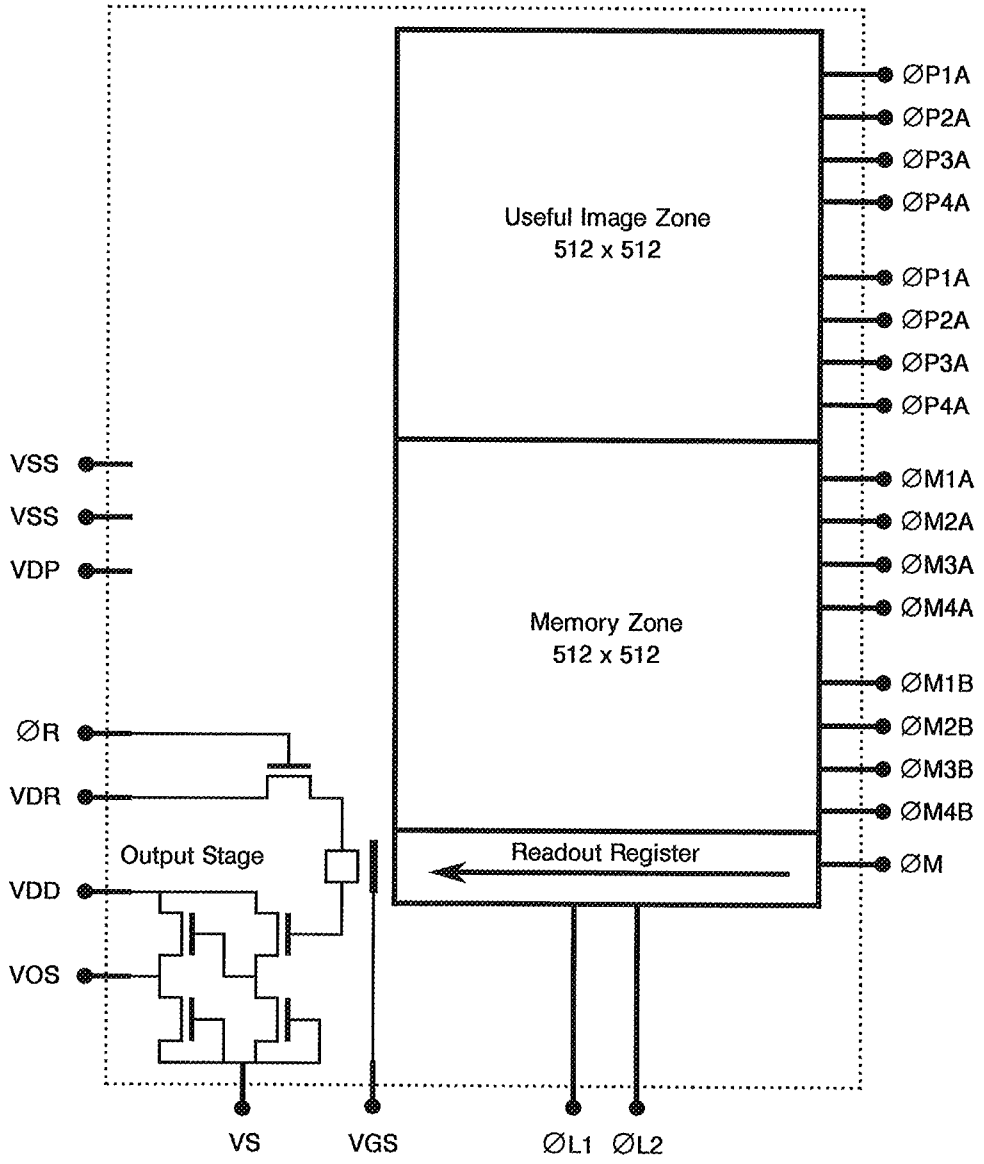


OUTPUT TIMING DIAGRAM FOR READOUT REGISTER AND RESET CLOCK AT 4MHz



Cross-over of complementary clocks diaL1, diaL2 between 30% and 70% of their maximum amplitude.

FIGURE 3(c) - FUNCTIONAL DIAGRAM



The image and memory area consist of:

- 526 lines (10 lines for the shaded zone of the optical shield + 512 useful lines + 4 isolation lines).
- A video line is made of 548 stages: 16 prescan elements + 20 isolation pixels + 512 useful pixels.

FIGURE 3(c) - FUNCTIONAL DIAGRAM (CONTINUED)

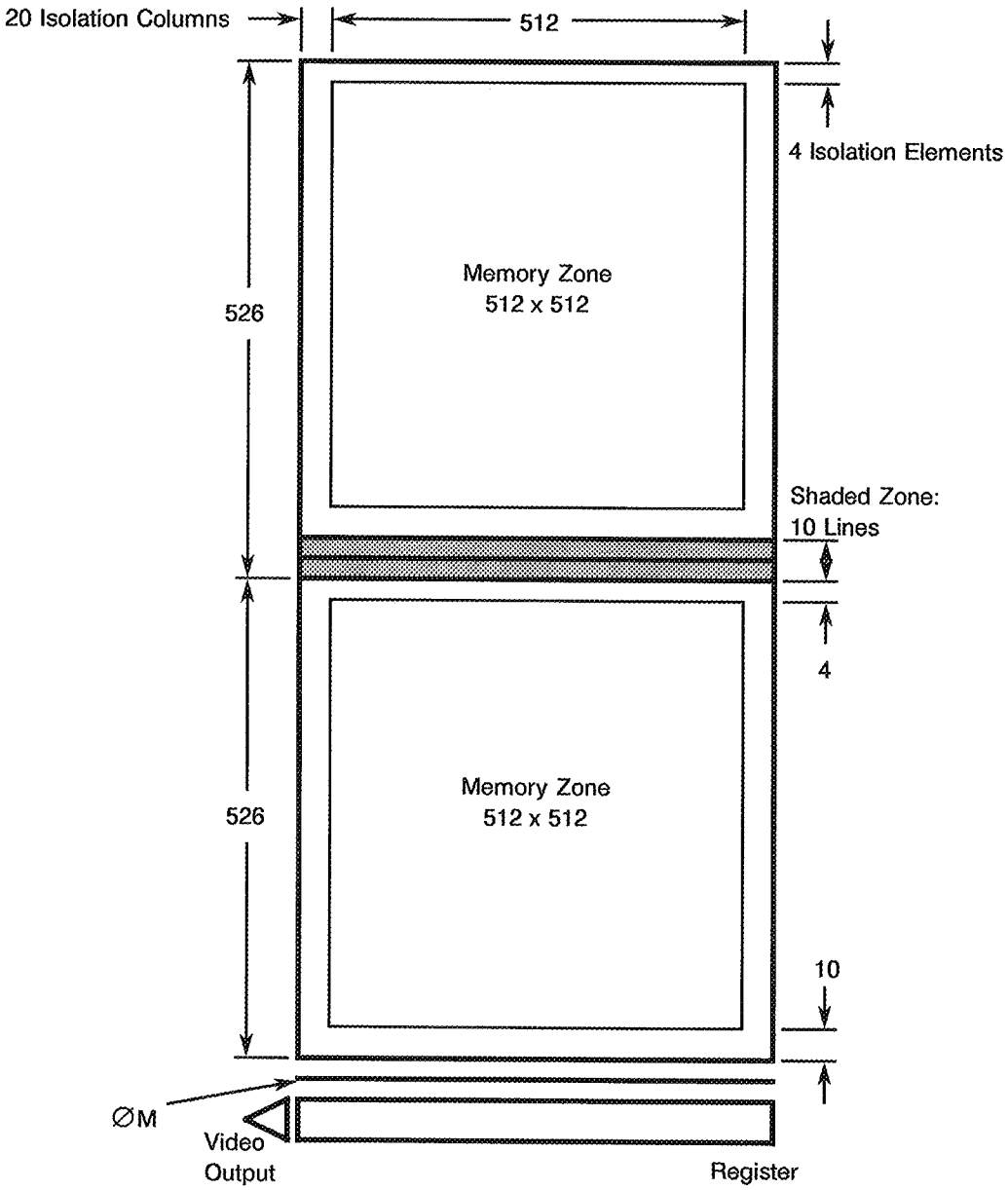
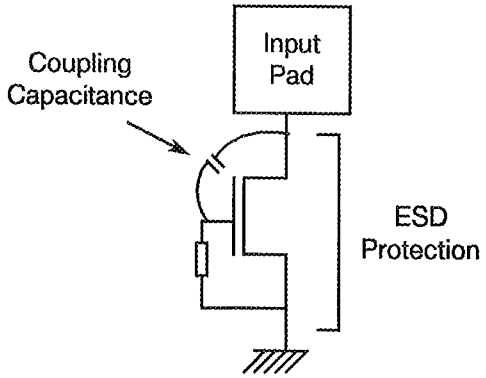


FIGURE 3(d) - INPUT PROTECTION NETWORKS

Due to MPP mode, input protection network are only available on PIN ϕR, VGS, VDR, VDP, VDD.



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC 25000, Electrical-Optical tests for CCDs.

(b) ESA/SCC Generic Specification No. 9020 for Charge Coupled Devices, Silicon Photosensitive.

(c) DIN3140, "MAβ-und Toleranzangaben für Optikeinzelteile; oberflächenbeschichtungen" (Description of dimensions and tolerances for optical components; indication for coatings).

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the components specified herein are stated in this specification and ESA/SCC Generic Specification No. 9020 for Charge Coupled Devices. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

(a) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during qualification and maintenance of qualification.

(b) Para. 5.2.2, Total Dose Irradiation Testing: If specified in a Purchase Order, shall be performed during procurement on a lot acceptance basis at the total dose irradiation level specified in the Purchase Order.

(c) $C\phi Pi$, $C\phi Mi$, $C\phi Li$, $C\phi M$, and $C\phi R$ are measured by sampling 3 devices per wafer lot, but not on deliverable devices.

(d) CVF is measured by sampling 5 devices per wafer lot, but not on deliverable devices.

4.2.2 Deviations from Final Production Tests (Chart II)

(a) Para. 9.6, the acceleration during constant accelerating test shall not exceed 5.0Kg.

(b) Para. 9.8, the pressure during seal test shall not exceed 3kg/cm^2.

(c) Para. 9.8.1, Leak Rate: 5×10^{-7} atm/cm^3/sec.

4.2.3 Deviations from Burn-in Tests (Chart III)

(a) Para. 7.1.1(a), "High Temperature Reverse Bias (H.T.R.B.)" test and subsequent electrical measurements related to this test shall not be performed.

(b) Para. 9.8, the pressure during seal test shall not exceed 3kg/cm^2.

(c) Para. 9.8.1, Leak Rate: 5×10^{-7} atm/cm^3/sec.

4.2.4 Deviations from Qualification Tests (Chart IV)

(a) Para. 9.6, the acceleration during constant accelerating test shall not exceed 10Kg.

(b) Para. 9.8, the pressure during seal test shall not exceed 3kg/cm^2.

(c) Para. 9.8.1, Leak Rate: 5×10^{-7} atm/cm^3/sec.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

(a) Para. 9.6, the acceleration during constant accelerating test shall not exceed 10Kg.

(b) Para. 9.8, the pressure during seal test shall not exceed 3kg/cm^2.

(c) Para. 9.8.1, Leak Rate: 5×10^{-7} atm/cm^3/sec.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the components specified herein shall be checked. They shall conform to those shown in Figure 2(a).

4.3.2 Geometrical Characteristics

The geometrical characteristics of the components specified herein shall be checked. They shall conform to those shown in Figure 2(b).

4.3.3 Weight

The maximum weight of the components specified herein shall be 15 grammes.

4.3.4 Terminal Strength

The requirements for terminal strength testing are specified in Section 9 of ESA/SCC Generic Specification No. 9020.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the components specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

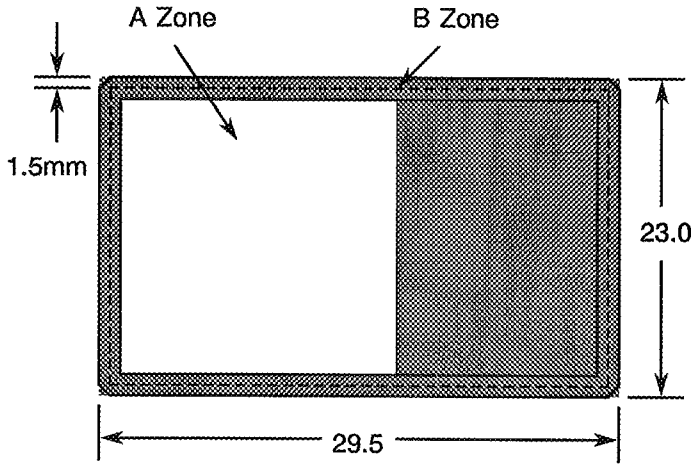
The case shall be hermetically sealed and have a ceramic body and glass window. The flatness of the underside of package shall be better than 0.1mm/cm, measured between edges, across the complete surface.

4.4.2 Lead Material and Finish

For lead material shall be Type 'G' with Type '7' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500.

4.4.3 Window

Window material shall be sapphire. The optical quality of the window including coating, if required for both sides, shall be better than as defined in DIN3140.



- A Zone is the non shanded zone.
- No specification for outside of B Zone.
- No defect larger than 10 000um2 inside of B Zone.
- Inclusion/scratch : 10um max. in A Zone.
- No chips or cracks inside of B Zone.
- Parallelism : better than 200 arcs seconds.
- Surface flatness : better than 4 circular fringes at 633nm.

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700, and the following paragraphs. When the component is too small to accommodate all of the marking specified, as much as space permits shall be marked and the marking information, in full, shall accompany the component in its primary package.

The information to be marked and the order of precedence, shall be as follows:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

4.5.2 Lead Identification

An index shall be located at the top of the package in the position defined in Note 1 to Figure 2(a). The pin numbering must be read with the index on the left-hand side.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:

961000201BE

Detail Specification Number
Type Variant (see Table 1(a))
Testing Level (B or C, as applicable)
Total Dose Irradiation Level (if applicable)

The Total Dose Irradiation Level designation shall be added for those devices for which a sample has been successfully tested to the level in question. For these devices, a code letter shall be added in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS

4.6.1 Electrical and Electro-optical Measurements at Reference Temperature

The parameters to be measured in respect of electrical and electro-optical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at T_{ref} ±3 °C.

4.6.2 Electrical and Electro-optical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. Unless otherwise specified, the measurements shall be performed at −40(+5−0) and +85(+0−5) °C respectively.

4.6.3 Circuits for Electrical and Electro-optical Measurements

Circuits for use in performing electrical and electro-optical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to H.T.R.B. and Power Burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at T_{ref} ±3 °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for High Temperature Reverse Bias Burn-in

Not applicable.

4.7.3 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9020. The conditions for power burn-in shall be as specified in Table 5(b) of this specification.

4.7.4 Electrical Circuits for High Temperature Reverse Bias Burn-in

Not applicable.

4.7.5 Electrical Circuits for Power Burn-in

Circuits for use in performing the power burn-in test are shown in Figure 5(b) of this specification.

TABLE 2 - ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT REFERENCE TEMPERATURE

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
					MIN	MAX	
01	Leakage Current on Input Gates	I_L	4(b)	V_{IH} = 12V T_{amb} = +25 ± 3 °C	-	300	pA
02 to 05	Input Clamp Voltage (to VSS)	V_{IC}	4(c)	I_{IN} (Under Test) = −500µA at $V_{IN} \leq -3.5V$ V_{IN} (Remaining Pins) = 0V (Pins A2 - A10 - E1 - F1)	-1.5	-	V
06 to 29	Insulation Leakage Current between Pins (Input Current)	I_E	4(d)	V_{IH} = 15V (Pins A2-A3-A4-A8-A9-A10-A11-B11-C11-D11-E1-F1-F11-G1-G11-H1-H11-J2-J3-J4-J8-J9-J11) Pin E1 see Note to Fig. 4(d)	-	1.0	uA
30	Power Supply Current 1	I_{DD1}	4(e)	Room Temperature STATIC V_{DR} = ϕR (High Level) = Table 1(a) V_{IN} (Remaining Pins) = 0V V_{OS} = Open V_{DD} = 18V V_{SS} = 0V (Pins A1 and J1)	Item 6		mA
31	Power Supply Current 2	I_{DD2}	4(g)	DYNAMIC V_{IN} (Remaining Pins) = See Test Table V_{DD} = 18V, V_{SS} = 0V (Pins A1 and J1)	Item 7		mA
32	DC Output Level	V_{ref}	4(e)	STATIC V_{DR} = 14V ϕR (High Level) = Table 1(a) V_{IN} (Remaining Pins) = 0V V_{OS} = Open V_{DD} = 18V V_{SS} = 0V (Pin C1)	Item 9		V
33	Output Impedance	Z_S	4(f)	DYNAMIC V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 10		Ω

TABLE 2 - ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT REFERENCE TEMPERATURE (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
					MIN	MAX	
34	Saturation Voltage for the Image Area	V_{SAT}	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 11		mV
35	Vertical Charge Transfer Inefficiency	VCTI	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 12		%
36	Horizontal Charge Transfer Inefficiency	HCTI	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 13		%
37	Average Dark Signal	VDS	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 14		mV
38	Dark Signal Non-uniformity, standard deviation σ	DSNU(σ)	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 15		mV
39	Number of Dark Signal Defects beyond a3 Limit	Ndef3	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 17		-
40	Number of Dark Signal Defects beyond a4 Limit	Ndef4	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 18		-
41	DSNU Limit for Ndef3	a3	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 19		mV

TABLE 2 - ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT REFERENCE TEMPERATURE (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
					MIN	MAX	
42	DSNU Limit for Ndef4	a4	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 20		mV
43	Responsivity	R	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 21		V/μJ/cm²
44	Photoresponse Non-uniformity, standard deviation σ	PRNU(σ)	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 22		%
45	Number of PRNU Defects beyond a1 Limit	Ndef1	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 24		-
46	Number of PRNU Defects beyond a2 Limit	Ndef2	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 25		-
47	PRNU Limit for Ndef1	a1	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 26		%
48	PRNU Limit for Ndef2	a2	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 27		%
49	Spectral Responsivity in Optical Band B1	R(B1)	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 28		V/μJ/cm²

TABLE 2 - ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT REFERENCE TEMPERATURE (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
					MIN	MAX	
50	Spectral Responsivity in Optical Band B2	R(B2)	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 29		V/μJ/cm²
51	Spectral Responsivity in Optical Band B3	R(B3)	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 30		V/μJ/cm²
52	Spectral Responsivity in Optical Band B4	R(B4)	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 31		V/μJ/cm²
53	Spectral Responsivity in Optical Band B5	R(B5)	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 32		V/μJ/cm²
54	Spectral Responsivity in Optical Band B6	R(B6)	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 33		V/μJ/cm²
55	Spectral Responsivity in Optical Band B7	R(B7)	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 34		V/μJ/cm²
56	Linearity Error	LE	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 35		%
57	Temporal Noise	V_N	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 36		μV

TABLE 2 - ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT REFERENCE TEMPERATURE (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
					MIN	MAX	
58	Offset Voltage	V_{Offset}	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 37		mV
59	Amplitude of Reset Feedthrough	V_{Reset}	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 38		mV
60	Reference Level Settling Time	$t_{D\text{-}Ref}$	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 39		ns
61	Reference Level Duration	$t_{U\text{-}Ref}$	4(g)	V_{IN} (Remaining Pins) = See Test Table V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 40		ns
62	Reference Level Error Band	ΔU_{Ref}	4(h)	V_{IN} (Remaining Pins) = See Test Table V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 41		mV
63	Signal Level Settling Time	$t_{D\text{-}Signal}$	4(h)	V_{IN} (Remaining Pins) = See Test Table V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 42		ns
64	Signal Level Duration	$t_{U\text{-}Signal}$	4(h)	V_{IN} (Remaining Pins) = See Test Table V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 43		ns
65	Signal Level Error Band	ΔU_{Signal}	4(h)	V_{IN} (Remaining Pins) = See Test Table V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 44		mV

TABLE 2 - ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT REFERENCE TEMPERATURE (CONT'D)

No.	CHARACTERISTICS	SYMBOL	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
					MIN	MAX	
66 to 69	Electrode Capacitance	CϕPi	4(g)	For V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 45		pF
70 to 74	Electrode Capacitance	CϕMi	4(g)	For V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 46		pF
75 to 76	Electrode Capacitance	CϕLi	4(g)	For V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 47		pF
77	Electrode Capacitance	CϕR	4(g)	For V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 48		pF
78	Electrode Capacitance	CϕP	4(g)	For V_{IN} (Remaining Pins) = See Test Table V_{OS} = Open V_{DD} = 18V, V_{SS} = 0V (Pin C1)	Item 49		pF

TABLE 3 - ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES

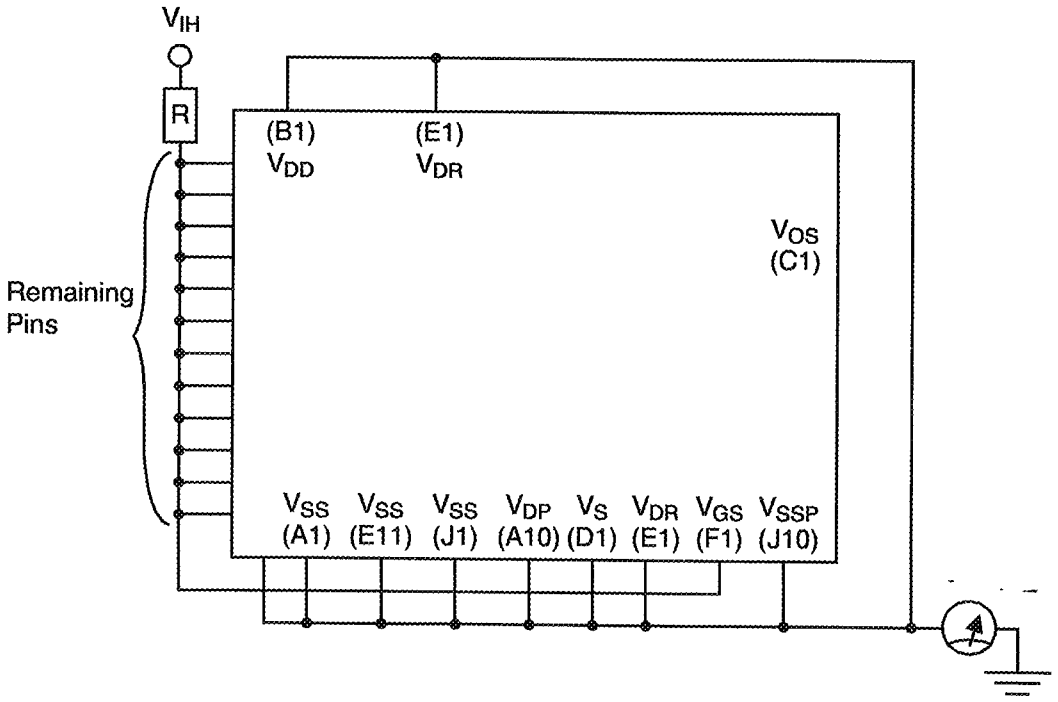
No.	CHARACTERISTICS	SYMBOL	TEST METHOD ESA/SCC 25000	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
30	Power Supply Current 1 over T_{op}	I_{DD1} (T_{op})	Para. 5.3	4(e)	DYNAMIC V_{OS} = Open Remaining pins = Fig 4(a)	Table 1(a) Item 8		mA
37	Average Dark Signal over T_{op}	VDS2 (T_{op})	Para. 6.20	4(g)	V_{OS} = Open Remaining pins = Fig 4(a)	Table 1(a) Item 15		mV
43	Responsivity over T_{op}	R (T_{op})	Para. 6.17	4(g)	V_{OS} = Open Remaining pins = Fig 4(a)	Table 1(a) Item 22		V/μJ/cm²

FIGURE 4 - CIRCUITS FOR ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS

FIGURE 4(a) - BIASING VOLTAGE LEVELS

PARAMETER	SYMBOL	CONDITIONS	UNIT
Output Amplifier Drain Supply	V_{DD}	18 (+0.5 −0.5)	V
Protection Drain Bias	V_{DP}	5 (+1.0 −1.0)	V
Reset Bias	V_{DR}	14 (+0.5 −0.5)	V
Register Output Gate Bias	V_{GS}	3.0 (+0.5 −0.5)	V
Output Amplifier Gate Bias	V_S	0	V
Substrate Bias	V_{SS}	0	V
Image Zone Clocks	ϕP low ϕP high	−12.5 (+0.5 −0.5) 3 (+0.5 −0.5)	V
Memory Zone Clocks	ϕM low ϕM high	−12.5 (+0.5 −0.5) 3 (+0.5 −0.5)	V
Output Zone Clocks	ϕL low ϕL high	−12.5 (+0.5 −0.5) 3 (+0.5 −0.5)	V
Reset Clock	ϕR low ϕR high	6 (+1.0 −1.0) 16 (+0.5 −0.5)	V

FIGURE 4(b) - LEAKAGE CURRENT ON INPUT GATES



NOTES

1. R = 1.0MΩ.

FIGURE 4 - CIRCUITS FOR ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS (CONTINUED)

FIGURE 4(c) - INPUT CLAMP VOLTAGE

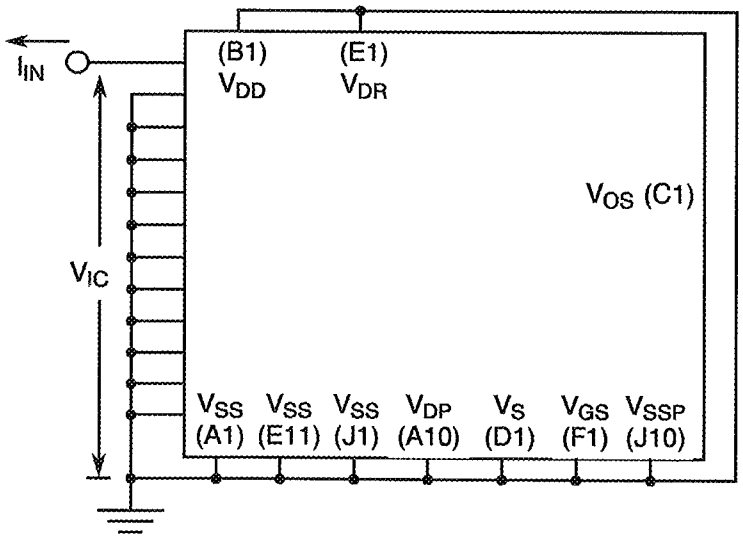
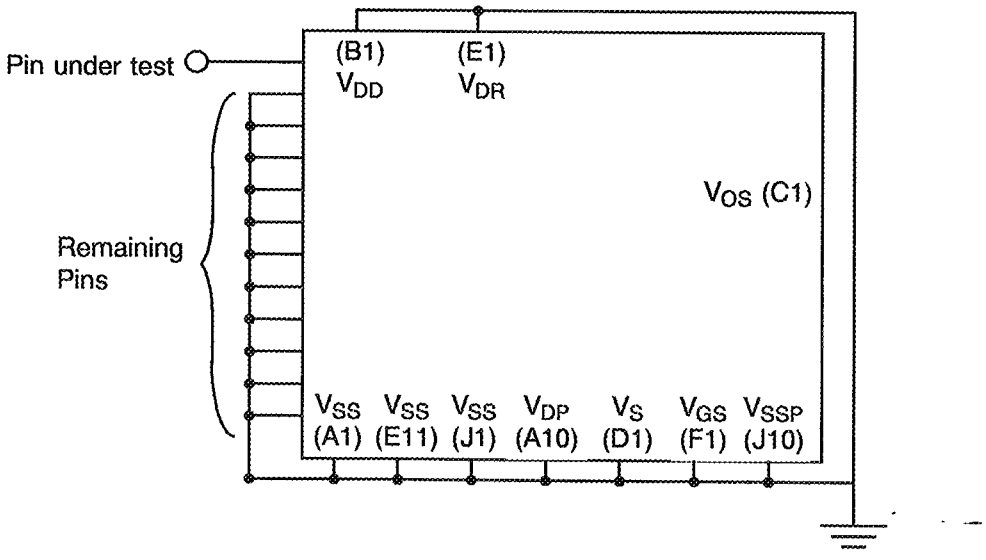


FIGURE 4(d) - INSULATION LEAKAGE CURRNT BETWEEN PINS



NOTES

1. For the measurements of pin E1 (V_{DR}), pins A10 (V_{DP}), B1 (V_{DD}) and C1 (V_{OS}) must be open.

FIGURE 4 - CIRCUITS FOR ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS (CONTINUED)

FIGURE 4(e) - POWER SUPPLY CURRENT AND DC OUTPUT LEVEL

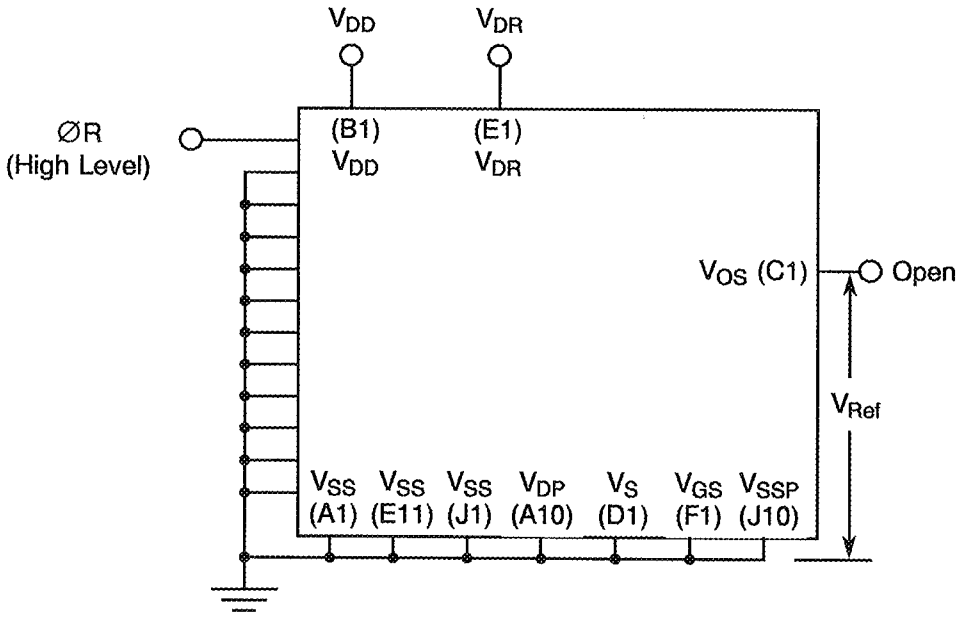
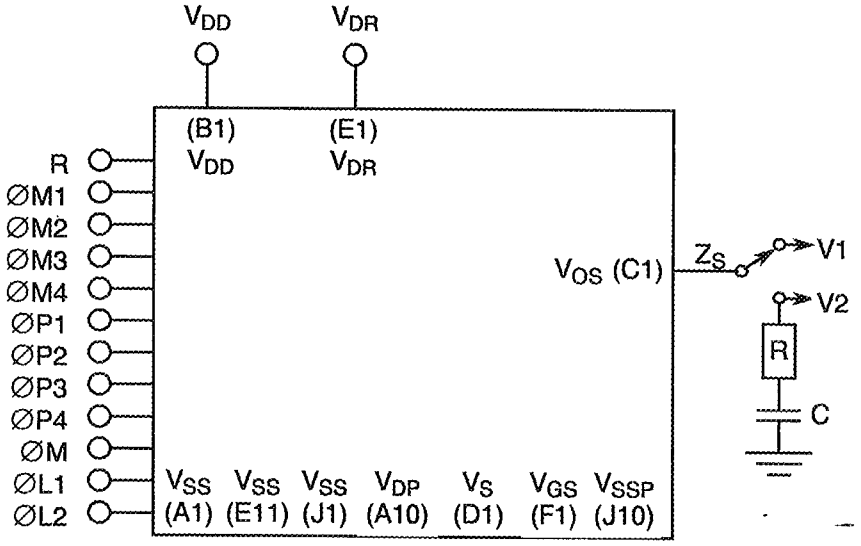


FIGURE 4(f) - OUTPUT IMPEDANCE

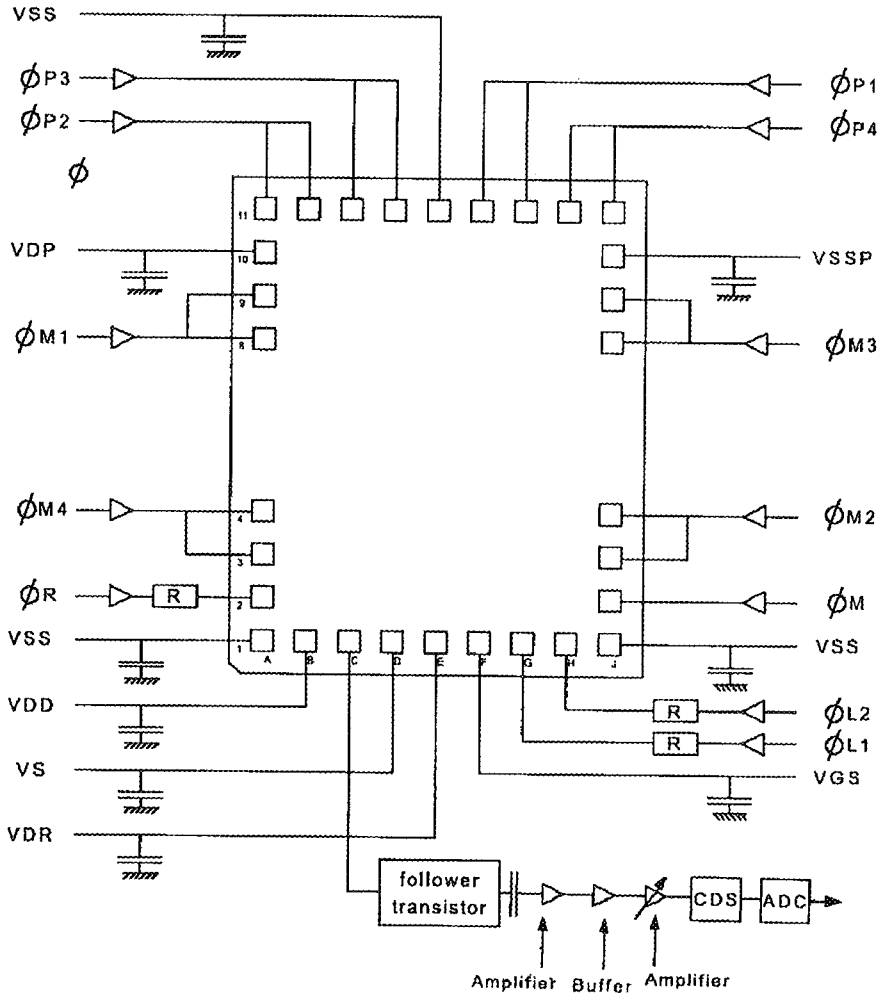


NOTES

1. All other pins shall be connected, and if required, shorted to ground.

FIGURE 4 - CIRCUITS FOR ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS (CONTINUED)

FIGURE 4(g) - DRIVING CIRCUIT

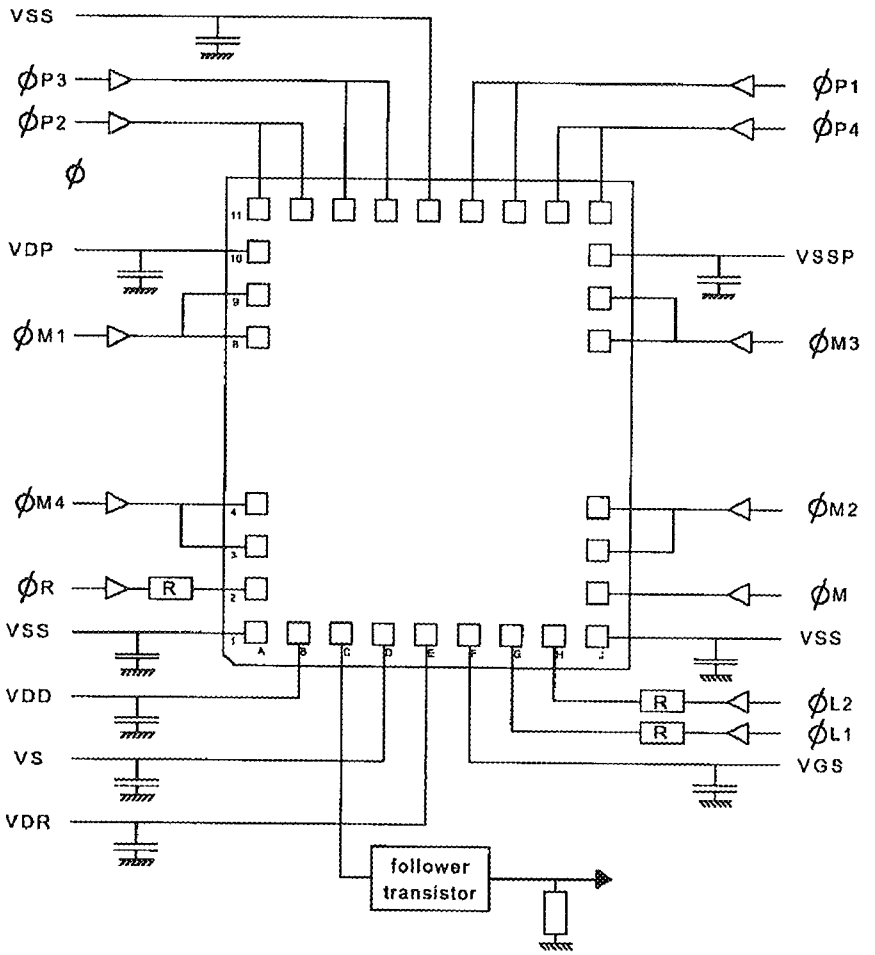


NOTES

1. R = Serial resistors to be adjusted to obtain a rise time compatible with the appropriate timing diagram.
2. C = Decoupling capacitors to be adjusted to adequately decouple.

FIGURE 4 - CIRCUITS FOR ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS (CONTINUED)

FIGURE 4(h) - VIDEO SIGNAL



NOTES

1. R = Serial resistors to be adjusted to obtain a rise time compatible with the appropriate timing diagram.
2. C = Decoupling capacitors to be adjusted to adequately decouple.

FIGURE 4 - CIRCUITS FOR ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS (CONTINUED)

OUTPUT WAVEFORM FEATURES

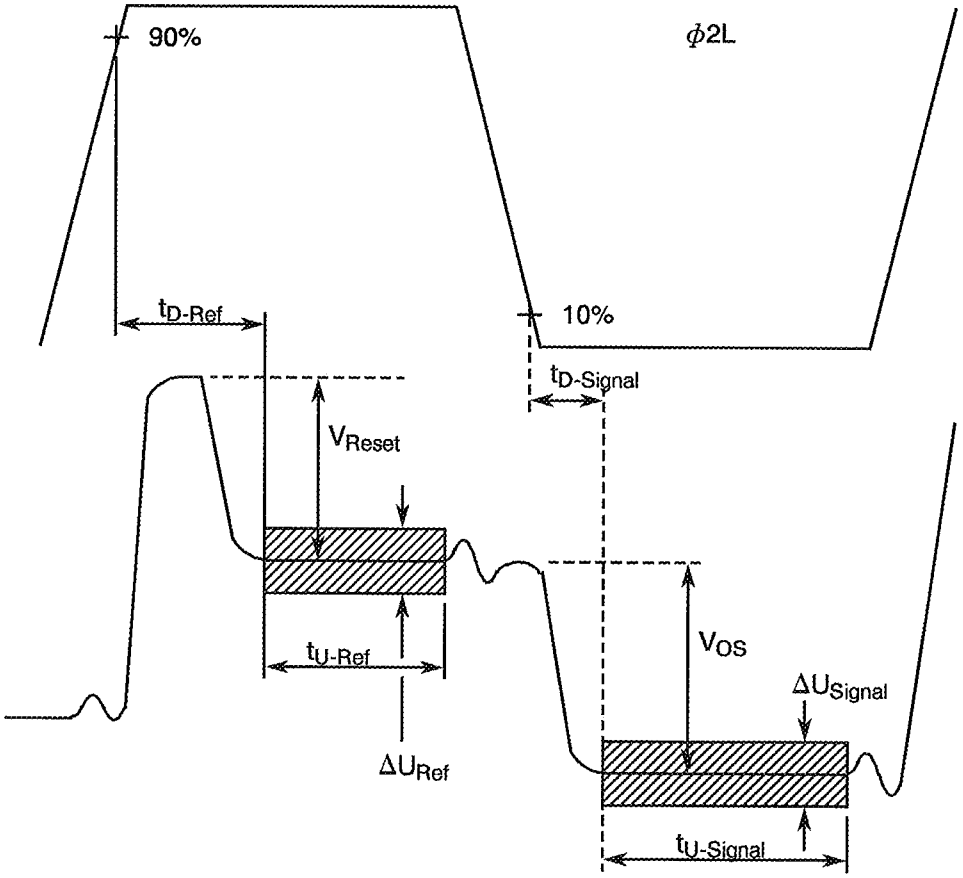


TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
01	Leakage Current on Input Gates	I_L	As per Table 2	As per Table 2	±100	pA
06 to 29	Insulation Leakage Current between Pins (Input Current)	I_E	As per Table 2	As per Table 2	±1.0	µA
30	Power Supply Current 1	I_{DD1}	As per Table 2	As per Table 2	±10	%

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

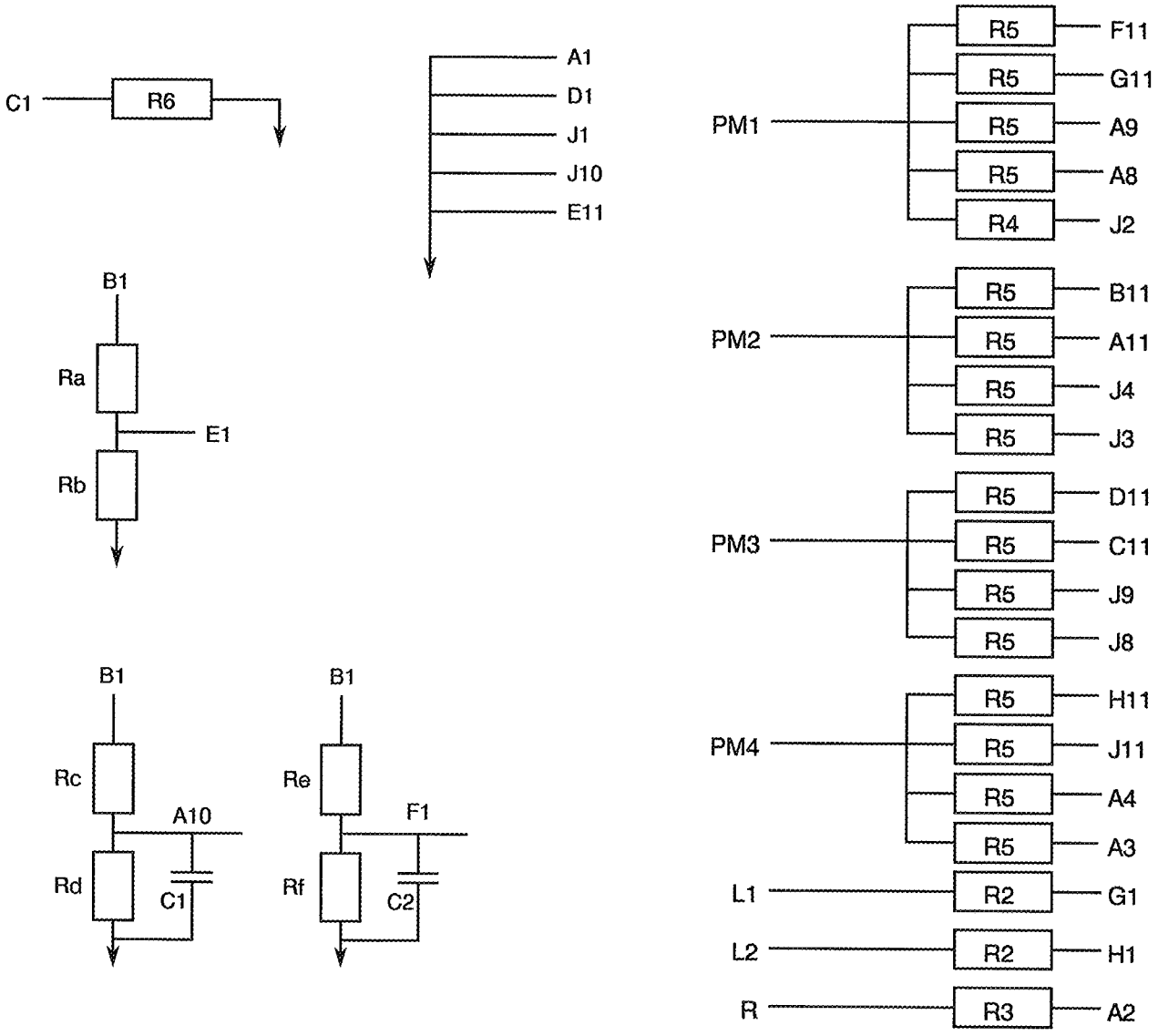
TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

No.	CHARACTERISTICS		SYMBOL	CONDITIONS	UNIT
1	Ambient Temperature		T_{amb}	+125(+0−5)	°C
2	Output Amplifier Drain Supply	(B1)	V_{DD}	18.5	V
3	Reset Bias	(E1)	V_{DR}	14.5	V
4	Protection Drain Bias		V_{DP}	5.5	V
5	Register Output Gate Bias	(F1)	V_{GS}	2.3	V
6	Output Amplifier Gate Bias	(D1)	V_S	0	V
7	Substrate Bias	(A1-E11-J1)	V_{SS}	0	V
8	Image Zone Clocks	(A11-B11-C11-D11-F11-G11-H11-J11)	ϕP	High +2.5 Low -14.5	V
9	Memory Zone Clocks	(J2)	ϕM	High +2.5 Low -14.5	V
10	Readout Register Clocks	(G1-H1)	ϕL	High +2.5 Low -14.5	V
11	Reset Clock	(A2)	ϕR	High +16.5 Low 0	V
12	Image Zone to Memory Zone and Memory Zone to Output Register Frequency		F_I	10k	Hz
13	Output Register and Reset Frequency		F_L	300k	Hz

FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

Not applicable.

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS



NOTES

1. Ra = 3.6KΩ, Rb = 13KΩ, Rc = 13KΩ, Rd = 5.6KΩ, Re = 15KΩ, Rf = 2.2KΩ, R6 = 10KΩ, Capacitance C1 and C2 = 0.1μF, R2 = R5 = 200Ω, R3 = R4 = 1kΩ.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9020)

4.8.1 Electrical and Electro-optical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{ref} \pm 3$ °C.

4.8.2 Electrical and Electro-optical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{ref} \pm 3$ °C.

4.8.3 Electrical and Electro-optical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{ref} \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9020. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(b) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9020. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

4.9 TOTAL DOSE IRRADIATION TESTING

4.9.1 Application

If specified in Para. 4.2.1 of this specification, total dose irradiation testing shall be performed in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.9.2 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6 of this specification.

4.9.3 Electrical and Electro-optical Measurements

For all Variants, the parameters to be measured prior to irradiation exposure are I_L in accordance with Table 2 and those parameters scheduled in the individual Table 1(a) for Variant 01, with the Conditions and Limits as specified in the individual Table 1(a) for the Variant in question. Only devices which meet these requirements shall be included in the test sample.

The parameters to be measured during and on completion of irradiation testing are scheduled in Table 7 of this specification.

TABLE 6 - ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	LIMITS		UNIT
						MIN.	MAX.	
01	Leakage Current on Input Gates	I_L	As per Table 2	As per Table 2	±100	As per Table 2		pA
06 to 29	Insulation Leakage Current between Pins (Input Current)	I_E	As per Table 2	As per Table 2	±1.0	As per Table 2		µA
31	Power Supply Current 1	I_{DD1}	As per Table 2	As per Table 2	±10	As per Table 2		mA
32	DC Output Level	V_{ref}	As per Table 2	As per Table 2	-	As per Table 2		V
34	Saturation Voltage for the Image Area	V_{SAT}	As per Table 2	As per Table 2	±15	As per Table 2		mV
37	Average Dark Signal	VDS	As per Table 2	As per Table 2	±30	As per Table 2		mV
38	Dark Signal Non-uniformity, standard deviation σ	DSNU(σ)	As per Table 2	As per Table 2	-	As per Table 2		mV
39	Number of Dark Signal defects beyond a3 limit	Ndef3	As per Table 2	As per Table 2	-	As per Table 2		-
40	Number of Dark Signal defects beyond a3 limit	Ndef4	As per Table 2	As per Table 2	-	As per Table 2		-
43	Responsivity	R	As per Table 2	As per Table 2	±5.0	As per Table 2		V/µJ/cm²
44	Photoresponse Non-uniformity, standard deviation σ	PRNU(σ)	As per Table 2	As per Table 2	-	As per Table 2		%
45	Number of PRNU Defects beyond a1 Limit	Ndef1	As per Table 2	As per Table 2	-	As per Table 2		-
46	Number of PRNU Defects beyond a2 Limit	Ndef2	As per Table 2	As per Table 2	-	As per Table 2		-

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING

See Figure 5(b) : Electrical circuit for power burn-in and operating life test

TABLE 7 - ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS			UNIT
					T0 (1)	T1 (1)	T2 (1)	
14	Average Dark Signal	VDS	As per Table 2	As per Table 2	2.0	75	300	mV
50	Leakage Current on Input Gates	I_L	As per Table 2	As per Table 2	300	300	300	pA
51	Power Supply Current 1	I_{DD1}	As per Table 2	As per Table 2	7.0	10	10	mA

NOTES

1. T0 = Initial Measurement

   T1 = Measurements on completion of Irradiation Testing

   T2 = Measurements after annealing

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION

TYPE VARIANT No. 01

No.	CHARACTERISTICS	SYMBOL	LIMITS			UNITS	REMARKS
			MIN.	TYP.	MAX.		
1	Operating Temperature Range	T_{op}	−20	-	+85	°C	
2	Reference Temperature	T_{ref}	+19	+22	+25	°C	
3	Flatness of Image Area	P	-	-	30	µm	At +25 ± 3 °C
4	Spectral Range for Optical Coating on Window	WOC	400	-	900	nm	< 1% per side
5	Timing Diagram	TD	-	-	-	-	TD1
6	Power Supply Current 1	I_{DD1}	-	-	7	mA	Static
7	Power Supply Current 2	I_{DD2}	N/A			mA	Dynamic
8	Power Supply Current 1 over T_{op}	I_{DD2} (T_{op})	-	-	8	mA	Dynamic
9	DC Output Level	V_{Ref}	-	-	13	V	
10	Output Impedance	Z_S	N/A			Ω	
11	Saturation Voltage for the Image Area	V_{SAT}	600	-	-	mV	
12	Vertical Charge Transfer Inefficiency	VCTI	-	-	6.0	%	At Vsat/2
13	Horizontal Charge Transfer Inefficiency	HCTI	-	-	3.0	%	At Vsat/2
14	Average Dark Signal	VDS	-	-	8.0	mV	Ti = 1S
15	Average Dark Signal (Image Area + Storage Area) over T_{OP}	VDS(T_{op})	-	-	100	mV	Ti = 100mS
16	Dark Signal Non-uniformity, standard deviation σ	DSNU(σ)	-	-	3.0	mV	Ti = 1S
17	Number of Dark Signal Defects beyond a3 limit	Ndef3	-	-	10	-	Ti = 1S

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION (CONTINUED)

TYPE VARIANT No. 01

No.	CHARACTERISTICS	SYMBOL	LIMITS			UNITS	REMARKS
			MIN.	TYP.	MAX.		
18	Number of Dark Signal Defects beyond a4 limit	Ndef4	N/A			-	Ti = 1S
19	DSNU Limit for Ndef3	a3	-	-	10	mV	Ti = 1S
20	DSNU Limit for Ndef4	a4	N/A			mV	Ti = 1S
21	Responsivity	R	6.0	-	-	V/μJ/cm²	BG38 optical filter
22	Responsivity over T_{op}	$R(T_{op})$	6.0	-	-	V/μJ/cm²	BG38 optical filter
23	Photoresponse Non-uniformity, standard deviation σ	PRNU(σ)	-	-	2.0	%	At Vsat/2
24	Number of PRNU defects beyond a1 limit	Ndef1	-	-	10	-	At Vsat/2
25	Number of PRNU defects beyond a2 limit	Ndef2	-	-	0	-	At Vsat/2
26	PRNU limit for Ndef1	a1	-	-	20	%	At Vsat/2
27	PRNU limit for Ndef2	a2	-	-	50	%	At Vsat/2
28	Spectral Responsivity in Optical Band B1	R(B1)	N/A			V/μJ/cm²	
29	Spectral Responsivity in Optical Band B2	R(B2)	N/A			V/μJ/cm²	517/81nm
30	Spectral Responsivity in Optical Band B3	R(B3)	N/A			V/μJ/cm²	610/98nm
31	Spectral Responsivity in Optical Band B4	R(B4)	N/A			V/μJ/cm²	703/94nm
32	Spectral Responsivity in Optical Band B5	R(B5)	N/A			V/μJ/cm²	827/98nm
33	Spectral Responsivity in Optical Band B6	R(B6)	N/A			V/μJ/cm²	900/105nm
34	Spectral Responsivity in Optical Band B7	R(B7)	N/A			V/μJ/cm²	
35	Linearity Error	LE	N/A			%	
36	Temporal Noise	V_N	N/A			μV	
37	Offset Voltage	V_{Offset}	N/A			mV	

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION (CONTINUED)

TYPE VARIANT No. 01

No.	CHARACTERISTICS	SYMBOL	LIMITS			UNITS	REMARKS
			MIN.	TYP.	MAX.		
38	Amplitude of Reset Feedthrough	V_{Reset}	N/A			mV	
39	Reference Level Settling Time	$t_{D\text{-}Ref}$	N/A			ns	
40	Reference Level Duration	$t_{U\text{-}Ref}$	N/A			ns	
41	Reference Level Error Band	ΔU_{Ref}	N/A			mV	
42	Signal Level Settling Time	$t_{D\text{-}Signal}$	N/A			ns	
43	Signal Level Duration	$t_{U\text{-}Signal}$	N/A			ns	
44	Signal Level Error Band	ΔU_{Signal}	N/A			mV	
45	Electrode Capacitance	$C\phi P$	N/A			pF	
46	Electrode Capacitance	$C\phi M$	N/A			pF	
47	Electrode Capacitance	$C\phi L$	N/A			pF	
48	Electrode Capacitance	$C\phi R$	N/A			pF	
49	Charge to Voltage Conversion Factor	CVF	N/A			µV/e	5 non deliverable devices/lot

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION

TYPE VARIANT No. 02

No.	CHARACTERISTICS	SYMBOL	LIMITS			UNITS	REMARKS
			MIN.	TYP.	MAX.		
1	Operating Temperature Range	T_{op}	−40	-	+85	°C	
2	Reference Temperature	T_{ref}	−23	−20	−17	°C	
3	Flatness of Image Area	P	-	-	30	µm	At +25 ± 3 °C
4	Spectral Range for Optical Coating on Window	WOC	400	-	900	nm	< 1% per side
5	Timing Diagram	TD	-	-	-	-	TD1
6	Power Supply Current 1	I_{DD1}	-	-	5	mA	Static
7	Power Supply Current 2	I_{DD2}	N/A			mA	Dynamic
8	Power Supply Current 1 over T_{op}	I_{DD1} (T_{op})	-	-	8	mA	Static
9	DC Output Level	V_{Ref}	-	-	13	V	
10	Output Impedance	Z_S		700		Ω	
11	Saturation Voltage for the Image Area	V_{SAT}	800	950	-	mV	
12	Vertical Charge Transfer Inefficiency	VCTI	-	-	6.0	%	At Vsat/2
13	Horizontal Charge Transfer Inefficiency	HCTI	-	-	3.0	%	At Vsat/2
14	Average Dark Signal	VDS	-	-	2.0	mV	Ti = 40S
15	Average Dark Signal (Image Area + Storage Area) over T_{OP}	VDS(T_{op})	-	-	100	mV	Ti = 100mS
16	Dark Signal Non-uniformity, standard deviation σ	DSNU(σ)	-	-	2.0	mV	Ti = 1S
17	Number of Dark Signal Defects beyond a3 limit	Ndef3	-	-	10	-	Ti = 40S

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION (CONTINUED)

TYPE VARIANT No. 02

No.	CHARACTERISTICS	SYMBOL	LIMITS			UNITS	REMARKS
			MIN.	TYP.	MAX.		
18	Number of Dark Signal Defects beyond a4 limit	Ndef4	N/A			-	
19	DSNU Limit for Ndef3	a3	-	-	20	mV	Ti = 40S
20	DSNU Limit for Ndef4	a4	N/A			mV	
21	Responsivity	R	9.0	10.8	-	V/μJ/cm²	BG38 optical filter
22	Responsivity over T_{op}	$R(T_{op})$	6.0	-	-	V/μJ/cm²	BG38 optical filter
23	Photoresponse Non-uniformity, standard deviation σ	PRNU(σ)	-	-	2.0	%	At Vsat/2
24	Number of PRNU defects beyond a1 limit	Ndef1	-	-	10	-	At Vsat/2
25	Number of PRNU defects beyond a2 limit	Ndef2	-	-	0	-	At Vsat/2
26	PRNU limit for Ndef1	a1	-	-	20	%	At Vsat/2
27	PRNU limit for Ndef2	a2	-	-	50	%	At Vsat/2
28	Spectral Responsivity in Optical Band B1	R(B1)	N/A			V/μJ/cm²	
29	Spectral Responsivity in Optical Band B2	R(B2)	6.0	8.5	-	V/μJ/cm²	517/81nm
30	Spectral Responsivity in Optical Band B3	R(B3)	7.0	13.6	-	V/μJ/cm²	610/98nm
31	Spectral Responsivity in Optical Band B4	R(B4)	8.0	14.5	-	V/μJ/cm²	703/94nm
32	Spectral Responsivity in Optical Band B5	R(B5)	8.0	14.5	-	V/μJ/cm²	827/98nm
33	Spectral Responsivity in Optical Band B6	R(B6)	6.0	10	-	V/μJ/cm²	900/105nm
34	Spectral Responsivity in Optical Band B7	R(B7)	N/A			V/μJ/cm²	
35	Linearity Error	LE	-	-	3.0	%	20mV to 500mV
36	Temporal Noise	V_N	-	-	400	μV	
37	Offset Voltage	V_{Offset}	N/A			mV	

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION (CONTINUED)

TYPE VARIANT No. 02

No.	CHARACTERISTICS	SYMBOL	LIMITS			UNITS	REMARKS
			MIN.	TYP.	MAX.		
38	Amplitude of Reset Feedthrough	V_{Reset}	N/A			mV	
39	Reference Level Settling Time	$t_{D\text{-}Ref}$	N/A			ns	
40	Reference Level Duration	$t_{U\text{-}Ref}$	N/A			ns	
41	Reference Level Error Band	ΔU_{Ref}	N/A			mV	
42	Signal Level Settling Time	$t_{D\text{-}Signal}$	N/A			ns	
43	Signal Level Duration	$t_{U\text{-}Signal}$	N/A			ns	
44	Signal Level Error Band	ΔU_{Signal}	N/A			mV	
45	Electrode Capacitance	$C\phi P$	-	-	5 000	pF	
46	Electrode Capacitance	$C\phi M$	-	-	5 000	pF	
47	Electrode Capacitance	$C\phi L$	-	-	300	pF	
48	Electrode Capacitance	$C\phi R$	-	-	30	pF	
49	Charge to Voltage Conversion Factor	CVF	3.0	-	-	µV/e	5 non deliverable devices/lot

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION

TYPE VARIANT No. 03

No.	CHARACTERISTICS	SYMBOL	LIMITS			UNITS	REMARKS
			MIN.	TYP.	MAX.		
1	Operating Temperature Range	T_{op}	−40	-	+85	°C	
2	Reference Temperature	T_{ref}	−23	−20	−17	°C	
3	Flatness of Image Area	P	-	-	30	µm	At +25 ± 3 °C
4	Spectral Range for Optical Coating on Window	WOC	400	-	900	nm	< 1% per side
5	Timing Diagram	TD	-	-	-	-	TD1
6	Power Supply Current 1	I_{DD1}	-	3.0	5	mA	Static
7	Power Supply Current 2	I_{DD2}	N/A			mA	Dynamic
8	Power Supply Current 1 over T_{op}	I_{DD1} (T_{op})	-	-	8	mA	Static
9	DC Output Level	V_{Ref}	-	9.8	13	V	
10	Output Impedance	Z_S	700			Ω	
11	Saturation Voltage for the Image Area	V_{SAT}	800	950	-	mV	
12	Vertical Charge Transfer Inefficiency	VCTI	-	-	6.0	%	At Vsat/2
13	Horizontal Charge Transfer Inefficiency	HCTI	-	-	3.0	%	At Vsat/2
14	Average Dark Signal	VDS	-	-	2.0	mV	Ti = 40S
15	Average Dark Signal (Image Area + Storage Area) over T_{OP}	VDS(T_{op})	-	-	100	mV	Ti = 100mS
16	Dark Signal Non-uniformity, standard deviation σ	DSNU(σ)	-	-	1.0	mV	Ti = 40S
17	Number of Dark Signal Defects beyond a3 limit	Ndef3	-	-	10	-	Ti = 40S

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION (CONTINUED)

TYPE VARIANT No. 03

No.	CHARACTERISTICS	SYMBOL	LIMITS			UNITS	REMARKS
			MIN.	TYP.	MAX.		
18	Number of Dark Signal Defects beyond a4 limit	Ndef4	N/A			-	
19	DSNU Limit for Ndef3	a3	-	-	20	mV	Ti = 40S
20	DSNU Limit for Ndef4	a4	N/A			mV	
21	Responsivity	R	9.0	10.8	-	V/μJ/cm²	BG38 optical filter
22	Responsivity over T_{op}	$R(T_{op})$	6.0	-	-	V/μJ/cm²	BG38 optical filter
23	Photoresponse Non-uniformity, standard deviation σ	PRNU(σ)	-	-	2.0	%	At Vsat/2
24	Number of PRNU defects beyond a1 limit	Ndef1	-	-	10	-	At Vsat/2
25	Number of PRNU defects beyond a2 limit	Ndef2	-	-	0	-	At Vsat/2
26	PRNU limit for Ndef1	a1	-	-	20	%	At Vsat/2
27	PRNU limit for Ndef2	a2	-	-	50	%	At Vsat/2
28	Spectral Responsivity in Optical Band B1	R(B1)	N/A			V/μJ/cm²	
29	Spectral Responsivity in Optical Band B2	R(B2)	6.0	8.5	-	V/μJ/cm²	517/81nm
30	Spectral Responsivity in Optical Band B3	R(B3)	7.0	13.6	-	V/μJ/cm²	610/98nm
31	Spectral Responsivity in Optical Band B4	R(B4)	8.0	14.5	-	V/μJ/cm²	703/94nm
32	Spectral Responsivity in Optical Band B5	R(B5)	8.0	14.5	-	V/μJ/cm²	827/98nm
33	Spectral Responsivity in Optical Band B6	R(B6)	6.0	10	-	V/μJ/cm²	900/105nm
34	Spectral Responsivity in Optical Band B7	R(B7)	N/A			V/μJ/cm²	
35	Linearity Error	LE	-	-	3.0	%	20mV to 500mV
36	Temporal Noise	V_N	-	-	400	μV	
37	Offset Voltage	V_{Offset}	N/A			mV	

TABLE 1(a) - TYPE VARIANT DETAILED INFORMATION (CONTINUED)

TYPE VARIANT No. 03

No.	CHARACTERISTICS	SYMBOL	LIMITS			UNITS	REMARKS
			MIN.	MIN.	MAX.		
38	Amplitude of Reset Feedthrough	V_{Reset}	N/A			mV	
39	Reference Level Settling Time	$t_{D\text{-}Ref}$	N/A			ns	
40	Reference Level Duration	$t_{U\text{-}Ref}$	N/A			ns	
41	Reference Level Error Band	ΔU_{Ref}	N/A			mV	
42	Signal Level Settling Time	$t_{D\text{-}Signal}$	N/A			ns	
43	Signal Level Duration	$t_{U\text{-}Signal}$	N/A			ns	
44	Signal Level Error Band	ΔU_{Signal}	N/A			mV	
45	Electrode Capacitance	$C\phi P$	N/A			pF	
46	Electrode Capacitance	$C\phi M$	N/A			pF	
47	Electrode Capacitance	$C\phi L$	N/A			pF	
48	Electrode Capacitance	$C\phi R$	N/A			pF	
49	Charge to Voltage Conversion Factor	CVF	N/A			µV/e	5 non deliverable devices/lot