Radiation Pre-Evaluation of Actel A1280A, RH1280 and A1460A

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Abstract

The objective of this work has been to perform Heavy Ion, Proton and Total Dose Tests of three different types of Field Programmable Gate Arrays (FPGA).

I. INTRODUCTION

Actel FPGA's have gradually evolved since the initial device type first was introduced. This study comprises two families of available Actel FPGA's named "ACT2" and "ACT3". The ACT2 family added to the original family transparent latches to the input and output paths in the I/O-modules, and introduced S-modules, basically a C-module followed by a dedicated flip-flop. The S-module flip-flop can be configured as either an edge-triggered unit, or a transparent latch. The ACT3 series replaced the transparent latches in the I/O modules with triggered flip-flops driven by a high performance clock.

Within the last few years the SEU and Total Dose vulnerability have been tested for various Actel FPGA types. The Total dose results show large variation in tolerance for various types of FPGA's, while the Heavy Ion results indicate about the same sensitivity for the different FPGA types, but large difference in sensitivity between C, S and I/O modules. In order to recommend the use of these devices in space application, additional testing and analysis is needed to further characterise these types of components.

II. SAMPLE SELECTION

The following three different types of Actel FPGA's have been tested

Actel A1280A employing antifuse technology implemented in silicon gate, 1.0 μm, two-level metal CMOS.

Number of test samples:	12
Screening level:	Mil Temp
Date code:	9510
Chip manufacturer:	Matshushita
Package:	176-pin CPGA

Actel A1460A implemented in silicon gate, 0.8 μ m, two-level metal CMOS.

Number of test samples:	11
Screening level:	Mil Temp
Date code:	9451
Chip manufacturer:	Matshushita
Package:	207-pin CPGA

RH1280 is manufactured by Lookheed Martin Federal Systems in a Rad Hard process and distributed by Actel. Basically, the device resembles the A1280A in structure, but differs in timing. The devices employ antifuse technology implemented in silicon gate, 0.8 μm, two-level metal CMOS on an epi process.

Number of test samples:	5
Screening level:	QML
Date code:	9617 (?)
Chip manufacturer:	Loral Federal Systems
Package:	172-pin CQFP

III. TEST TECHNIQUES

A. General

The general concept is to load data into the DUT's, pause for a pre-set time and thereafter read data and check for errors.

A flow chart of the test sequence is given in Fig 1. Any detected errors will be store in memory, the DUT will be reseted and new data will be loaded again. The cycle will then be repeated. Failing read/write operations from/to the DUT will determine the functionality criteria. The clock speed used for SEU test was 50 kHz. For convenience, the same clock speed was use for in-situ function test at total dose irradiation. For each DUT errors can be traced down to logic module, logic value and position.

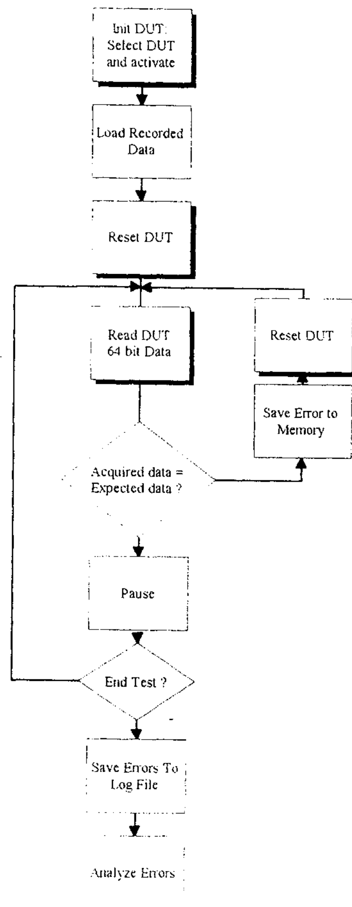

Fig. 1 Flow chart of the test sequence.

B. Test Boards

Three different types of printed circuit board, one for each FPGA type, were designed and manufactured. Each test board can house 3 Device Under Test (DUT). The DUT's will be tested using a "virtual golden chip" test method. The principal of the measuring technique is to compare each output from the DUT with the correct data controlled via a PC.

The DUT is continually cycled while the outputs of selected ring counters are compared by the "golden chip" with three times over sampling. When an error is found (when outputs do not match), the state of all outputs and position in cycle of the failing ring counter will be temporarily stored in the memory. The ring counters (DUT) are then reset.

C. Dut Layout

The general layout structure for all three types of FPGA's consist of ring counters for each type of logical modules.
The S-module is the more complex of the two modules and can be forced to act as a C-module by "by-pass" of other functions. The S-module is very sensitive to SEU while the C-module part of the S-module has till now been considered identical to the C-module in SEU sensitivity.
Information given by Actel pointed to the fact that a flip-flop made out of two C-modules has different SEU vulnerability than a flip-flop made up of a C-module and a "by-pass S-module". The DUT layout for the C-modules was designed to test the information from Actel.

The I/O module is considered equal to the C-module in SEU sensitivity.

For all three device types the C -module rings have been designed using two type of macros, DFP1B for logic "1" (high level) and DFPC for logic "0" (low level). Every second flip-flop is the inverted logical function of the presiding flip-flop. Flip-flops made up of a C-module and a "by-pass S" use the same technique and have been created by the use of the same macros and knowledge of the actual physical location of the individual modules on the chip. This information have been provided by Actel. The S-module rings have been designed using macro DFP1E and tested at logic "1" only. Design of the I/O module has been performed for A1280 and RH1280 with macros IR and ORH for input and output, respectively, and for A1460A with macros IREC and ORECTH for input and output, respectively.

IV. HEAVY ION TEST

A. *Equipment & Facility*

Heavy ion test was performed at the Tandem Van de Graaff accelerator facility at Brookhaven National Laboratory.

The irradiations were performed with all three test boards mounted at the same time on a movable frame. The three test boards were mounted on top of each other displaced in distanse so as the DUT's from all boards could be exposed to the heavy ion beam. Thus, for the heavy ion test of 3 times 3 devices it was not necessary to open up the vacuum chamber for change of devices or test boards.
Each board was separately connected via feed through connectors through the vacuum chamber. During irradiation the samples were monitored for latch-up.

Table I. Ion Beam Data

Ion Specie	Energy (MeV)	Tilt Angle (Degree)	LET (MeV m g/cm2)	Range (μm)
F-19	140	0	3.4	120
		45	4.8	85
		60	6.8	60
Si-28	190	0	7.8	79
		45	11.0	56
		60	15.6	39
Ni-58	265	0	26.6	42
		35	32.5	35
		45	37.6	30
		60	53.2	21
I-127	345	0	59.9	33
		30	84.7	23
		45	120.0	16

B. *Results*

The results are presented for each device type in a graphical form showing the SEU cross section per cm^2 per bit versus the LET values. The LET range was obtained by changing the ion species and the angle of incidence between the beam and the chip. Table I provide the data of the ions used. Cross sections given in the figure captions are taken to be the asymptotic value at large LET. The threshold value is taken to be the value at 1 % of the cross section value.

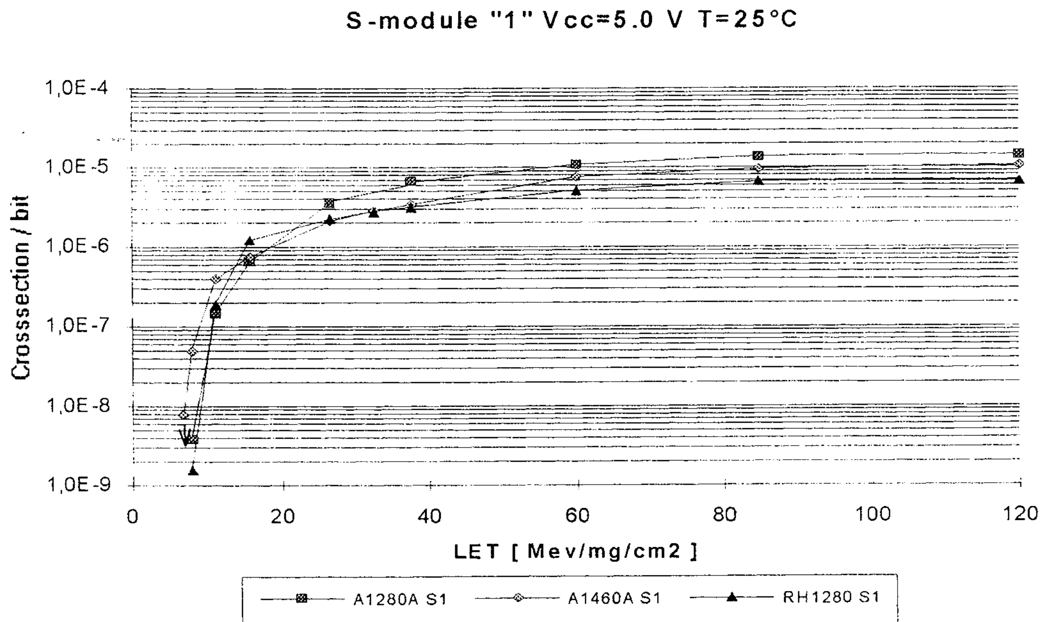

Fig 2: S-Module Upset Cross Section for logic "1"
S/W Macro : DFP1E for logic "1"
Test Condition : Static, Vcc = 5 V
Tamb = Room Temp
Test Devices : A1280A, RH1280, A1460A

Comments : Average data of 3 test samples from each device type. The cross section for RH1280, $6E^{-6}$ cm^2/bit, is a factor of 2 better than A1280A.

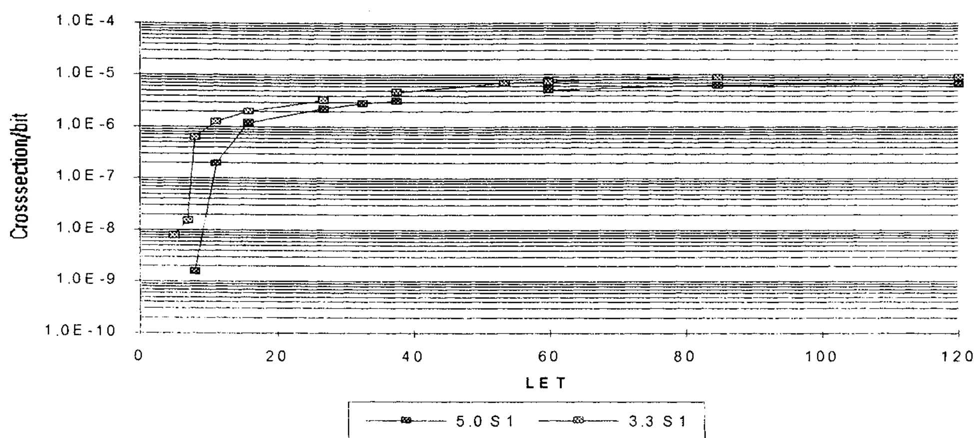

Fig 3: **RH1280 S-Module 5V and 3.3V Upset Cross Section for logic "1"**

S/W Macro : DFP1E for logic "1"
Test Condition : Static, Vcc = 5 V, 3.3V
Tamb = Room Temp
Test Devices : RH1280
RH1280 :
Cross Section : 6 E-6 cm^2/bit
Threshold : 10 MeV/mg/cm^2
Comments : Average data of 3 test samples. The cross section for 5V is a factor 2 better than 3.3V. The threshold is lower for 3.3V.

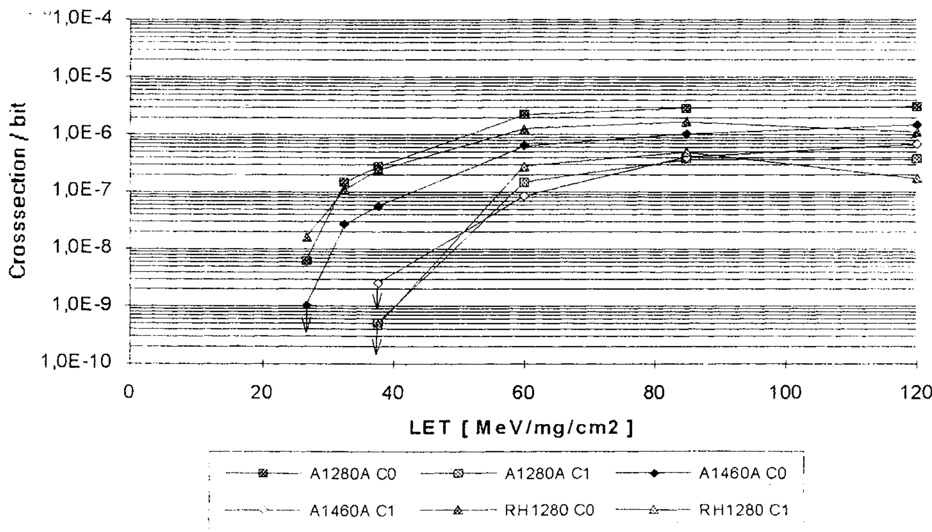

Fig 4: **C-Module Upset Cross Section for logic "1" and "0"**

S W Macro : DFP1B logic "1" , DFPC logic "0"
Test Condition : Static, Vcc = 5 V
Tamb = Room Temp
Test Devices : A1280A, RH1280, A1460A

Comments : Average data of 3 test samples from each device type.
The cross sections for "1" are within a factor 2 at LET=60 MeV/mg/cm^2 for the three device types and in average a factor 10 lower than the cross section for logic "0".

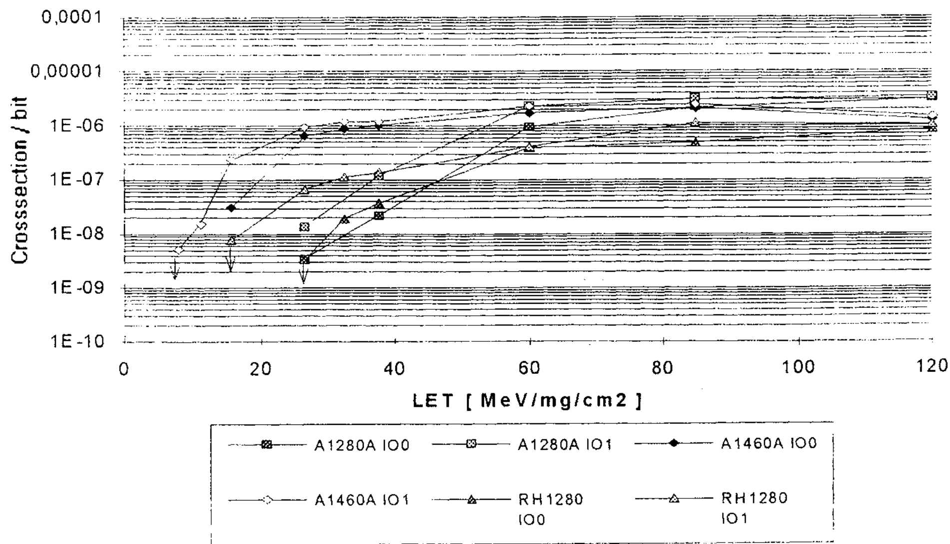

Fig 5:	**I/O-Module Upset Cross Section for logic "1" and "0"**	Comments :	Average data of 3 test samples from each device type. The cross sections for RH1280 are a factor 2 lower than the other two. A1460 has a low threshold value at just above LET 10 MeV/mg/cm^2 .
S/W Macro :	1280: ORH output "1", IP input "0" A1460A: ORECTH "1", IREC "0"		
Test Condition :	Static, Vcc = 5 V Tamb = Room Temp		
Test Devices :	A1280A, RH1280, A1460A		

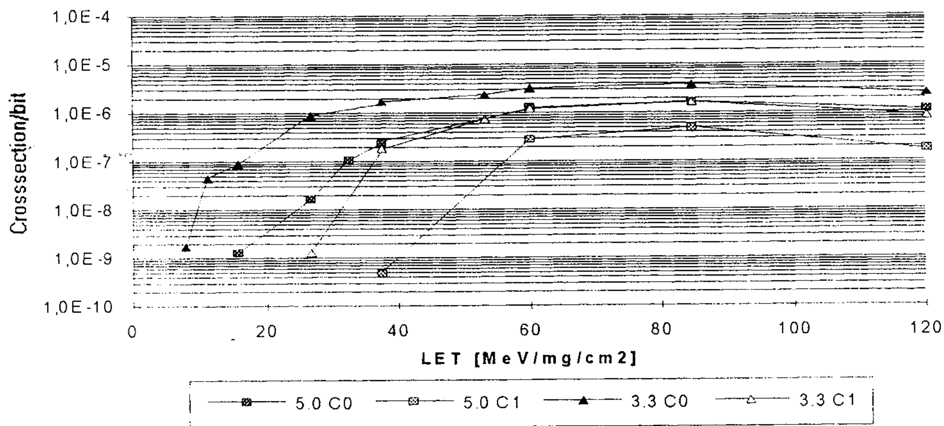

Fig 6:	**RH1280 C-Module Upset Cross Section for 5V and 3.3V logic "1" and "0"**	Comments :	Average data of 3 test samples. 3.3V data show a factor 3-5 higher cross section and 10-15 MeV/mg/cm^2 lower threshold values.
S/W Macro :	DFP1B logic "1", DFPC logic "0"		
Test Condition :	Static, Vcc = 5 V and 3.3V Tamb = Room Temp		
Test Devices :	RH1280		

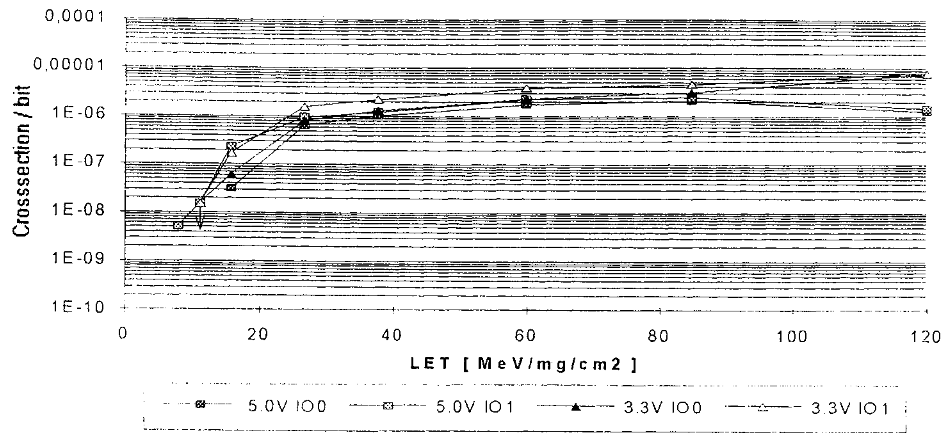

Fig 7: A1460 I/O-Module Upset Cross Section for 5V and 3.3V logic "1" and "0"

Comments : Average data of 3 test samples. The data show a similar cross section and threshold.

S/W Macro : ORECTH logic "1" , IREC logic "0"
Test Condition : Static, Vcc = 5 V and 3.3V
Tamb = Room Temp
Test Devices : A1460A

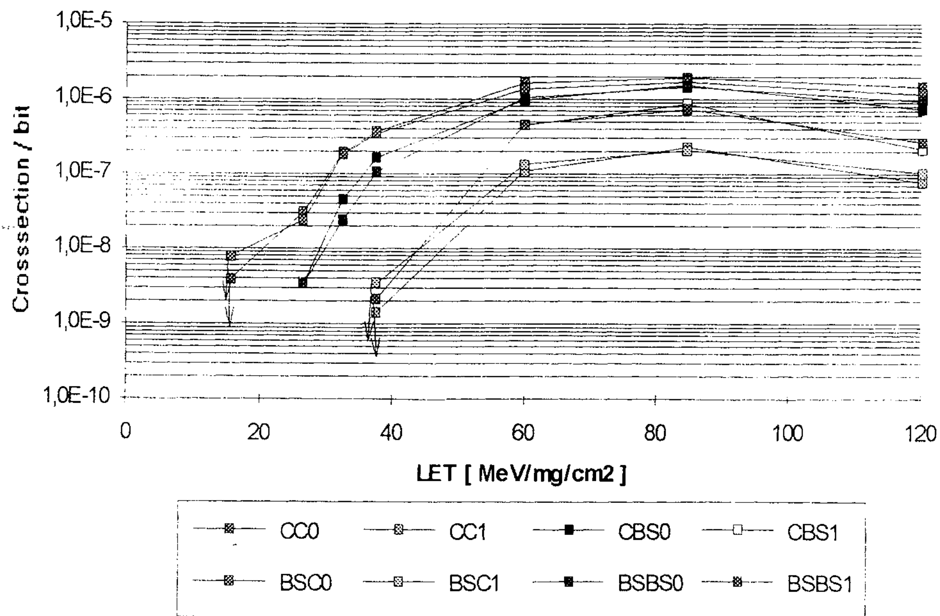

Fig 8: RH1280 C-Module - By-pass S Upset Cross Section , 5V "1" and "0"

S W Macro : DFP1B logic "1" , DFPC logic "0"
Test Condition : Static, Vcc = 5 V
Tamb = Room Temp
Test Devices : RH1280
Comments : Average data of 3 test samples.
The graph shows SEU data for flip-flops made up of C-C, C-BypassS (CBS) and BypassS-BypassS modules for "0" and "1" respectively.

V. PROTON TESTS

A. Equipment & Facility

Proton test was performed at the Proton Irradiation Facility (PIF) at Paul Scherrer Institute, Villigen, Switzerland. Protons of energy of 300 MeV was used with a flux of maximum10^8 protons/s / cm^2. The ion energy on target can instantly and continuously be attenuated by Aluminium slides from maximum energy down to about 30 MeV. Energy attenuation of the proton beam results in strongly reduced flux.
Due to the limited number of proton induced upsets for the chosen FPGA types, the present tests were only performed at proton energies of 300 and 150 MeV. The DUT is irradiated in air at normal incident angle.

B. Results

The RH1280 and the A1460A were tested at 3.3 V and at 5 V. Only S-module upsets were observed for RH1280. A1460A indicated I/O upsets as well. In Fig 9, the average proton upset cross section for both 3.3 V and 5 V are shown.

Table II. Proton induced upsets on RH1280. Average data of three test samples.

Vcc (Volt)	Energy (MeV)	Fluence (prot/cm2)	S-Module # Upsets	S-Module Cross Section (/cm2 *bit)
3.3	150	4,9E+10	2	3,2E-13
3.3	300	3,2E+11	46	1,2E-12
5	150	5E+10	1	1,6E-13
5	300	2,6E+11	12	3,6E-13

Table III. Proton induced upset for A1460A. Average data of three test samples.

Vcc	Energy Mev	Fluence	S-Module #upsets	I/O-Module #upsets	S-Module Cross Section '/cm2 * bit	I/O-Module Cross Section '/cm2 * bit
3,3	300	2,0E+11	22	5	8,6E-13	2,0E-13
5	300	1,0E+11	9	0	3,0E-13	7,8E-14

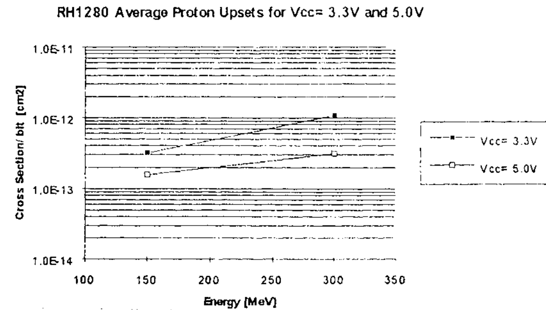

Fig 9 :	**Actel RH1280, S-Modules Average Proton Induced Upset Cross**
S/W Macro :	DFP1E for logic "1"
Test Condition :	Static, Vcc = 5 V, 3.3 V Tamb = Room Temp
Test Samples :	RH1280
Data Points:	300 MeV; Average over 3 test samples 150 MeV; one test sample
Average Cross Section (σ) :	300 MeV , 5V 3.6 E-13 cm^2 /bit 300 MeV , 3.3 V 1.2 E-12 cm^2 /bit

VI. TOTAL DOSE TEST

A. Equipment & Facility

Three samples of each types A1280A and A1460A were tested. Each device type were irradiated under steady state Vcc=5.0 V at a dose rate of 560 rad(Si) per hour. All parts were programmed with the test pattern presented earlier.
The supply current and function of devices were monitored in-situ. Functional tests were performed at 50 kHz with V_{CC}= 5.0 V. The definition of functional failure is when read data do not match with pre-defined data.
Function, the supply current and the supply voltage for each DUT were measured and stored about every 10th minute. After irradiation, the devices were subjected to biased room temperature anneal for one week.

B. Results

The results for A1280A show that the supply current start to increase already at about 5 krad(Si) cumulated dose. At 15 Krad(Si) the current has reached 200 mA. Pre-irradiation current value was in average around 0.02 mA.

For A1460A, the supply current as a function of cumulated dose and following biased room temperature anneal are shown in Figs 10 and 11 Pre-irradiation current value was in average about 0.7 mA.

The supply current started to slowly increase due to irradiation at about 15 krad(Si) resulting in an average value of about 20 mA at 50 krad(Si) cumulated dose. First functional failure was detected at 54 krad(Si).

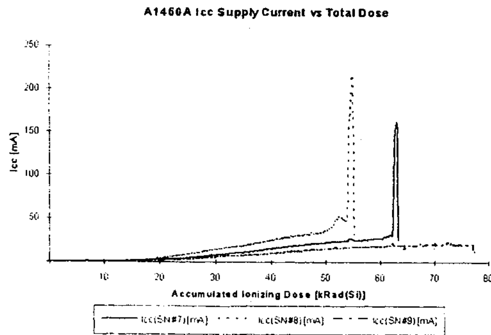

Fig 10. A1460A Icc as a function of cumulated total dose. Large variation between the test samples are observed.

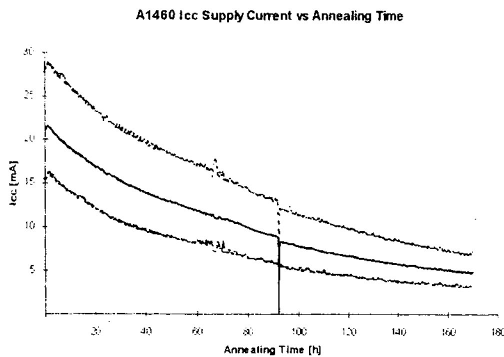

Fig 11. Room temperature biased anneal. Icc as a function of time. The dip above 90 h is due to shut down of main power. The device type show fast anneal of radiation damages.

VII. DISCUSSIONS

A. Heavy Ion

No latch-up was detected for any of the device types, either at 5V nor at 3.3V.

Actel have indicated that flip-flops made out of two C-modules may have different SEU vulnerability than flip-flops made out of a C-module and a "by-pass S-module". The design for the present study was made to cope with the this information. The results, however, give no clear indication of different SEU sensitivity depending how the C-module flip-flop state is created. Fig 8 give an overview of the different variants of C-module registers. The spread that can be observed are likely due to poor statistics in the various data points and also individual spread among the devices. None of the RH1280 devices were marked, but claimed by Actel to come from the same manufacturing lot.

Upset rate calculations using Space Radiation, Empirical model (ver. 4.0) are given below for GEO Polar orbit. The calculations are performed assuming 100 mil of Al shielding and the standard Solar Minimum (M1, 1975.144) model. The calculations are based on the present data with equal amount of logic zero's and one's.

Table IV. Summary of Cross Sections and Threshold values

	C		S		I/O	
Device	Cross Section cm2	Thres-hold MeV/mg/cm2	Cross Section cm2	Thres-hold MeV/mg/cm2	Cross Section cm2	Thres-hold MeV/mg/cm2
5 Volt						
A1280A	3,0E-06	27	1,5E-05	10	3,0E-06	15
RH1280	1,7E-06	27	6,0E-06	10	1,0E-06	15
A1460A	3,0E-06	32	1,5E-05	8	2,0E-06	10
3.3 Volt						
RH1280	4E-06	15	1E-05	6	2E-06	10
A1460A	6E-06	15	2E-05	6	7E-06	8

Table V. Upset rates /day /bit for registers made out of C, S and I/O modules in GEO orbit.

	GEO	5 Volt	
Device	C	S	I/O
A1280A	9,7E-08	5,4E-06	1,8E-07
RH1280	6,9E-08	4,5E-06	5,7E-08
A1460A	2,2E-07	1,1E-05	2,5E-06

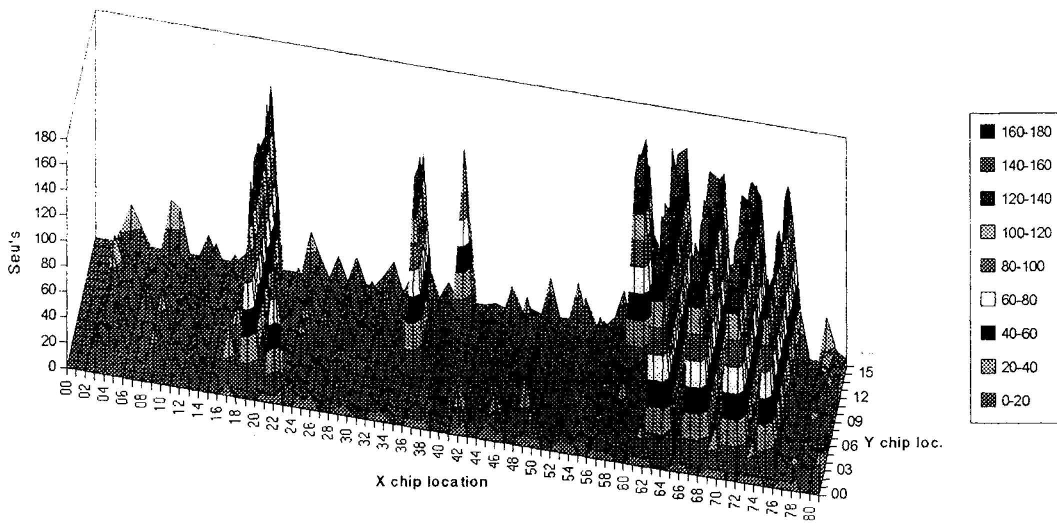

Fig. 12. Total collected data versus physical location on the RH1280 chip. The x-y plane represents the physical location on chip and the z-axis gives the total number of recorded upsets. The large peaks corresponds to S-module registers. I/O modules are located along the borders and the rest consist of different configurations of C modules.

Table VI. Heavy ion upset rates /day /bit for registers made out of C, S and I/O modules in Polar (800 km circular, 97°) orbit.

Device	Polar C	5 Volt S	I/O
A1280A	2,4E-08	1,6E-06	4,6E-08
RH1280	1,7E-08	1,3E-06	1,4E-08
A1460A	5,5E-08	3,3E-06	7,2E-07

Table VII. Proton upset rates /day /bit for registers made out of C, S and I/O modules in LEO (450 circular, 51°) orbit.

Device	LEO C	5 Volt S	I/O
RH1280	-	1,7E-07	-
A1460A	-	5,0E-07	4,8E-08

B. Protons

The proton test indicated that only upsets in S-module registers could be observed for 5 Volt supply current. a few upsets could be detected for the I/O registers, indicating a factor 4 lower cross section than for the S-module registers.

For S-modules and Vcc = 3.3 V, the upset cross sections seem to be a factor 3 higher than for 5V supply voltage. Upset rates in space are given in Table VII for Low Earth Orbit (LEO) using Space Radiation calculation with actual data and the trapped proton model AP8MIN, behind 200 mil shielding and the International Geomagnetic Ref. field as input.

C. Total Dose

The A1280A was found to degrade severely already at low levels of cumulated dose. A1280A begins to draw significant current well before failure, increasing almost linearly until a level of about 18 krad(Si). At this point, the current jumped abruptly to a level above 500 mA. The variation between the three samples was small. According to the literature, this large jump in current is a consistent characteristic of the A1280A device and has been reported to occurred as low as 12 krad(Si). This phenomenon has not been found to occur for the smaller type, A1020, in the ACT2 family.

The Actel A1280A type has earlier been the subject of several total dose tests.

Previous studies have found the A1280A family devices to function to levels from about 8 krad(Si) up to 25 krad(Si), which is in line with the results

found in the present study. The samples used in this study were burned in. The effect of burn in on the dose susceptibility for the 1280A is marginal according to other experiments. The wide range of total dose results from different laboratories may be influenced by slight differences in test programs and test methodologies. However, the lot-to-lot variations found in other studies are more likely the cause of reported differences in A1280A behaviour.

The total dose irradiation and room temperature anneal for the A1460A device type of commercial grade are shown in Fig 10 and Fig 11. The results are more promising than that for A1280A. The average pre-irradiation current value was about 0.7 mA. For the first 10 krad(Si) cumulated dose, the supply current increased only about 0.1 mA. For 20 krad(Si) cumulated dose, one sample increased up to 3.7 mA, while the other two increased up to about 1.6 mA. The variation in current increase among the three test samples are remarkably large. Two of the three samples also exhibit the phenomenon of abrupt jump in current value similar to what was observed for A1280A.

VIII. CONCLUSION

The three types tested indicate similar heavy ion sensitivity, with the RH1280 more SEU hard than the other two.

Upset calculations using Space Radiation and experimental cross indicates that S-module registers would likely not be accepted in critical space applications due to the high upset rate.

In space applications at LEO, the inclination of the orbit will have a large impact on the number of upsets a device will see. Detailed assessments of the proton upsets must be performed for each programme. In general, the tested FPGA tend to be worse than other complex device types.

The A1460A indicated very little changes in supply current up to 10 krad(Si) and no functional failure could be detected with the present test method up to 50 krad(Si). With some shielding this device may well be used in some space application from a total dose point of view. The A1280A exhibits large currents already at 10 krad(Si) and fail to function around 18 krad(Si). Other experiments have shown that large differences could be expected from lot to lot, but all fail to function before 20 krad(Si).

IX. REFERENCE DOCUMENTS

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