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PROJECT

Radiation Pre-Evaluation of Field Programmable Gate Array (FPGA)

ESA Contract No 11407/95/NL/CN

TITLE

Final Report

EUROPEAN SPACE AGENCY
CONTRACT REPORT

This work described in this report was done under ESA contract. Responsibility for the contents resides in the author or organisation that prepared it.

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SUMMARY

This document form the Final Report of the ESTEC/Contract No 11407/95/NL/CN. The objective of the contract has been to perform Heavy Ion Tests (WP2), Proton Tests (WP3) and Total Dose Tests (WP4) of three different types of Field Programmable Gate Arrays (FPGA) according to a pre-defined Test Plan. The Test Plan formed part of WP1, which also included definition and procurement of FPGA's, design and programming of test patterns, design and manufacturing of test fixtures, developing of the control and monitor test software and initial testing using a ^{252}Cf source.

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1. ABSTRACT

This document form the Final Report of the ESTEC/Contract No 11407/95/NL/CN. The objective of the contract has been to perform Heavy Ion Tests (WP2), Proton Tests (WP3) and Total Dose Tests (WP4) of three different types of Field Programmable Gate Arrays (FPGA) according to a pre-defined Test Plan. The Test Plan formed part of WP1, which also included definition and procurement of FPGA's, design and programming of test patterns, design and manufacturing of test fixtures, developing of the control and monitor test software and initial testing using a ^{252}Cf source.

2. INTRODUCTION

Field Programmable Gate Arrays (FPGAs) are attractive for space application because of good density, low cost and quick turn-around time. FPGA devices from Actel Corp. have become popular with space flight designers. However, these devices are targeted for commercial and military markets and generally no guarantee of radiation hardness is provided by the manufacturer.

Actel FPGA's are programmed by "burning" one or more anti-fuses, which otherwise have a very high electrical resistance and act to separate electrical nodes. During programming, anti-fuses are burned, providing a low resistance path between nodes.

Actel FPGA's have gradually evolved since the initial device type first was introduced. This study comprises two families of available Actel FPGA's named "ACT1", "ACT2" and "ACT3". ACT1 devices are composed entirely of combinatorial modules (C-modules) and I/O modules; neither module has any storage (memory) capability. Flip-flops can be constructed by configuring a single C-module as a transparent latch, or by using two C-modules as an edge-triggered flip-flop. The ACT2 family added transparent latches to the input and output paths in the I/O-modules, and introduced S-modules, basically a C-module followed by a dedicated flip-flop. The S-module flip-flop can be configured as either an edge-triggered unit, or a transparent latch. The ACT3 series replaced the transparent latches in the I/O modules with triggered flip-flops driven by a high performance clock.

Within the last few years the SEU and Total Dose vulnerability have been tested for various Actel FPGA types. The Total dose results show large variation in tolerance for various types of FPGA's, while the Heavy Ion results indicate about the same sensitivity for the different FPGA types, but large difference in sensitivity between C, S and I/O modules. In order to recommend the use of these devices in space application, additional testing and analysis is needed to further characterise these types of components.

3. APPLICABLE DOCUMENTS

ESTEC/Contract No 11407/95/NL/CN "Radiation Pre-Evaluation of Field Programmable Gate Array (FPGA)"

QCA/RHS-FPGA1.WP-NOV.94, Issue 2 "Statement of Work for Radiation Pre-Evaluation of Field Programmable Gate Array (FPGA)"

SE/PROP/0030/G, "Technical and Management Proposal"

ESA/SCC Basic Specification No 25100 Single Event Effects Test Method and Guidelines

ESA/SCC Basic Specification No 22900 Total Dose Steady-State Irradiation Test Method.

Radiation Pre-Evaluation of FPGA, WP1 Report, Saab Ericsson SE/REP/0040/K
WP2 Report, Saab Ericsson SE/REP/0041/K
WP3 Report, Saab Ericsson SE/REP/0042/K
WP4 Report, Saab Ericsson SE/REP/0043/K

3.1. Reference Documents

R. Koga, W.R. Crain, K. B. Crawford, S. J. Hansel, S. D. Pinkerton and T. K. Tsubota, "The Impact of ASIC Devices on the SEU Vulnerability of Space-borne Computers, IEEE Trans. Nucl. Sci., NS-39, pp. 1685-1692, Dec. 1992.

Field Programmable Gate Arrays: Evaluation for Space-Flight Applications, JPL Publication 92-22, September 15, 1992.

G. K. Lum, R. J. May and L. E. Robinette, "Total Dose Hardness of FPGAs, "IEEE Trans. Nucl. Sci, NS-41, pp. 2487-2493, Dec. 1994.

R. Katz, R. Barto, P. McKerracher, B. Carkhuff and R. Koga, "SEU Hardening of Field Programmable Gate Arrays (FPGAs) for Space Applications and Device characterisation, "IEEE Trans. Nucl. Sci., Dec. 1994, p. 2179.

R. B. Katz and G. M. Swift, "Data on Anti-fuse/FPGA Reliability in the Heavy Ion Environment, "presented at 1995 IEEE Radiation Effects Data Workshop, submitted to IEEE Trans. Nucl. Sci.

4. SAMPLE SELECTION

The following three different types of Actel FPGA's have been tested during this Radiation Pre-Evaluation Programme. All test samples have been supplied by Actel to Saab Ericsson (SE) free of charge .

4.1. Actel A1280A

The A1280A is a second generation FPGA from Actel (ACT2), with chip manufactured by Matshushita, consisting of three types of user resource modules; logic modules for both combinatorial and sequential designs (C- and S modules) and I/O modules. The devices employ antifuse technology implemented in silicon gate, 1.0 μm, two-level metal CMOS. This device has 1232 dedicated flip-flops (624 S- and 608 C-modules) and a maximum of 140 I/O's.

Number of test samples:	12
Screening level:	Mil Temp
Date code:	9510
Chip manufacturer:	Matshushita
Package:	176-pin CPGA

Marking / *Top side*	Marking / *Bottom side*
ESD symbol	
Actel logo	U1H-272
A1280A	PC510029
PG176M 9510	

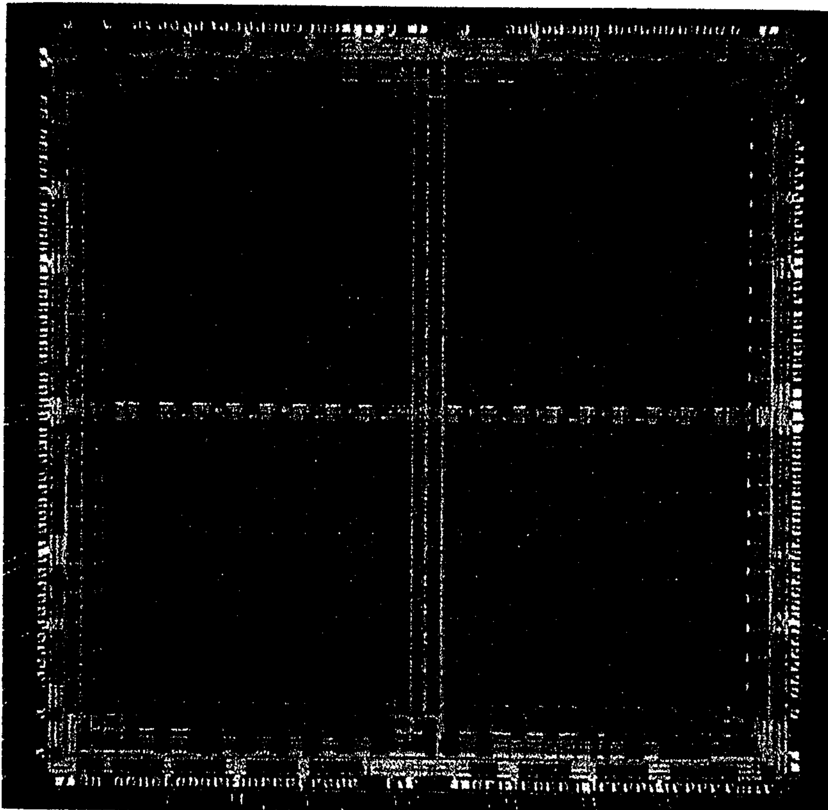


Fig 4.1.1 Overview of A1280A chip, magnification 10X.

4.2. Actel A1460A

The A1460A is a third generation FPGA from Actel (ACT3) consisting of three types of user resource modules; logic modules for both combinatorial and sequential designs (C- and S modules) and I/O modules. The ACT3 family architecture is an upgrade from the ACT2. The S-module is an enhanced version of the ACT2 multiplexor-based combinatorial-sequential module. The I/O module is enhanced significantly to give an I/O performance of 10 ns Clock-to-out. The devices employ the same antifuse technology as ACT2 implemented in silicon gate, 0.8 µm, two-level metal CMOS. This device has 768 dedicated flip-flops (432 S- and 416 C-modules) and maximum 168 I/O's.

Number of test samples:	11
Screening level:	Mil Temp
Date code:	9451
Chip manufacturer:	Matshushita
Package:	207-pin CPGA

Marking / *Top side*	Marking / *Bottom side*
Actel logo A1460A PG207M 9451	JL18 PC450116

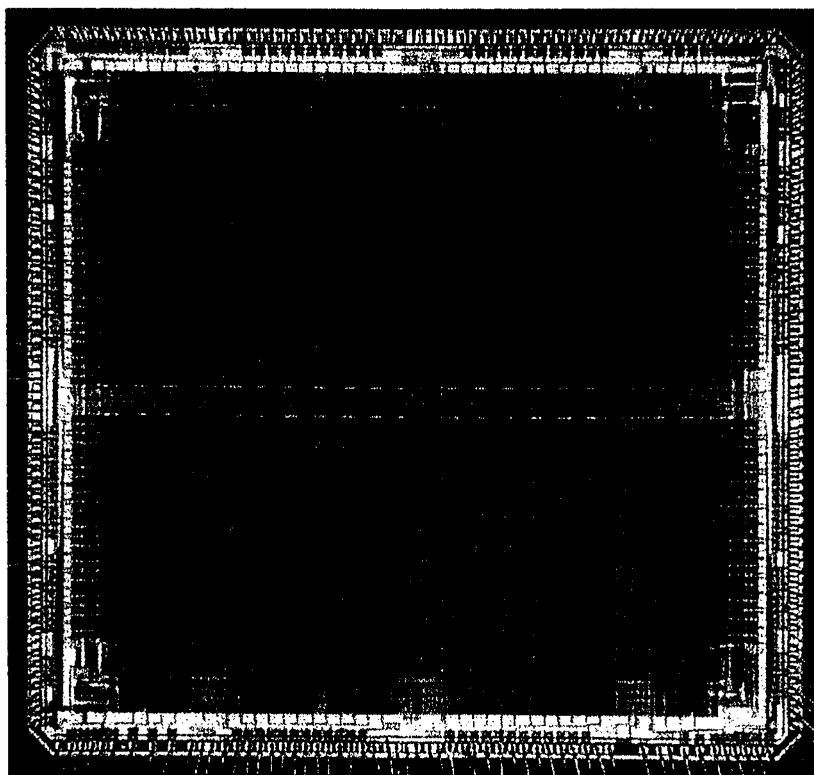


Fig 4.2.1 Overview of A1460A chip, magnification 10X.

4.3. Actel RH1280

The RH1280 is manufactured by Loral Federal Systems in a Rad Hard process and distributed by Actel. Loral and Actel have joint agreement to develop Rad Hard FPGA in the Actel concept with the Loral Rad Hard CMOS process. Basically, the device resembles the A1280A in structure, but differs in timing. The devices employ antifuse technology implemented in silicon gate, 0.8 µm, two-level metal CMOS on an epi process.

Number of test samples:	5
Screening level:	QML
Date code:	9617 (?)
Chip manufacturer:	Loral Federal Systems
Package:	172-pin CQFP

Marking / *Top side*	Marking / *Bottom side*
"None"	"None"

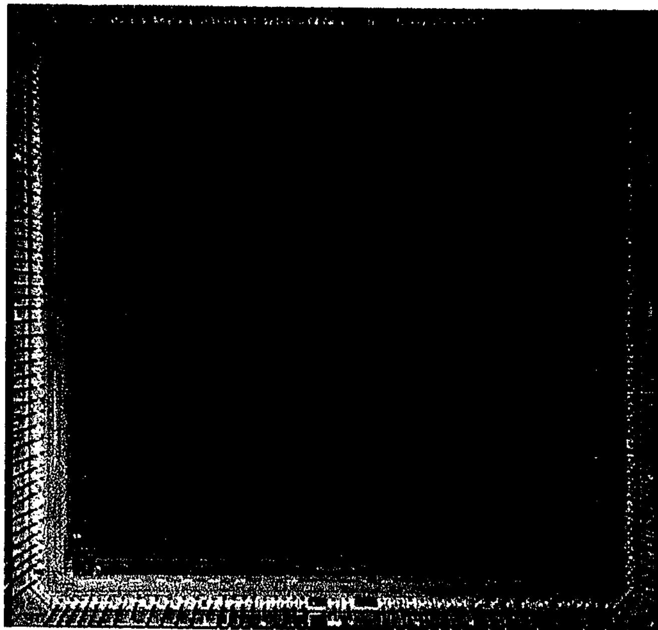


Fig 4.3.1 Overview of RH1280 chip, magnification 10X.

5. TECHNIQUES

5.1. General

The general concept is to load data into the DUT's, pause for a pre-set time and thereafter read data and check for errors. A schematic picture is shown in Fig 5.1.1.

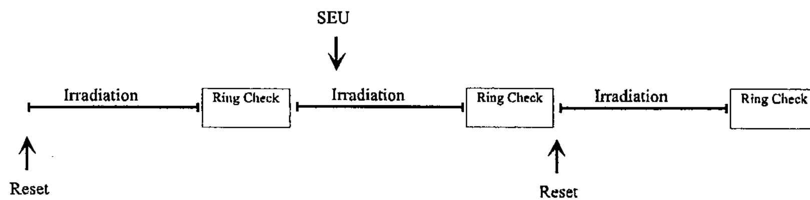


Fig 5.1.1 Schematic view of test sequence.

A flow chart of the test sequence is given in the Fig 5.1.2. Any detected errors will be store in memory, the DUT will be reseted and new data will be loaded again. The cycle will then be repeated. Failing read/write operations from/to the DUT will determine the functionality criteria. The clock speed will be 50 kHz. For each DUT errors can be traced down to logic module, logic value and position.

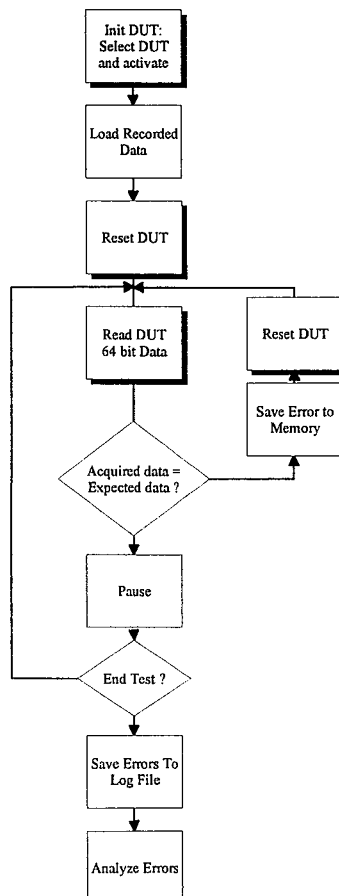


Fig 5.1.2 Flow chart of the test sequence.

5.2. Test Boards

Three different types of printed circuit board, one for each FPGA type, were designed and manufactured. Each test board can house 3 Device Under Test (DUT). Illustration of the RH1280 test board is given in Fig 5.2.1. The DUT's will be tested using a "virtual golden chip" test method. The principal of the measuring technique is to compare each output from the DUT with the correct data controlled via a PC. The general concept of the error detection and test sequence is shown in Fig 5.1.2. The DUT is continually cycled while the outputs of selected ring counters are compared by the "golden chip" with three times over sampling. When an error is found (when outputs do not match), the state of all outputs and position in cycle of the failing ring counter will be temporarily stored in the memory. The ring counters (DUT) are then reseted. After each test run the data are analysed and stored in a database by the controlling PC. The PC can be remote controlled via thin Ethernet network in order to cope with the long distance transmission as required at the proton facility. For all tests, the devices will be clocked at frequency of 50 kHz.

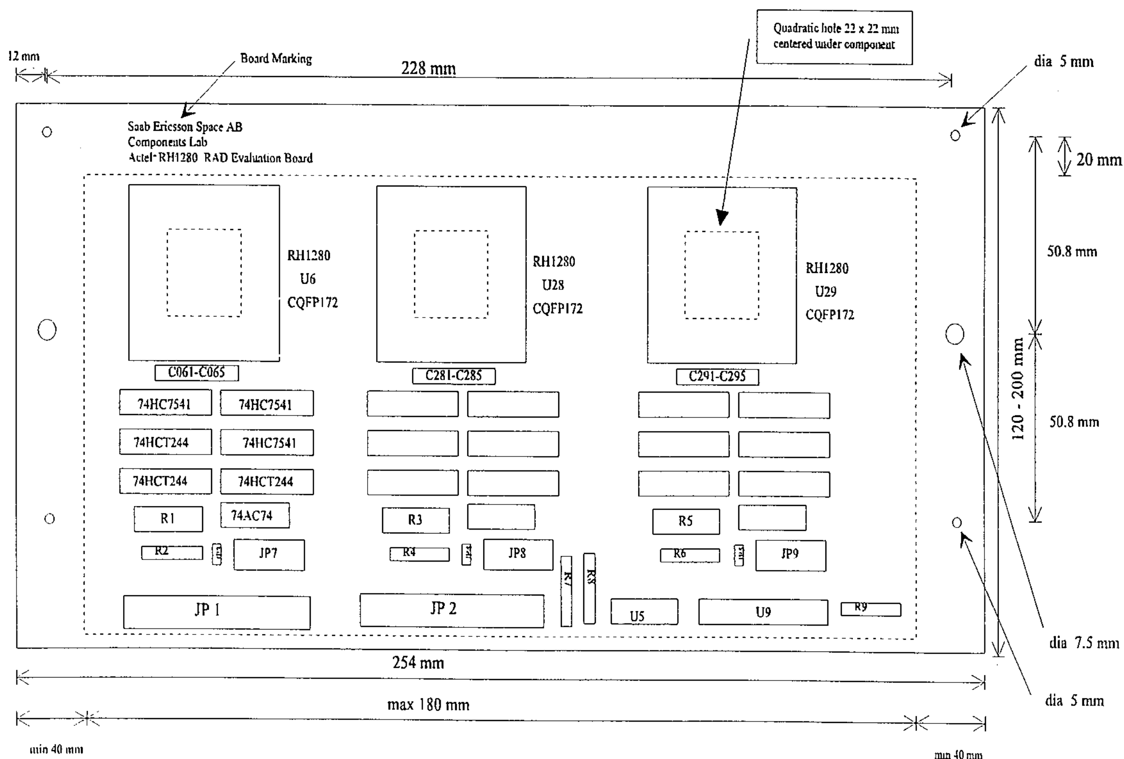


Fig 5.2.1 Lay-out of the RH1280 test board. The test boards for all three FPGA types are prepared for both 5V and 3.3 V power on the DUT's

5.3. DUT Layout

5.3.1. General

The general layout structure for all three types of FPGA's consist of ring counters for each type of logical modules that can be used to program the FPGA's. A block diagram of the DUT layout for A1280A and RH1280 is shown in Fig 5.3.1.1.

The S-module is the more complex of the two modules and can be forced to act as a C-module by "bypass" of other functions. The S-module is very sensitive to SEU while the C-module part of the S-module has up till now been considered identical to the C-module in SEU sensitivity. The I/O module is considered equal to the C-module in SEU sensitivity.

Information from Actel presented during the WP1 meeting pointed to the fact that a flip-flop made out of two C-modules has different SEU vulnerability than a flip-flop made up of a C-module and a "bypass S-module". The design of the DUT layout for the C-modules was changed after the WP1 meeting with respect to the original outlines to cope with the new information from Actel.

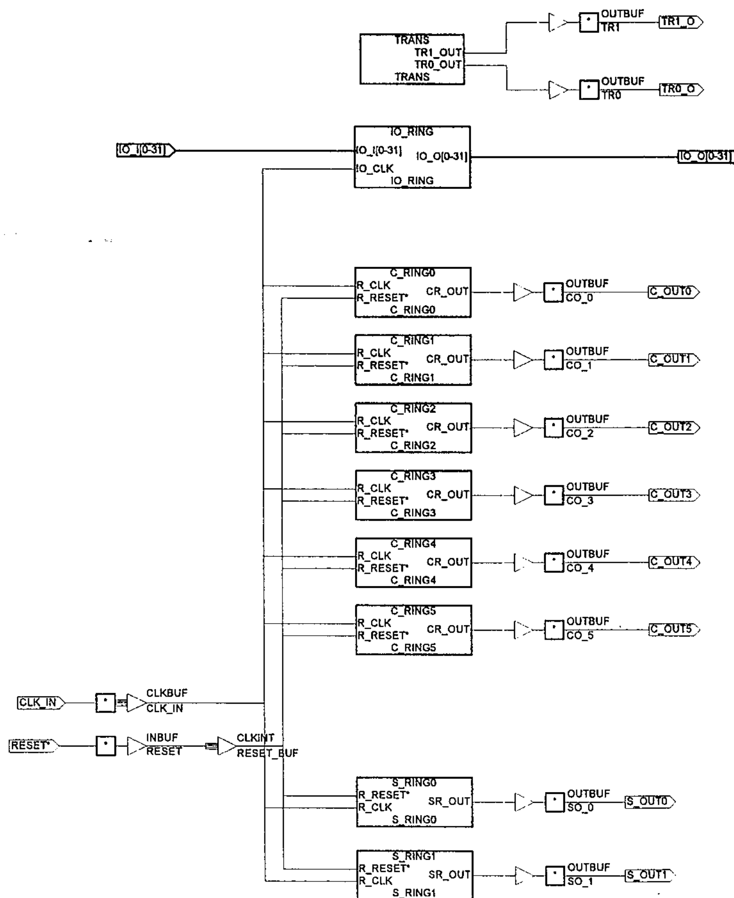


Fig 5.3.1.1 Block diagram for DUT layout of A1280A and RH1280

5.3.2. A1280A and RH1280 Types

For C and I/O modules the flip-flop's are arranged as consecutive 0 1 0 1 etc in individually controlled 64-bit ring counters. For S modules, the registers have been tested at high level only ("1"). The DUT's of 1280A and the RH1280 have the following programmed structure:

-two 64-bit S-modules, -128 flip-flops using 128 S-modules
-two 64-bit C-C-modules, - 128 flip-flops using 256 C- modules
-one 64-bit C-"bypass S" modules - 128 flip-flops using 64 C- and 64 "bypass S"
-one 64-bit "bypass S"-C modules - 128 flip-flops using 64 C- and 64 "bypass S"
-two 64-bit "bypass S"-"bypass S" - 128 flip-flops using 256 "bypass S"
-one 64-bit I/O-modules - 64 flip-flops using 64 S-modules as 32 Input and 32 Output.

In total, 419 C-modules, 576 S-modules and 64 I/O-modules are used out of the available 608, 624 and 140, respectively.

The C -module rings have been designed using two type of macros, DFP1B for logic "1" (high level) and DFPC for logic "0" (low level). Every second flip-flop is the inverted logical function of the presiding flip-flop. Flip-flops made up of a C-module and a "bypass S" use the same technique and have been created by the use of the same macros and knowledge of the actual physical location of the individual modules on the chip. This information have been provided by Actel. The S-module rings have been designed using macro DFP1E and tested at logic "1" only. Design of the I/O module has been performed with macros IR and ORH for input and output, respectively. Schematic design blocks are shown in Fig 5.3.2.1, 5.3.2.2 and 5.3.2.3 for the C-, S- and I/O modules, respectively.

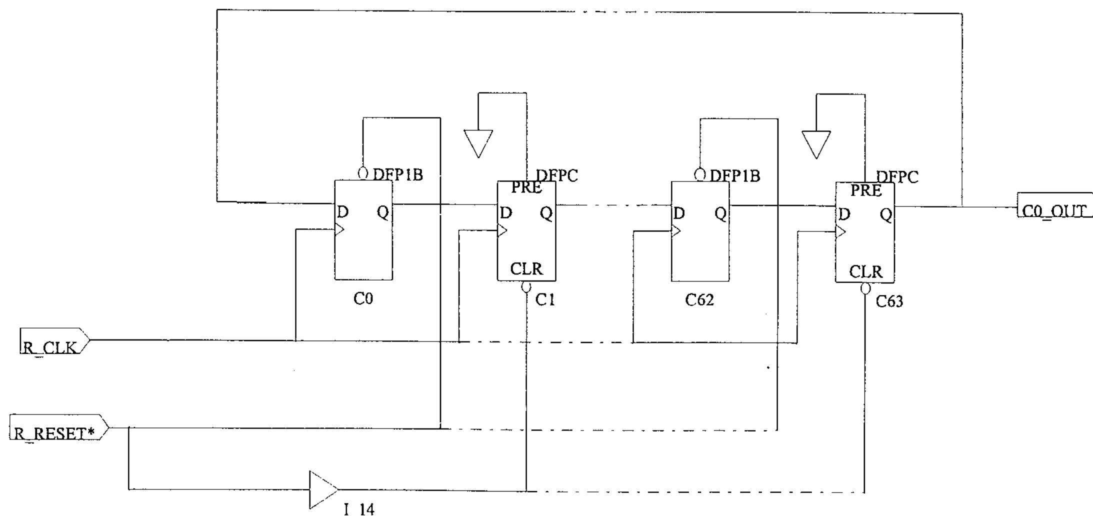


Fig 5.3.2.1 Design block for ring counters of C-module to 1280A and RH1280

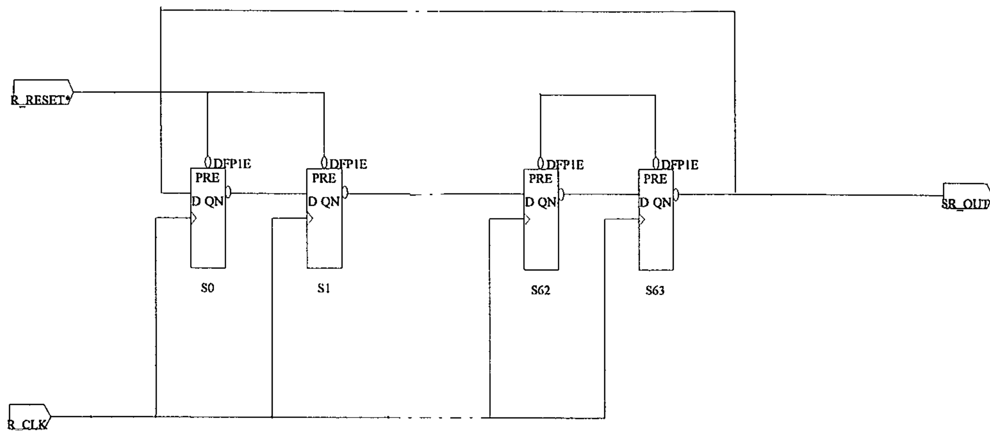


Fig 5.3.2.2 Design Block for ring counters of S-module to 1280A and RH1280

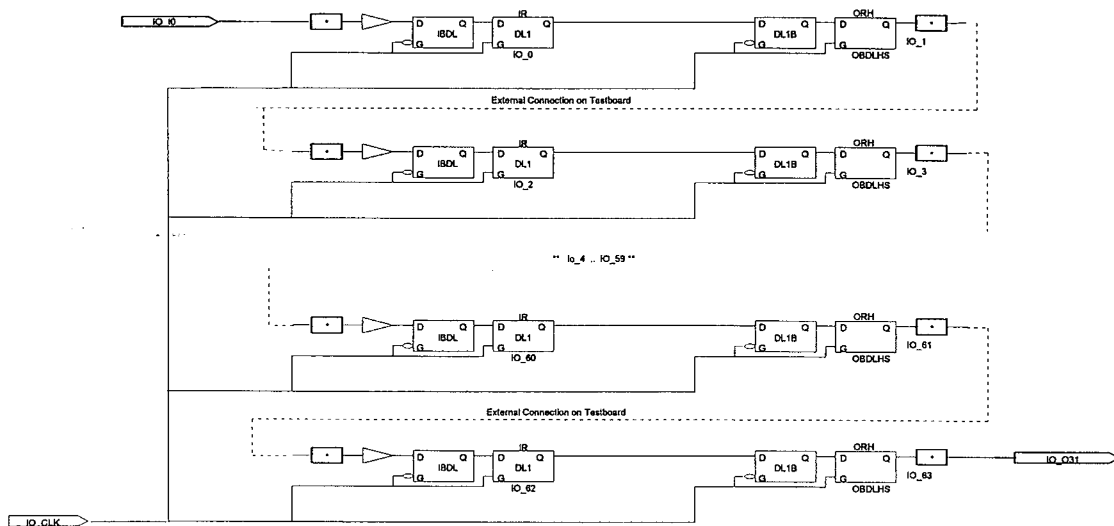


Fig 5.3.2.3 Design block for ring counters of I/O-module to 1280A and RH1280

5.3.3. A1460A Type

The 1460 type is programmed in the same way as the 1280-types but due to the smaller size the number of ring counters have been reduced. The DUT's of 1460 have the following structure:

-two 64-bit S-modules, -128 flip-flops using 128 S-modules
-one 64-bit C-C-modules, - 64 flip-flops using 128 C- modules
-one 64-bit C-"bypass S" modules - 64 flip-flops using 64 C- and 64 "bypass S"
-one 64-bit "bypass S"-"bypass S" - 64 flip-flops using 128 "bypass S"

-one 64-bit I/O-modules - 32 Input and 32 Output.

In total, 192 C-modules, 332 S-modules and 64 I/O modules are used out of the available 416, 432, and 168 , respectively.

The C -module rings have been designed using the macros, DFP1B for logic "1" and DFPC for logic "0". Every second flip-flop is the inverted logical function of the preceding flip-flop. Flip-flops made up of a C-module and a "bypass S" use the same technique and have been created by the use of the same macros and knowledge of the actual physical location of the individual modules on the chip. The S-module rings have been designed using macro DFP1E and tested at logic "1" only. Design of the I/O module ring has been performed with macros IREC and ORECTH for input and output, respectively. Schematic design layouts for the C-, S- and I/O modules are presented in the WP1 report.

6. ^{252}Cf TEST RESULTS

A dedicated vacuum system for SEU test by ^{252}Cf at Saab Ericsson Space/Components Lab. was used to verify functionality of programmed DUT's, test boards and software monitoring system. The ^{252}Cf source consist of a thin evaporated layer of Californium on metal backing. The source activity was at the time of test 48 kBq. The average nominal stopping power value for the fission fragments is LET=43 MeV/cm^2/mg. However, due to low penetration depth in Si (~13μm), metal and polysilicon layers, the real stopping power value is more likely around a LET of 20- 25 MeV/cm^2/mg. Test results are given in Table 6.1 below.

Table 6.1 Test result from ^{252}Cf.

FPGA Type	Flux ion/s	Test Time [h]	Module	Number of SEU's	Cross Section/bit [cm^2]
1280A	6.5	370	C	1	4.5E-10
			S	5026	2.3E-6
			I/O	1	1.8E-9
1460	11.4	110	C	0	<5.8E-10
			S	681	1.2E-6
			I/O	137	4.7E-7
RH1280	12.0	13.6	C	0	<4.7E-9
			S	52	7.4E-7
			I/O	0	<2.8E-8

7. HEAVY ION TEST

7.1. Equipment & Facility

Heavy ion test was performed at the Tandem Van de Graaff accelerator facility at Brookhaven National Laboratory. This accelerator is able to accelerate about 60 different nuclides over the full range of the periodic table. A handful of standard ion species can be changed from one to another in less than 30 minutes. The beam on target can be accurately attenuated down to a few 100 particles/sec, focused down to less than 1 mm in diameter or, on the other hand, easily defocused and /or swept for uniformly exposing large areas. The facility provides beam diagnostic and control with continuous monitoring of beam fluence and flux via plastic scintillators.

The irradiations were performed in a large vacuum chamber with all three test boards mounted at the same time on a movable frame. The test boards for the three types were mounted on top of each other displaced in such away as the DUT's from all boards were exposed to the front side. Thus, for the heavy ion test of the 3 times 3 devices it was not necessary to open up the vacuum chamber for change of devices or test boards. Each board was separately connected via feed through connectors through the vacuum chamber.

Three samples of each device type were delidded and mounted on the three boards and serialised as S/N #1, S/N #2 and S/N #3 for each device type. Each device were individually biased. During irradiation the samples were monitored for latch-up. In case latch-up should occur, a specially made bias supply will shut off the bias within 5 microsecond and automatically bias the devices again within a second. Table 7.1.1 provides the data of the ions used in the heavy ion tests. The LET range was obtained by changing the ion species and the angle of incidence between the beam and the chip.

Table 7.1.1 Ion Beam Data

Ion Specie	Energy (MeV)	Tilt Angle (Degree)	LET (MeV/mg/cm2)	Range (μm)
F-19	140	0	3.4	120
		45	4.8	85
		60	6.8	60
Si-28	190	0	7.8	79
		45	11.0	56
		60	15.6	39
Ni-58	265	0	26.6	42
		35	32.5	35
		45	37.6	30
		60	53.2	21
I-127	345	0	59.9	33
		30	84.7	23
		45	120.0	16

7.2. Results

The results are presented individually for each device type in a graphical form showing the SEU cross section per cm^2 per bit versus the LET values. The LET range was obtained by changing the ion species and the angle of incidence between the beam and the chip. Table 7.1.1 provide the data of the ions used. Cross sections given in the figure captions is taken to be the asymptotic value at large LET. The threshold value is taken to be the value at 1 % of the cross section value.

7.2.1. Actel A1280A

Graphical illustration of the upset probabilities are given in Figs 7.2.1.1-7.2.1.4 for S, C and I/O modules, respectively.

For S-modules, the high SEU sensitivity resulted in good statistical accuracy. The three samples showed very similar results with no differences in SEU cross section for logical "1" (high). For C and I/O modules, the SEU sensitivity are lower which results in small error rates, particularly for the lower LET values. In Fig 7.2.1.3, the results from the various combinations of C-modules are presented.

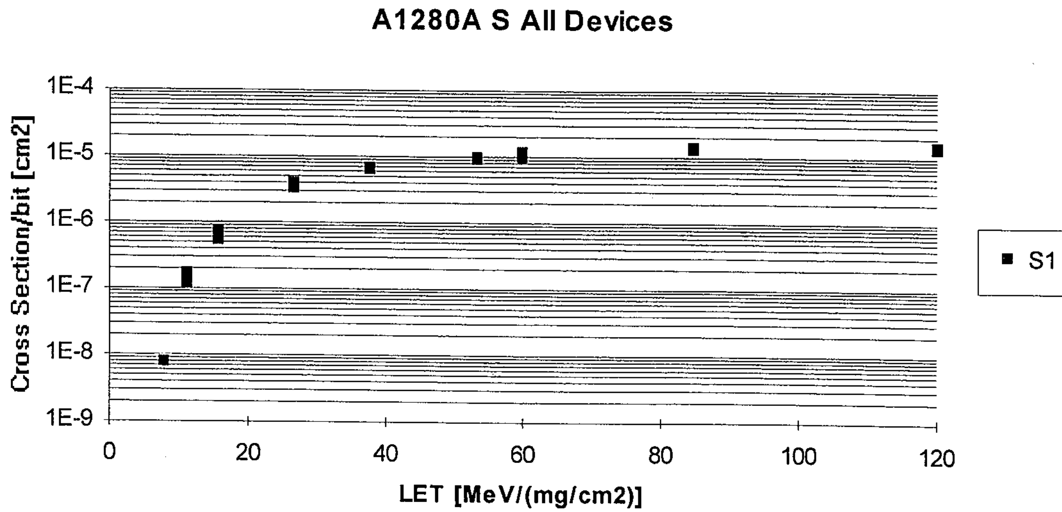


Fig 7.2.1.1 : SEU Cross Section for Actel A1280A S-Modules

S/W Macro :	DFP1E for logical "1"
Test Condition :	Static, Vcc = 5 V, T_{amb} = Room Temp
Test Samples :	A1280A S/N #1, #2, #3 To minimise effects of total dose damage, only two devices of the three were irradiated at each LET value
Cross Section (σ) :	1.5 E-5 cm^2/bit
Threshold :	10 MeV/mg/cm^2

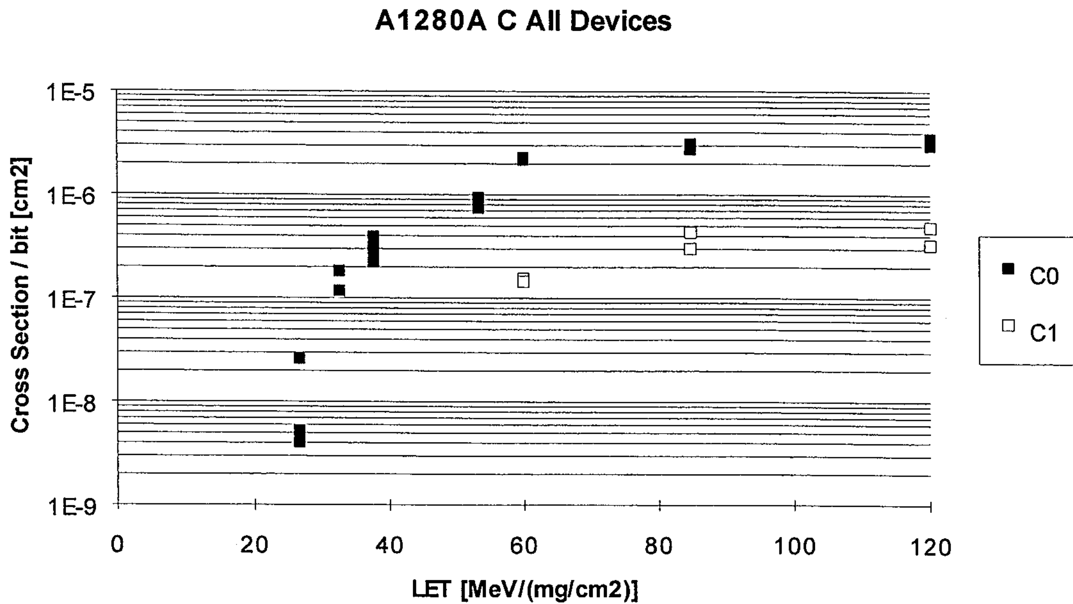


Fig 7.2.1.2 : SEU Cross Section for Actel A1280A C-Modules

S/W Macro :	DFP1B for logic "1"
	DFPC for logic "0"
Test Condition :	Static, Vcc = 5 V, Tamb = Room Temp
Test Samples :	A1280A S/N #1, #2, #3
Cross Section (σ) :	Logic "0" 3 E-6 cm^2 /bit
	Logic "1" 4 E-7 cm^2 /bit
Threshold :	Logic "0" 27 MeV/mg/cm^2

Note : Logic "1" , LET=53.2 MeV/mg/cm^2 no error detected, limit assuming one error = 2.6 E-9 cm^2 /bit

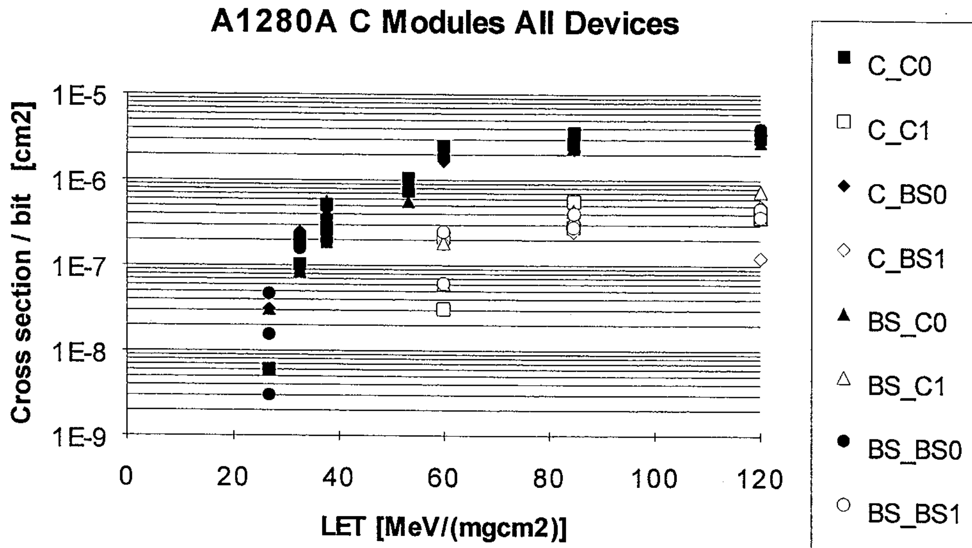


Fig 7.2.1.3 : SEU Cross Section for Actel A1280A flip-flops from different C-Modules pairs as defined in para 5.3.2.

S/W Macro : DFP1B for logic "1"
DFPC for logic "0"

Test Condition : Static, Vcc = 5 V, Tamb = Room Temp

Test Samples : A1280A S/N #1, #2, #3

Cross Section (σ) :

Threshold :

Note : Summed data of "logic pairs" are given in Fig 7.2.1.2

Legend:

C_C0	; C- C-modules, "0".
C_C1	; C- C-modules, "1".
C_BS0	; C and Bypass S modules, "0".
C_BS1	; C- and Bypass S- modules, "1".
BS_C0	; Bypass S-and C- modules, "0".
BS_C1	; Bypass S-and C- modules, "1".
BS_BS0	; Bypass S-and Bypass S-modules, "0".
BS_BS1	; Bypass S-and Bypass S- modules, 1".

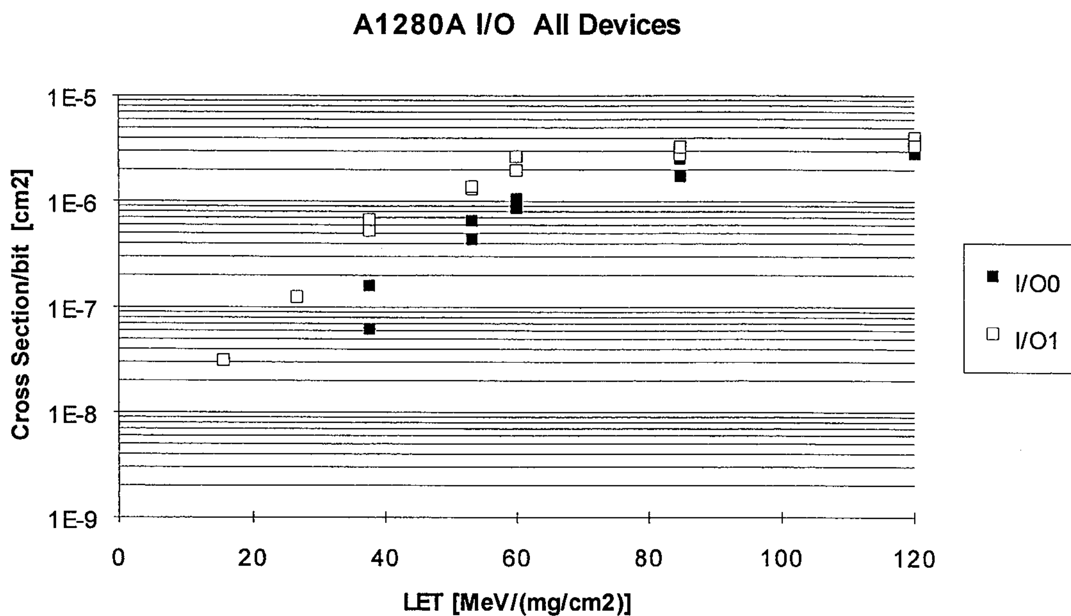


Fig 7.2.1.4 : SEU Cross Section for Actel A1280A I/O-Modules

S/W Macro : IR for "Input" (I/O0)
ORH for "Output" (I/O1)
Test Condition : Static, Vcc = 5 V, Tamb = Room Temp
Test Samples : A1280A S/N #1, #2, #3
Cross Section (σ) : "Input" (I/O0) 3 E-6 cm^2 /bit
"Output" (I/O1) 3 E-6 cm^2 /bit
Threshold : "Output" (I/O1) 15 MeV/mg/cm^2

Note : "Input" (I/O0) , LET=32.5 MeV/mg/cm^2 no error detected, limit assuming one error = 4.7 E-8 cm^2 /bit

7.2.2. Actel RH1280

The same design has been used for RH1280 and A1280A. The RH1280 was tested in the same way as the A1280A with the exception that this type was tested at 3.3 V as well as for 5 V. The results are given in Figs 7.2.2.1 - 7.2.2.7
In Fig 7.2.2.7, the results from the various combinations of C-modules to a flip-flop are presented.

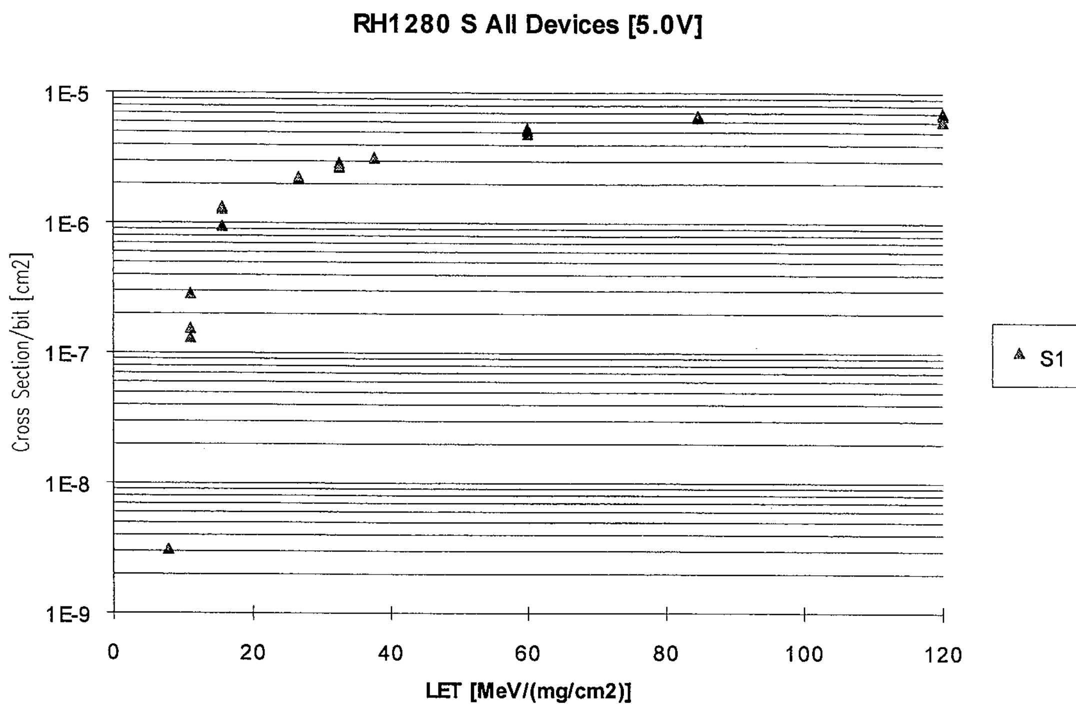


Fig 7.2.2.1 : SEU Cross Section for Actel RH1280 S-Modules

S/W Macro :	DFP1E for logic "1"
Test Condition :	Static, Vcc = 5 V, Tamb = Room Temp
Test Samples :	RH1280 S/N #1, #2, #3
Cross Section (σ) :	6 E-6 cm ^{2} /bit
Threshold :	10 MeV/mg/cm^2

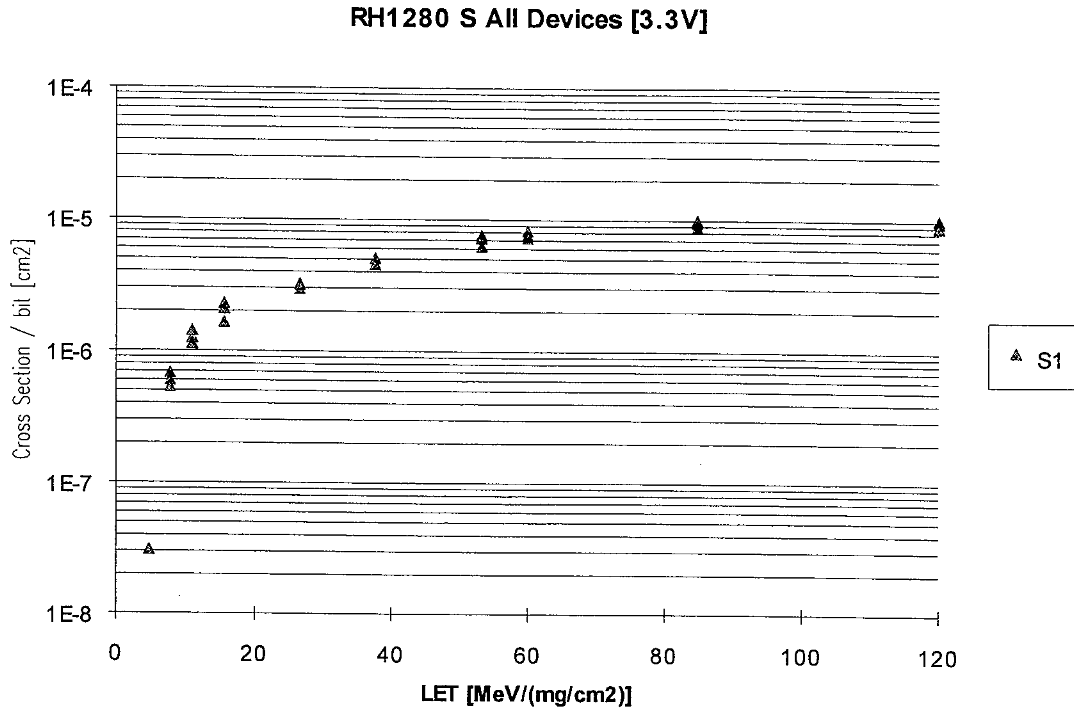


Fig 7.2.2.2 : SEU Cross Section for Actel RH1280 S-Modules

S/W Macro : DFP1E for logic "1"
Test Condition : Static, Vcc = 3.3 V, Tamb = Room Temp
Test Samples : RH1280 S/N #1, #2, #3
Cross Section (σ) : 1 E-5 cm^2/bit
Threshold : 6 MeV/mg/cm^2

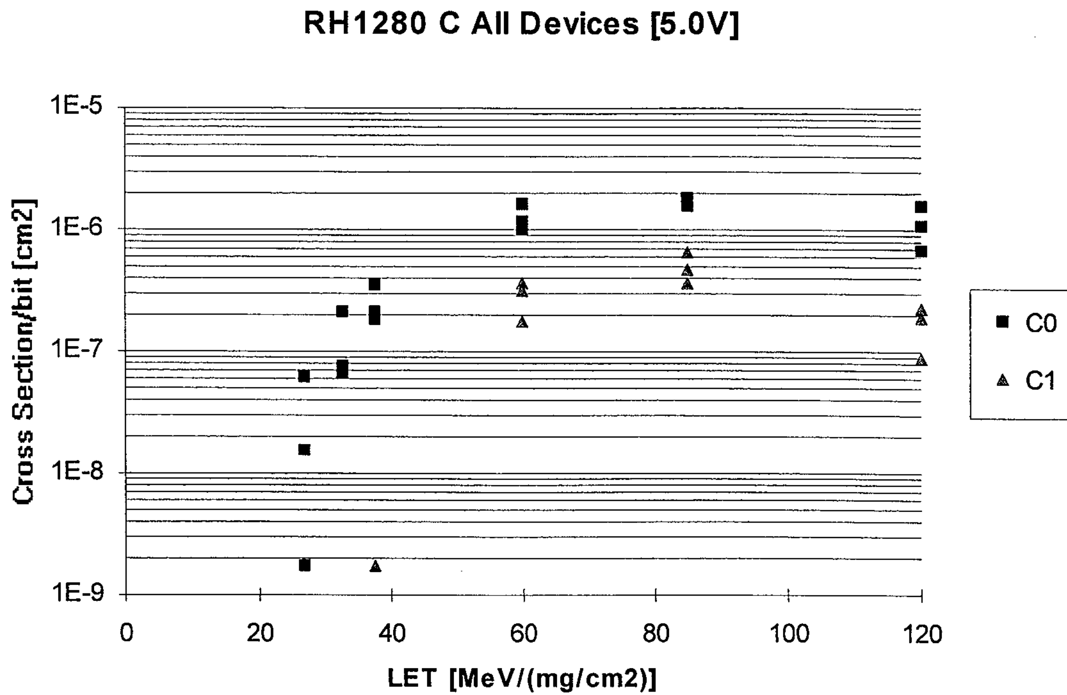


Fig 7.2.2.3 : SEU Cross Section for Actel RH1280 C-Modules

S/W Macro :	DFP1B for logic "1"
	DFPC for logic "0"
Test Condition :	Static, Vcc = 5 V, Tamb = Room Temp
Test Samples :	RH1280 S/N #1, #2, #3
Cross Section (σ) :	"0" 1.7 E-6 cm^2 /bit
	"1" 5 E-7 cm^2 /bit
Threshold :	"0" 27 MeV/mg/cm^2
	"1" 40 MeV/mg/cm^2

RH1280 C All Devices [3.3 V]

Cross Section/bit [cm2] — 1E-5, 1E-6, 1E-7, 1E-8, 1E-9

LET [MeV/(mg/cm2)] — 0, 20, 40, 60, 80, 100, 120

C0
C1

Fig 7.2.2.4 : SEU Cross Section for Actel RH1280 C-Modules

S/W Macro :	DFP1B for logic "1"
	DFPC for logic "0"
Test Condition :	Static, Vcc = 3.3 V, Tamb = Room Temp
Test Samples :	RH1280 S/N #1, #2, #3
Cross Section (σ) :	"0" 4 E-6 cm^2 /bit
	"1" 1.5 E-6 cm^2 /bit
Threshold :	"0" 15 MeV/mg/cm^2
	"1" 30 MeV/mg/cm^2

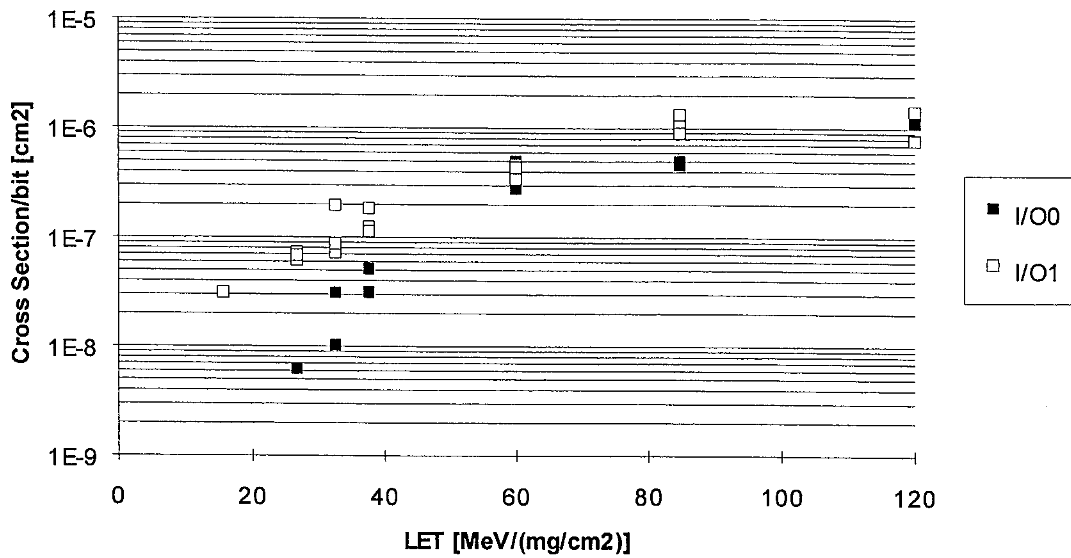


Fig 7.2.2.5 : SEU Cross Section for Actel RH1280 I/O-Modules

S/W Macro :	IP for "Input" ("0")
	ORH for "Output" ("1")
Test Condition :	Static, Vcc = 5 V, Tamb = Room Temp
Test Samples :	RH1280 S/N #1, #2, #3
Cross Section (σ) :	Input (I/O0) 1 E-6 cm^2 /bit
	Output (I/O1) 1 E-6 cm^2 /bit
Threshold :	Input (I/O0) 30 $MeV/mg/cm^2$
	Output (I/O1) 15 $MeV/mg/cm^2$

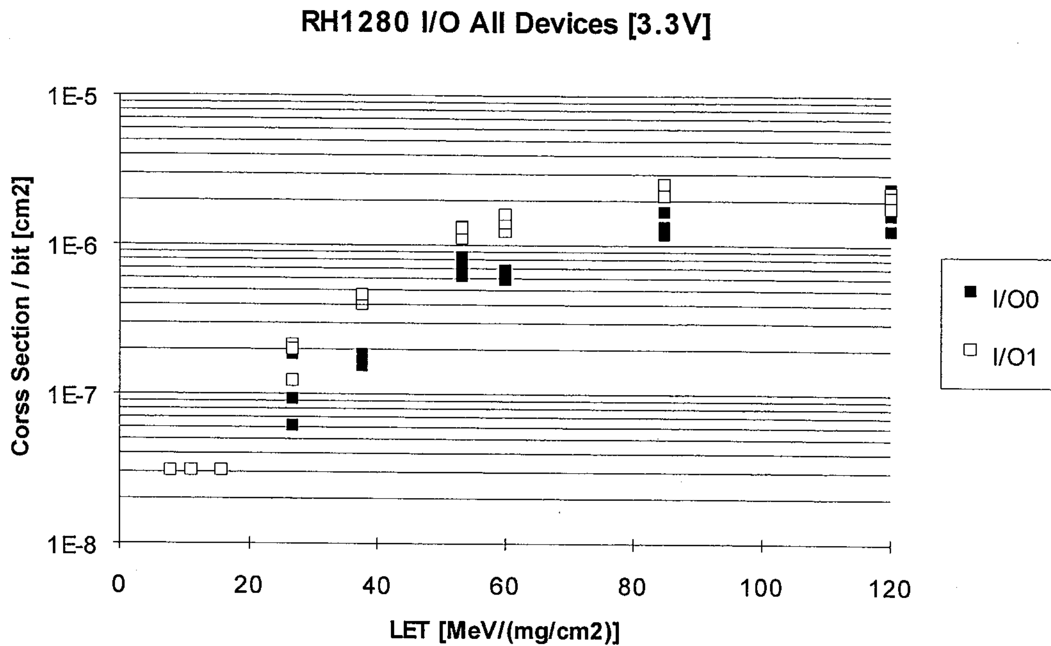


Fig 7.2.2.6 : SEU Cross Section for Actel RH1280 I/O-Modules

S/W Macro :	IP for "Input" ("0")
	ORH for "Output" ("1")
Test Condition :	Static, Vcc = 3.3 V, Tamb = Room Temp
Test Samples :	RH1280 S/N #1, #2, #3
Cross Section (σ) :	Input (I/O0) 2 E-6 cm^2 /bit
	Output (I/O1) 2 E-6 cm^2 /bit
Threshold :	Input (I/O0) ≈10 $MeV/mg/cm^2$
	Output (I/O1) ≈10 $MeV/mg/cm^2$

Fig 7.2.2.7 : SEU Cross Section for Actel RH1280 flip-flops from different C-Modules pairs as defined in para 5.3.2.

S/W Macro : DFP1B for logic "1"
DFPC for logic "0"

Test Condition : Static, Vcc = 5 V and 3.3 V,
Tamb = Room Temp

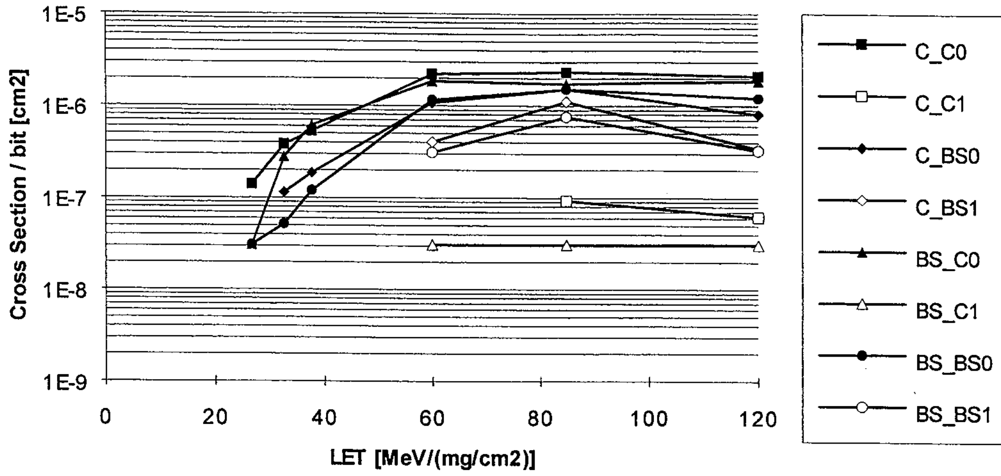
Test Samples : RH1280 S/N #1, #2, #3

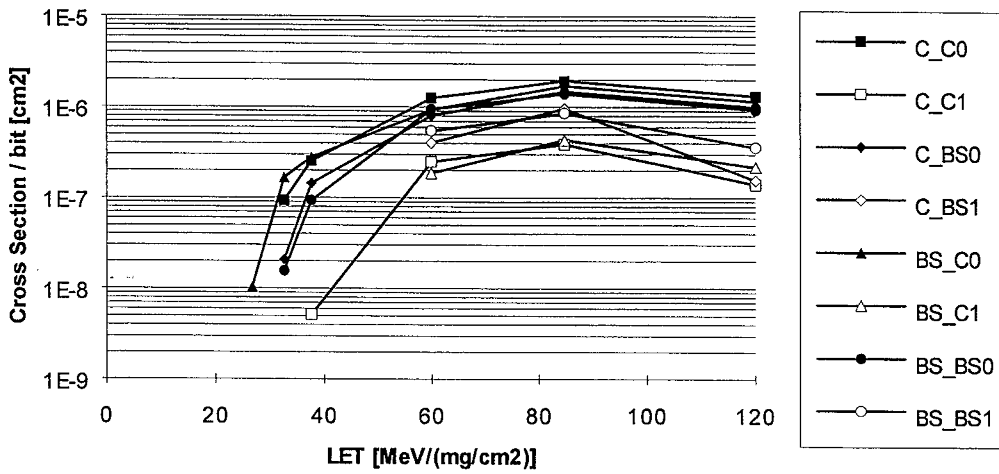
Cross Section (σ) : See Figs 7.2.3 and 7.2.4

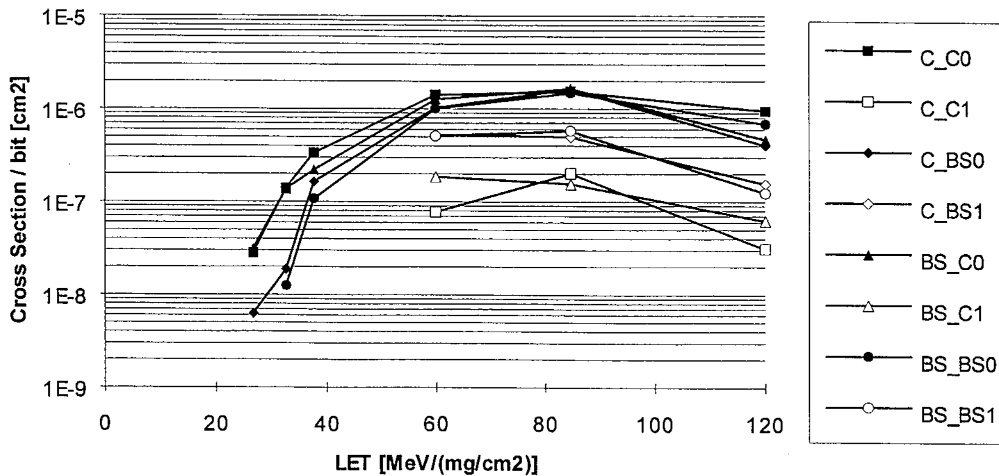
Threshold : See Figs 7.2.3 and 7.2.4

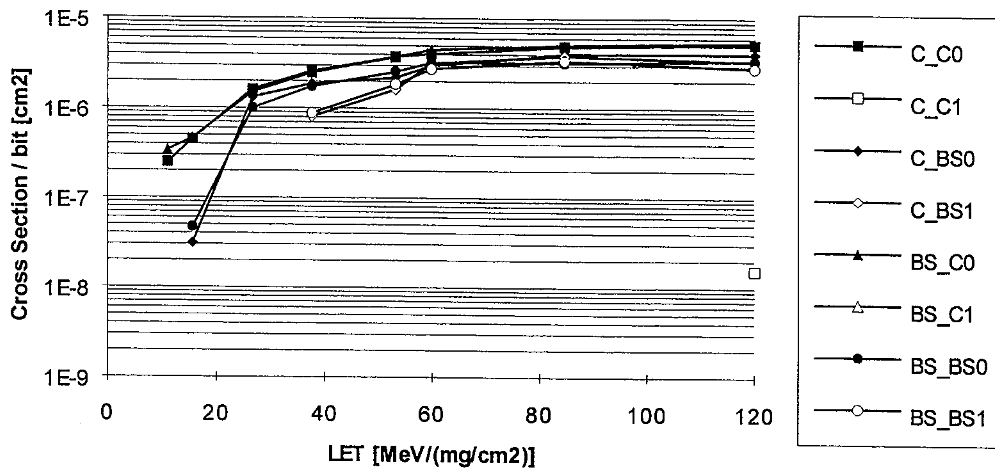
Note : The following 2 pages of illustrations give the results for each device and for each design pair
The 'dips' that can be observed, specially for 3.3 V refer to tilted angle results

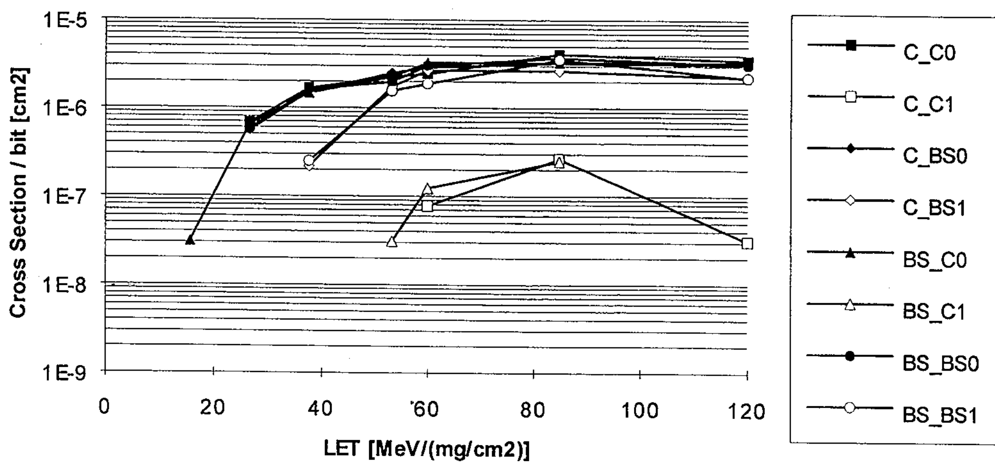
C_C0 ; C- C-modules, logic value "0".
C_C1 ; C- C-modules, logic value "1".
C_BS0 ; C and Bypass S modules, logic value "0".
C_BS1 ; C- and Bypass S- modules, logic value "1".
BS_C0 ; Bypass S-and C- modules, logic value "0".
BS_C1 ; Bypass S-and C- modules, logic value "1".
BS_BS0 ; Bypass S-and Bypass S- modules, logic value "0".
BS_BS1 ; Bypass S-and Bypass S- modules, logic value "1".

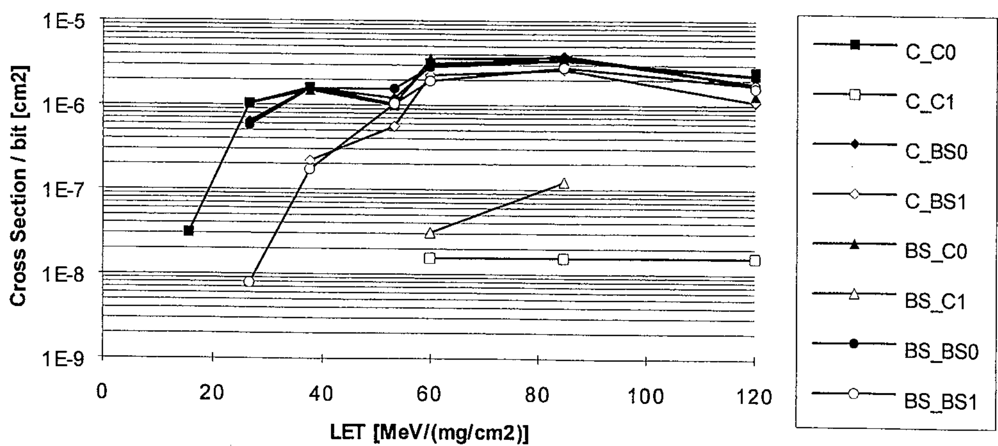

RH1280 C Modules Device 1 [5.0V]
Cross Section / bit [cm2]
1E-5
1E-6
1E-7
1E-8
1E-9
0
20
40
60
80
100
120
LET [MeV/(mg/cm2)]
C_C0
C_C1
C_BS0
C_BS1
BS_C0
BS_C1
BS_BS0
BS_BS1


RH1280 C Modules Device 2 [5.0V]
Cross Section / bit [cm2]
1E-5
1E-6
1E-7
1E-8
1E-9
0
20
40
60
80
100
120
LET [MeV/(mg/cm2)]
C_C0
C_C1
C_BS0
C_BS1
BS_C0
BS_C1
BS_BS0
BS_BS1


RH1280 C Modules Device 3 [5.0V]
Cross Section / bit [cm2]
1E-5
1E-6
1E-7
1E-8
1E-9
0
20
40
60
80
100
120
LET [MeV/(mg/cm2)]
C_C0
C_C1
C_BS0
C_BS1
BS_C0
BS_C1
BS_BS0
BS_BS1


RH1280 C Modules Device 1 [3.3V]
Cross Section / bit [cm2]
1E-5
1E-6
1E-7
1E-8
1E-9
0
20
40
60
80
100
120
LET [MeV/(mg/cm2)]
C_C0
C_C1
C_BS0
C_BS1
BS_C0
BS_C1
BS_BS0
BS_BS1


RH1280 C Modules Device 2 [3.3V]
Cross Section / bit [cm2]
1E-5
1E-6
1E-7
1E-8
1E-9
0
20
40
60
80
100
120
LET [MeV/(mg/cm2)]
C_C0
C_C1
C_BS0
C_BS1
BS_C0
BS_C1
BS_BS0
BS_BS1


RH1280 C Modules Device 3 [3.3V]
Cross Section / bit [cm2]
1E-5
1E-6
1E-7
1E-8
1E-9
0
20
40
60
80
100
120
LET [MeV/(mg/cm2)]
C_C0
C_C1
C_BS0
C_BS1
BS_C0
BS_C1
BS_BS0
BS_BS1

7.2.3. Actel A1460A

SEU data for 5V and 3.3V are presented in Figs 7.2.3.1- 7.2.3.6. The same macros have been used for C- and S-modules as for the other device types.

In Fig 7.2.3.5, the results from the various combinations of C-modules to a flip-flop are presented.

C_C0	; C- C-modules, logic value "0".
C_C1	; C- C-modules, logic value "1".
C_BS0	; C and Bypass S modules, logic value "0".
C_BS1	; C- and Bypass S- modules, logic value "1".
BS_C0	; Bypass S-and C- modules, logic value "0".
BS_C1	; Bypass S-and C- modules, logic value "1".
BS_BS0	; Bypass S-and Bypass S- modules, logic value "0".
BS_BS1	; Bypass S-and Bypass S- modules, logic value "1".

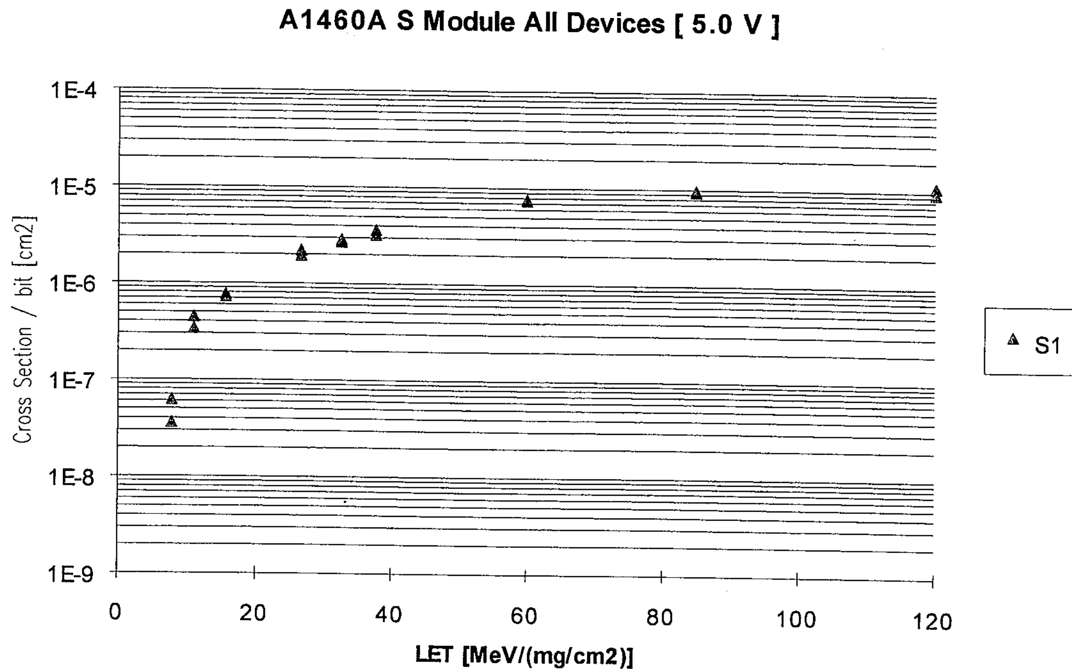


Fig 7.2.3.1 : SEU Cross Section for Actel A1460A S-Modules

S/W Macro : DFP1E for logic "1"
Test Condition : Static, Vcc = 5 V, Tamb = Room Temp
Test Samples : A1460A S/N #1, #2, #3
Cross Section (σ) : 1 E-5 cm^2 /bit
Threshold : 8 $MeV/mg/cm^2$

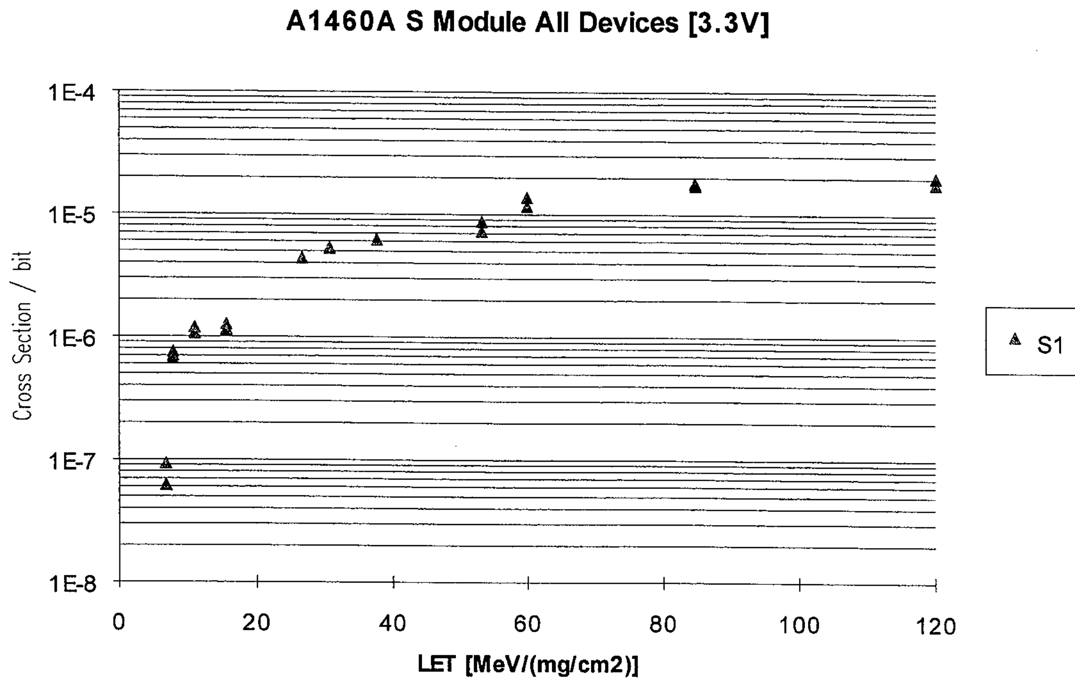


Fig 7.2.3.2 : SEU Cross Section for Actel A1460A S-Modules

S/W Macro :	DFP1E for logic "1"
Test Condition :	Static, Vcc = 3.3 V, Tamb = Room Temp
Test Samples :	A1460A S/N #1, #2, #3
Cross Section (σ) :	2 E-5 cm^2 /bit
Threshold :	6 MeV/mg/cm^2

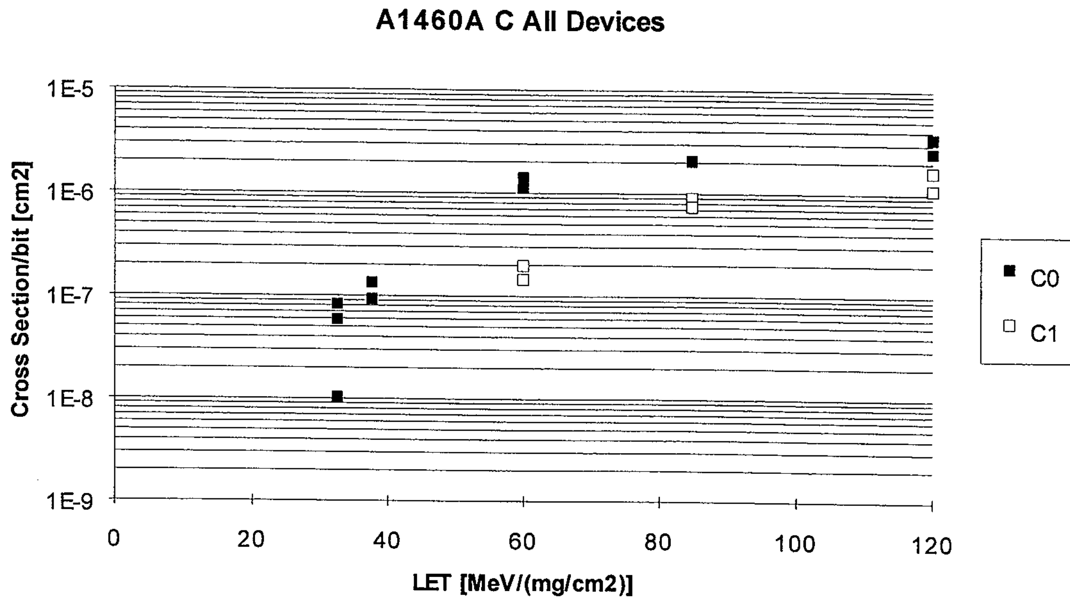


Fig 7.2.3.3 : SEU Cross Section for Actel A1460A C-Modules, 5 V

S/W Macro : DFP1B for logic "1"
DFPC for logic "0"

Test Condition : Static, Vcc = 5 V, Tamb = Room Temp

Test Samples : A1460A S/N #1, #2, #3

Cross Section (σ) : "0" 1.5 E-6 cm^2 /bit
"1" 6 E-7 cm^2 /bit

Threshold : "0" 32 MeV/mg/cm^2

Note : Logic "1" , LET=53.2 MeV/mg/cm^2 no error detected, limit assuming one error = 6 E-9 cm^2 /bit

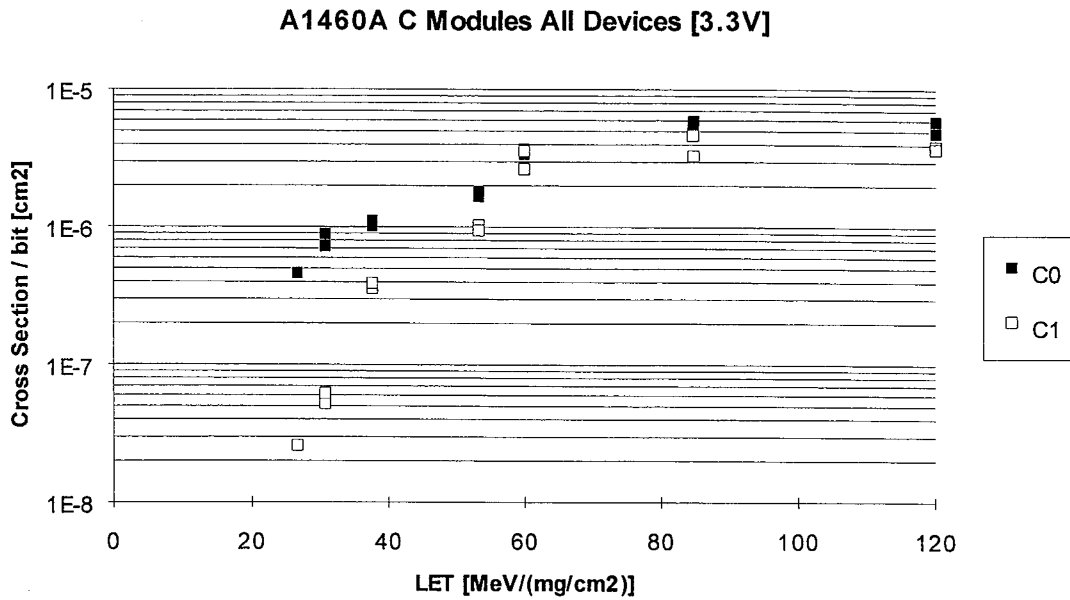


Fig 7.2.3.4 : SEU Cross Section for Actel A1460A C-Modules, 3.3 V

S/W Macro :	DFP1B for logic "1"
	DFPC for logic "0"
Test Condition :	Static, Vcc = 3.3 V, Tamb = Room Temp
Test Samples :	A1460A S/N #1, #2, #3
Cross Section (σ) :	"0" 3 E-6 cm^2 /bit
	"1" 2 E-6 cm^2 /bit
Threshold :	"0" ~20 MeV/mg/cm^2
	"1" ~30 MeV/mg/cm^2

A1460A C Modules All Devices 5.0V

Cross Section / bit [cm2]
1E-5
1E-6
1E-7
1E-8
1E-9
0 20 40 60 80 100 120
LET [MeV/(mg/cm2)]
C_C0
C_C1
C_BS0
C_BS1
BS_C0
BS_C1
BS_BS0
BS_BS1

A1460A C Modules All Devices [3.3V]

Cross Section / bit [cm2]
1E-5
1E-6
1E-7
1E-8
0 20 40 60 80 100 120
LET [MeV/(mg/cm2)]
C_C0
C_C1
C_BS0
C_BS1
BS_C0
BS_C1
BS_BS0
BS_BS1

Fig 7.2.3.5 : SEU Cross Section for Actel A1460A C-Modules, 5V and 3.3 V.
Overview of data for flip-flops designed as defined in para 5.3.3 Summed data are given in Figs 7.2.3.3 and 7.2.3.4.

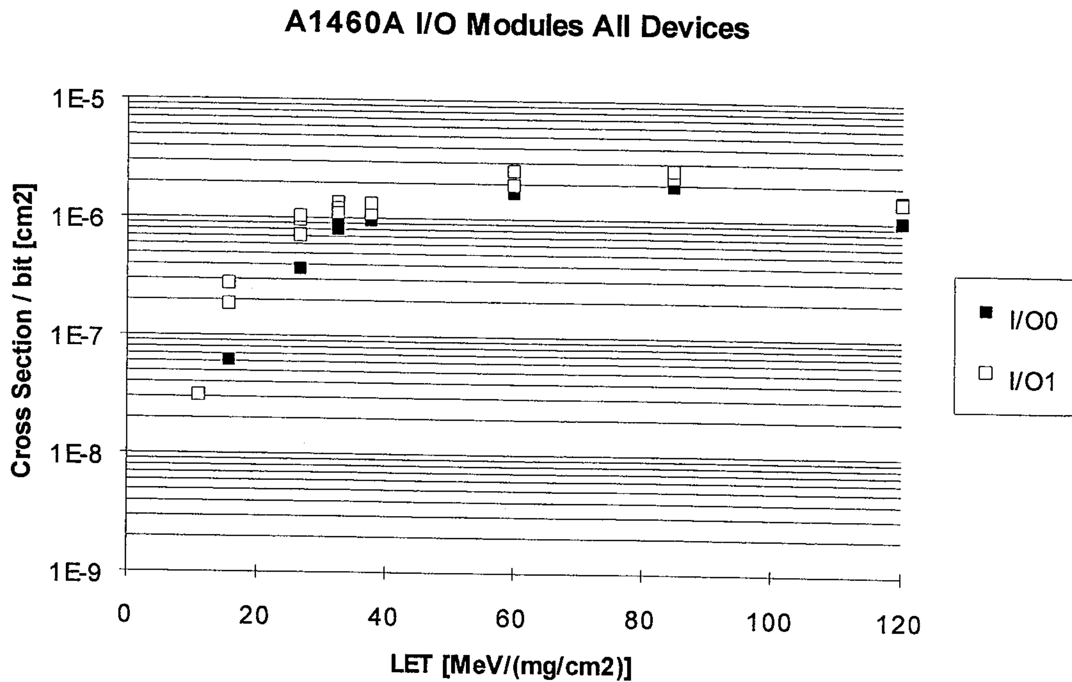


Fig 7.2.3.6 : SEU Cross Section for Actel A1460A I/O-Modules

S/W Macro :	IREC for Input "0"
	ORECTH for Output "1"
Test Condition :	Static, Vcc = 5 V, Tamb = Room Temp
Test Samples :	A1460A S/N #1, #2, #3
Cross Section (σ) :	2 E-6 cm^2 /bit
Threshold :	10 MeV/mg/cm^2

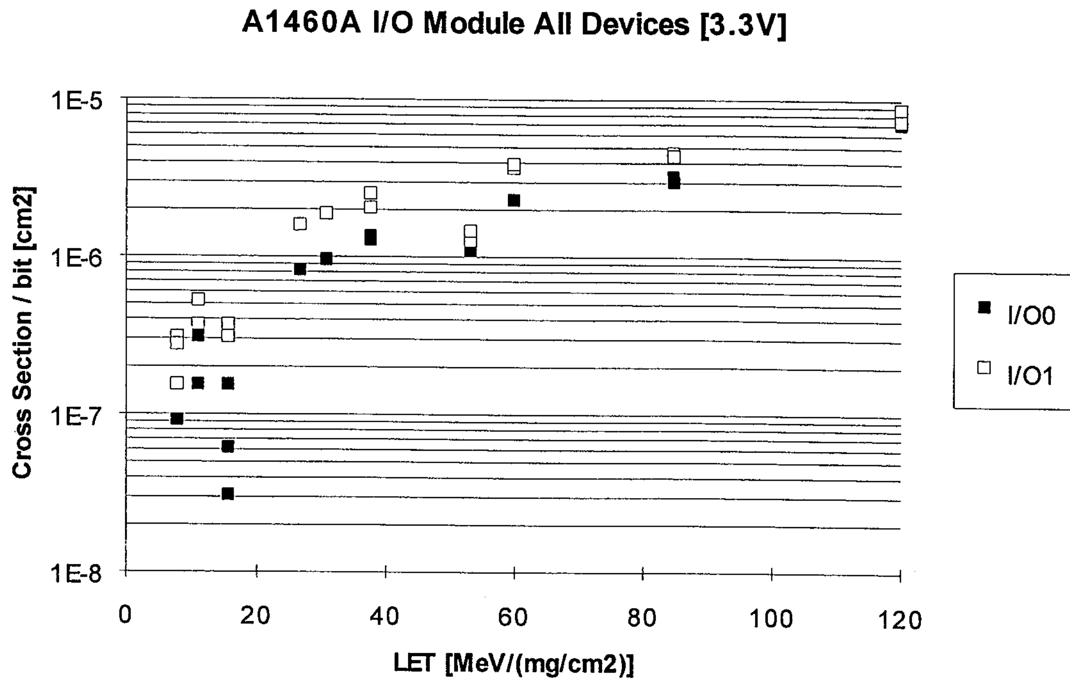


Fig 7.2.3.7 : SEU Cross Section for Actel A1460A I/O-Modules

S/W Macro :	IREC for Input "0" ORECTH for Output "1"
Test Condition :	Static, Vcc = 3.3 V, Tamb = Room Temp
Test Samples :	A1460A S/N #1, #2, #3
Cross Section (σ) :	7 E-6 cm^2 /bit
Threshold :	8 MeV/mg/cm^2

8. PROTON TESTS

8.1. Equipment & Facility

Proton test was performed at the Proton Irradiation Facility (PIF) at Paul Scherrer Institute, Villigen, Switzerland. Proton energy of 300 MeV can be achieved in a flux of maximum 10^8 protons/s / cm^2. The ion energy on target can instantly and continuously be attenuated by Aluminium slides from maximum energy down to about 30 MeV. Energy attenuation of the proton beam results in strongly reduced flux. Due to the limited number of proton induced upsets for the chosen FPGA types, the present tests were only performed at proton energies of 300 and 150 MeV.

Three samples of each device type were prepared for the proton tests. Due to various problems with both data aquisition system and the proton beam, the allocated beam time did not allow proton test of all three device types. Priority was given to RH1280 and A1460A. The samples for RH1280 and A1460A were identical to those used in the Heavy ion tests and serialised as S/N #1, #2, #3 for each type. The test board for one type at the time was mounted on a movable frame in front of the beam just behind the proton energy degrader system. The DUT is irradiated in air at normal incident angle. The facility provides beam diagnostic and control with continuous monitoring of beam fluence and flux via plastic scintillators. The irradiation cave is prohibited area during "beam on", which require controlling equipment to be placed about 50 meters away from the DUT. The PC monitoring system was placed close to the DUT in the irradiation area and remote controlled by a second computer in the control room using thin Ethernet network.

8.2. Results

8.2.1. Actel RH1280

The RH1280 was tested at 3.3 V as well as for 5 V. The results are given in Figs 8.2.1.1 - 8.2.1.3. Proton upsets could only be observed for flip-flops made out of S-modules. In Fig 8.2.1.1, the average proton upset cross section of the tested devices for both 3.3 V and 5 V have been shown. The spread in cross section between individual devices are shown in Fig 8.2.1.2 and 8.2.1.3 for 3.3 V and 5 V, respectively. The test results are also given in Table 8.2.1.1.

Table 8.2.1.1 Test results of proton induced upsets on RH1280

Device (S/N #)	Vcc (Volt)	Energy (MeV)	Fluence (prot/cm2)	S-Module # Upsets	S-Module Cross Section (/cm2 *bit)
1	3.3	150	4,9E+10	2	3,2E-13
1	3.3	300	1E+11	21	1,6E-12
1	3.3	300	9,5E+10	14	1,2E-12
2	3.3	300	7,9E+10	3	3,0E-13
3	3.3	300	5E+10	8	1,3E-12
1	5	150	5E+10	1	1,6E-13
1	5	300	1,1E+11	8	4,7E-13
2	5	300	1E+11	2	1,6E-13
3	5	300	5E+10	2	3,1E-13

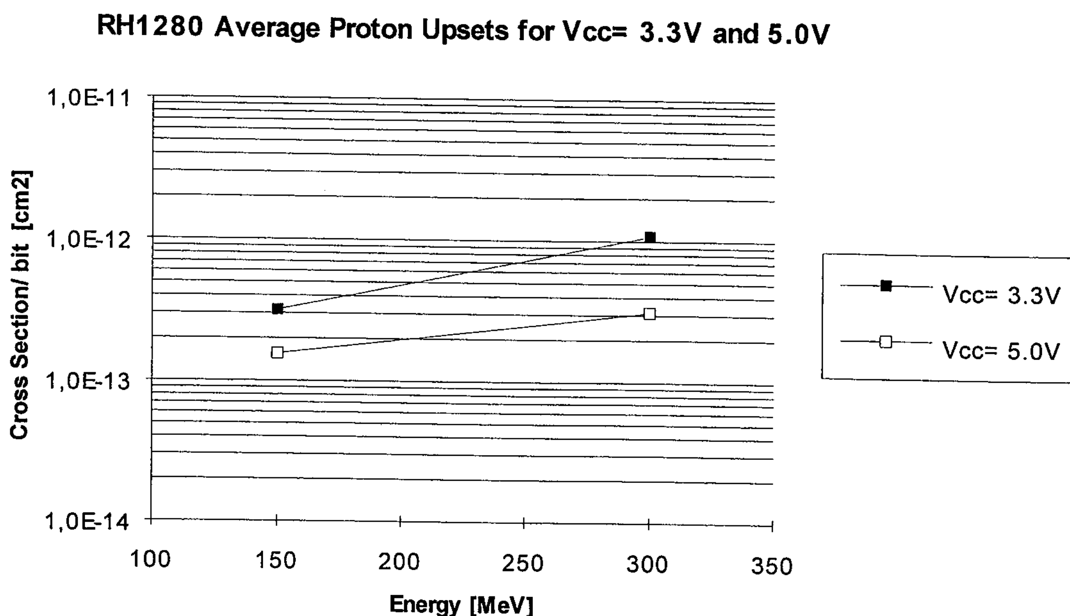


Fig 8.2.1.1 : Actel RH1280, S-Modules
Average Proton Induced Upset Cross Section versus Proton Energy

S/W Macro :	DFP1E for logic "1"
Test Condition :	Static, Vcc = 5 V, 3.3 V
	Tamb = Room Temp
Test Samples :	RH1280, S/N #1, #2, #3
Data Points:	300 MeV; Average of S/N #1, #2, #3
	150 MeV; S/N #1
Average Cross Section (σ) :	300 MeV , 5V 3.6 E-13 cm^2/bit
	300 MeV , 3.3 V 1.2 E-12 cm^2/bit

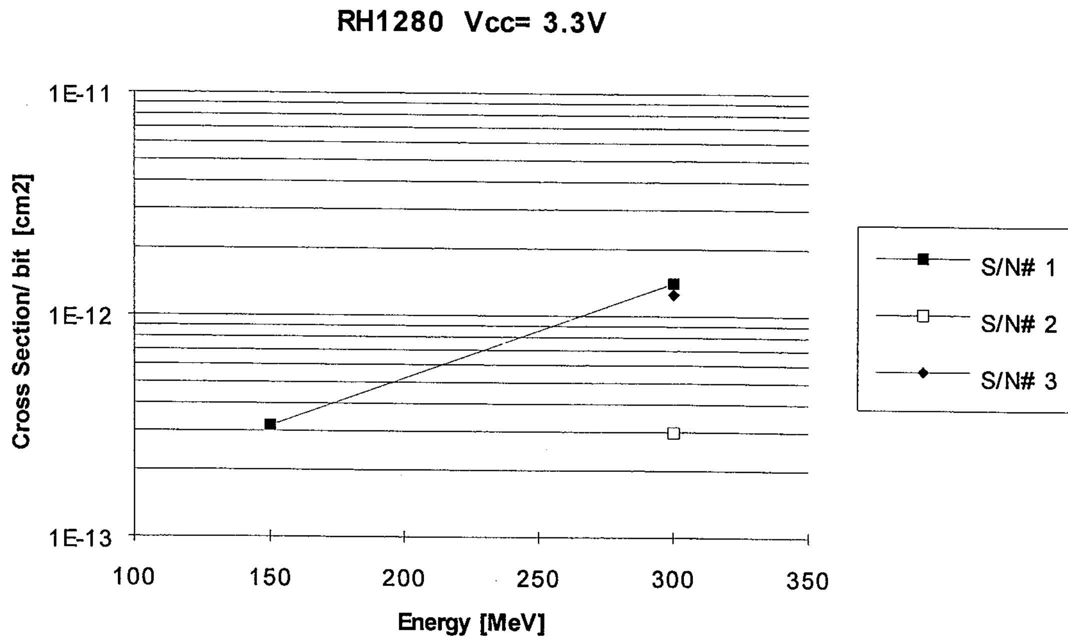


Fig 8.2.1.2 : Actel RH1280 S-Modules 3.3 V Proton Induced Upset Cross Section versus Proton Energy

S/W Macro : DFP1E for logic "1"
Test Condition : Static, Vcc = 3.3 V, Tamb = Room Temp
Test Samples : RH1280 S/N #1, #2, #3

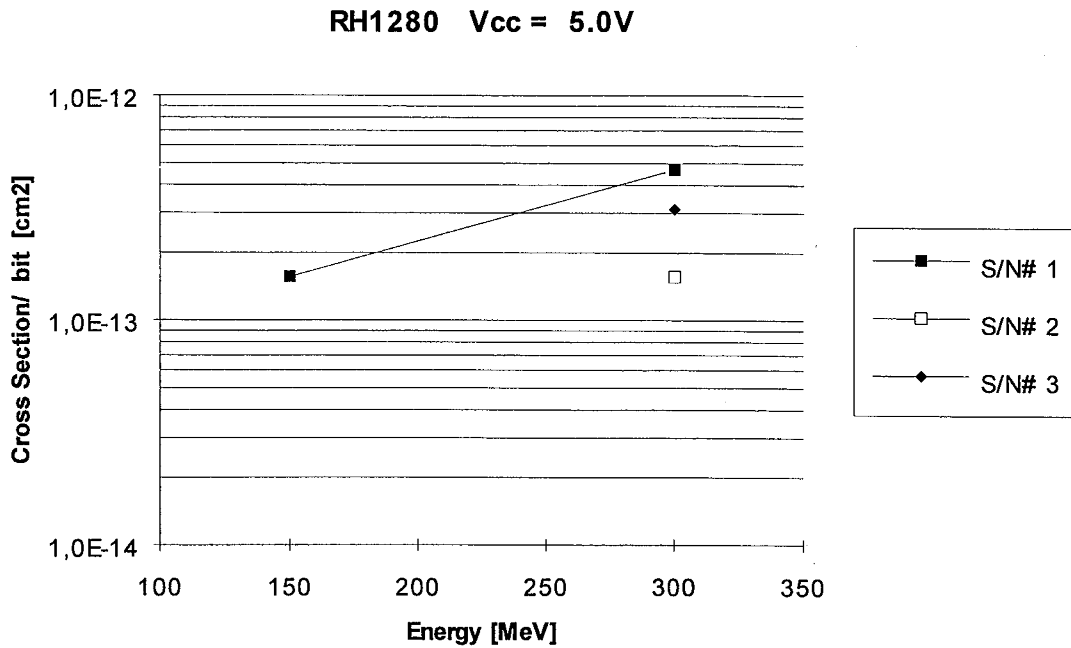


Fig 8.2.1.3 : Actel RH1280 S-Modules 5 V Proton Induced Upset Cross Section versus Proton Energy

S/W Macro : DFP1E for logic "1"
Test Condition : Static, Vcc = 5 V, Tamb = Room Temp
Test Samples : RH1280 S/N #1, #2, #3

8.2.2. Actel A1460A

The A1460 type has been tested at 3.3 V as well as for 5 V. The results are given in Table 8.2.2.1. Proton upsets were observed for flip-flops made out of both S- and I/O-modules. Device S/N #3 failed to work during second irradiation period likely due to total dose damage. The devices have also been used in the heavy ion tests. Because of shortage of beam time, device S/N #1 with already increased leakage current from the heavy ion test was not tested for proton upset.

Table 8.2.2.1 Test results of proton induced upsets on A1460A

Device	Vcc	Energy Mev	Fluence	S-Module # upsets	I/O-Module #upsets	S-Module Cross Section '/cm2 * bit	I/O-Module Cross Section '/cm2 * bit
2	3,3	300	1,0E+11	11	3	8,6E-13	2,3E-13
3	3,3	300	1,0E+11	11	2	8,6E-13	1,6E-13
3	5	300		3		Function failure	
2	5	300	1,0E+11	9	0	3,0E-13	7,8E-14

9. TOTAL DOSE TEST

9.1. Equipment & Facility

The total dose tests were performed at the hospital Sahlgrenska Sjukhuset, Göteborg. This facility has a ^{60}Co gamma source suitable for low dose rate testing. The dosimetry calibration are taken care of by the local medicine physicist. The dosimetry detectors undergoes calibration to a substandard on regular basis and the determined dose is correct within 5 %.

Three samples serialised as S/N #7, #8, #9 for each of the types 1280A and 1460 were tested for total dose. The RH1280 manufactured in the Loral Rad Hard process is considered to be radiation hard to more than 100 Krad(Si), and was therefore not an item for total dose test.

Each device type were irradiated under steady state Vcc=5.0 V at a dose rate of 560 rad(Si) per hour. All parts were programmed with the test pattern presented in section 5. The supply current and function of devices were monitored in-situ. Functional tests were performed at 50 kHz with V_{CC}= 5.0 V. The definition of functional failure is when read data do not match with pre-defined data. Function, the supply current and the supply voltage for each DUT were measured and stored about every 10th minute. The test was perused up to 80 krad(Si) total dose for A1460A and to 25 krad(Si) and functional failure for A1280A. After irradiation, the devices were subjected to biased room temperature anneal for one week.

9.2. Results

9.2.1. Actel A1280A

The results for A1280A show that the supply current start to increase already at about 5 krad(Si) cumulated dose. The behaviour for all 3 devices are about the same. The supply current as a function of cumulated dose and subsequent anneal time for the three test samples are shown in Fig 9.2.1.1. At 15 Krad(Si) the current has reached 200 mA. Pre-irradiation current value was in average around 0.02 mA.

Device S/N#7 and S/N#9 failed to function at 18.3 krad(Si) and 18.6 krad(Si), respectively. At failure the devices pulled more than 500 mA each. At failure of two devices the power supply became over loaded and the power to the devices ran into power limitation. The voltage dropped to 4.3 V over the devices. At this moment S/N#8 indicated failure as well. Within two hours at this very high power consumption the current for S/N #7, #9 returned to little below the current value just before the functional failure and the devices were functioning again. All three samples functioned for 2-3 krad(Si) more before they finally stopped. No exact cumulated dose for functional failure for S/N#8 could be recorded due to power problem. The final function failure for S/N#8 occurred at 22 krad(Si) cumulated dose.
The dip in the current curve for the biased anneal is due to shut down of main power.

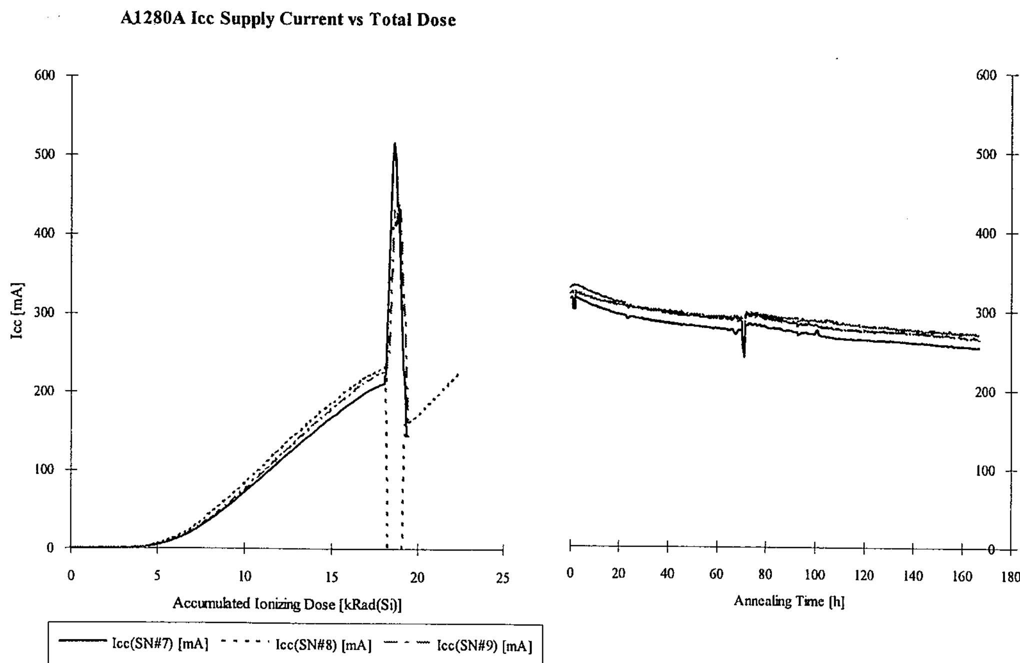


Fig 9.2.1.1 A1280A Icc supply current versus cumulated total dose and biased room temperature anneal.

9.2.2. Actel A1460A

For A1460A, the supply current as a function of cumulated dose and following biased room temperature anneal are shown in Figs 9.2.2.1 and 9.2.2.2 Pre-irradiation current value was in average about 0.7 mA. The supply current started to slowly increase due to irradiation at about 15 krad(Si) resulting in an average value of about 20 mA at 50 krad(Si) cumulated dose. First functional failure was detected at 54 krad(Si) for S/N #8. S/N #7 and #9 failed to function at 62 and 77 krad(Si), respectively.

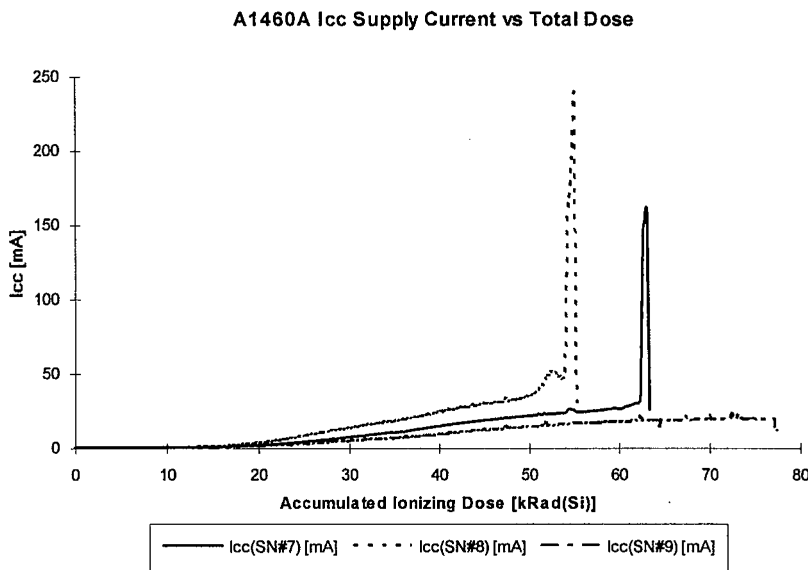


Fig 9.2.2.1 A1460 Icc as a function of cumulated total dose.

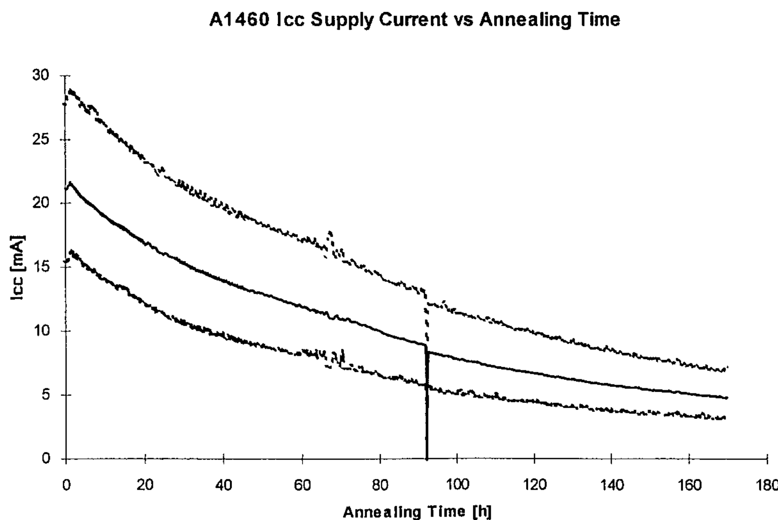


Fig 6.2.2.2 Room temperature biased anneal. Icc as a function of time. The dip above 90 h is due to shut down of main power. With increasing Icc, the curves correspond to S/N #9, #7 and #8

10. DISCUSSIONS

10.1. Heavy Ion

No latch-up was detected for any of the device types, either at 5V nor at 3.3V.
As expected, the SEU rate increased with decreasing supply voltage. In average, the cross section increased with a factor of 2 for all modules and FPGA types when going from 5V to 3.3V supply voltage.
In this study, the maximum LET at normal incidence on chip was 60 MeV/mg/cm^2. Higher LET values were achieved by tilting the device with respect to incoming ion beam. For some of the data points taken at large tilted angle, the cross sections tend to be lower or reduced compared to the expected value. This is most pronounced for 3.3 V and the heavier ions and at large angles, and likely due to decreased vertical penetration depth and subsequent reduction of charge collection in the sensitive volume.

The heavy ion data presented in this study are not valid for the device in general, but only valid for the macros used to program the devices. The determined cross sections for flip-flops made out of S-modules were about 1 E-5 cm^2 /bit for A1280A and A1460A, while the RH1280 appears to be about a factor 2 harder. S-module was only tested at logic one state. For flip-flops made out of two C-modules, the cross sections ranges from about 2 E-6 cm^2 /bit for logic zero (low level) to about 5 E-7 cm^2 /bit for logic one's (high level). The macros used are very similar, the main difference being that DFPC (zero's) has a reset input, DFP1B (one's) has not.

Actel indicated during the WP1 meeting that flip-flops made out of two C-modules may have different SEU vulnerability than flip-flops made out of a C-module and a "bypass S-module". The design for the present study was changed to cope with the this information. The present results, however, give no clear indication of different SEU sensitivity depending how the C-module flip-flop state is created. Figure 7.2.2.1 give an overview of the different variants of C-module registers. The spread that can be observed are likely due to poor statistics in the various data points and also individual spread among the devices. None of the RH1280 devices were marked, but claimed by Actel to come from the same manufacturing lot. An overview of the total collected data as a function of the physical location on the RH1280 chip is shown in Fig 10.1.1.

Individual cross sections and threshold values are given in connection with data illustrations in section 7 and summarised in Table 10.1.1. Upset rate calculations using Space Radiation (ver. 4.0) are given below for GEO and Polar orbits. The calculations are performed assuming 100 mil of Al shielding and the standard Solar Minimum (M1, 1975.144) model. The calculations are based on actual data which gives an average cross sections for each module assuming equal amount of logic zero's and one's. It will also give an average value for all C module combinations.

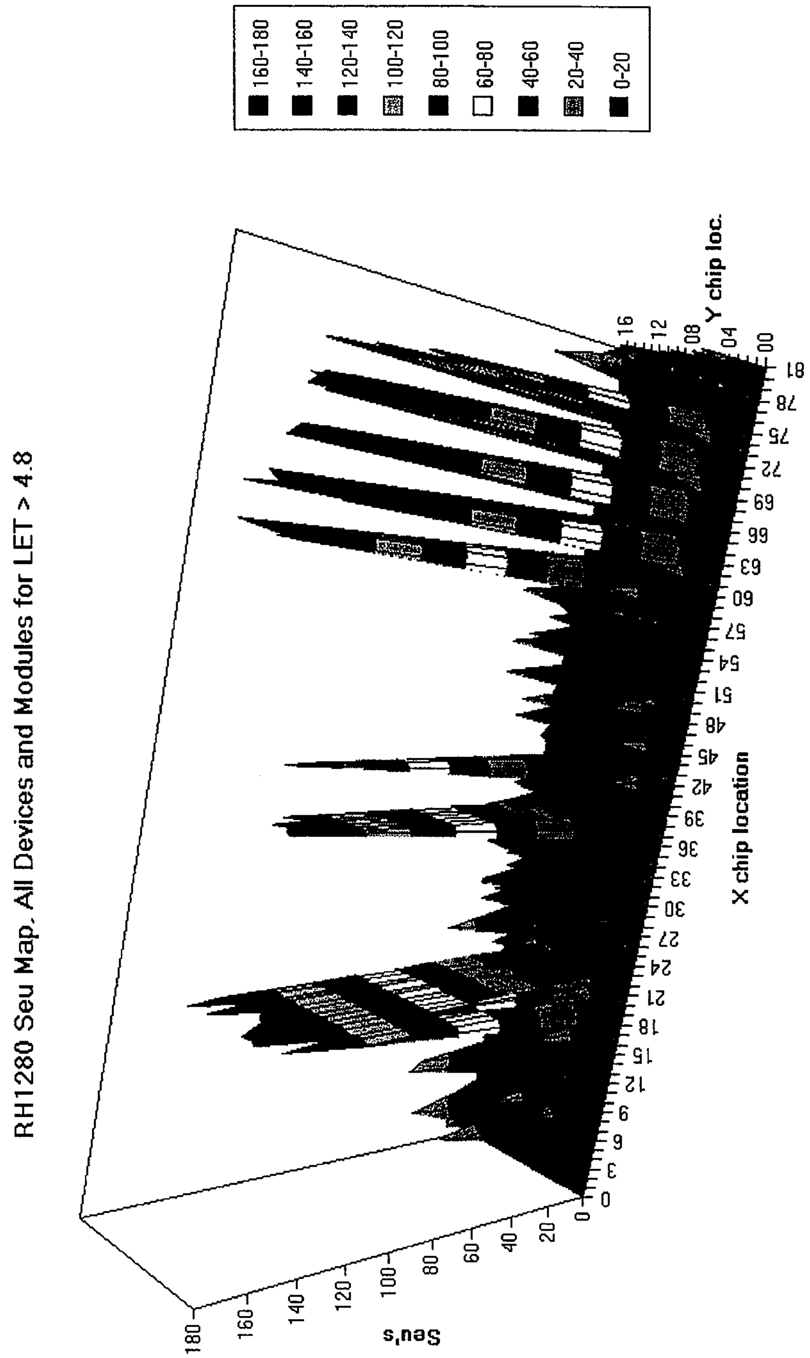


Fig 10.1.1 Total collected data versus physical location on the RH1280 chip. The x-y plane represents the physical location on chip and the z-axis gives the total number of recorded upsets. The large peaks corresponds to S-module registers. I/O modules are located along the borders and the rest consist of different configurations of C modules.

Table 10.1.1 Summary of Cross Sections and Threshold values for some tested macros.

	C DFPC Cross Section cm2	C DFPC Threshold MeV/mg/cm2	S DFP1E Cross Section cm2	S DFP1E Threshold MeV/mg/cm2	I/O * Cross Section cm2	I/O * Threshold MeV/mg/cm2
5 Volt						
A1280A	3,0E-06	27	1,5E-05	10	3,0E-06	15
RH1280	1,7E-06	27	6,0E-06	10	1,0E-06	15
A1460A	3,0E-06	32	1,5E-05	8	2,0E-06	10
3.3 Volt						
RH1280	4E-06	15	1E-05	6	2E-06	10
A1460A	6E-06	15	2E-05	6	7E-06	8

*IR,IRH for A1280A, RH1280
*IREC,ORECTH for A1460A

Table 10.1.2 Upset rates /day /bit for registers made out of C, S and I/O modules in GEO (35750 circular, 0°) orbit. Upset rates valid for tested macros only.

Device	GEO C DFP1B/DFPC	5 Volt S DFP1E	I/O IR/ORH, IREC/ORECTH
A1280A	9,7E-08	5,4E-06	1,8E-07
RH1280	6,9E-08	4,5E-06	5,7E-08
A1460A	2,2E-07	1,1E-05	2,5E-06

Table 10.1.3 Upset rates /day /bit for registers made out of C, S and I/O modules in Polar (800 circular, 97°) orbit. Upset rates valid for tested macros only

Device	Polar C DFP1B/DFPC	5 Volt S DFP1E	I/O IR/ORH, IREC/ORECTH
A1280A	2,4E-08	1,6E-06	4,6E-08
RH1280	1,7E-08	1,3E-06	1,4E-08
A1460A	5,5E-08	3,3E-06	7,2E-07

Table 10.1.4 Comparison of upset rates /day /bit for registers build out of different combinations of C modules in RH1280 operated at 5 Volts in GEO and polar orbits. The average cross section from the three tested devices have been used as input for the calculations. Upset rates valid for the tested macros only.

Orbit	Register Blocks			
	C-C	BS-BS	C-BS	BS-C
GEO	7,6E-08	6,0E-08	6,8E-08	7,0E-08
Polar	1,9E-08	1,5E-08	1,7E-08	1,7E-08

10.2. Protons

The fairly high threshold value determined in the heavy ion test for C and I/O modules of the tested FPGA types indicated that it will be difficult to achieve any proton data within practical measuring time. The proton test also proved that only upsets in S-module registers could be observed for 5 Volt supply current. For A1460A and 3.3V, a few upsets could be detected for the I/O registers, indicating a factor 4 lower cross section than for the S-module registers.

The upset cross section for protons at Vcc= 5V and 3.3V are given in the data figure caption in section 8. For S-modules and Vcc = 3.3 V, the upset cross sections seem to be a factor 3 higher than for 5V supply voltage. Upset rates in space are given in Table 10.2.1 for Low Earth Orbit (LEO) using Space Radiation calculation with actual data and the trapped proton model AP8MIN, behind 200 mil shielding and the International Geomagnetic Ref. field as input.

Table 10.2.1 Upset rates /day /bit for registers made out of C, S and I/O modules in LEO (450 circular, 51°) orbit. Upset rates valid for tested macros only

Device	LEO 5 Volt		
	C	S	I/O
RH1280	-	1,7E-07	-
A1460A	-	5,0E-07	4,8E-08

10.3. Total Dose

The A1280A was found to degrade severely already at low levels of cumulated dose. As shown in Fig 9.2.1.1, A1280 begins to draw significant current well before failure, increasing almost linearly until a level of about 18 krad(Si). At this point, the current jumped abruptly to a level above 500 mA. The variation between the three samples was small. According to the literature, this large jump in current is a consistent characteristic of the A1280A device and has been reported to occurred as low as 12 krad(Si). This phenomenon has not been found to occur for the smaller type, A1020, in the ACT2 family.

The Actel A1280A type has earlier been the subject of several total dose tests. The A1280A family was originally a 1.2 μ design which is now available as a 1.0 μ shrink, the device tested for this work. Previous studies have found the A1280A family devices to function to levels from about 8 krad(Si) up to 25 krad(Si), which is inline with the results found in the present study. The samples used in the this study were burned in. The effect of burn in on the dose susceptibility for the 1280A is marginal according to other experiments. The wide range of total dose results from different laboratories may be influenced by slight differences in test programs and test methodologies. However, the lot-to-lot variations found in other studies are more likely the cause of reported differences in A1280 behaviour.

The A1460 type belonging to the Act 3 family has not yet been the subject of many radiation tests. The results for this device type of commercial grade are more promising than that for A1280A. The average pre-irradiation current value was about 0.7 mA. For the first 10 krad(Si) cumulated dose, the supply current increased only about 0.1 mA. For 20 krad(Si) cumulated dose, S/N #8 increased from 0.74 to 3.7 mA, while S/N #7 and S/N #9 increased from around 0.7 to about 1.6 mA. The variation in current increase among the three test samples are remarkably large. Two of the three samples also exhibit the phenomenon of abruptly jump in current value similar to what was observed for A1280.

11. CONCLUSION

The three types tested indicate similar heavy ion sensitivity, with the RH1280 type more SEU hard than the other two. The cross sections and threshold values are only valid for the specific macros used in the present work. Upset calculations using Space Radiation and experimental cross sections show that the commercial FPGA A1460A in GEO will exhibit about 1.7 S-register (432 bits) upsets per year and device, while registers made out of C modules (208 bits) will upset 0.1 times per year and device. About the same upset rates will be observed for the A1280A. Even if the number of upsets for the RH1280 will be lower, (C: 0.008 upsets/year/device (304 bits) S: 1 upsets/year/device (624 bits)) S-module registers would likely not be accepted in critical space applications due to the high upset rate.

In space applications at LEO, the inclination of the orbit will have a large impact on the number of upsets a device will see. Detailed assessments of the proton upsets must be performed for each programme. In general, the tested FPGA tend to be worse than other complex device types.

The RH1280 type is considered Rad Hard and will not give rise to any total dose problem. The A1460A indicated very little changes in supply current up to 10 krad(Si) and no functional failure could be detected with the present test method up to 50 krad(Si). With some shielding this device may well be used in some space application from a total dose point of view. The A1280A exhibits large currents already at 10 krad(Si) and fail to function around 18 krad(Si). Other experiments have shown that large differences could be expected from lot to lot, but all fail to function before 20 krad(Si).

In summary, the RH1280 seem to be useful for many space applications, particularly if only C- and I/O- modules are used. However, the SEU sensitivity of the programmed device is a function of which macro(s) that has been used. The A1460A may also be interesting, specially if some extra shielding can be provided to minimise the current increase due to total dose damage. The total dose tolerance of the A1280A, however, is so poor that this device type will likely not be used in any long term project without heavy shielding.